

2SK3134(L), 2SK3134(S)

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

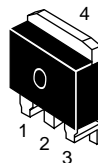
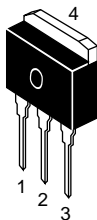
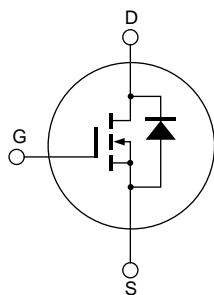
ADE-208-721B (Z)
3rd. Edition
February 1999

Features

- Low on-resistance
 $R_{DS(on)} = 4 \text{ m}\Omega$ typ.
- Low drive current
- 4 V gate drive device can be driven from 5 V source

Outline

LDBPAK



1. Gate
2. Drain
3. Source
4. Drain

2SK3134(L),2SK3134(S)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	75	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	300	A
Body-drain diode reverse drain current	I_{DR}	75	A
Avalanche current	I_{AP} ^{Note 3}	35	A
Avalanche energy	E_{AR} ^{Note 3}	122	mJ
Channel dissipation	P_{ch} ^{Note 2}	100	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

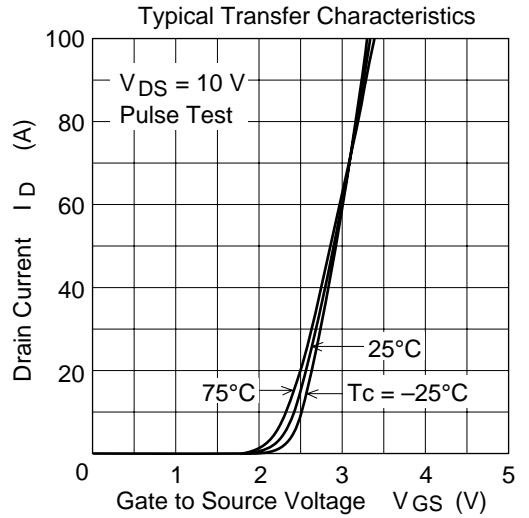
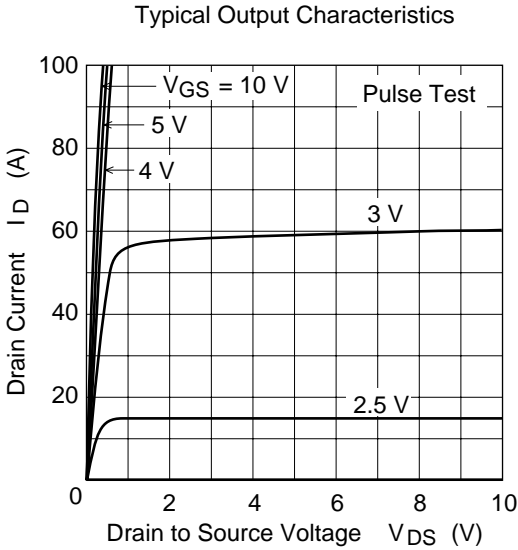
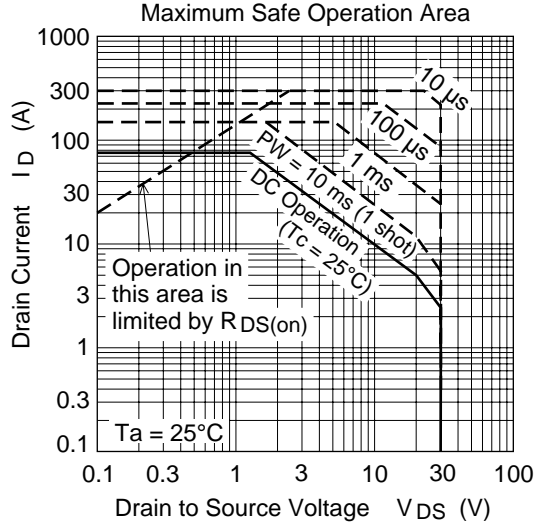
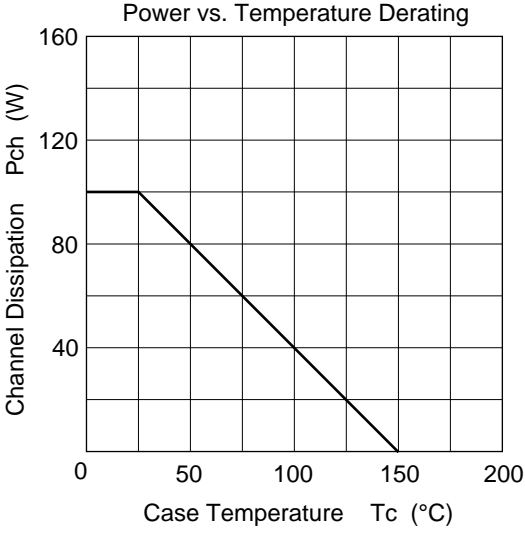
- Note: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ C$
3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

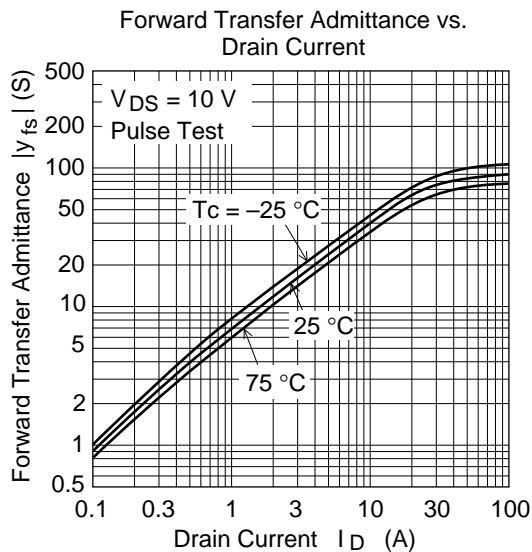
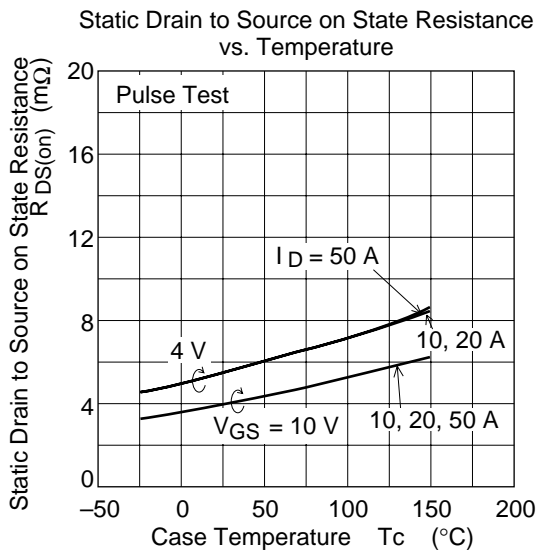
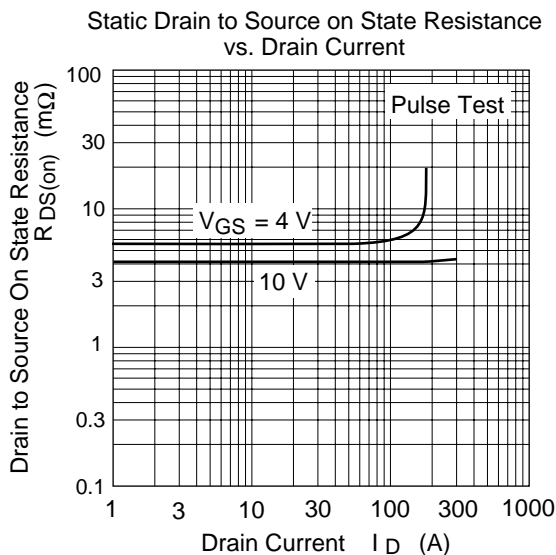
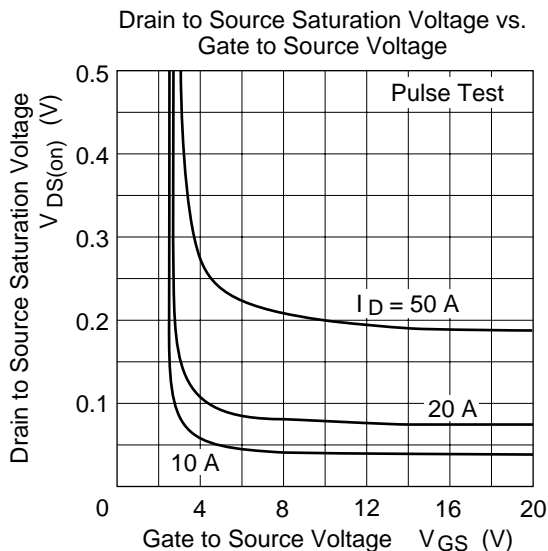
Electrical Characteristics (Ta = 25°C)

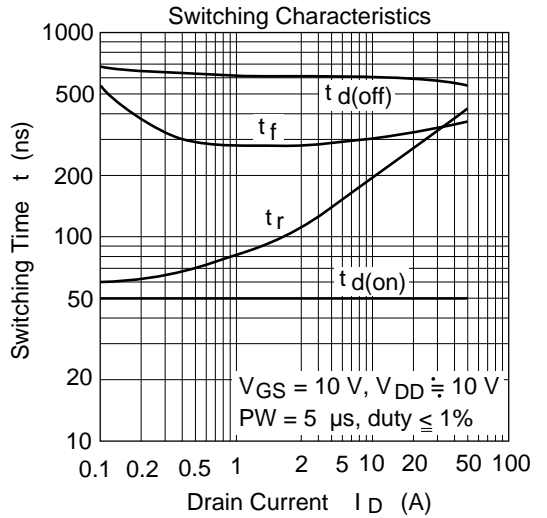
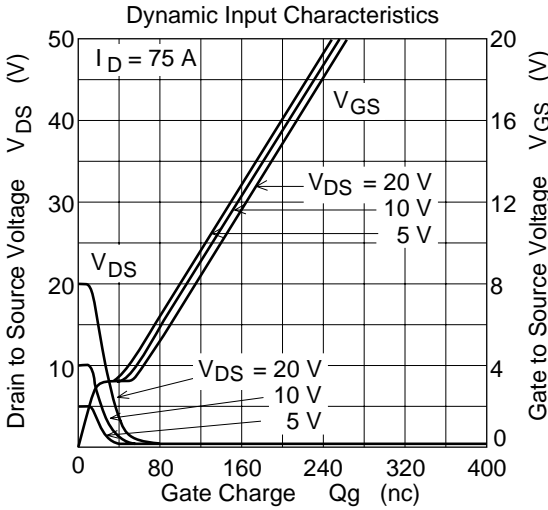
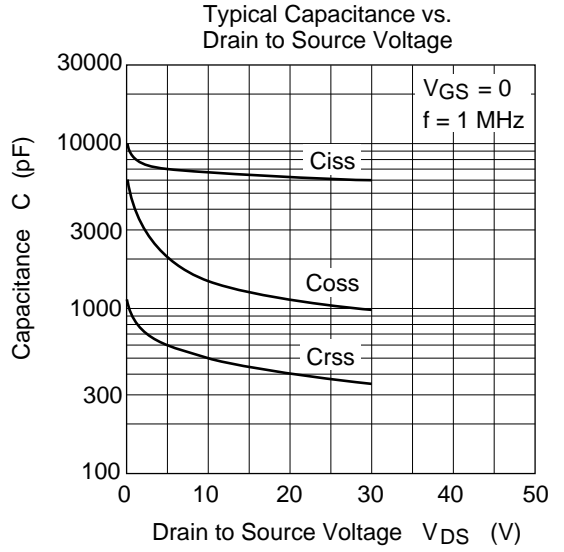
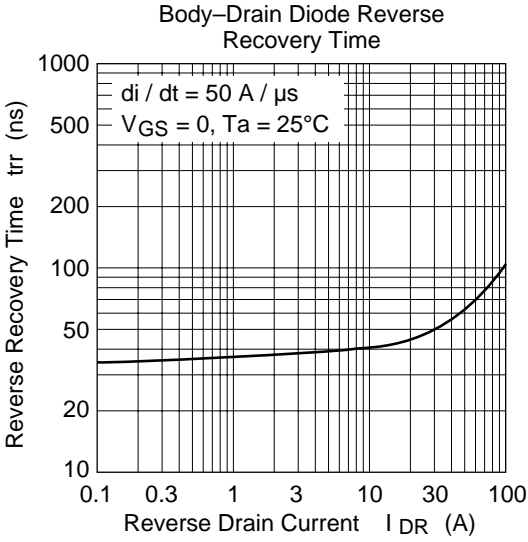
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 30 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$ ^{Note 1}
Static drain to source on state resistance	$R_{DS(on)}$	—	4.0	5.0	$\text{m}\Omega$	$I_D = 40 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note 1}
		—	5.5	8.5	$\text{m}\Omega$	$I_D = 40 \text{ A}, V_{GS} = 4 \text{ V}$ ^{Note 1}
Forward transfer admittance	$ y_{fs} $	50	80	—	S	$I_D = 40 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note 1}
Input capacitance	C_{iss}	—	6800	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	1550	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	500	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	130	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	16	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	30	—	nc	$I_D = 75 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	50	—	ns	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$
Rise time	t_r	—	370	—	ns	$R_L = 0.25 \Omega$
Turn-off delay time	$t_{d(off)}$	—	550	—	ns	
Fall time	t_f	—	380	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.05	—	V	$I_F = 75 \text{ A}, V_{GS} = 0$
Body–drain diode reverse recovery time	t_{rr}	—	80	—	ns	$I_F = 75 \text{ A}, V_{GS} = 0$ $di_F/dt = 5 \text{ A}/\mu\text{s}$

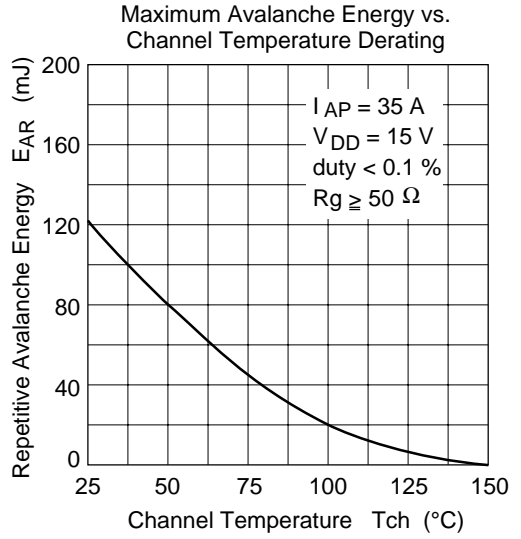
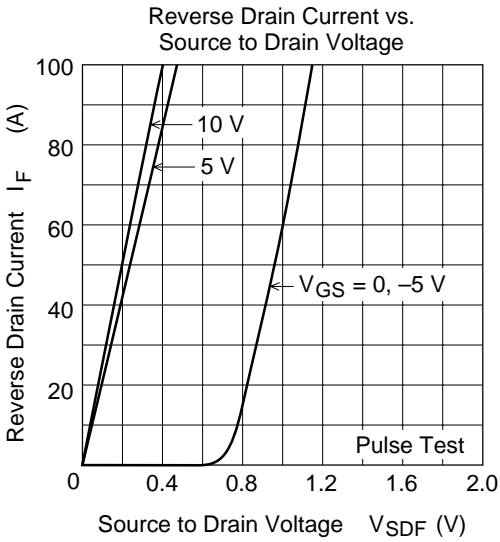
Note: 1. Pulse test

Main Characteristics

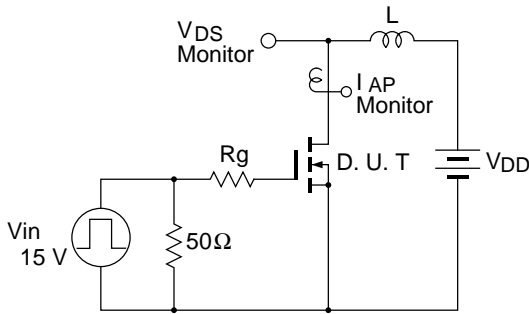




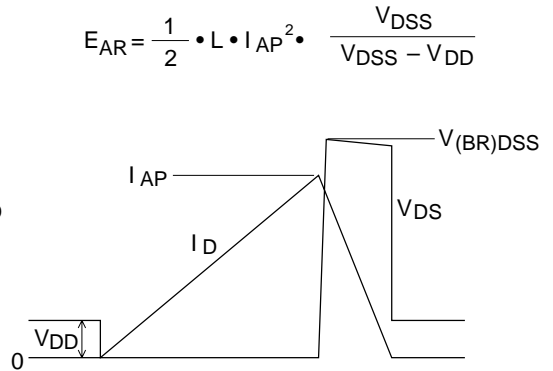




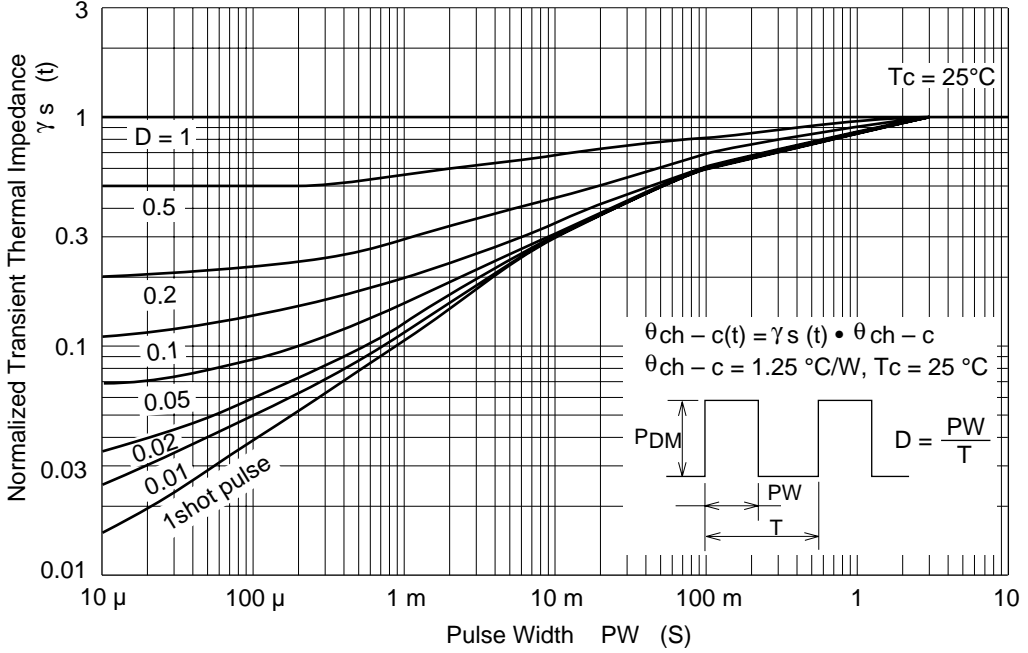
Avalanche Test Circuit



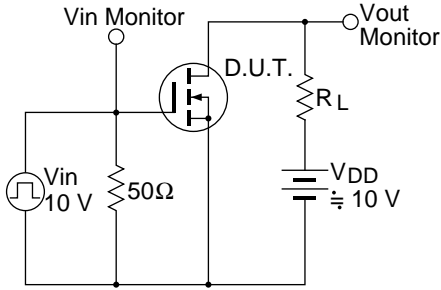
Avalanche Waveform



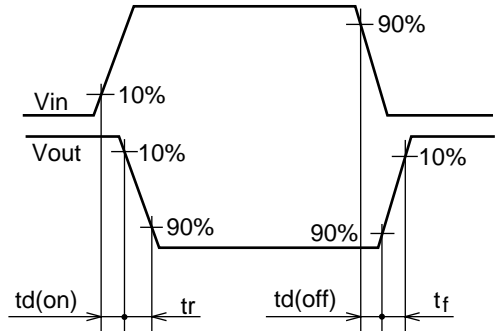
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

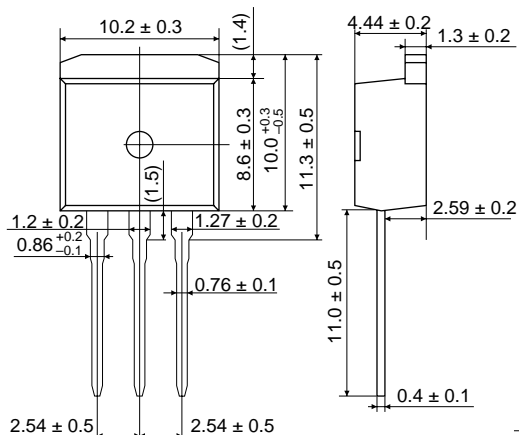


Waveform

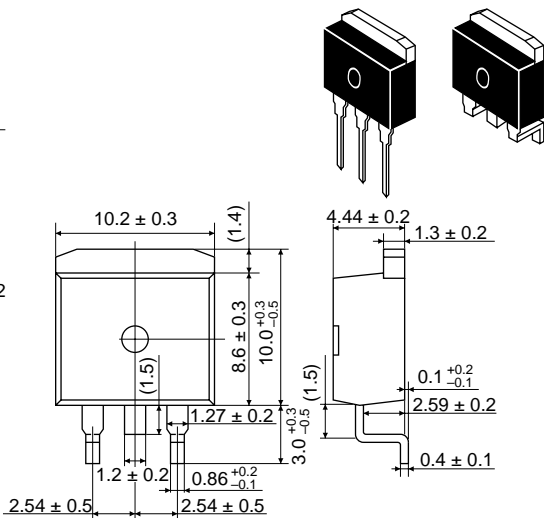


Package Dimensions

Unit: mm



Ⓛ type



Ⓢ type

Hitachi Code	LDPAK
EIAJ	—
JEDEC	—

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