TP6401

240-OUTPUT STN COMMON DRIVER

DataSheet

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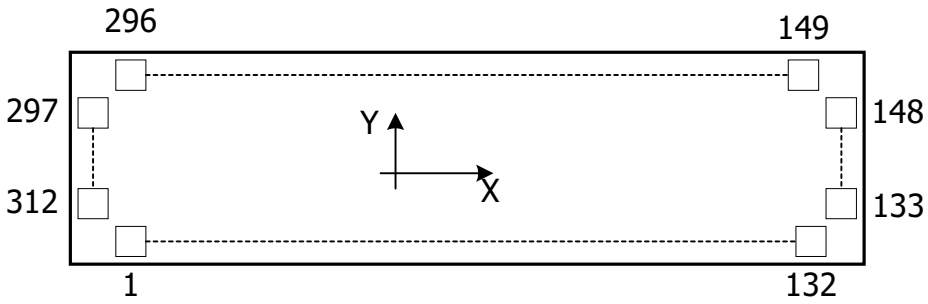
Description

The TP6401 is an 240 output, 3-level low-resistance common (row) driver suitable for high-quality, high-response-speed MLS (Multi Line Selection) driving.
The TP6401 receives signals from LCD controllers such as the SED1335, and when used in conjunction with the TP6410, can be used to structure a 4-line MLS drive.
The TP6401 uses a slim-chip form that is useful for making LCD panels slimmer. It also supports reduced logic system voltage operation, making it suitable for a broad range of applications.
The TP6401 has a pad layout supporting easy mounting, and supports bi-directional selection of driver output order, and has the highest use efficiency for 1/240 and 1/480 duty panels.

Features

- LCD driver outputs • 240
- Low output ON resistance
- High duty drive supported • • • • • • • • • • • • • • • • • 1/480 (Reference value)
- Broad range of LC drive voltages • • • • • • • • • • • • • +14 to +42V(VCC=2.7 to 5.5V)
- Output shift direction pin select is possible
- Non-biased display OFF function
- Logic system power source • • • • • • • • • • • • • • • • 2.7V to 5.5V
- LC power source offset bias can be adjusted relative to the VDDH and GND levels
- Slim chip shape
- D_{0B} • Au Bump die
- T_{0A} • TCP

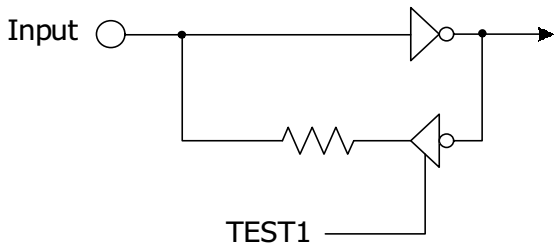
Pad Layout



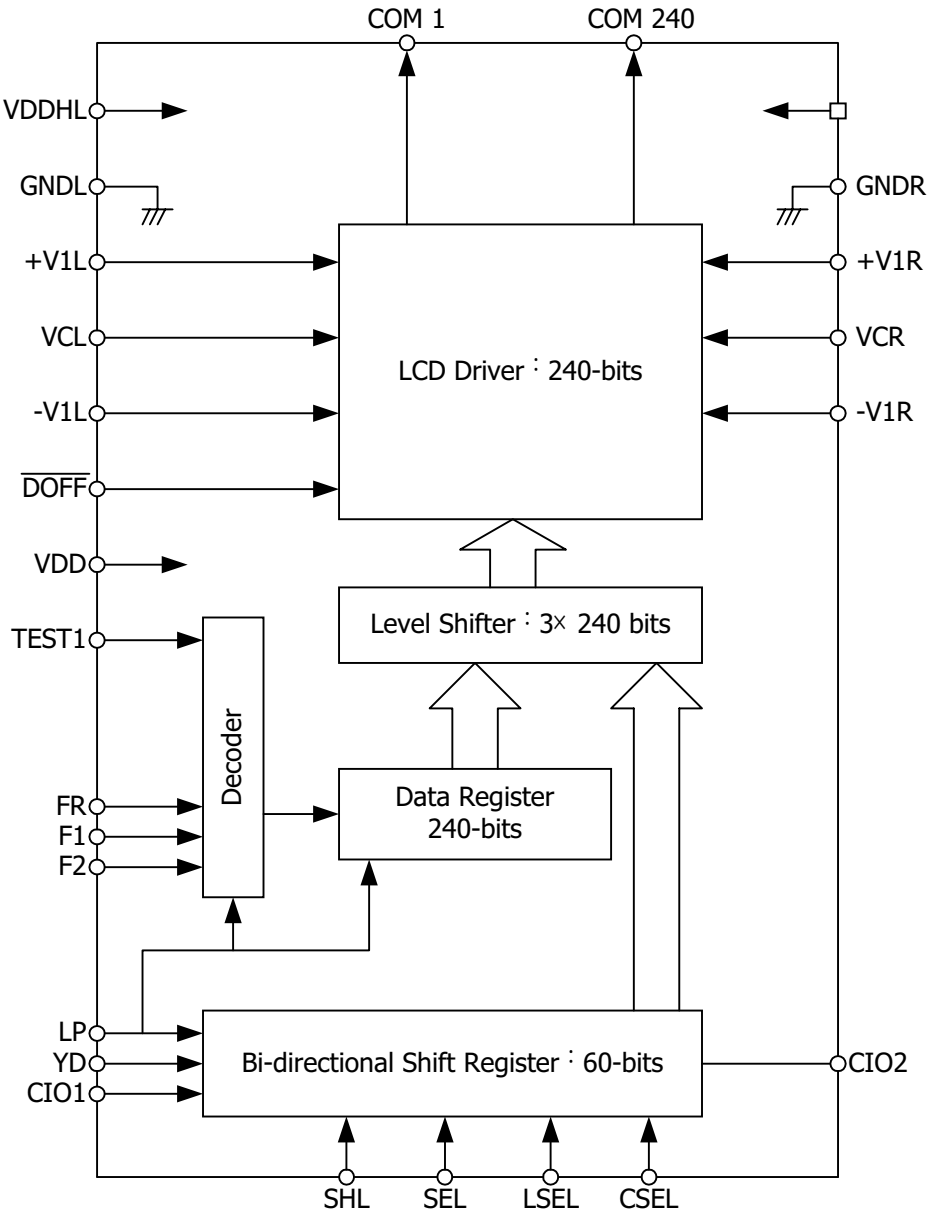
TERMINAL FUNCTIONS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Number of Terminals</th></tr>
<tr><td>COM1 to COM240</td><td>O</td><td>Common (row) output to drive LC.
Output transition occurs on falling edge of LP.</td><td>240</td></tr>
<tr><td>CIO1
CIO2</td><td>I/O</td><td>Carry signal I/O.
This is set to input or output depending on the level of the SHL input. Output transition occurs on falling edge of LP.</td><td>2</td></tr>
<tr><td>YD</td><td>I</td><td>Frame start/pulse input, with terminator. (*1)</td><td>1</td></tr>
<tr><td>F1, F2</td><td>I</td><td>Drive pattern select signal input, with terminator. (*1)</td><td>2</td></tr>
<tr><td>LP</td><td>I</td><td>Shift clock input for display data.
(Triggers on falling edge.) With terminator. (*1)</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and CIO terminal I/O control input.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">Output Shift Direction</th><th colspan="2">CIO</th></tr>
<tr><th>CIO1</th><th>CIO2</th></tr>
<tr><td>L</td><td>1 → 240</td><td>Input</td><td>output</td></tr>
<tr><td>H</td><td>240 → 1</td><td>Output</td><td>Input</td></tr>
</table>
The numbers in parentheses are for 100 output mode.</td><td>1</td></tr>
<tr><td>LSEL</td><td>I</td><td>1/2 H operation select signal input.
L: Normal operation. H: 1/2 operation.</td><td>1</td></tr>
<tr><td>CSEL</td><td>I</td><td>Chip select signal input for when a cascade connection is used.
L: Leading chip
H: Other chips</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC Drive Output AC signal input. With terminator (*1)</td><td>1</td></tr>
<tr><td>$\overline{\text{DOFF}}$</td><td>I</td><td>LC display blanking control input. With a low level input, all common outputs are temporarily set to the VC level.
The contents of the latches are maintained. With terminator (*1)</td><td>1</td></tr>
<tr><td>TEST1</td><td>I</td><td>Test1 signal input. Normally tied at L.</td><td>1</td></tr>
<tr><td>VCC, GNDL, GNDR</td><td>Power</td><td>Power source for logic:
GND: 0 V , VCC: +2.7 to 5.5 V</td><td>3</td></tr>
<tr><td>VCL, VCR, +V1L, +V1R, -V1L, -V1R, VDDHL, VDDHR</td><td>Power</td><td>LC Drive Power:
GND: 0 V,
VDDH: + 14.0 to 42.0 V, VDDH≧+V1≧VC≧–V1≧GND</td><td>8</td></tr>
<tr><td>DM</td><td></td><td>Dummy pad</td><td>11</td></tr>
<tr><td></td><td></td><td>Total</td><td>274</td></tr>
</table>

NOTE: *1



Block Diagram



Explanation of Each Block

Shift Register

This is a bi-directional shift register used for transmitting common data. The display data shifts on the falling edge of LP.

Level Shifter

The level shifter is a voltage level converter circuit which converts the signal voltage level from a logic system level to the LC driver system voltage level.

LCD Driver

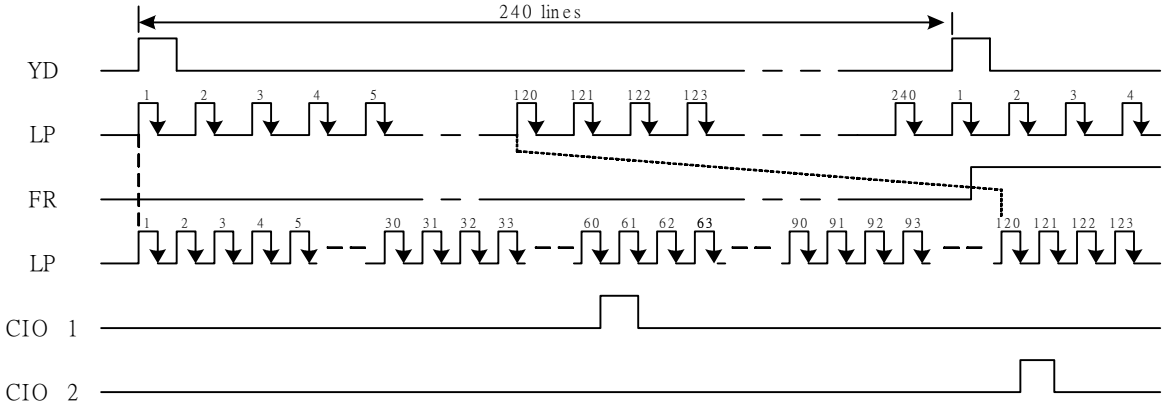
The LCD driver outputs the LC drive voltage.
The relationship between the display blanking signal $\overline{\text{DOFF}}$, the field recognition signals F1 & F2, the AC signal FR, and the common output voltage is as follows:

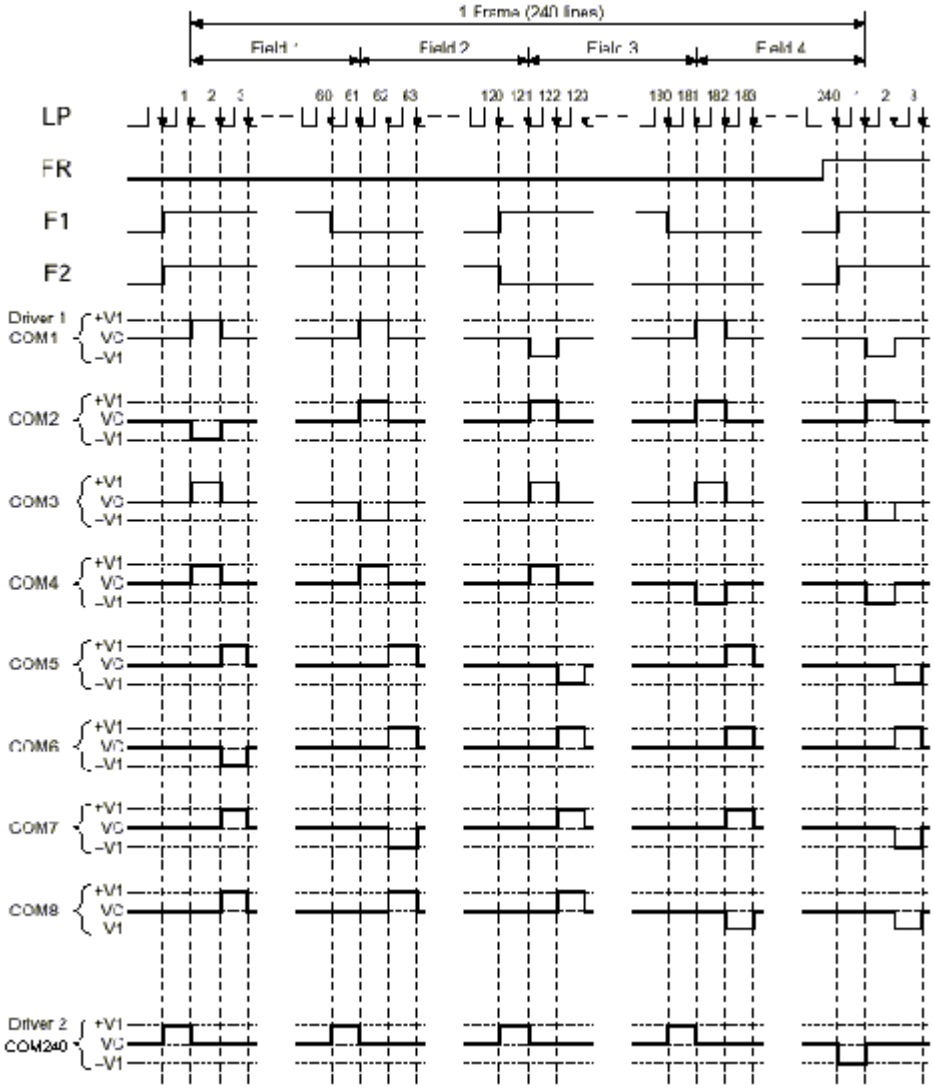
$\overline{\text{DOFF}}$	H								L
FR	L				H				---
F1,F2	1,1	0,1	1,0	0,0	1,1	0,1	1,0	0,0	---
Line 1	+V1	+V1	-V1	+V1	-V1	-V1	+V1	-V1	Vc
Line 2	-V1	+V1	+V1	+V1	+V1	-V1	-V1	-V1	Vc
Line 3	+V1	-V1	+V1	+V1	-V1	+V1	-V1	-V1	Vc
Line 4	+V1	+V1	+V1	-V1	-V1	-V1	-V1	+V1	Vc

Voltage level relationships: + V1 > VC > –V1 (VC is the center voltage level)

Timing Diagram (1)

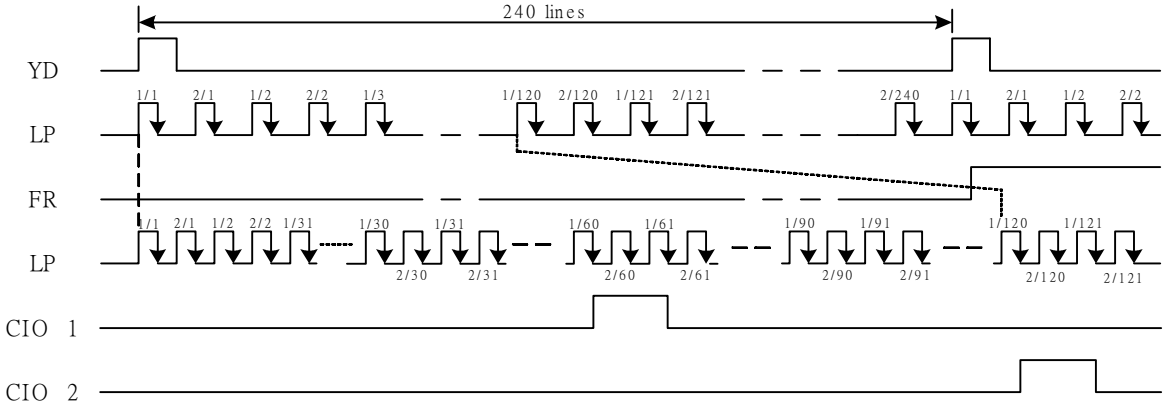
1/240 duty, normal operation.
SHL = L, SEL = L, LSEL = L, CSEL = L (This diagram provided only as a reference.)

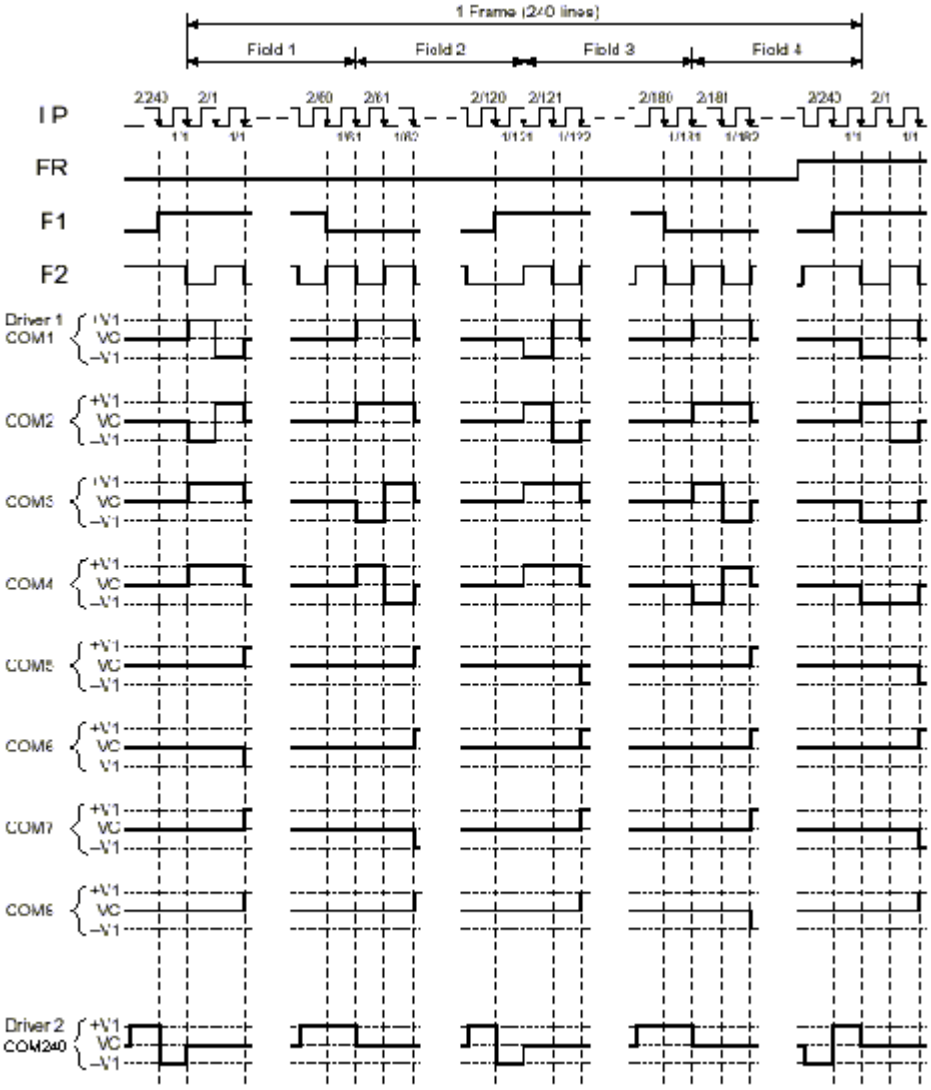




Timing Diagram (2)

1/240 duty, 1/2 H operation.
SHL = L, SEL = L, LSEL = H, CSEL = L (This diagram provided only as a reference.)

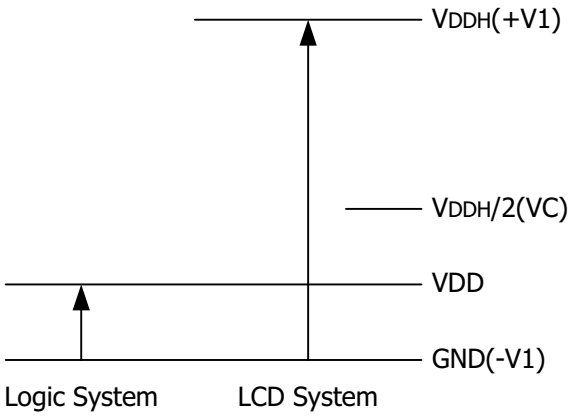




ABSOLUTE MAXIMUM RATINGS

Item	Signal	Rated Value	Units
Power voltage (1)	VCC	– 0.3 to +7.0	V
Power voltage (2)	VDDH	– 0.3 to + 45.0	V
Power voltage (3)	± V1, VC	GND – 0.3 to VDDH + 0.3	V
Input voltage	V1	GND – 0.3 to VCC + 0.3	V
Output voltage	Vo	GND – 0.3 to VCC + 0.3	V
CIO output current	Io1	20	mA
Operating temperature	Topr	– 30 to +85	℃
Storage temperature 1	Tstg 1	– 65 to +150	℃
Storage temperature 2	Tstg 2	– 55 to +100	℃

NOTE 1:The voltages are all relative to GND = 0 V.
NOTE 2:Storage temperature 1 is for the chip alone, and storage temperature 2 is for the TCP product.
NOTE 3:Ensure that the relationship between +V1, VC, and –V1 is always as follows: VDDH≧+V1≧VC≧–V1≧GND.



NOTE4:The LSI may be permanently damaged if the logic system power is floating or VCC is less than or equal to 2.6 V when power is applied to the LC drive system. Special caution must be paid to the power sequences during power up and power down.

Electrical Characteristics

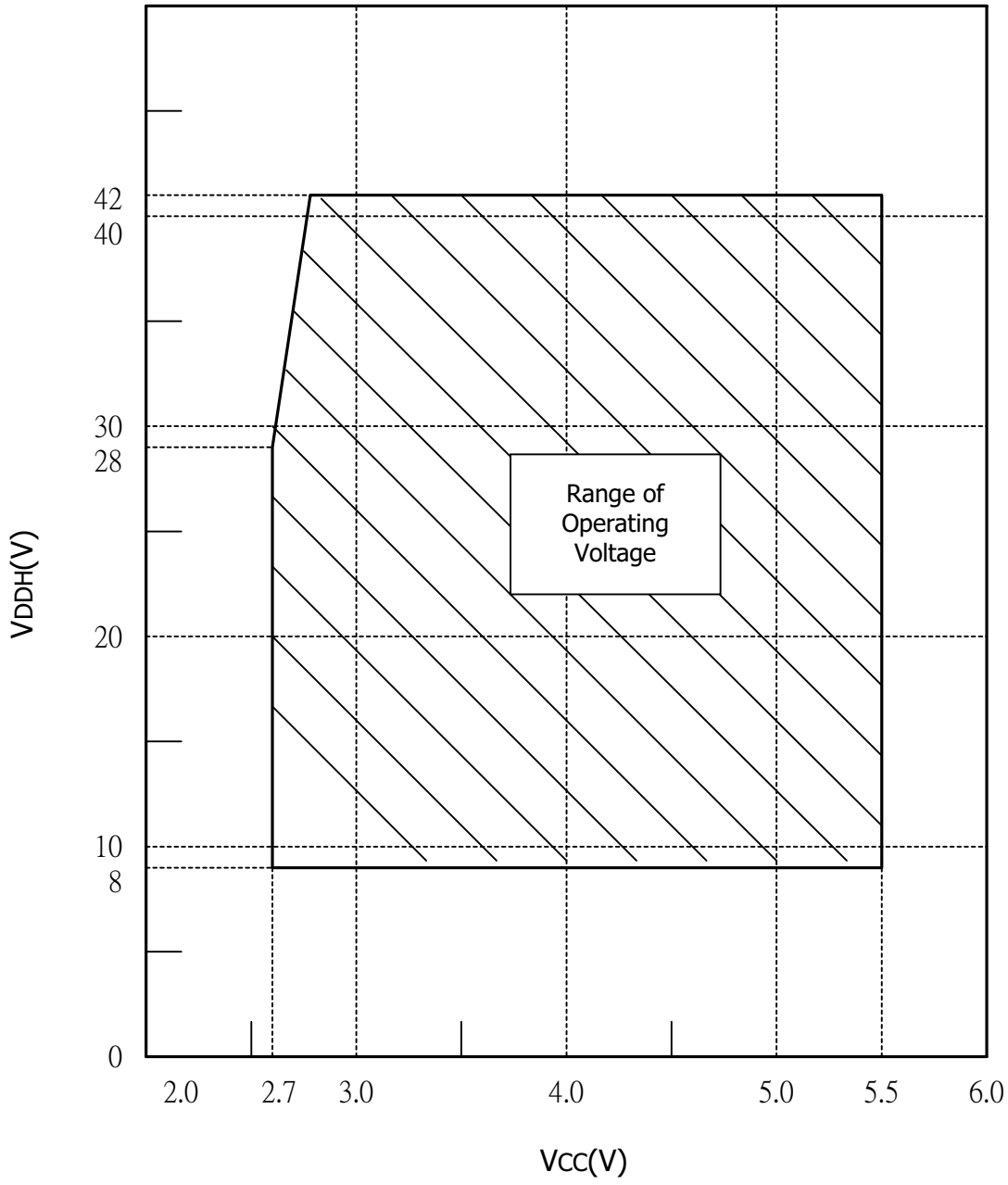
DC Characteristics

Unless otherwise noted, GND = 0 V, VCC = + 5.0 V± 10%, Ta = –30 to 85℃

Item	Signal	Parameter		Applicable Terminals	Min	Typ	Max	Unit
Power Supply Voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Range Operating Voltage	V_{DDH}	Function		V_{DDH}	8.0		42.0	V
Power Supply Voltage (2)	$+V_1$	Recommended Value		$+V_1$			V_{DDH}	V
Power Supply Voltage (3)	V_C	Recommended Value		V_C		$V_{DDH}/2$		V
Power Supply Voltage (4)	$-V_1$	Recommended Value		$-V_1$	GND			V
High-level Input Voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		CIO1,CIO2,FR,YD,LP,SHL ,SEL,LSEL,CSEL, ,F1,F2, TEST1	0.8V_{CC}			V
Low-level Input Voltage	V_{IL}						0.2V_{CC}	V
High-level Output Voltage	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH}=-0.3mA	CIO1,CIO2	V_{CC}-0.4			V
Low-level Output Voltage	V_{OL}		I_{OL}=0.3mA				0.4	V
Input Leakage Current	I_{LI}	GND≦V_{IN}≦V_{CC}		LP,YD,SHL,SEL,LSEL,CSE L,F1,F2,DOFF,TEST1, FR			2.0	μA
Input / Output Leakage Current	$I_{LI/O}$	GND≦V_{IN}≦V_{CC}		CIO1,CIO2			5.0	μA
Static Current	I_{GND}	V_{DDH} = 14.0~42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND			25	μA
Output Resistance	R_{COM}	△V_{ON} =0.5V Recommended parameter	V_{DDH}= +30.0V	COM 1 to COM 120		0.55	0.7	μA
			V_{DDH}= +40.0V			0.5	0.7	μA
Average Operating Consumption Current (1)	I_{CC}	V_{CC}=+5.0V,V_{IH}=V_{CC},V_{IL}=GND,f_{LP}=16.8 kHz,f_{FR}=70Hz,Input data: 1/240No load		V_{CC}		10	25	pF
		V_{CC} =3.0 V All other parameters the same as V_{CC}=5.0 V.				7	17	pF
Average Operating Consumption Current (2)	I_{DDH}	V_{DDH}=+V_1=+30.0V,V_C=$V_{DDH}/2$,–V_1=0.0 V,V_{CC}= 5.0 V All other parameters the same as the I_{CC} item.		V_{DD}H		6	13	
Input Terminal Capacity	C_I	Freq.= 1 MHZ Chip alone Ta = 25℃		LP,YD,SHL,SEL,LSEL,CSE L,F1,F2,DOFF,TEST1,FR			10	
Input / Output Terminal Capacity	$C_{I/O}$			CIO1,CIO2			18	

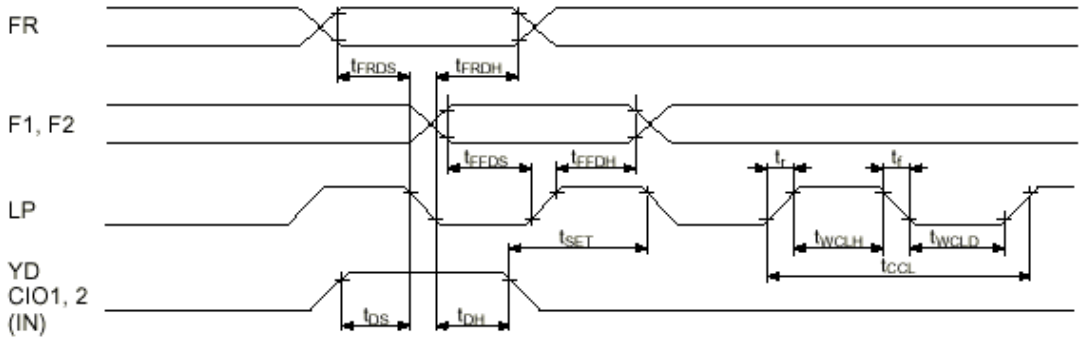
Range of Operating Voltages: V_{CC} – V_{DDH}

It is necessary to set the voltage for V_{DDH} within the V_{CC} – V_{DDH} operating voltage range shown in the diagram below.



AC Characteristics

Input Timing Characteristics



The FR latched at the nth LP is reflected in the output at the n+1th LP.

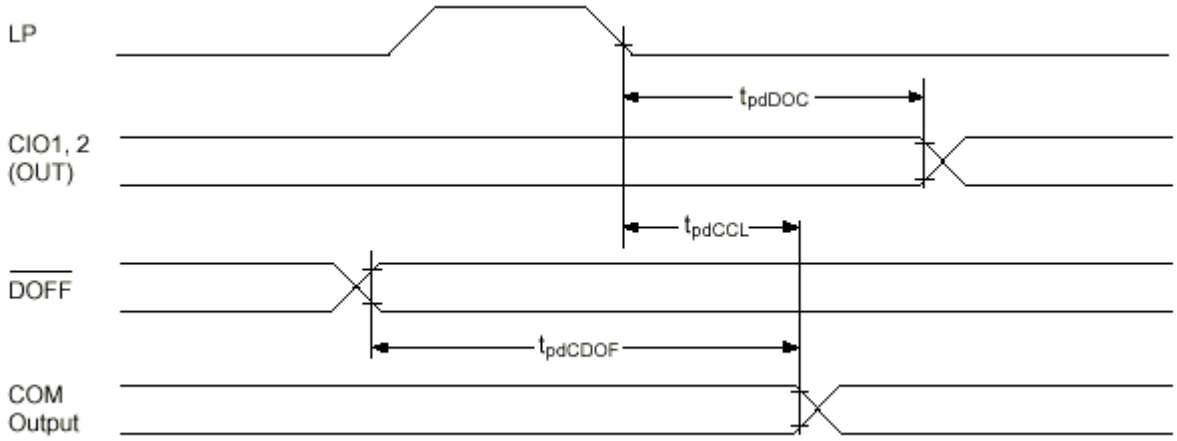
(VCC = +5.0 V± 10%, Ta = –30 to +85℃)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	tCCL		500		ns
LP "H" Pulse Width	tWCLH		55		ns
LP "L" Pulse Width	tWCLL		330		ns
FR Setup Time	tFRDS		100		ns
FR Hold Time	tFRDH		40		ns
F1, F2 Setup Time	tFFDS		100		ns
F1, F2 Hold Time	tFFDH		40		ns
Input Signal Rise Time	tr			50	ns
Input Signal Fall Time	tf			50	ns
CIO Setup Time	tDS		100		ns
CIO Hold Time	tDH		40		ns
YD→LP Allowable Time	tSEL		80		ns

(VCC = +2.7 V to 4.5 V, Ta = –30 to +85℃)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	tCCL		800		ns
LP "H" Pulse Width	tWCLH		100		ns
LP "L" Pulse Width	tWCLL		660		ns
FR Setup Time	tFRDS		200		ns
FR Hold Time	tFRDH		80		ns
F1, F2 Setup Time	tFFDS		200		ns
F1, F2 Hold Time	tFFDH		80		ns
Input Signal Rise Time	tr			100	ns
Input Signal Fall Time	tf			100	ns
CIO Setup Time	tDS		200		ns
CIO Hold Time	tDH		80		ns
YD→LP Allowable Time	tSEL		150		ns

Output Timing Characteristics



(VCC = 5.0 V± 10%, VDDH = +14.0 to +42.0 V, Ta = –30 to +85C)

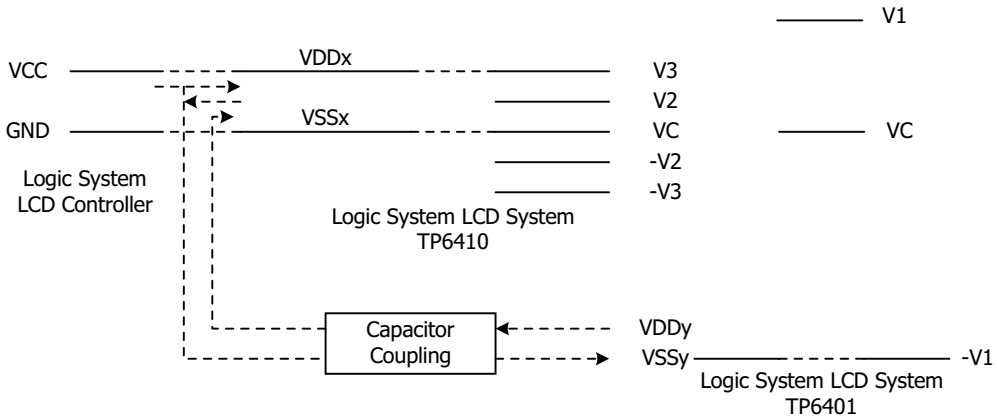
Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	CL = 15 pF		600	ns
Delay time from LP to COM output	t_{pdCCL}	V_{DDH}=14.0V to 40.0 V		500	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			1400	ns

(VCC = +2.7 V to 4.5 V, VDDH = +14.0 to +28.0 V, Ta = –30 to +85C)

Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	CL = 15 pF		600	ns
Delay time from LP to COM output	t_{pdCCL}	V_{DDH}=14.0V to 40.0 V		500	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			1400	ns

The Power Supply

Method of Forming Each Voltage Level



When the TP6410 and the TP6401 are used to form an extremely low power module system, the power relationships as shown in the figure above between the TP6410 and TP6401 logic systems, and the LCD system power supply, and the LCD controller power supply are optimal.

In this case, care is required when it comes to signal propagation in the logic system.

LCD Controller → TP6410Direct

LCD Controller → TP6401Capacitor coupling is required

TP6410 → TP6401Capacitor coupling is required

TP6401 → TP6410Capacitor coupling is required

Cautions at Power Up and Power Down

Because the voltage level in the LCD system is high voltage, if the logic system power supply of this LSI is floating or if VCC is 2.6 V or less when the LCD system high voltage (30 V or above) is applied , or if the LCD drive signal is output before the voltage level that is applied to the LCD system has stabilized , then there is the risk that there will be an over current condition in this LSI, resulting in permanent damage to this LSI.

It is recommended that the display OFF function (DOFF) is used until the LCD system voltage stabilizes to insure that the LCD drive output power level is at the VC level.

Be sure to follow the sequences below when turning the power supplies ON and OFF:

When turning the power supply ON:

Logic system ON → LCD drive system ON, or simultaneously ON.

When turning the power supply OFF:

LCD drive system OFF → Logic system OFF, or simultaneously OFF.

As a countermeasure to guard against over current conditions, it is effective to insert a high-speed fuse or a guard resistance in series with the LC power supply. The guard resistance value must be optimized depending on the capacity of the LC cell.

Example of Connection

Large Screen LCD Structure Diagram