PCK351

1:10 clock distribution device with 3-State outputs

1. Description

The PCK351 is a high-performance 3.3 V LVTTL clock distribution device. The PCK351 enables a single clock input to be distributed to ten outputs with minimum output skew and pulse skew. The use of distributed V_{CC} and GND pins in the PCK351 ensures reduced switching noise.

The PCK351 is characterized for operation over the supply range 3.0 V to 3.6 V, and over the industrial temperature range −40 to +85 °C.

2. Features

- 1:10 LVTTL clock distribution
- Low output to output skew
- Low output pulse skew
- Over voltage tolerant inputs and outputs
- LVTTL-compatible inputs and outputs
- Distributed V_{CC} and ground pins reduce switching noise
- Balanced High-drive outputs (−32 mA I_{OH}, 32 mA I_{OL})
- Reduced power dissipation due to the state-of-the-art QUBiC-LP process
- Supply range of +3.0 V to +3.6 V
- Package options include plastic small-outline (D) and shrink small-outline (DB) packages
- Industrial temperature range −40 to +85 °C
- PCK351 is identical to and replaces PTN3151.

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3. Quick reference data

Table 1:   Quick reference data

GND = 0 V; T_{amb} = 25 °C; t_r = $t_f \leq$ 3.0 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}/t_{PLH}	propagation delay: A to Y_n	C_L = 50 pF; V_{CC} = 3.3 V	3.1	3.6	4.1	ns
C_I	input capacitance	V_I = V_{CC} or GND	-	4	-	pF
C_O	output capacitance	V_I = V_{CC} or GND	-	6	-	pF
C_{PD}	power dissipation capacitance[1]	C_L = 50 pF; f = 1 MHz	-	48	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;
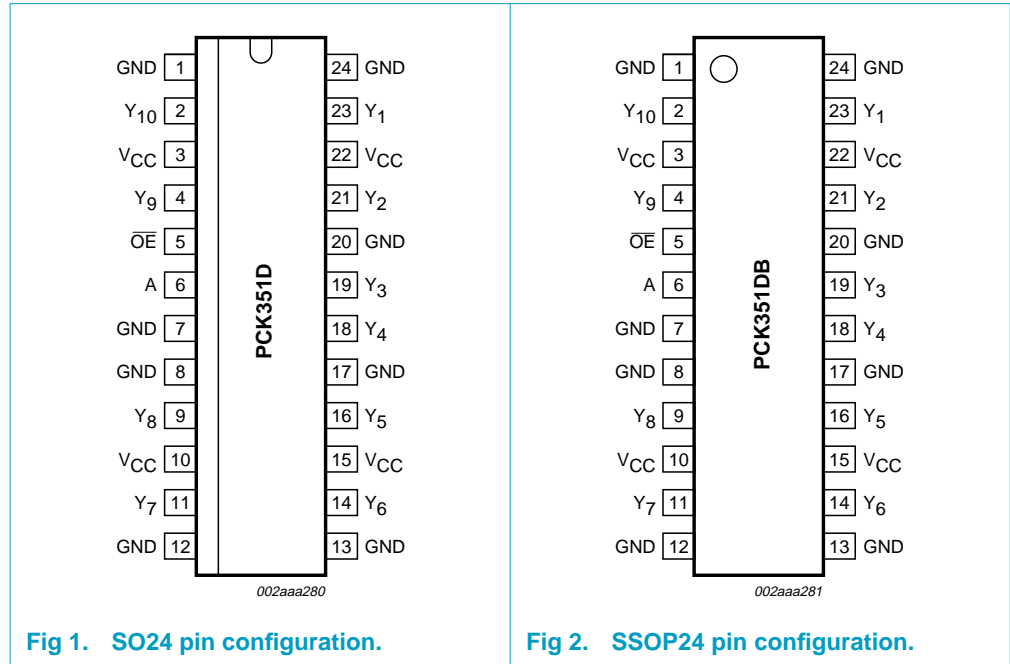
V_{CC} = supply voltage in Volts.

4. Ordering information

Table 2:   Ordering information

Type number	Package			
	Name	**Description**		**Version**
PCK351D	SO24	plastic small outline package; 24 leads; body width 7.5 mm		SOT137-1
PCK351DB	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm		SOT340-1

9397 750 09791

Product data   **Rev. 01 — 14 May 2002**   **2 of 17**

5. Pinning information

5.1 Pinning

Fig 1. SO24 pin configuration.

Fig 2. SSOP24 pin configuration.

5.2 Pin description

Table 3: **Pin description**

Symbol	Pin	Description
GND	1, 7, 8, 12, 13, 17, 20, 24	ground (0 V)
Y_{10} to Y_1	2, 4, 9, 11, 14, 16, 18, 19, 21, 23	outputs
V_{CC}	3, 10, 15, 22	supply voltage
$\overline{OE}$	5	output enable input (Active-LOW)
A	6	data input

6. Functional description

6.1 Function table

Table 4:   Function table

Inputs		Outputs
A	**$\overline{OE}$**	**Y_n**
L	H	Z
H	H	Z
L	L	L
H	L	H

[1]   H = HIGH voltage level;

L = LOW voltage level;

Z = high-impedance OFF-state.

6.2 Logic symbol

Fig 3.   Logic symbol.

6.3 Logic diagram

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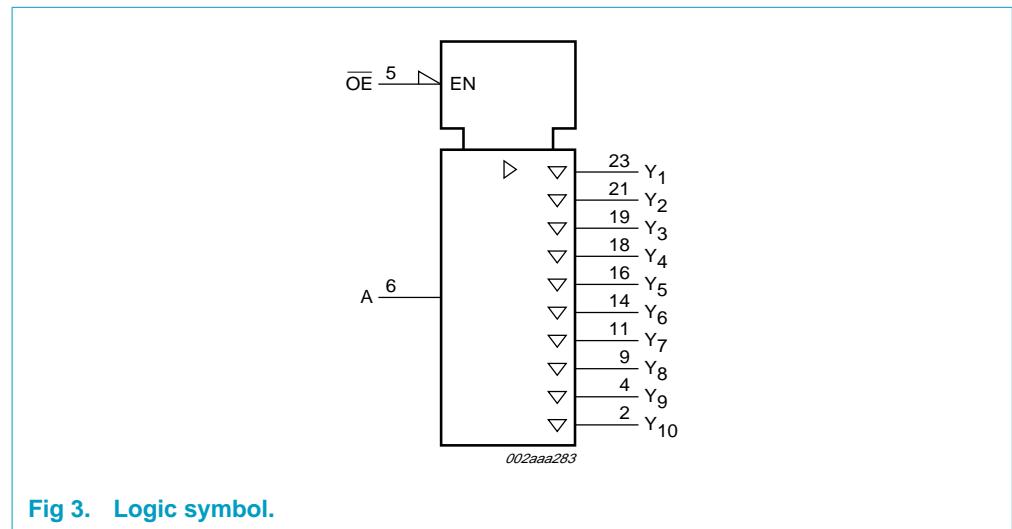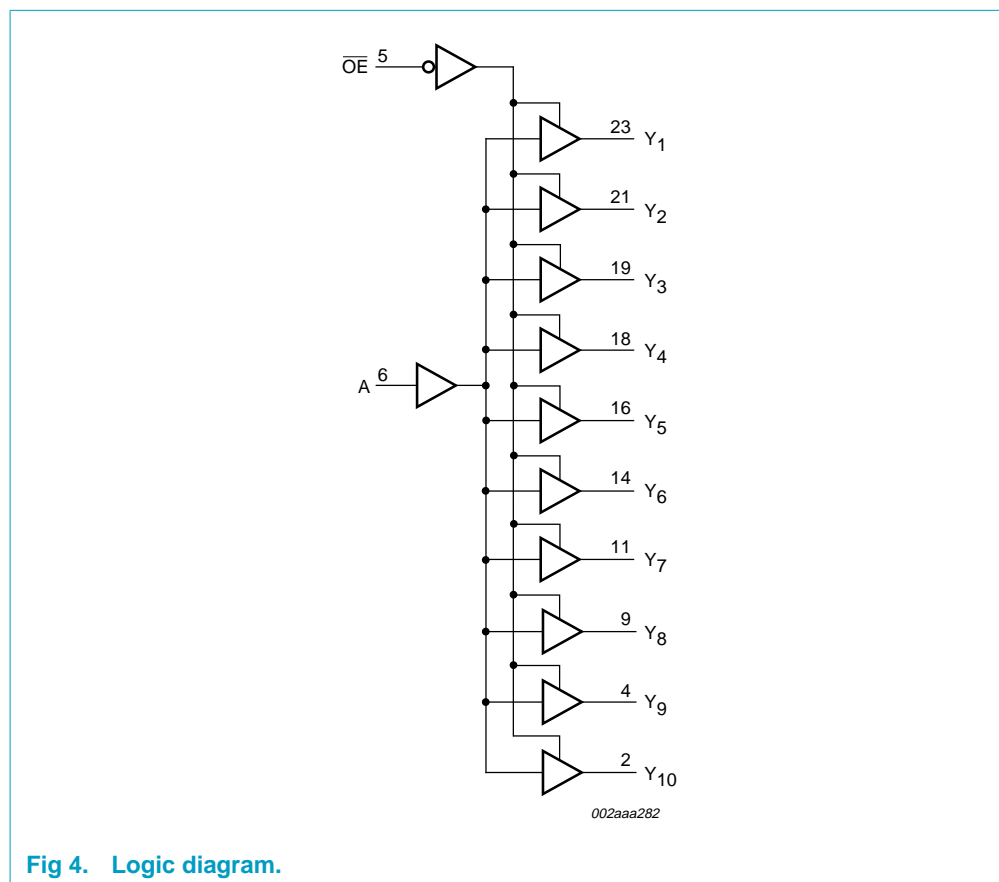**Fig 4.   Logic diagram.**

7. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1], [2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage range		−0.5	+4.6	V
V_I	input voltage range	[3]	−0.5	+7.0	V
V_O	output voltage range	[3]	−0.5	+3.6	V
I_{IK}	input clamp current	$V_I < 0$ V	-	−18	mA
I_{OK}	output clamp current	$V_I < 0$ V	-	−50	mA
I_O	output sink current		-	64	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±75	mA
T_{stg}	storage temperature		−65	+150	°C
P_D	maximum power dissipation				
	SO package	$T_{amb} = +55$ °C	-	0.65	W
	SSOP package	$T_{amb} = +55$ °C	-	1.7	W

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 'recommended operating conditions' is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] The input and output negative voltage ratings may be exceeded if the input and output clamp currents are observed.

8. Recommended operating conditions

Table 6: Recommended operating conditions

See note 1.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		3.0	3.6	V
V_{IH}	HIGH-level input voltage		2.0	5.5	V
V_I	input voltage		0	0.8	V
T_{amb}	ambient temperature	see Table 7 "DC characteristics" and Table 8 "AC characteristics" per device	−40	+85	°C
t_r, t_f	input rise and fall times	$V_{CC} = 3.3 \pm 0.3$ V	-	100	ns/V

[1] Unused pins (input or I/O) must be held HIGH or LOW.

9. Static characteristics

Table 7: **DC characteristics**

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	input diode voltage	V_{CC} = 3.0 V; I_I = −18 mA		-	-	−1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 3.0 V; I_{OH} = −32 mA		2.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 3.0 V; I_{OL} = 32 mA		-	-	0.5	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; V_I = GND or 5.5 V		-	-	±1.0	µA
I_{LO}	output leakage current	V_{CC} = 3.6 V; V_O = 2.5 V		−15	-	−150	mA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6 V; V_O = 3 V	[1]	-	-	±10	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0; outputs HIGH		-	-	0.3	mA
		V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0; outputs LOW		-	-	25	mA
		V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0; outputs disabled		-	-	0.3	mA
C_I	input capacitance	V_{CC} = 3.3 V; V_I = V_{CC} or GND; f = 10 MHz		-	4	-	pF
C_O	output capacitance	V_{CC} = 3.3 V; V_O = V_{CC} or GND; f = 10 MHz		-	6	-	pF

[1]   Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

10. Dynamic characteristics

Table 8: **AC characteristics**

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} = 3.3 V; T_{amb} = 25 °C						
t_{PLH}/t_{PHL}	propagation delay A to Y_n	C_L = 50 pF; see Figures 5 and 8	3.1	3.6	4.1	ns
t_{PZH}/t_{PZL}	propagation delay $\overline{OE}$ to Y_n	C_L = 50 pF; see Figures 6 and 8	1.8	3.8	5.5	ns
t_{PHZ}/t_{PLZ}	propagation delay $\overline{OE}$ to Y_n	C_L = 50 pF; see Figures 6 and 8	1.8	4.0	5.9	ns
$t_{sk(o)}$	output-to-output skew A to Y_n	C_L = 50 pF; see Figures 7 and 8	-	0.3	0.5	ns
$t_{sk(p)}$	pulse skew A to Y_n	C_L = 50 pF; see Figures 7 and 8	-	0.2	0.8	ns
$t_{sk(pr)}$	part-to-part skew A to Y_n	C_L = 50 pF; see Figures 7 and 8	-	-	1	ns
t_r	rise time A to Y_n	C_L = 50 pF; see Figures 5 and 8	-	-	-	ns
t_f	fall time A to Y_n	C_L = 50 pF; see Figures 5 and 8	-	-	-	ns
V_{CC} = 3.3 to 3.6 V; T_{amb} = 0 °C to +70 °C						
t_{PLH}/t_{PHL}	propagation delay A to Y_n	C_L = 50 pF; see Figures 5 and 8	-	-	-	ns
t_{PZH}/t_{PZL}	propagation delay $\overline{OE}$ to Y_n	C_L = 50 pF; see Figures 6 and 8	1.3	-	5.9	ns
t_{PHZ}/t_{PLZ}	propagation delay $\overline{OE}$ to Y_n	C_L = 50 pF; see Figures 6 and 8	1.7	-	6.3	ns
$t_{sk(o)}$	output-to-output skew A to Y_n	C_L = 50 pF; see Figures 7 and 8	-	-	0.5	ns
$t_{sk(p)}$	pulse skew A to Y_n	C_L = 50 pF; see Figures 7 and 8	-	-	0.8	ns
$t_{sk(pr)}$	part-to-part skew A to Y_n	C_L = 50 pF; see Figures 7 and 8	-	-	1	ns
t_r	rise time A to Y_n	C_L = 50 pF; see Figures 5 and 8	-	-	1.5	ns
t_f	fall time A to Y_n	C_L = 50 pF; see Figures 5 and 8	-	-	1.5	ns

Table 9: **Switching characteristics**

Temperature and V_{CC} coefficients over recommended operating free-air temperature and V_{CC} range; note 1.

Symbol	Parameter	Conditions	Max	Unit
$\Delta t_{PLH(T)}$	temperature coefficient of LOW-to-HIGH propagation delay A to Y_n (average value)	note 2	65	ps/10 °C
$\Delta t_{PHL(T)}$	temperature coefficient of HIGH-to-LOW propagation delay A to Y_n (average value)	note 2	45	ps/10 °C
$\Delta t_{PLH(V)}$	V_{CC} coefficient of LOW-to-HIGH propagation delay A to Y_n (average value)	note 3	−140	ps/100 mV
$\Delta t_{PHL(V)}$	V_{CC} coefficient of HIGH-to-LOW propagation delay A to Y_n (average value)	note 3	−120	ps/100 mV

[1] These data were extracted from characterization material and are not tested at the factory.

[2] $\Delta t_{PLH(T)}$ and $\Delta t_{PHL(T)}$ are virtually independent of V_{CC}.

[3] $\Delta t_{PLH(V)}$ and $\Delta t_{PHL(V)}$ are virtually independent of temperature.

9397 750 09791

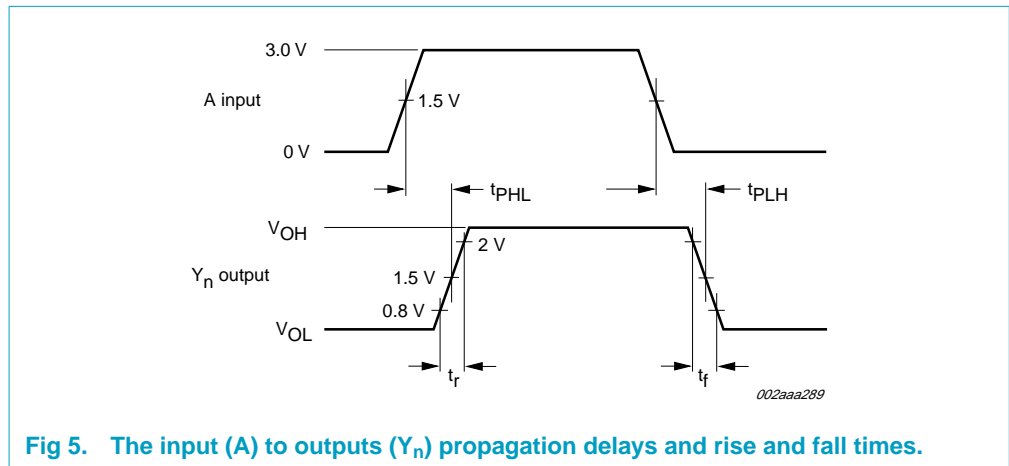**Product data** **Rev. 01 — 14 May 2002** **8 of 17**

10.1 AC waveforms

Fig 5. The input (A) to outputs (Y$_n$) propagation delays and rise and fall times.

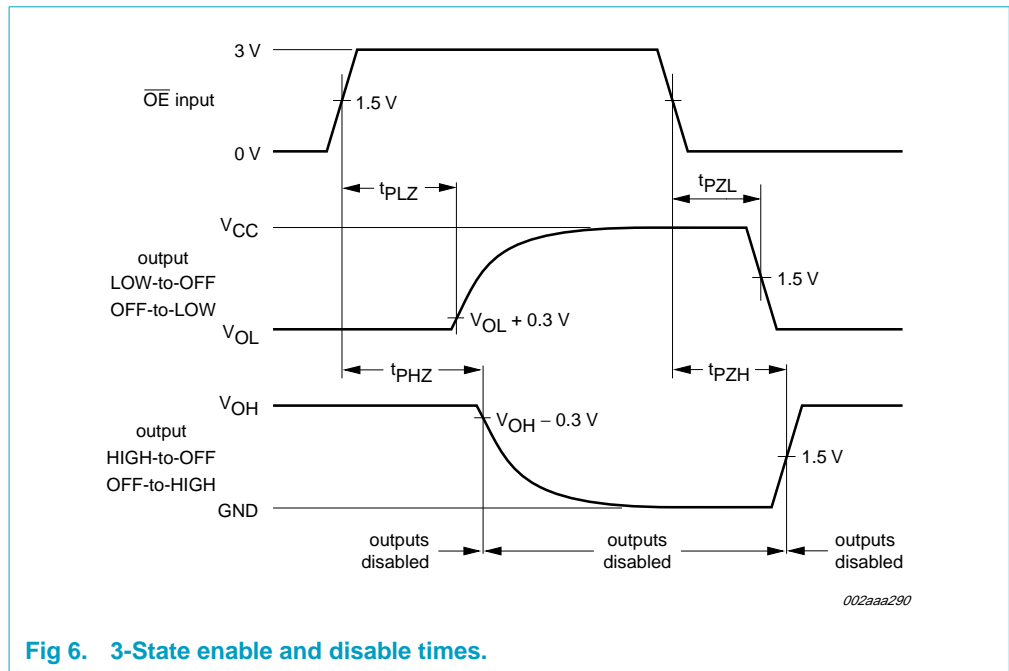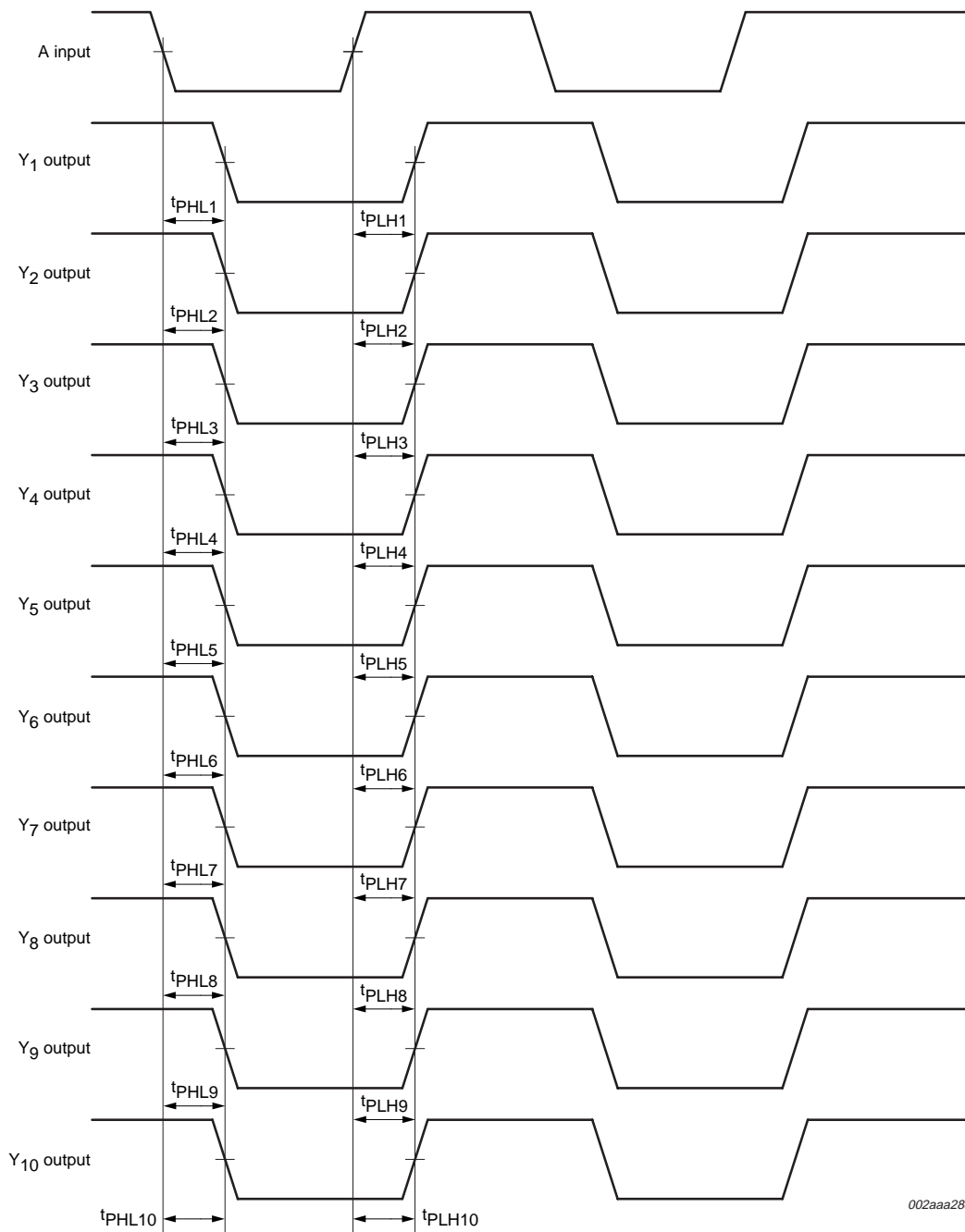**Fig 6.** 3-State enable and disable times.

(1) Output-to-output skew is the highest values of positive and negative edge skew:

$t_{sk(o)} = t_{PLHn(max)} - t_{PLHn(min)}$ and $t_{sk(o)} = t_{PHLn(max)} - t_{PHLn(min)}$ for n = 1 to 10.

(2) Output pulse skew is the highest value of: $t_{sk(p)} = |t_{PLHn} - t_{PHLn}|$ for n = 1 to 10.

(3) Part-to-part skew $t_{sk(pr)}$ represents the positive and negative edge skew between outputs of several devices operating under identical conditions.

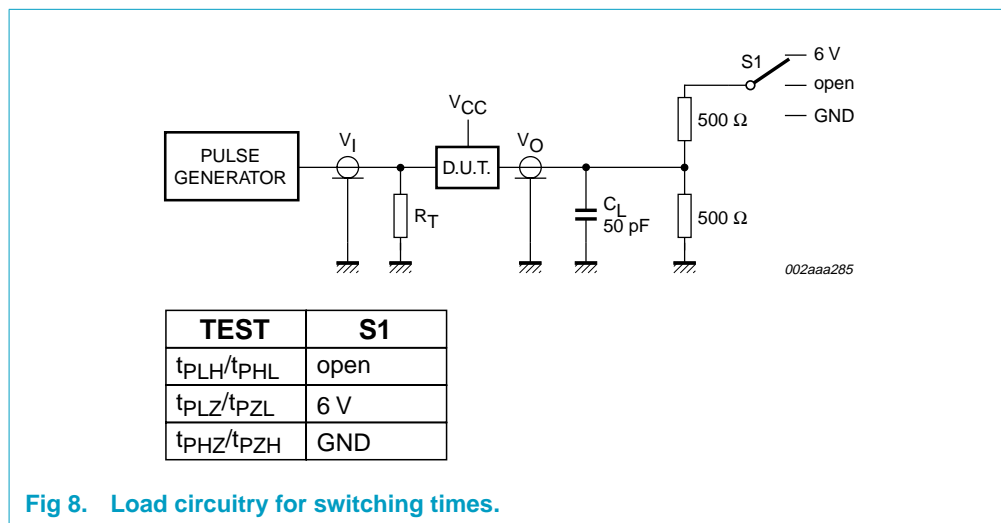**Fig 7. Calculation of $t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$.**

TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

Fig 8.   Load circuitry for switching times.

11. Package outline

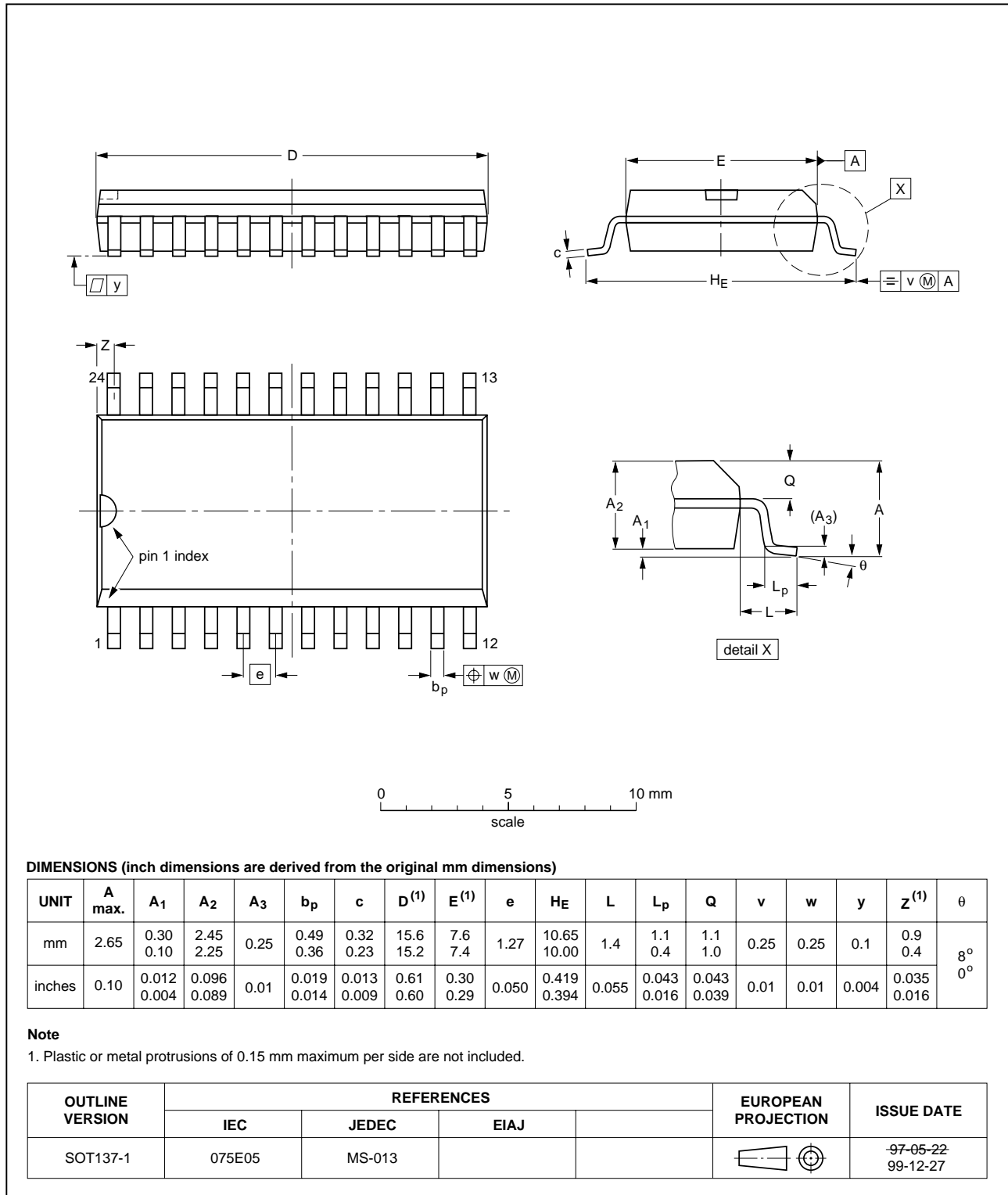**SO24: plastic small outline package; 24 leads; body width 7.5 mm**   **SOT137-1**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(1)	e	Hₑ	L	Lₚ	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

Fig 9. SO24 package outline (SOT137-1).

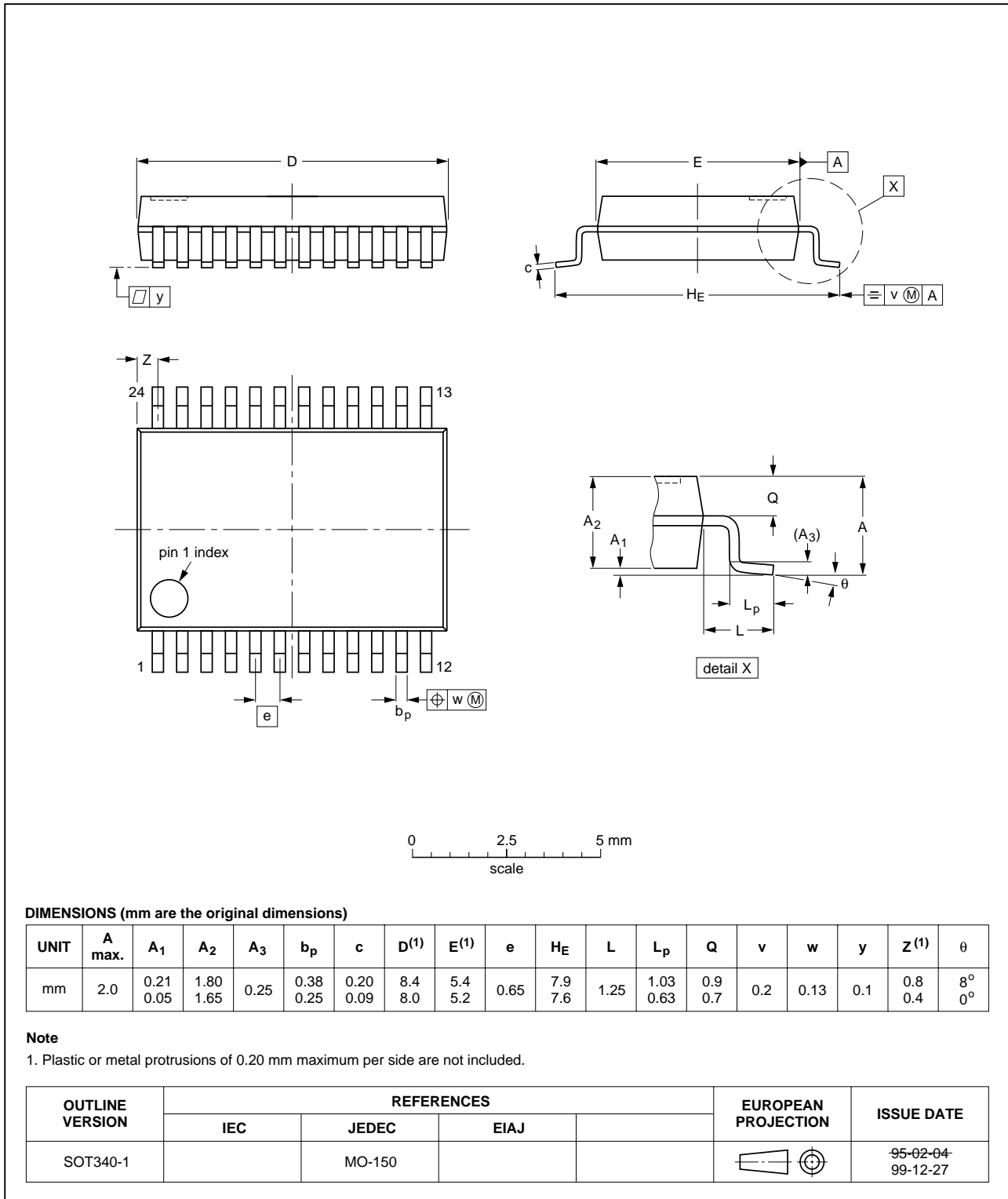**SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm**

SOT340-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				95-02-04 99-12-27

Fig 10. SSOP24 package outline (SOT340-1).

12. Soldering

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

9397 750 09791

Product data **Rev. 01 — 14 May 2002** **14 of 17**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

12.5 Package related soldering information

Table 10: **Suitability of surface mount IC packages for wave and reflow soldering methods**

Package[1]	Soldering method	
	Wave	**Reflow**[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

13. Revision history

Table 11: **Revision history**

Rev	Date	CPCN	Description
01	20020514	-	Product data; initial version. Engineering Change Notice 853-2344 28198.

14. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

15. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contents

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