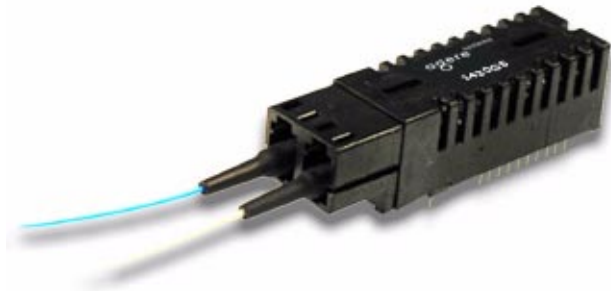


NetLight® 1430G5 Type SONET/SDH Long-Reach Transceivers with Clock Recovery



Available in a small form factor, plastic package, the 1430G5 are high-performance, cost-effective transceivers for SONET/SDH long-reach applications at 155 Mbits/s.

Features

- SONET LR-1/SDH L1.1 Compliant (ITU-T G.957 Specifications)
- Small form factor, RJ-45 size, multisourced 20-pin package
- Requires single 3.3 V power supply
- Clock recovery
- Fiber pigtail
- Uncooled 1300 nm laser transmitter with automatic output power control
- Transmitter disable input
- Analog alarm outputs

- Wide dynamic range receiver with InGaAs PIN photodetector
- LVTTTL signal-detect output
- Low power dissipation
- Raised ECL (LVPECL) logic data interfaces
- Operating case temperature range: -40°C to $+85^{\circ}\text{C}$
- Agere Systems Inc. Reliability and Qualification Program for built-in quality and reliability

Description

The 1430G5-Type transceiver is a high-speed, cost-effective optical transceiver that is compliant with the International Telecommunication Union Telecommunication (ITU-T) G.957 specifications for use in SONET and SDH long-reach applications. The 1430G5 operates at the OC-3/STM-1 rate of 155 Mbits/s. The transceiver features Agere Systems' optics and is packaged in a narrow-width plastic housing with two 1 meter fiber pigtails terminated with LC connectors. The 20-pin package and pinout conform to a multisource transceiver agreement.

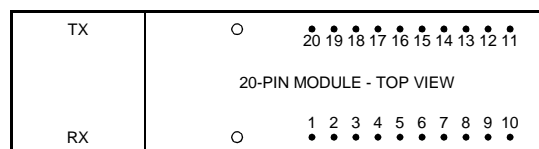
The transmitter features differential LVPECL logic level data inputs, a LVTTTL logic level disable input. The receiver features differential LVPECL logic level data and clock outputs, and a LVTTTL logic level signal-detect output.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCC	0	3.6	V
Operating Case Temperature Range	T _C	-40	85	°C
Storage Case Temperature Range	T _{stg}	-40	85	°C
Lead Soldering Temperature/Time	—	—	250/10	°C/s
Operating Wavelength Range	λ	1.1	1.6	nm

Pin Information



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Figure 1. 1430G5 and 1430H5-Type Transceivers, 20-Pin Configuration, Top View

Table 1. Transceiver Pin Descriptions

Pin Number	Symbol	Name/Description	Logic Family
Receiver			
MS	MS	Mounting Studs. The mounting studs are provided for transceiver mechanical attachment to the circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground.	NA
1	Photodetector Bias	Photodetector Bias. This lead supplies bias for the PIN photodetector diode.	NA
2	VEER	Receiver Signal Ground.	NA
3	VEER	Receiver Signal Ground.	NA
4	CLK-	Received Recovered Clock Out. The rising edge occurs at the rising edge of the received data output. The falling edge occurs in the middle of the received data bit period.	LVPECL
5	CLK+	Received Recovered Clock Out. The falling edge occurs at the rising edge of the received data output. The rising edge occurs in the middle of the received data bit period.	LVPECL
6	VEER	Receiver Signal Ground.	NA
7	VCCR	Receiver Power Supply.	NA
8	SD	Signal Detect. Normal operation: logic one output. Fault condition: logic zero output.	LVTTTL
9	RD-	Received DATA Out. No Internal terminations will be provided.	LVPECL
10	RD+	Received DATA Out. No internal terminations will be provided.	LVPECL

Pin Information (continued)

Table 1. Transceiver Pin Descriptions (continued)

Pin Number	Symbol	Name/Description	Logic Family
Transmitter			
11	VCCT	Transmitter Power Supply.	NA
12	VEET	Transmitter Signal Ground.	NA
13	TDIS	Transmitter Disable.	LVTTTL
14	TD+	Transmitter DATA In.	LVPECL
15	TD-	Transmitter DATA In Bar.	LVPECL
16	VEET	Transmitter Signal Ground.	NA
17	Bmon-	Laser Diode Bias Current Monitor—Negative End. The laser bias current is accessible as a dc-voltage by measuring the voltage developed across pins 17 and 18.	NA
18	BMON+	Laser Diode Bias Current Monitor—Positive End. See pin 17 description.	NA
19	PMON-	Laser Diode Optical Power Monitor—Negative End. The back-facet diode monitor current is accessible as a dc-voltage by measuring the voltage developed across pins 19 and 20.	NA
20	PMON+	Laser Diode Optical Power Monitor—Positive End. See pin 19 description.	NA

Electrostatic Discharge

Caution: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow EIA[®] Standard EIA-625.

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Agere Systems employs a human-body model (HBM) for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 k Ω , capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold established for the 1430G5 transceiver is ± 1000 V.

Application Information

The 1430 receiver section is a highly sensitive fiber-optic receiver. Although the data outputs are digital logic levels (LVPECL), the device should be thought of as an analog component. When laying out system application boards, the 1430 transceiver should receive the same type of consideration one would give to a sensitive analog component.

Printed-Wiring Board Layout Considerations

A fiber-optic receiver employs a very high gain, wide bandwidth transimpedance amplifier. This amplifier detects and amplifies signals that are only tens of nA in amplitude when the receiver is operating near its sensitivity limit. Any unwanted signal currents that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's signal detect (SD) circuit. To minimize the coupling of unwanted noise into the receiver, careful attention must be given to the printed-wiring board.

At a minimum, a double-sided printed-wiring board (PWB) with a large component-side ground plane beneath the transceiver must be used. In applications that include many other high-speed devices, a multi-layer PWB is highly recommended. This permits the placement of power and ground on separate layers, which allows them to be isolated from the signal lines.

Multilayer construction also permits the routing of sensitive signal traces away from high-level, high-speed signal lines. To minimize the possibility of coupling noise into the receiver section, high-level, high-speed signals such as transmitter inputs and clock lines should be routed as far away as possible from the receiver pins.

Application Information (continued)

Noise that couples into the receiver through the power supply pins can also degrade performance. It is recommended that the pi filter, shown in Figure 3, be used for both the transmitter and receiver power supplies.

Data, Clock, and Signal Detect Outputs

The data, clock, and signal detect outputs of the 1430 transceiver are driven by open-emitter NPN transistors, which have an output impedance of approximately 7 Ω. Each output can provide approximately 50 mA maximum current to a 50 Ω load terminated to VCC – 2.0 V.

Due to the high switching speeds of ECL outputs, transmission line design must be used to interconnect components. To ensure optimum signal fidelity, both data outputs (RD+/RD–) and clock outputs (CLK+/CLK–) should be terminated identically. The signal lines connecting the data clock outputs to the next device should be equal in length and have matched impedances. Controlled impedance stripline or microstrip construction must be used to preserve the quality of the signal into the next component and to minimize reflections back into the receiver, which could degrade

its performance. Excessive ringing due to reflections caused by improperly terminated signal lines makes it difficult for the component receiving these signals to decipher the proper logic levels and can cause transitions to occur where none were intended. Also, by minimizing high-frequency ringing, possible EMI problems can be avoided.

The signal-detect output is LVTTTL logic. A logic low at this output indicates that the optical signal into the receiver has been interrupted or that the light level has fallen below the minimum signal detect threshold. This output should not be used as an error rate indicator, since its switching threshold is determined only by the magnitude of the incoming optical signal.

Transceiver Processing

The transceiver and plug can withstand normal wave soldering and aqueous spray cleaning processes. However, the transceiver is not hermetic, and should not be subjected to immersion in cleaning solvents. The transceiver case should not be exposed to temperatures in excess of 125 °C. The fiber pigtail cannot exceed 85 °C. The transceiver pins can be wave soldered at 250 °C for up to 10 seconds.

Transceiver Optical and Electrical Characteristics

Table 2. Transmitter Optical and Electrical Characteristics (Tc = –40 °C to +85 °C; Vcc = 3.135 V—3.465 V)

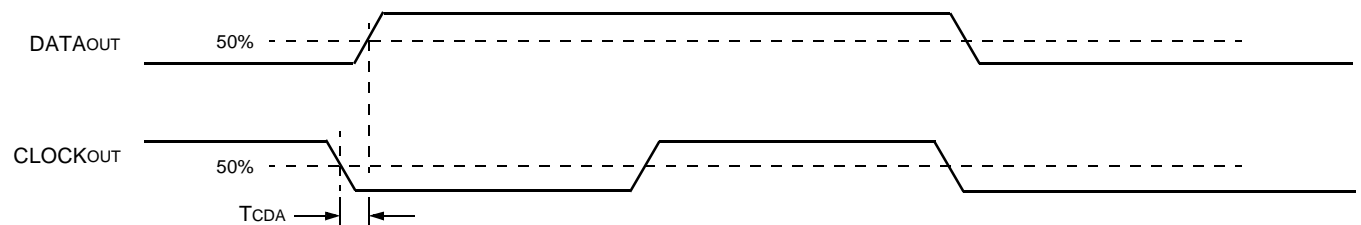
Parameter	Symbol	Min	Max	Unit
Average Optical Output Power L-1.1	Po	–5.0	0	dBm
Optical Wavelength L-1.1	λc	1280	1335	nm
Spectral Width	Δλ20	—	1	nm
Side-mode Suppression Ratio	SMSR	30	—	dB
Dynamic Extinction Ratio	EXT	10	—	dB
Power Supply Current	ICCT	—	200	mA
Input Data Voltage:				
Low	VIL	VCC – 1.810	VCC – 1.475	V
High	VIH	VCC – 1.165	VCC – 0.880	V
Transmit Disable Voltage	VD	VCC – 1.165	VCC	V
Transmit Enable Voltage	VEN	VEE	VEE + 0.8	V
Laser Bias Voltage	VBIAS	0	0.70	V
Laser Back-facet Monitor Voltage	VBF	0.01	0.20	V

Application Information (continued)

Table 3. Receiver Optical and Electrical Characteristics (Tc = -40 °C to +85 °C; Vcc = 3.135 V—3.465 V)

Parameter	Symbol	Min	Max	Unit
Average Sensitivity: L-1.1	PI	—	-34	dBm
Maximum Input Power L-1.1*	P _{MAX}	-10	—	dBm
Link Status Switching Threshold: Decreasing Light L-1.1	LST _D	-45	-35	dBm
Increasing Light L-1.1	LST _I	—	-34.5	dBm
Link Status Hysteresis	HYS	0.5	6.0	dB
Power Supply Current	ICCR	—	200	mA
Output Data Voltage/Clock Voltage: Low	V _{OL}	V _{CC} - 1.86	V _{CC} - 1.50	V
High	V _{OH}	V _{CC} - 1.025	V _{CC} - 0.88	V
Signal Detect Output Voltage: Low	V _{OL}	0.0	0.8	V
High	V _{OH}	2.4	V _{CC}	V
Clock Duty Cycle	DC	45	55	%
Output Clock Random Jitter	J _c	—	0.01	UI
Output Clock Random Jitter Peaking	J _p	—	0.1	dB
Clock/Data Alignment L-1.1 (See Figure 2.)	TCDA	-0.8	0.8	ns
Jitter Tolerance/Jitter Transfer	<i>Telcordia Technologies™</i> GR-253-CORE and ITU-TG.958 Compliant			

* For 1×10^{-10} BER with an optical input using $2^{23} - 1$ PRBS.



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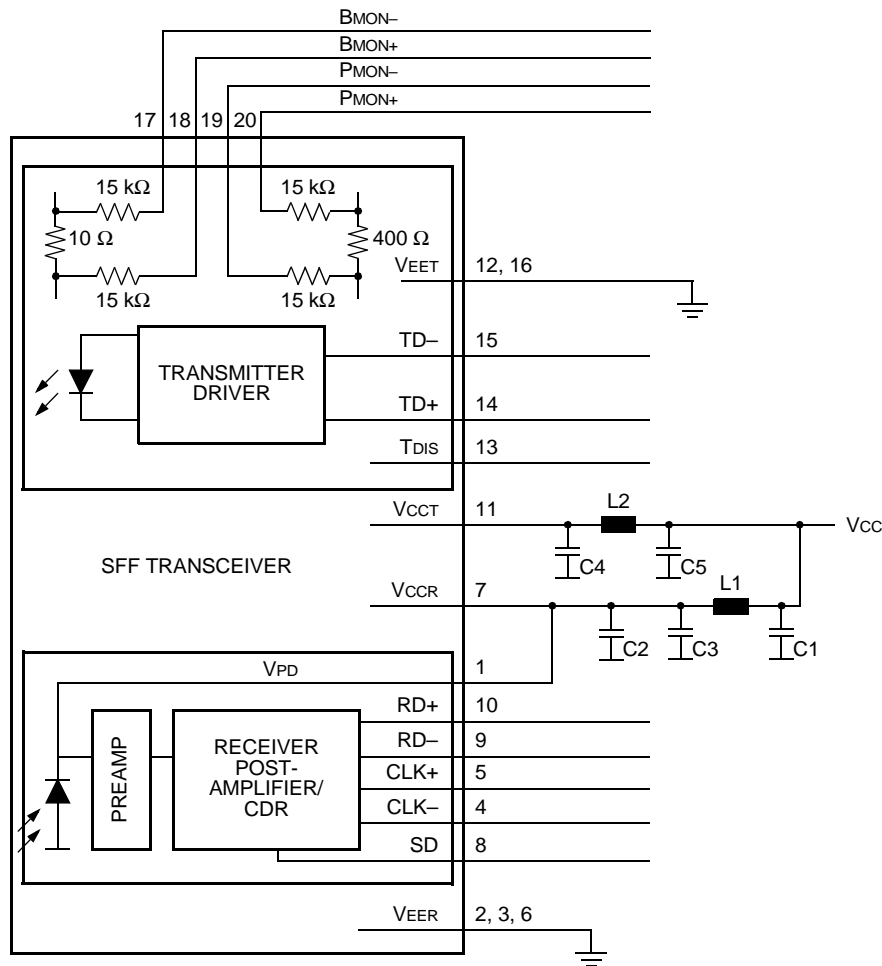
Figure 2. Clock/Data Alignment

Qualification and Reliability

To help ensure high product reliability and customer satisfaction, Agere Systems is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronic modules are qualified to Agere Systems' internal standards using MIL-STD-883 test methods and procedures and using sampling techniques consistent with *Telcordia Technologies* requirements. The 1430 transceiver is required to pass an extensive and rigorous set of qualification tests.

This qualification program fully meets the intent of *Telcordia Technologies* reliability practices GR-468-CORE requirements. In addition, the design, development, and manufacturing facilities of Agere Systems' Optoelectronics unit have been certified to be in full compliance with the latest *ISO*[®]-9001 quality system standards.

Electrical Schematic



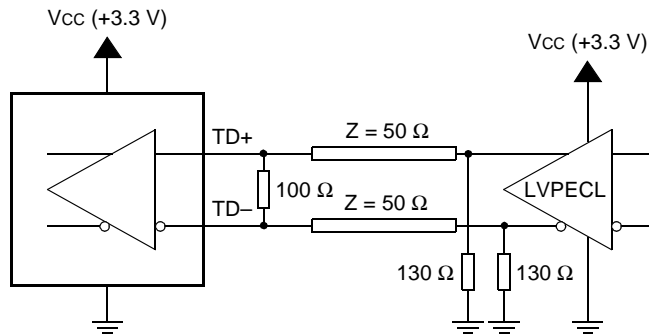
- Notes:
 L1 = L2 = 1 μ H—4.7 μ H*
 C1 = C2 = 10 nF†
 C3 = 4.7 μ F—10 μ F
 C4 = C5 = 4.7 μ F—10 μ F

* Ferrite beads can be used as an option.
 † For all capacitors, MLC caps are recommended.

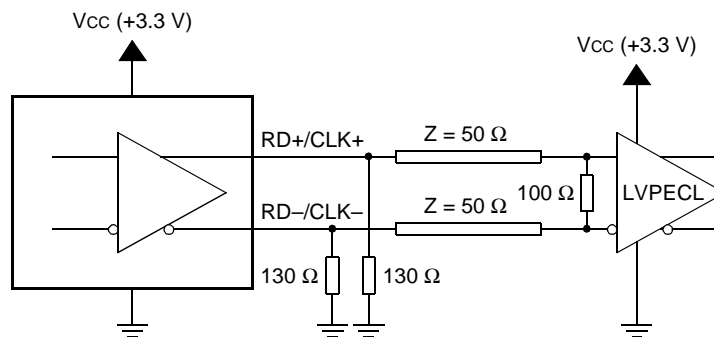
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Figure 3. Power Supply Filtering for the Small Form Factor Transceiver

Application Schematics



A. Transmitter Interface (LVPECL to LVPECL)



B. Receiver Interface (LVPECL to LVPECL)

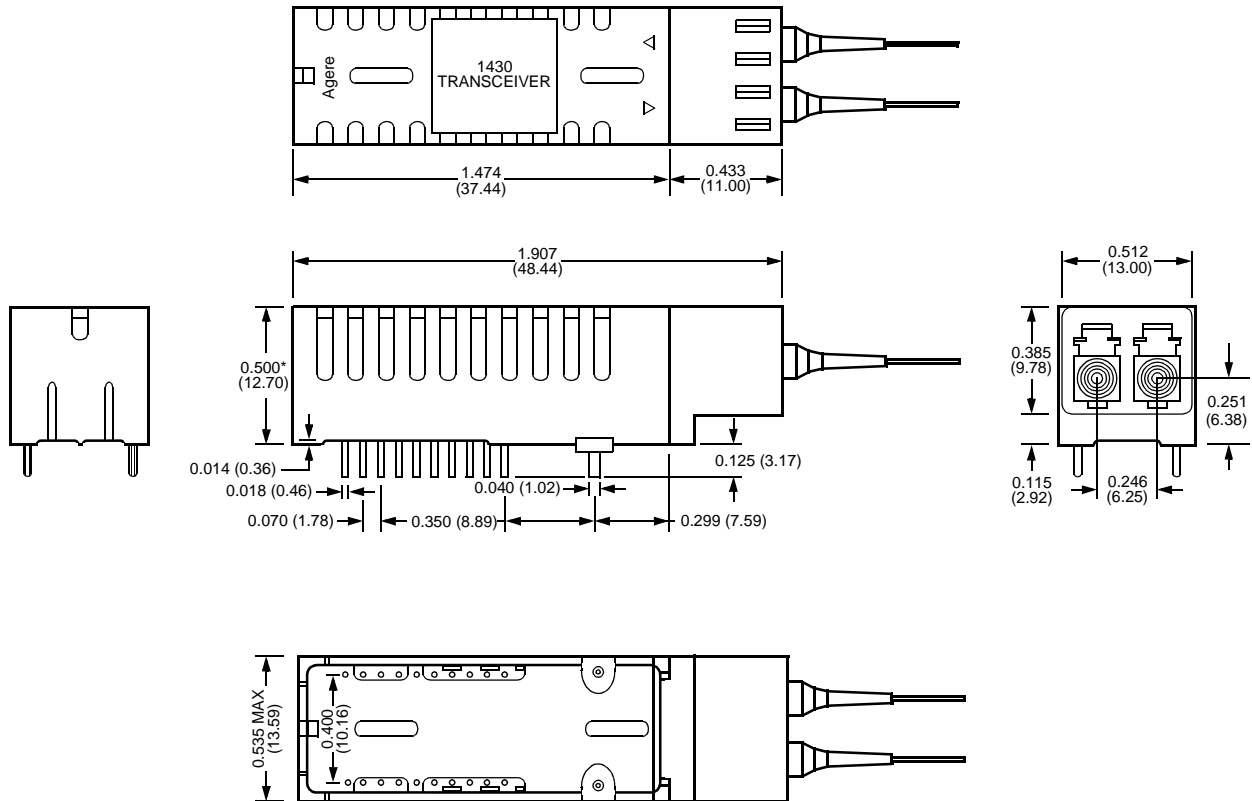
Figure 4. 3.3 V Transceiver Interface with 3.3 V ICs

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Outline Diagrams

Package Outline

Dimensions are in inches and (millimeters).



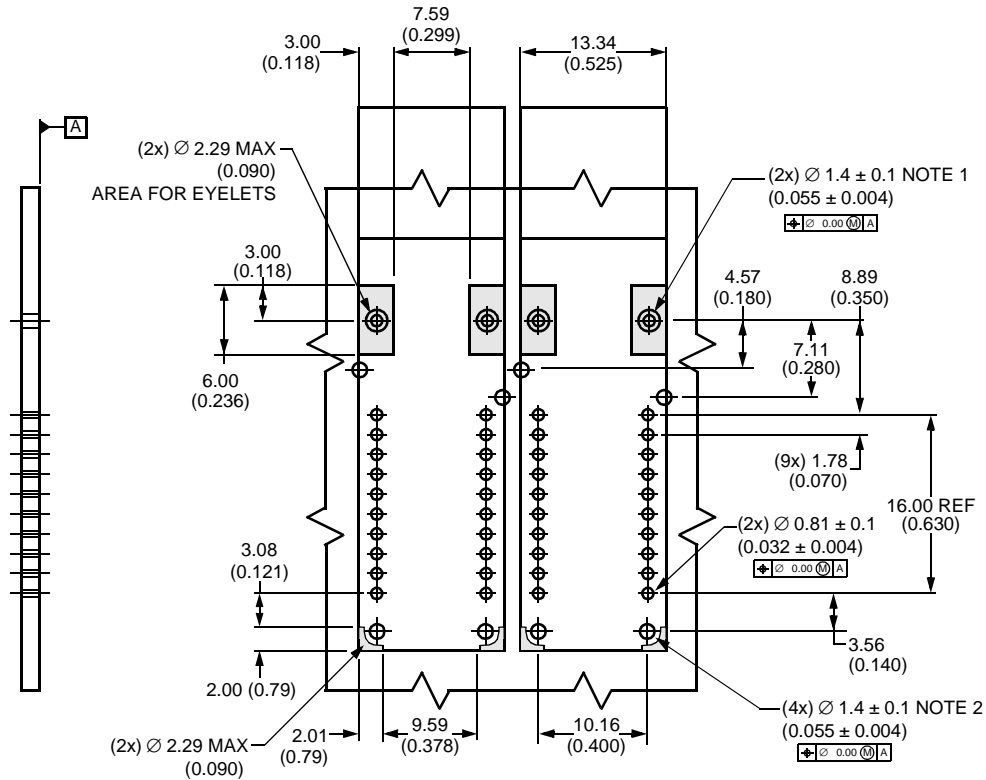
* Dimension does not comply with multisource agreement.

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Outline Diagrams (continued)

Printed-Wiring Board Layout *, †

Dimensions are in inches and (millimeters).



NOTES:

1. HOLES FOR MOUNTING STUDS MUST BE TIED TO CHASSIS GROUND.
2. HOLES FOR HOUSING LEADS MUST BE TIED TO SIGNAL GROUND.

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* The hatched areas are keep-out areas reserved for housing standoffs. No metal traces of ground connection in keep-out area.
† Twenty-pin module shown; 10-pin module requires only 16 PWB holes.

Laser Safety Information

Class I Laser Product

FDA/CDRH Class I laser product. All versions of the transceiver are Class I laser products per CDRH, 21 CFR 1040 Laser Safety requirements. All versions are Class I laser products per IEC[®] 60825-1:1993. The transceiver has been classified with the FDA under accession number 8720009.

CAUTION: Use of controls, adjustments, and procedures other than those specified herein may result in hazardous laser radiation exposure.

This product complies with 21 CFR 1040.10 and 1040.11.
8.8 μm/125 μm single-mode fiber pigtails and connector

Wavelength = 1.3 μm
Maximum power = 1.6 mW

Because of size constraints, laser safety labeling is not affixed to the module but is attached to the outside of the shipping carton.

Product is not shipped with power supply.

NOTICE
Unterminated optical connectors may emit laser radiation. Do not view with optical instruments.

Ordering Information

Description	Device Code	Comcode
2x10 Single-mode Transceiver for OC-3 /STM-1 Long-reach (155 Mbits/s) with Fiber Pigtails and LC Connector	1430G5LL	108455049

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IEC is a registered trademark of the International Electrotechnical Commission.

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