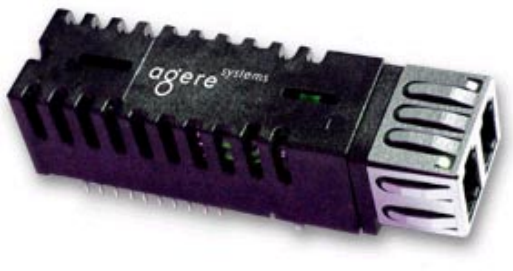
Data Sheet
August 2001

NetLight® 1417K5A 2.5 Gbits/s 1300 nm Laser Transceiver with Clock and Data Recovery



Available in a small form factor, RJ-45 size, plastic package, the 1417K5A Transceiver is a high-performance, cost-effective, optical transceiver for SONET/SDH applications.

Features

- Small form factor, RJ-45 size, 20-pin package
- LC duplex receptacle
- Uncooled 1300 nm laser transmitter with automatic output power control
- Transmitter disable input
- Wide dynamic range receiver with InGaAs PIN photodetector
- Recovered clock outputs
- TTL signal-detect output
- Low power dissipation
- Single 3.3 V power supply
- LVPECL/CML compatible data inputs and CML compatible data outputs
- Operating temperature range: 0 °C to 70 °C
- Agere Systems Inc. Reliability and Qualification Program for built-in quality and reliability

Applications

- SONET SR OC-48, SDH I-16 applications
- High-speed, optical data interface for shelf-to-shelf interconnect

Description

The 1417K5A transceiver is a high-speed, cost-effective optical transceiver intended for 2.488 Gbits/s shelf-to-shelf optical interconnect applications as well as SONET SR OC-48 and SDH I-16. The transceiver features proven Agere Systems optics and is packaged in a narrow-width plastic housing with an LC duplex receptacle. The receptacle fits into an RJ-45 form factor outline. The 20-pin package pinout conforms to a multisource transceiver agreement.

The transmitter features the ability to interface to both LVPECL and CML differential logic level data inputs. The transmitter also features a TTL logic level disable input and laser bias and back-facet monitor outputs. The receiver features differential CML logic level data and clock outputs, a TTL logic level signal-detect output and direct access to the PIN photodetector bias input for photocurrent monitoring purposes.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	0	5	V
Operating Temperature Range	T_C	0	70	°C
Storage Temperature Range	T_{stg}	–40	85	°C
Lead Soldering Temperature/Time	—	—	250/10	°C/s
Operating Wavelength Range	λ	1.1	1.6	µm

Qualification and Reliability

To help ensure high product reliability and customer satisfaction, Agere Systems is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronic modules are qualified to Agere Systems internal standards as well as other appropriate industry standards using MIL-STD-883 test methods and procedures, and using sampling techniques consistent with *Telcordia*® requirements.

In addition, Agere Systems has been certified to be in full compliance with the latest *ISO*® -9001 Quality System Standards.

Pin Information

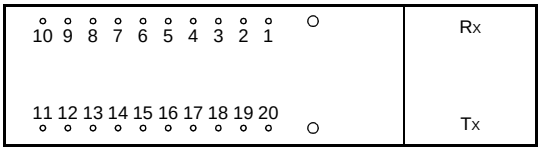


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Figure 1. 1417K5A Transceiver, 20-Pin Configuration (top view)

Pin Information

Table 1. Transceiver Pin Descriptions

Pin Number	Symbol	Name/Description	Logic Family
		Receiver	
MS	MS	**Mounting Studs.** The mounting studs are provided for transceiver mechanical attachment to the circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground.	NA
1	V_{PD}	**Photodetector Bias Input.** This lead supplies bias for the PIN photodetector diode	NA
2	V_{EER}	**Receiver Signal Ground.**	NA
3	V_{EER}	**Receiver Signal Ground.**	NA
4	CLK–	**Received Recovered $\overline{\text{Clock}}$ Out.** The rising edge occurs at the rising edge of the Received Data output. The falling edge occurs in the middle of the Received Data baud period.	CML
5	CLK+	**Received Recover Clock Out.** The falling edge occurs at the rising edge of the Received Data output. The rising edge occurs in the middle of the Received Data baud period.	CML
6	V_{EER}	**Receiver Signal Ground.**	NA
7	V_{CCR}	**Receiver Power Supply.**	NA
8	SD	**Signal Detect.** Normal operation: logic 1 output. Fault condition: logic 0 output	LVTTL
9	RD–	**Received $\overline{\text{DATA}}$ Out.**	CML
10	RD+	**Received DATA Out.**	CML
		Transmitter	
11	V_{CCT}	**Transmitter Power Supply.**	NA
12	V_{EET}	**Transmitter Signal Ground.**	NA
13	T_{DIS}	**Transmitter Disable.**	LVTTL
14	TD+	**Transmitter DATA In**. An internal 50 Ω termination is provided, consisting of a 100 Ω resistor between the TD+ and TD– pins.	LVPECL/CML
15	TD–	**Transmitter $\overline{\text{DATA}}$ In**. See TD+ pin for terminations.	LVPECL/CML
16	NIC	**No Internal Connection.**	NA
17	B_{MON}–	**Laser Diode Bias Current Monitor, Negative End.** The laser bias current is accessible as a dc voltage by measuring the voltage developed across pins 17 and 18.	NA
18	B_{MON}+	**Laser Diode Bias Current Monitor, Positive End.** Optional feature; if not used, do not connect. See pin 17 description.	NA
19	P_{MON}–	**Laser Diode Optical Power Monitor, Negative End.** Optional feature; if not used, do not connect. The back-facet diode monitor current is accessible as a voltage proportional to the photocurrent through a 200 Ω resistor between pins 19 and 20.	NA
20	P_{MON}+	**Laser Diode Optical Power Monitor, Positive End.** Optional feature; if not used, do not connect. See pin 19 description.	NA

Electrostatic Discharge

Caution: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow *EIA*® Standard *EIA*-625.

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Agere Systems employs a human-body model (HBM) for ESD susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold established for the 1417K5A transceiver is ±1000 V.

Application Information

The 1417 receiver section is a highly sensitive fiber-optic receiver. Although the data outputs are digital logic levels (CML), the device should be thought of as an analog component. When laying out system application boards, the 1417 transceiver should receive the same type of consideration typically given to a sensitive analog component.

Printed-Wiring Board Layout Considerations

A fiber-optic receiver employs a very high gain, wide-bandwidth transimpedance amplifier. This amplifier detects and amplifies signals that are only tens of nA in amplitude when the receiver is operating near its sensitivity limit. Any unwanted signal currents that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's signal detect (SD) circuit. To minimize the coupling of unwanted noise into the receiver, careful attention must be given to the printed-wiring board.

At a minimum, a double-sided printed-wiring board (PWB) with a large component-side ground plane beneath the transceiver must be used. In applications that include many other high-speed devices, a multilayer PWB is highly recommended. This permits the placement of power and ground on separate layers, which allows them to be isolated from the signal lines. Multilayer construction also permits the routing of sensitive signal traces away from high-level, high-speed signal lines. To minimize the possibility of coupling noise into the receiver section, high-level, high-speed signals such as transmitter inputs and clock lines should be routed as far away as possible from the receiver pins.

Noise that couples into the receiver through the power supply pins can also degrade performance. It is recommended that a pi filter, shown in Figure 4, be used for both the transmitter and receiver power supplies.

Data, Clock, and Signal Detect Outputs

Due to the high switching speeds of CML outputs, transmission line design must be used to interconnect components. To ensure optimum signal fidelity, both data outputs should be terminated identically. The signal lines connecting the data outputs to the next device should be equal in length and have matched impedances. Controlled impedance stripline or microstrip construction must be used to preserve the quality of the signal into the next component and to minimize reflections back into the receiver, which could degrade its performance. Excessive ringing due to reflections caused by improperly terminated signal lines makes it difficult for the component receiving these signals to decipher the proper logic levels and can cause transitions to occur where none was intended. Also, by minimizing high-frequency ringing, possible EMI problems can be avoided.

The signal-detect output is positive LVTTL logic. A logic low at this output indicates that the optical signal into the receiver has been interrupted or that the light level has fallen below the minimum signal-detect threshold. This output should not be used as an error rate indicator, since its switching threshold is determined only by the magnitude of the incoming optical signal.

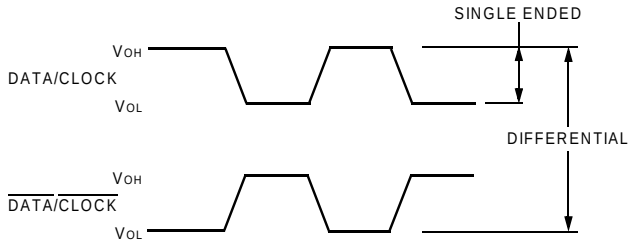

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Figure 2. Data Input/Output Logic Level Definitions

Application Information (continued)

Transceiver Processing

When the process plug is placed in the transceiver's optical port, the transceiver and plug can withstand normal wave soldering and aqueous spray cleaning processes. However, the transceiver is not hermetic, and should not be subjected to immersion in cleaning solvents. The transceiver case should not be exposed to temperatures in excess of 125 °C. The transceiver pins can be wave soldered at 250 °C for up to 10 seconds. The process plug should only be used once. After removing the process plug from the transceiver, it must not be used again as a process plug; however, if it has not been contaminated, it can be reused as a dust cover.

Transceiver Optical and Electrical Characteristics

Table 2. Transmitter Optical and Electrical Characteristics (T_A = 0 °C to 70 °C; V_{CC} = 3.135 V—3.465 V)

Parameter	Symbol	Min	Max	Unit
Average Optical Output Power (EOL)	P_O	–10.0	–3.0	dBm
Optical Wavelength	λ_C	1266	1360	nm
Spectral Width	$\Delta\lambda_{RMS}$	—	4	nm
Dynamic Extinction Ratio	EXT	8.2	—	dB
Output Optical Eye	Compliant with SONET GR-253-CORE and ITU-T G.957 Eye Mask Requirements			
Power Supply Current	I_{CCT}	—	150	mA
Input Data Voltage: Single Ended* Differential*	 V_{INp-p} V_{INp-p}	 150 300	 800 1600	 mVp-p mVp-p
Transmit Disable Voltage†	V_D	V_{CC} – 0.9	V_{CC}	V
Transmit Enable Voltage†	V_{EN}	V_{EE}	V_{EE} + 0.8	V
Laser Bias Voltage	V_{BIAS}	0.0	0.7	V
Laser Back-Facet Monitor Voltage	V_{BF}	0.01	0.2	V

* 50 Ω load, measured single ended. Differential operation is necessary for optimum performance. (See Figure 2 for visual representation.)
† TTL compatible interface.

Transceiver Optical and Electrical Characteristics (continued)

Table 3. Receiver Optical and Electrical Characteristics (T_A = 0 °C to 70 °C; V_{CC} = 3.135 V—3.465 V)

Parameter	Symbol	Min	Max	Unit
Average Sensitivity*	P_I	—	–18	dBm
Maximum Input Power*	P_{MAX}	–3	—	dBm
Power Supply Current	I_{CCR}	—	350	mA
Output Data/Clock Voltage: Single Ended† Differential†	 V_{OUTp-p} V_{OUTp-p}	 300 600	 500 1000	 mVp-p mVp-p
Clock Duty Cycle	DC	45	55	%
Output Clock Random Jitter	J_C	—	0.01	UI
Output Clock Random Jitter Peaking	J_P	—	0.1	UI
Clock/Data Alignment‡	T_{CDA}	–40	40	ps
Jitter Tolerance/Jitter Transfer	*Telcordia* GR-253-CORE and ITU-G.958 Compliant			
Signal-detect Switching Threshold: Assert Deassert	 LST_D LST_I	 –45 —	 –19 –18.5	 dBm dBm
Signal-detect Hysteresis	HYS	0.5	6	dB
Signal-detect Voltage:‡ Low High	 V_{OL} V_{OH}	 0.0 2.4	 0.8 V_{CC}	 V V
Signal-detect Response Time	SDRT	—	100	µs

* $2^{23} – 1$ PRBS with a BER of 1×10^{-10}.
† 50 Ω load, measured single ended. Differential operation is necessary for optimum performance. (See Figure 2 for visual representation.)
‡ See Figure 3.

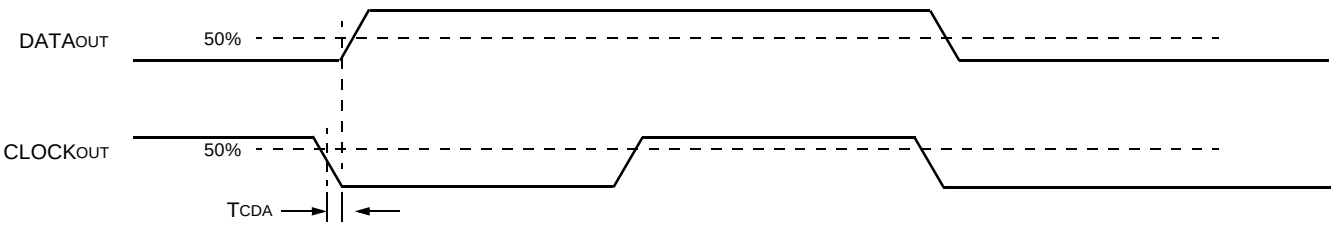

Figure 3. Clock Data/Alignment

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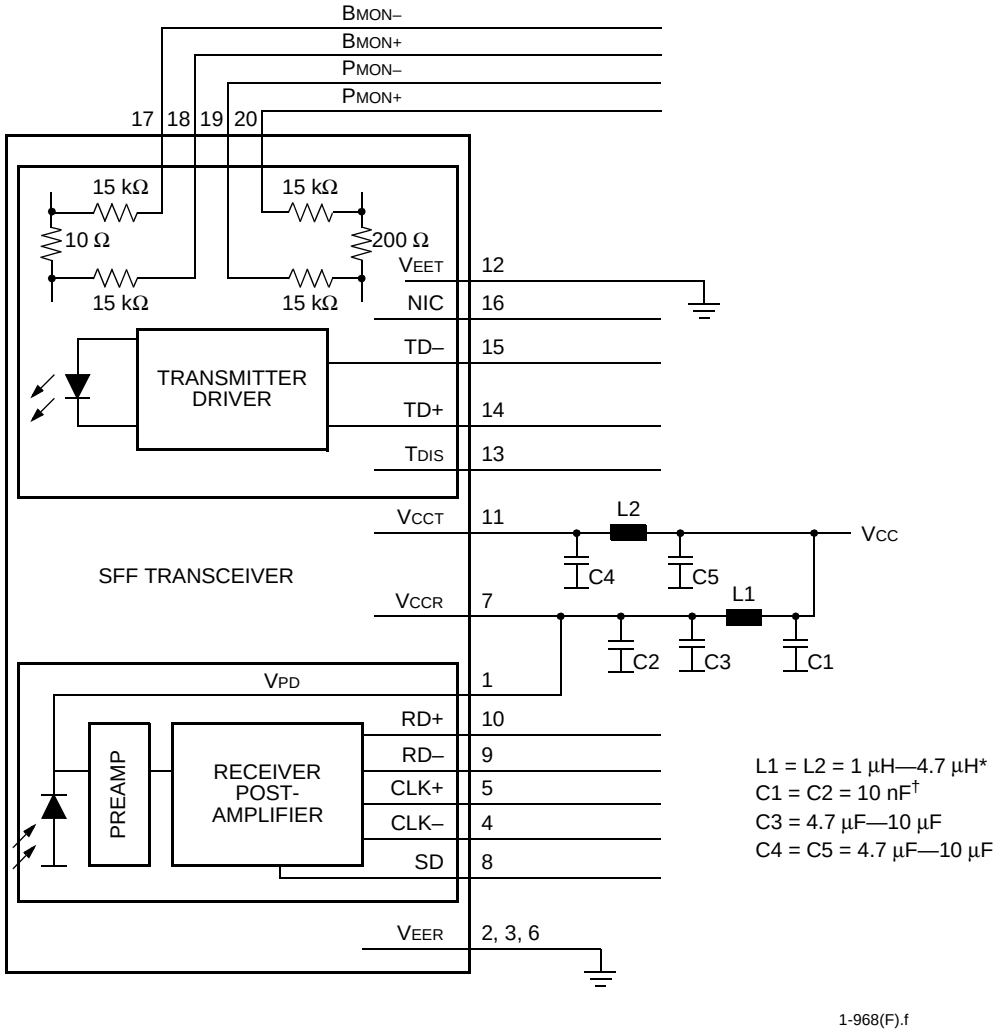
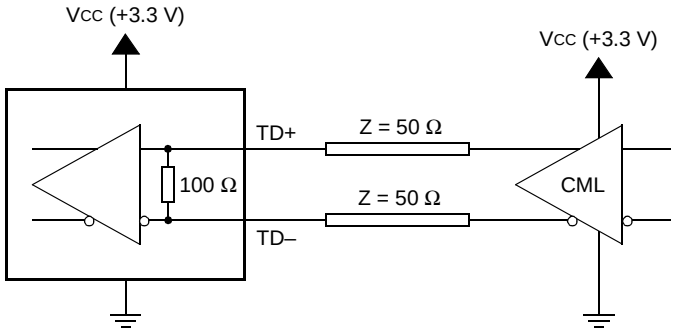
Transceiver Optical and Electrical Characteristics (continued)



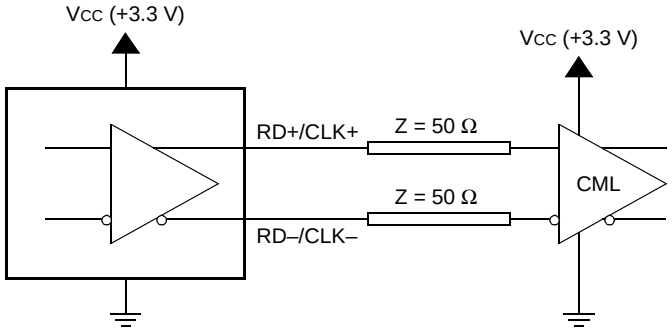
* Ferrite beads can be used as an option.
† For all capacitors, MLC caps are recommended

Figure 4. Power Supply Filtering of SFF Transceiver

Electrical Data Interface—Current Mode Logic (CML)



(A) TRANSMITTER INTERFACE—dc COUPLED—(CML)



(B) RECEIVER INTERFACE—dc COUPLED—(CML)

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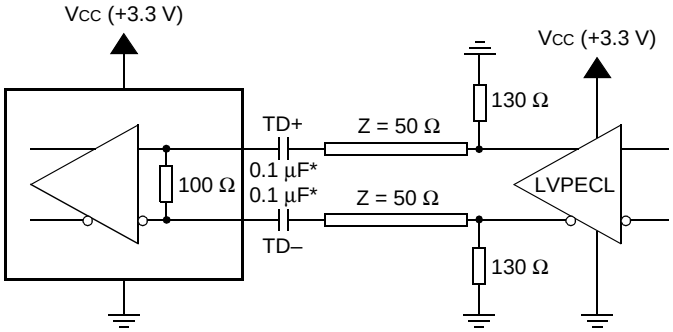
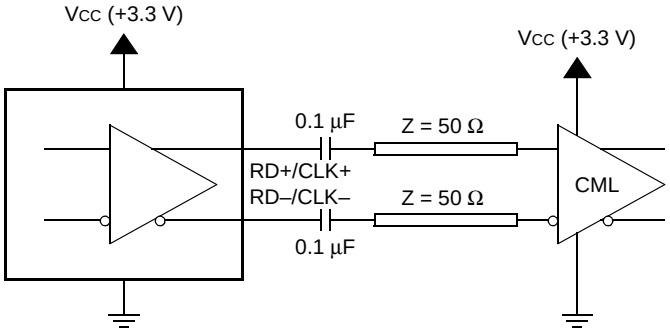
Figure 5. 3.3 V Transceiver Interface with 3.3 V ICs and CML

Alternate Electrical Data Interface Options



* Optional ac coupling capacitors; use ceramic X7R or equivalent.

(A) TRANSMITTER INTERFACE—ac OR dc COUPLED—(LVPECL)



(B) RECEIVER INTERFACE—ac COUPLED—(CML)

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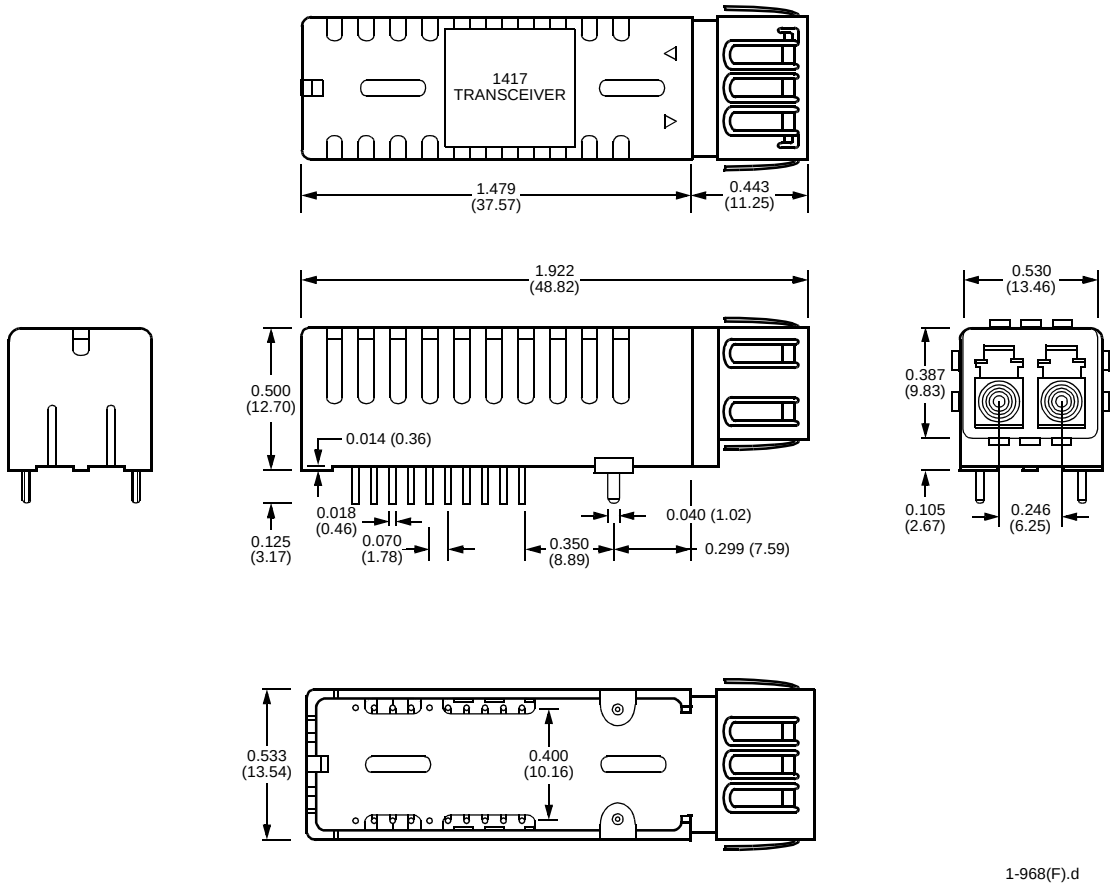
Figure 6. 3.3 V Transceiver Interface with 3.3 V ICs

Outline Diagrams

Package Outline

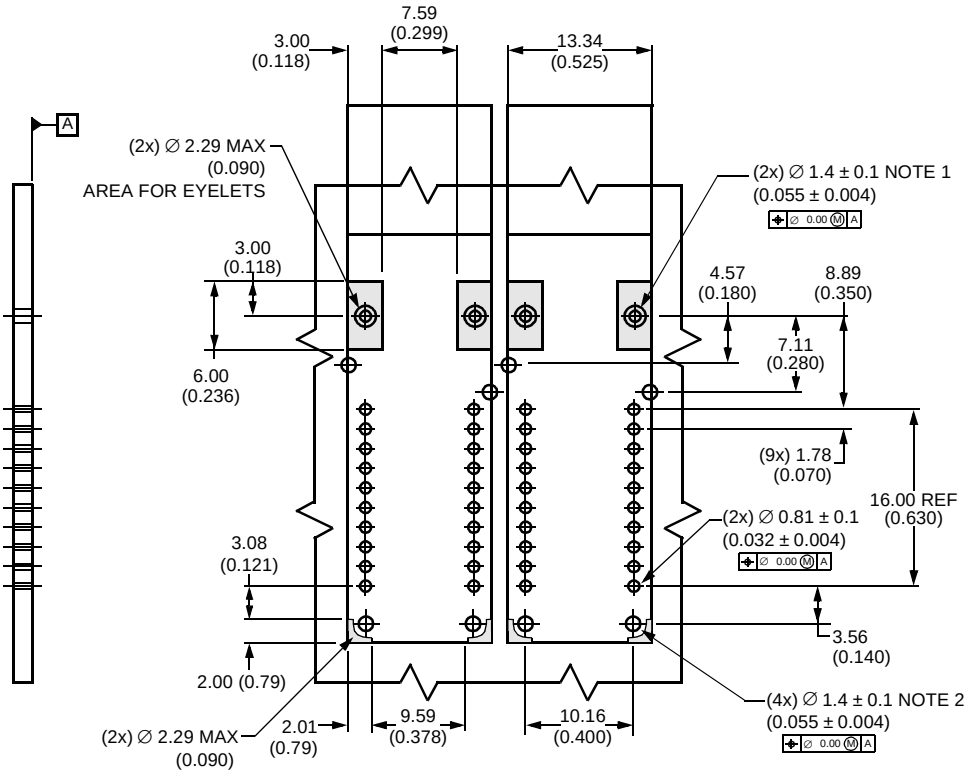
Dimensions are in inches and (millimeters).



Outline Diagrams (continued)

Printed-Wiring Board Layout *, †

Dimensions are in inches and (millimeters).



NOTES:
1. HOLES FOR MOUNTING STUDS MUST BE TIED TO CHASSIS GROUND.
2. HOLES FOR HOUSING LEADS MUST BE TIED TO SIGNAL GROUND.

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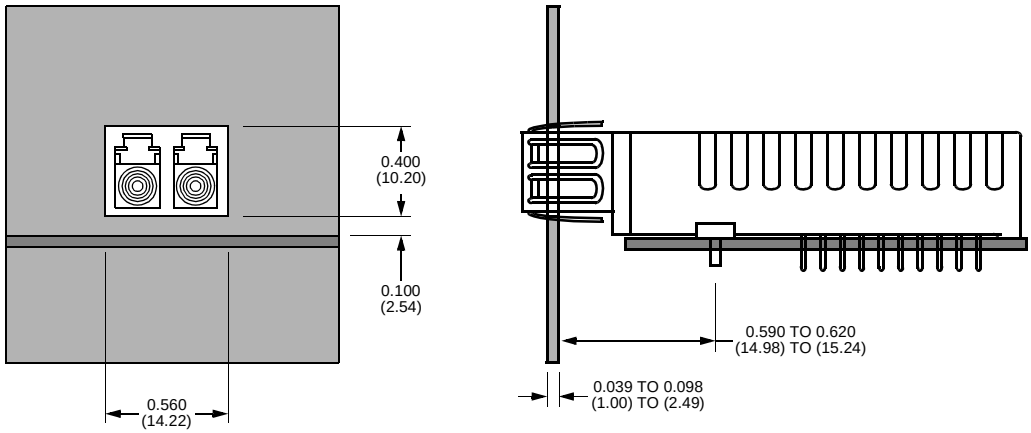
* The hatched areas are keep-out areas reserved for housing standoffs. No metal traces of ground connection in keep-out area.
† Twenty-pin module shown; 10-pin module requires only 16 PWB holes.

Outline Diagrams (continued

Recommended Panel Opening

Dimensions are in inches and (millimeters).



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Laser Safety Information

Class I Laser Product

FDA/CDRH Class I laser products. All versions of the transceiver are Class I laser products per CDRH, 21 CFR 1040 Laser Safety requirements. All versions are Class I laser products per *IEC*® 60825-1:1993. The transceiver has been certified with the FDA under accession number 9520668.

CAUTION: Use of controls, adjustments, and procedures other than those specified herein may result in hazardous laser radiation exposure.

This product complies with 21 CFR 1040.10 and 1040.11.
Wavelength = 1.3 μm
Maximum power = 1.58 mW

Product is not shipped with power supply.

NOTICE

Unterminated optical connectors may emit laser radiation.

Do not view with optical instruments.

Ordering Information

Table 4. Ordering Information

Description	Device Code	Comcode
2 X 10 Single-Mode SFF LC Receptacle Transceiver with Clock Recovery for 2.488 Gbits/s Applications	1417K5A	108748286

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ISO is a registered trademark of The International Organization for Standardization.
IEC is a registered trademark of the International Electrotechnical Commission.
EIA is a registered trademark of Electronic Industries Association.

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August 2001
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