GENERAL DESCRIPTION

EXtendar 48M (XRT95L53) is a highly integrated OC-48/STM-16, Quad OC-12/STM-4 & OC-3/STM-1 Multi-protocol Framer processor. This device combines standard OC-48/STM-16, Quad OC-12/STM-4, OC-3/STM-1 SONET framer functions with a flexible packet interface as well as a range of framing and encapsulation techniques integrated on a single chip. EXtendar 48M supports Generic Framing Procedure (GFP) in combination with Virtual Concatenation & LCAS, LAPS, POS, ATM and DS3 capabilities configurable on a per-channel basis. EXtendar 48M is the industry's first device to integrate 48 DS3/Fractional DS3 framers on a single chip. EXtendar 48M, in addition to the SONET OC-48/OC-12/OC-3 interfaces, supports OIF compliant SPI-3 interface with optional support for Exar's proprietary G-header interface. Using this industry first G-header interface, EXtendar 48M provides framing and encapsulation support for RPR, MPLS or proprietary client data that need to be transported over SONET. The unique combination of flexible packet framing and encapsulation features combined with optimal SONET transport capabilities make EXtendar 48M an ideal solution for Multi-service SONET transport, Core as well as DWDM systems.

APPLICATIONS

- Multi-Service Provisioning Platforms (MSPPs)
- SONET/SDH add/drop and terminal multiplexers
- Ethernet Over SONET Platforms (MTU/MDU)
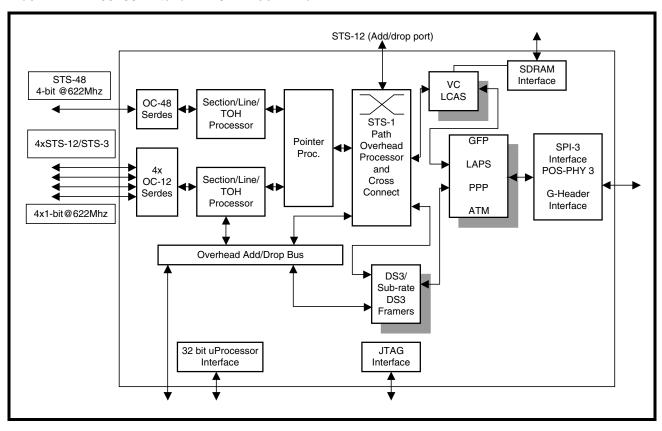- L2/L3 Switches & Routers

KEY FEATURES

- System-side Interfaces
  - Single OIF compliant SPI-3 interface with optional support for G-header interface
  - OC-12/STM-4 Serdes Interface (4x1-bit@622Mhz)
- Line-side Interfaces
  - Working and protect OC-48/STM-16 Serdes Interfaces (4-bit@622Mhz)
    - Supports TFI-5 interface
  - Quad OC-12/STM-4/OC-3/STM-1 Serdes Interfaces (4x1-bit@622Mhz/155Mhz)
- Support for flexible mapping of client data on a per channel basis into optimal SONET/SDH payloads using Frame-based GFP (GFP -F)
  - Maps Ethernet data into SONET/SDH payloads using GFP

- Maps PPP frames into SONET/SDH payloads using GFP -F
  - Supports GFP mapping of RPR, MPLS or proprietary client data using the G-header interface
  - Supports add/drop of client management frames from/to the microprocessor interface
- Supports a G-header interface in order to effectively map RPR, MPLS or proprietary client data over SONET
  - Compatible with OIF compliant SPI-3 interface
  - Performs G-header encapsulation/de-capsulation
  - G-header interface can be optionally disabled
- Support for contiguous pointer-based concatenation for higher order paths
  - Supports mapping of Gigabit Ethernet to STS-48C/AU4-16C, STS12C/AU4-16C or STS3C/AU4 or STS-1/AU3
- Support for a SPI-3 interface with up to 256 logical sub-channels and individual channel flow control
- Support for High Order and Low Order Virtual concatenation with optional Link Capacity Adjustment Scheme (LCAS)
  - Supports flexible mapping of multi-protocol traffic into standards based high order virtual concatenation channels of STS-3c-Xv/VC-4-Xv as well as STS-1-Xv/VC-3-Xv
  - Supports mapping of multi-protocol traffic into standards based low order virtual concatenation channels of VT6/VT2/VT1.5
  - Supports a total of 64 Virtual Concatenation Groups (VCG's)
  - Supports Link Capacity Adjustment Scheme per ITU-T G.7042
  - Provides up to 256 ms of differential delay compensation using external SDRAM interface
- Terminates and processes Section, Line and Path Overhead on OC-48/STM-16, OC-12/STM-4 and OC-3/STM-1 interfaces
  - Support for extensive performance monitoring on the SONET/SDH interfaces
- Support for on-chip STS-1 cross-connect between the OC-12 Add/drop interface and the Lineside interfaces
- Support for UPSR and 1+1 Linear Automatic Protection Switching

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- Supports mapping of data using POS/HDLC framing into SONET/SDH in accordance with RFC2615 & IETF 1662
  - Optionally supports PPP/BCP (Bridging Control Protocol) encapsulation
  - Performs ATM cell de-lineation and maps ATM packets into SONET/SDH using POS/HDLC
- Support for 48 DS3 and sub-rate DS3 framers on-chip
  - Maps/De-maps DS3 signals into SONET/SDH payloads
  - Supports extensive performance monitoring on DS3 data
  - Integrated fractional DS3/T3 and scrambling functions
- Supports mapping of Ethernet data over SDH using LAPS framing according to ITU-T X.86
- Supports a 32 bit micro-processor interface for management, configuration, gathering extended statistics and providing interrupts for alarm processing
- Supports performance monitoring and alarms as required by GR.253, G.707 and ANSI T1.105

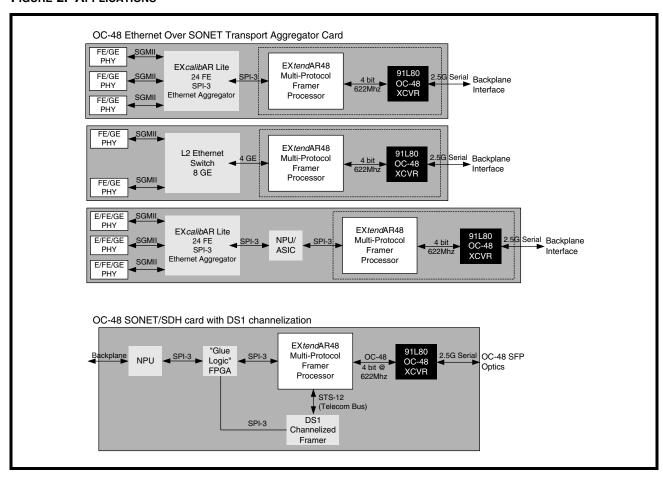**FIGURE 1. XRT95L53 EX*tend*AR-48M BLOCK DIAGRAM**

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT95L53	PBGA 780	-40°C to 85°C

TABLE 1: KEY FEATURE, ADVANTAGE AND BENEFITS MATRIX

	EXTENDAR 48M FEATURES	ADVANTAGE	EXTENDAR 48M BENEFITS
1	Supports a range of flexible encapsulation & framing features including GFP -F, LAPS, PPP/HDLC, BCP and ATM	Supports the latest standards of GFP -F and -T and provides flexibility of different encapsulation /framing features on a per channel basis	Supports a wide range of framing and encapsulation features ensuring the effective mapping of different types of client data
2	Supports 48 DS3 and sub-rate DS3 framers on a single chip	Supports a unique combination of DS3 framer functionality coupled with advanced packet encapsulation and SONET framing functions in a single chip	High level of integration reduces the total system BOM cost. Single device enables multiple applications
3	Supports High order and Low order virtual concatenation capability for 64 VC channels with LCAS	Supports both HO order Virtual concatenation as well as VT mapping support in a single chip.	Enables the optimal utilization of SONET bandwidth for various types of client data as well as ensures the dynamic allocation of bandwidth to meet service-level requirements.
4	Supports a proprietary G-Header interface compatible with OIF compliant SPI-3 interface	Enables support for RPR , MPLS and other proprietary client data types that need to be optimally transported over SONET.	Promotes flexibility and ease of use spanning multiple applications

FIGURE 2. APPLICATIONS

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REVISION HISTORY

REVISION #	DATE	DESCRIPTION
A1.0.0	February 2005	Initial release.

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