GENERAL DESCRIPTION

The XRT79L71 is a single channel, ATM UNI/PPP Physical Layer Processor with integrated DS3/E3 framing controller and Line Interface Unit with Jitter Attenuator that is designed to support ATM direct mapping and cell delineation as well as PPP mapping and Frame processing. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3/E3 rates. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT79L71 includes DS3/E3 Framing, Line Interface Unit with Jitter Attenuator that supports mapping of ATM or HDLC framed data. A flexible parallel microprocessor interface is provided for configuration and control. Industry standard UTOPIA II and POS-PHY interface are also provided.

GENERAL FEATURES:

- Integrated T3/E3 Line Interface Unit
- Integrated Jitter Attenuator that can be selected either in Receive or Transmit path
- Flexible integrated Clock Multiplier that takes single frequency clock and generates either DS3 or E3 frequency.
- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- HDLC Controller that provides the mapping/ extraction of either bit or byte mapped encapsulated packet from DS3/E3 Frame.
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports ATM cell or PPP Packet Mapping
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing.
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola, PowerPC, and Mips µPs
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 208 STBGA Package
- JTAG Interface

LINE INTERFACE UNIT

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3 Jitter Tolerance Requirements
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Meets ETSI TBR 24 and GR-499 Jitter Transfer Requirements
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- On chip advanced crystal-less Jitter Attenuator
- Jitter Attenuator can be selected in Receive or Transmit paths
- 16 or 32 bits selectable FIFO size
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards
- Jitter Attenuator can be disabled
- Typical power consumption 1.3W

DS3/E3 FRAMER

- DS3 framer supports both M13 and C-bit parity.
- DS3 framer meets ANSI T1.107 and T1.404 standards.
- Detects OOF,LOF,AIS,RDI/FERF alarms.
- Generation and Insertion of FEBE on received parity errors supported.
- Automatic insertion of RDI/FERF on alarm status.
- E3 framer meets G.832,G.751 standards.
- Framers can be bypassed.

ATM/PPP PROTOCOL PROCESSOR

TRANSMIT CELL PROCESSING

- Extracts ATM cells

- Supports ATM cell payload scrambling
- Maps ATM cells into E3 or DS3 frame
- PLCP frame and mapping of ATM cell streams

RECEIVE CELL PROCESSING

- Extraction of ATM cells from PLCP frame or directly from E3 or DS3 frame
- Termination of PLCP frame
- Supports payload cell de-scrambling

TRANSMIT PACKET PROCESSING

- Inserts PPP packets into data stream
- Maps HDLC data stream directly into DS3 or E3 frame
- Extracts in-band messaging packets
- Supports CRC-16/32, HDLC flag and Idle sequence generation

RECEIVE PACKET PROCESSING

- Extracts HDLC data stream from DS3 or E3 frame
- Inserts in-band messaging packets
- Detects and removes HDLC flags

UTOPIA/ SYSTEM INTERFACE

- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- Compliant with ATM Forum UTOPIA II interface
- Programmable FIFO size for both Transmit and Receive direction
- Compliant to POS-PHY Level 2 interface

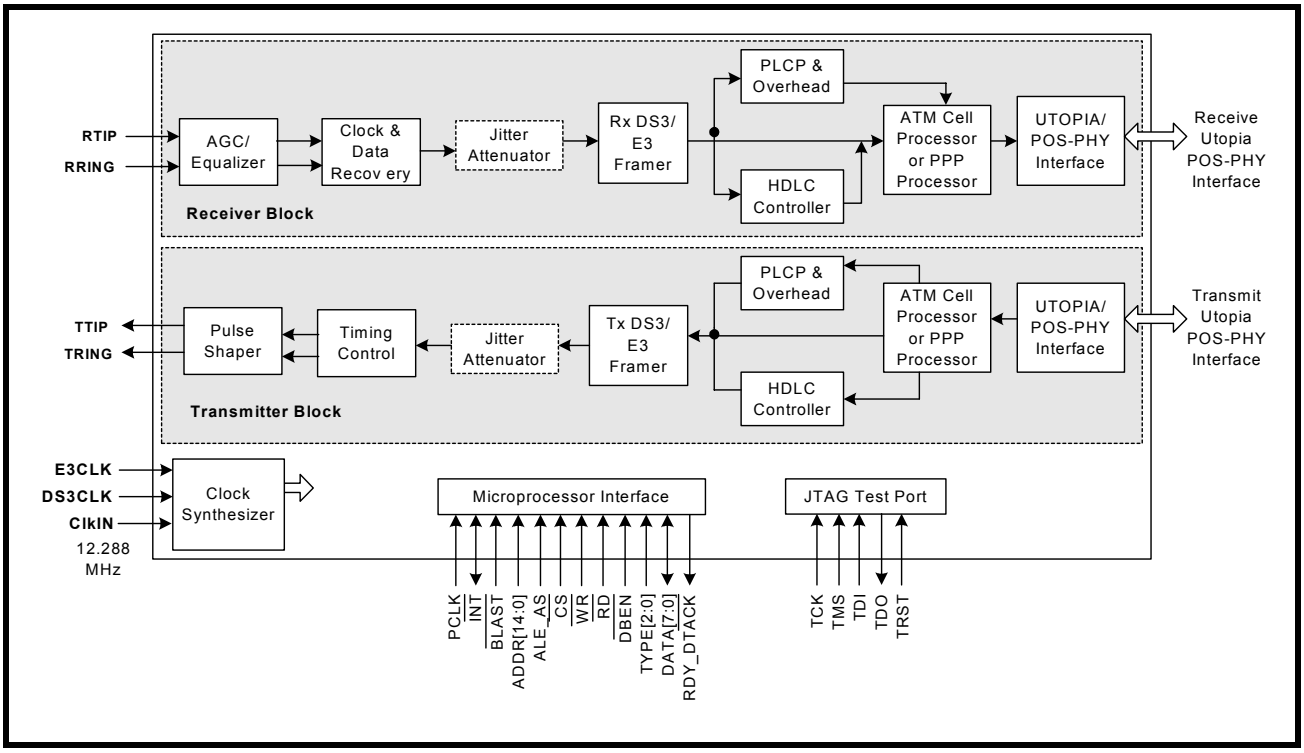
SERIAL INTERFACE

- Serial clock and data interface for accessing DS3/ E3 framer
- Serial clock and data interface for accessing cell/ packet processor

APPLICATIONS

- Digital Access and Cross Connect Systems
- 3G Base Stations
- DSLAMs
- Digital, ATM, WAN and LAN Switches

FIGURE 1. BLOCK DIAGRAM OF THE XRT79L71



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L71IB	17X17 mm 208 Ball Shrink Thin Ball Grid Array	-40°C to +85°C

TABLE 1: PIN OUT OF THE XRT79L71 (TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
1	RXGFCCLK	RXGFCMSB	RXUDATA_13	RXUDATA_9	RXUDATA_5	RXUDATA_2	RXUDATA_1	RXUCLAV	RXUADDR_0	RXUADDR_4	RXMOD	TXUCLK	TXPEOP	TXUCLKO	TXUADDR_3
2	RXPLOF	RXPRED	TXGFCCLK	RXUDATA_12	RXUDATA_8	RXUDATA_4	RXUDATA_0	RXUSOC	RXUADDR_1	RXUCLKO	RXPERR	TXPER	RXPDVAL	TXUADDR_4	TXUADDR_2
3	TXPOHFRAME	TXPOHCLK	RXGFC	RXUDATA_15	RXUDATA_11	RXUDATA_7	RXUDATA_3	RXUPRTY	RXUADDR_2	RXPEOP	RXUCLK	TXMOD	TXUCLAV	TXUSOC	TXUPRTY
4	RXNIB_2	RXNIB_3	RXPOHFRAME	RXCP	RXUDATA_14	RXUDATA_10	RXUDATA_6	RXUEN_L	RXUADDR_3	RSX_RSOF	TSX_TSOF	TXUEN_L	TXUDATA_10	TXUDATA_1	TXUDATA_2
5	RXSER	RXOUTCLK	RXNIB_0	RXPOOF									TXUDATA_4	TXUDATA_5	TXUDATA_6
6	RXCLK	RXFRAME	RXOHIND	RXNIB_1									TXUDATA_8	TXUDATA_9	TXUDATA_11
7	RXOHCLK	RXOHENABLE	RXOH	RXLOS									TXUDATA_13	TXUDATA_14	TXUDATA_15
8	RXOHFRAME	TXNOB_3	TXNOB_2	TXNIB_1									GPIO_1	GPIO_2	GPIO_3
9	TXNIB_0	TXOHIND	TXSER	TXNIBCLK									TDO	TDI	TMS
10	TXNIBFRAME	TXFRAME	TXINCLK	TXOHINS									TXDGND	MTIP	TRST
11	TXFRAMEREF	TXOHFRAME	TXOH	PDATA									TXDVDD	MRING	NC
12	TXOHENABLE	TXOHCLK	PDATA_1	PDATA_4									TXAGND	REFAGND	REFAVDD
13	TXAISEN	PDATA_2	PDATA_5	PINT_L	PADDR_6	DPADDR_3	DPADDR_7	DA_SEL	PDBEN_L	GPO_2	GPI_2	OGND	OVDD	ANAIO1	RRING
14	PDATA_3	PDATA_6	PRDY_L	PCS_L	PADDR_5	DPADDR_2	DPADDR_6	VDD	PTYPE_2	GPO_1	GPI_1	RESET_L	VDD	ANAIO2	RTIP
15	PDATA_7	PBLAST_L	PRD_L	PADDR_1	PADDR_4	DPADDR_1	DPADDR_5	GND	PTYPE_1	GPO_0	GPI_0	TESTMODE	GND	ICTB	TXON
16	PAS_L	PWR_L	PADDR_0	PADDR_2	PADDR_3	DPADDR_0	DPADDR_4	PCLK	PTYPE_0	CLKOUT	NIBBLEINTF	E3CLK	CLKGND	DS3CLK	CLKVDD

VDD	GND	GND	VDD	
VDD	GND	GND	VDD	
VDD	GND	GND	VDD	
VDD	GND	GND	VDD	

TABLE 1: PIN OUT OF THE XRT79L71 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
T	TXUADDR_1	TXUADDR_0	TXUDATA_0	TXUDAT_3	TXUDATA_7	TXUDATA_12	GPIO_0	DMO_0	TCK	TRING	TTIP	TXAVDD	RXAVDD	RXAGND	JAGND	JAAVDD

TABLE OF CONTENTS

1.0 BRIEF XRT79L71 ARCHITECTURE DESCRIPTION (SEE 79L71 PRODUCT BRIEF)

2.0 INTERRUPT STRUCTURE WITHIN THE XRT79L71 (SEE 79L71 PRODUCT BRIEF)

3.0 REGISTER MAP/DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC

COMMONCONTROL REGISTERS OF THE XRT79L71

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
COMMON CONTROL REGISTERS			
OPERATION CONTROL/GENERAL PURPOSE CONTROL REGISTERS			
0x0100	Operation Control Register - Byte 3	R/W	0x00
0x0101	Operation Control Register - Byte 2	R/W	0x00
0x0102	Operation Control Register - Byte 1	R/W	0x00
0x0103	Operation Control Register - Byte 0	R/W	0x00
0x0104	Device ID Register	R/W	0x7A
0x0105	Revision ID Register	R/W	?x??
0x0106 - 0x0111	Reserved		
0x0112	Operation Block Interrupt Status Register - Byte 1	RO	0x00
0x0113	Operation Block Interrupt Status Register - Byte 0	RO	0x00
0x0114 - 0x0115	Reserved		
0x0116	Operation Block Interrupt Enable Register - Byte 1	R/W	0x00
0x0117	Operation Block Interrupt Enable Register - Byte 0	R/W	0x00
0x0118	Reserved		
0x0119	Channel Interrupt Indicator - Receive Cell Processor/PPP Processor Block	R/O	0x00
0x011A - 0x011C	Reserved		
0x011D	Channel Interrupt Indicator - LIU/Jitter Attenuator Block	R/O	0x00
0x011E - 0x0120	Reserved		
0x0121	Channel Interrupt Indicator - Transmit Cell Processor/PPP Processor Block	R/O	0x00
0x0122 - 0x0126	Reserved		
0x0127	Channel Interrupt Indicator - DS3/E3 Framer Block - Byte 0	R/O	0x00
0x0128 - 0x0146	Reserved		
0x0147	Operation General Purpose Input/Output Register	R/W	0x00
0x0148 - 0x014A	Reserved		
0x014B	Operation General Purpose Input/Output Direction Register	R/W	0x00
0x014C - 0x04FF	Reserved		

COMMONCONTROL REGISTERS OF THE XRT79L71

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
COMMON CONTROL REGISTERS			
OPERATION CONTROL/GENERAL PURPOSE CONTROL REGISTERS			
RECEIVE UTOPIA/POS-PHY INTERFACE BLOCK CONTROL REGISTERS			
0x0500	Receive POS-PHY Interface - Receive Control Register - Byte 2	R/W	0x00
0x0501	Receive UTOPIA Interface - Receive Control Register - Byte 2 Receive POS-PHY Control Register - Byte 1	R/W	0x00
0x0502	Receive UTOPIA Interface - Receive Control Register - Byte 1 Receive POS-PHY Control Register - Byte 0	R/W	0x00
0x0503	Receive UTOPIA Interface - Receive Control Register - Byte 0	R/W	0x00
0x0504 - 0x0512	Reserved		
0x0513	Receive UTOPIA Interface - Port Address Register	R/W	
0x0514 - 0x0516	Reserved		
0x0517	Receive UTOPIA Interface - Port Number Register	R/W	0x00
0x0518 - 0x057F	Reserved		
TRANSMIT UTOPIA/POS-PHY INTERFACE BLOCK CONTROL REGISTERS			
0x0580	Transmit POS-PHY Interface - Transmit Control Register - Byte 2	R/W	0x00
0x0581	Transmit UTOPIA Interface - Transmit Control Register - Byte 2 Transmit POS-PHY Interface - Transmit Control Register - Byte 1	R/W	0x00
0x0582	Transmit UTOPIA Interface - Transmit Control Register - Byte 1 Transmit POS-PHY Interface - Transmit Control Register - Byte 0	R/W	0x00
0x0583	Transmit UTOPIA Interface - Transmit Control Register	R/W	0x00
0x0584 - 0x0592	Reserved		
0x0593	Transmit UTOPIA Interface - Transmit UTOPIA Port Address Register	R/W	0x00
0x0594 - 0x0596	Reserved		
0x0597	Transmit UTOPIA Interface - Transmit UTOPIA Port Number Register	R/W	0x00
0x0598 - 0x0FFF	Reserved	R/O	0x00

CHANNEL CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
DS3/E3 FRAMER BLOCK AND PLCP CONTROL REGISTERS			
0x1100	Operating Mode Register	R/W	0x2B
0x1101	I/O Control Register	R/W	0xA4

CHANNEL CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
DS3/E3 FRAMER BLOCK AND PLCP CONTROL REGISTERS			
0x1102 - 0x1103	Reserved		
0x1104	Block Interrupt Enable Register	R/W	0x00
0x1105	Block Interrupt Status Register	R/O	0x00
0x1106 - 0x110B	Reserved		
0x110C	DS3 Test Register	R/W	0x00
0x110D	Reserved	R/O	0x00
0x110E - 0x110F	Reserved		
0x1110	RxDS3 Configuration and Status RegisterRxE3 Configuration and Status Register # 1 (G.832 & G.751)	R/O	0x12
0x1111	RxDS3 Status RegisterRxE3 Configuration and Status Register # 2 (G.832 & G.751)	R/O	0x00

CHANNEL CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
CLEAR CHANNEL FRAMER BLOCK REGISTERS			
0x1112	RxDS3 Interrupt Enable RegisterRx E3 Interrupt Enable Register 1 (G.832 & G751)	R/W	0x00
0x1113	RxDS3 Interrupt Status RegisterRx E3 Interrupt Enable Register # 2 (G.832 & G.751)	RUR	0x00
0x1114	RxDS3 Sync Detect RegisterRx E3 Interrupt Status Register # 1 (G.832 & G.751)	R/W & RUR	0x00
0x1115	RxE3 Interrupt Status Register # 2 (G.832 & G.751)	RUR	0x00
0x1116	Reserved		
0x1117	RxDS3 FEAC Interrupt Enable and Status Register	R/W & RUR	0x00
0x1118	RxE3 LAPD Control Register	R/W & RUR	0x00
0x1119	RxLAPD Status Register	R/O	0x00
0x111A	RxE3 NR Byte Register (G.832) RxE3 Service Bits Register (G.751)	R/O	0x00
0x111B	RxE3 GC Byte Register (G.832)	R/O	0x00
0x111C	RxE3 TTB Register # 0 (G.832)	R/O	0x00

CHANNEL CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
	CHANNEL CONTROL REGISTERS		
	CLEAR CHANNEL FRAMER BLOCK REGISTERS		
0x111D	RxE3 TTB Register # 1 (G.832)	R/O	0x00
0x111E	RxE3 TTB Register # 2 (G.832)	R/O	0x00
0x111F	RxE3 TTB Register # 3 (G.832)	R/O	0x00
0x1120	RxE3 TTB Register # 4 (G.832)	R/O	0x00
0x1121	RxE3 TTB Register # 5 (G.832)	R/O	0x00
0x1122	RxE3 TTB Register # 6 (G.832)	R/O	0x00
0x1123	RxE3 TTB Register # 7 (G.832)	R/O	0x00
0x1124	RxE3 TTB Register # 8 (G.832)	R/O	0x00
0x1125	RxE3 TTB Register # 9 (G.832)	R/O	0x00
0x1126	RxE3 TTB Register # 10 (G.832)	R/O	0x00
0x1127	RxE3 TTB Register # 11 (G.832)	R/O	0x00
0x1128	RxE3 TTB Register # 12 (G.832)	R/O	0x00
0x1129	RxE3 TTB Register # 13 (G.832)	R/O	0x00
0x112A	RxE3 TTB Register # 14 (G.832)	R/O	0x00
0x112B	RxE3 TTB Register # 15 (G.832)	R/O	0x00
0x112C	RxE3 SSM Register (G.832)	R/O	0x00
0x112D - 0x112F	Reserved		
0x1130	Transmit DS3 Configuration Register Transmit E3 Configuration Register	R/W	0x07
0x1131	TxDS3 FEAC Configuration and Status Register	RUR & R/W	0x00
0x1132	TxDS3 FEAC Register	R/W	0x7E
0x1133	TxLAPD Configuration Register	R/O & R/W	0x08
0x1134	TxLAPD Status and Interrupt Register	RUR & R/W	0x00
0x1135	TxDS3 M-Bit Mask Register TxE3 GC Byte Register (G.832) TxE3 Service Bits Register (G.751)	R/W	0x00
0x1136	TxDS3 F-Bit Mask Register # 1 TxE3 MA Byte Register (G.832)	R/W	0x00
0x1137	TxDS3 F-Bit Mask Register # 2 TxE3 NR Byte Register (G.832)	R/W	0x00

CHANNEL CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
	CHANNEL CONTROL REGISTERS		
	CLEAR CHANNEL FRAMER BLOCK REGISTERS		
0x1138	TxDS3 F-Bit Mask Register # 3 Transmit Trail-Trace Message Register - Byte 1 (G.832)	R/W	0x00
0x1139	Transmit Trail-Trace Message Register - Byte 2 (G.832)	R/W	0x00
0x113A	Transmit Trail-Trace Message Register - Byte 3 (G.832)	R/W	0x00
0x113B	Transmit Trail-Trace Message Register - Byte 4 (G.832)	R/W	0x00
0x113C	Transmit Trail-Trace Message Register - Byte 5 (G.832)	R/W	0x00
0x113D	Transmit Trail-Trace Message Register - Byte 6 (G.832)	R/W	0x00
0x113E	Transmit Trail-Trace Message Register - Byte 7 (G.832)	R/W	0x00
0x113F	Transmit Trail-Trace Message Register - Byte 8 (G.832)	R/W	0x00
0x1140	Transmit Trail-Trace Message Register - Byte 9 (G.832)	R/W	0x00
0x1141	Transmit Trail-Trace Message Register - Byte 10 (G.832)	R/W	0x00
0x1142	Transmit Trail-Trace Message Register - Byte 11 (G.832)	R/W	0x00
0x1143	Transmit Trail-Trace Message Register - Byte 12 (G.832)	R/W	0x00
0x1144	Transmit Trail-Trace Message Register - Byte 13 (G.832)	R/W	0x00
0x1145	Transmit Trail-Trace Message Register - Byte 14 (G.832)	R/W	0x00
0x1146	Transmit Trail-Trace Message Register - Byte 15 (G.832)	R/W	0x00
0x1147	Transmit Trail-Trace Message Register - Byte 16 (G.832)	R/W	0x00
0x1148	TxE3 FA1 Error Mask Register (G.832) TxE3 FAS Error Mask Register # 1 (G.751)	R/W	0x00
0x1149	TxE3 FA2 Error Mask Register (G.832) TxE3 FAS Error Mask Register # 2 (G.751)	R/W	0x00
0x114A	TxE3 BIP-8 Error Mask Register (G.832) TxE3 BIP-4 Error Mask Register (G.751)	R/W	0x00
0x114B	TxE3 SSM Register	R/W	0x00
0x114C	Transmit DS3 Pattern Register	R/W	0x0C
0x114D - 0x114F	Reserved	R/O	0x00
0x1150	PMON Line Code Violation Count Register - MSB	RUR	0x00
0x1151	PMON Line Code Violation Count Register - LSB	RUR	0x00
0x1152	PMON Framing Bit/Byte Error Count Register - MSB	RUR	0x00
0x1153	PMON Framing Bit/Byte Error Count Register - LSB	RUR	0x00
0x1154	PMON P-Bit/BIP-8/BIP-4 Error Count Register - MSB	RUR	0x00

CHANNEL CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
	CHANNEL CONTROL REGISTERS		
	CLEAR CHANNEL FRAMER BLOCK REGISTERS		
0x1155	PMON P-Bit/BIP-8/BIP-4 Error Count Register - LSB	RUR	0x00
0x1156	PMON FEBE Event Count Register - MSB	RUR	0x00
0x1157	PMON FEBE Event Count Register - LSB	RUR	0x00
0x1158	PMON CP-Bit Error Count Register - MSB	RUR	0x00
0x1159	PMON CP-Bit Error Count Register - LSB	RUR	0x00
0x115A	PMON PLCP BIP-8 Error Count Register - MSB	RUR	0x00
0x115B	PMON PLCP BIP-8 Error Count Register - LSB	RUR	0x00
0x115C	PMON PLCP Framing Byte Error Count Register - MSB	RUR	0x00
0x115D	PMON PLCP Framing Byte Error Count Register - LSB	RUR	0x00
0x115E	PMON PLCP FEBE Event Count Register - MSB	RUR	0x00
0x115F	PMON PLCP FEBE Event Count Register - LSB	RUR	0x00
0x1160 - 0x1167	Reserved		
0x1168	PRBS Error Count Register - MSB	RUR	0x00
0x1169	PRBS Error Count Register - LSB	RUR	0x00
0x116A - 0x116C	Reserved		
0x116D	One Second Error Status Register	R/O	0x00
0x116E	One Second Accumulator - LCV Count Register - MSB	R/O	0x00
0x116F	One Second Accumulator - LCV Count Register - LSB	R/O	0x00
0x1170	One Second Accumulator - P-Bit/BIP-8/BIP-4 Error Count Register - MSB	R/O	0x00
0x1171	One Second Accumulator - P-Bit/BIP-8/BIP-4 Error Count Register - LSB	R/O	0x00
0x1172	One Second Accumulator - CP Bit Error Count Register - MSB	R/O	0x00
0x1173	One Second Accumulator - CP Bit Error Count Register - LSB	R/O	0x00
0x1174 - 0x1181	Reserved		
0x1182	Payload HDLC Control Register	R/W	0x00
0x1183	Transmit LAPD Byte Count Register	R/W	0x00
0x1184	Receive LAPD Byte Count Register	R/W	0x00
0x1185 - 0x118F	Reserved	R/O	0x00
0x1190	RxPLCP Configuration & Status Register	R/O & R/W	0x06
0x1191	RxPLCP Interrupt Enable Register	R/W	0x00

CHANNEL CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
CLEAR CHANNEL FRAMER BLOCK REGISTERS			
0x1192	RxPLCP Interrupt Status Register	RUR	0x00
0x1193 - 0x1197	Reserved		
0x1198	TxPLCP A1 Byte Error Mask Register	R/W	0x00
0x1199	TxPLCP A2 Byte Error Mask Register	R/W	0x00
0x119A	TxPLCP BIP-8 Byte Error Mask Register	R/W	0x00
0x119B	TxPLCP G1 Byte Register	R/W	0x00
0x119C - 0x11BF	Reserved		
0x11C0	LAPD Message Buffer Indirect Address Register	R/W	0x00
0x11C1	LAPD Message Buffer Indirect Data Register	R/W	0x00
0x11C2 - 0x12FF	Reserved	R/O	0x00

LIU/JITTER ATTENUATOR CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
LIU/JITTER ATTENUATOR CONTROL REGISTERS			
0x1300	LIU Transmit APS/Redundancy Control Register	R/W	0x00
0x1301	LIU Interrupt Enable Register	R/W	0x00
0x1302	LIU Interrupt Status Register	RUR	0x00
0x1303	LIU Alarm Status Register	R/O	0x00
0x1304	LIU Transmit Control Register	R/W	0x00
0x1305	LIU Receive Control Register	R/W	0x00
0x1306	LIU Channel Control Register	R/W	0x00
0x1307	Jitter Attenuator Control Register	R/W	0x00
0x1308	LIU Receive APS/Redundancy Control Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1700	Receive ATM Cell Processor - Receive Control Register - Byte 3	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1701	Receive ATM Cell Processor - Receive Control Register - Byte 2	R/W	0x00
0x1702	Receive ATM Cell Processor - Receive Control Register - Byte 1	R/W	0x00
0x1703	Receive ATM Cell Processor - Receive Control Register - Byte 0 Receive PPP Packet Processor - Receive PPP Interrupt Status Register	R/W	0x00
0x1704 - 0x1706	Reserved		
0x1707	Receive ATM Status Register	R/O	0x00
0x1708 - 0x1709	Reserved		
0x170A	Receive ATM Cell Processor - Receive Interrupt Status Register -Byte 1	RUR	0x00
0x170B	Receive ATM Cell Processor - Receive Interrupt Status Register - Byte 0 Receive PPP Packet Processor - Receive PPP Interrupt Status Register	RUR	0x00
0x170C - 0x170D	Reserved		
0x170E	Receive ATM Cell Processor - Receive Interrupt Enable Register - Byte 1	R/W	0x00
0x170F	Receive ATM Cell Processor - Receive Interrupt Enable Register - Byte 0 Receive PPP Packet Processor - Receive Interrupt Enable Register	R/W	0x00
0x1710	Receive PPP Packet Processor - Receive Good Packet Count Register - Byte 3	RUR	0x00
0x1711	Receive PPP Packet Processor - Receive Good Packet Count Register - Byte 2	RUR	0x00
0x1712	Receive PPP Packet Processor - Receive Good Packet Count Register - Byte 1	RUR	0x00
0x1713	Receive ATM Cell Processor - Cell Insertion/Extraction Memory Control Register Receive PPP Packet Processor - Receive Good Packet Count Register - Byte 0	R/O & R/W	0x00
0x1714	Receive ATM Cell Processor - Cell Insertion/Extraction Memory Data Register - Byte 3 Receive PPP Packet Processor - Receive FCS Error Count Register - Byte 3	R/O & R/W	0x00
0x1715	Receive ATM Cell Processor - Cell Insertion/Extraction Memory Data Register - Byte 2 Receive PPP Packet Processor - Receive FCS Error Count Register - Byte 2	R/O & R/W	0x00
0x1716	Receive ATM Cell Processor - Cell Insertion/Extraction Memory Data Register - Byte 1 Receive PPP Packet Processor - Receive FCS Error Count Register - Byte 1	R/O & R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1717	Receive ATM Cell Processor - Cell Insertion/Extraction Memory Data Register - Byte 0 Receive PPP Packet Processor - Receive FCS Error Count Register - Byte 0	R/O & R/W	0x00
0x1718	Receive ATM Cell Processor - UDF Data Register - Byte 3 Receive PPP Packet Processor - Receive Aborted Packet Count Register - Byte 3	R/W & RUR	0x00
0x1719	Receive ATM Cell Processor - UDF Data Register - Byte 2 Receive PPP Packet Processor - Receive Aborted Packet Count Register - Byte 2	R/W & RUR	0x00
0x171A	Receive ATM Cell Processor - UDF Data Register - Byte 1 Receive PPP Packet Processor - Receive Aborted Packet Count Register - Byte 1	R/W & RUR	0x00
0x171B	Receive ATM Cell Processor - UDF Data Register - Byte 0 Receive PPP Packet Processor - Receive Aborted Packet Count Register - Byte 0	R/W & RUR	0x00
0x171C	Receive PPP Packet Processor - Receive Runt Packet Count Register - Byte 3	RUR	0x00
0x171D	Receive PPP Packet Processor - Receive Runt Packet Count Register - Byte 2	RUR	0x00
0x171E	Receive PPP Packet Processor - Receive Runt Packet Count Register - Byte 1	RUR	0x00
0x171F	Receive PPP Packet Processor - Receive Runt Packet Count Register - Byte 0	RUR	0x00
0x1720	Receive ATM Cell Processor - Test Cell Header Byte Register - Byte 0	R/W	0x00
0x1721	Receive ATM Cell Processor - Test Cell Header Byte Register - Byte 1	R/W	0x00
0x1722	Receive ATM Cell Processor - Test Cell Header Byte Register - Byte 2	R/W	0x00
0x1723	Receive ATM Cell Processor - Test Cell Header Byte Register - Byte 3	R/W	0x00
0x1724	Receive ATM Cell Processor - Test Cell Error Count Register - Byte 3	RUR	0x00
0x1725	Receive ATM Cell Processor - Test Cell Error Count Register - Byte 2	RUR	0x00
0x1726	Receive ATM Cell Processor - Test Cell Error Count Register - Byte 1	RUR	0x00
0x1727	Receive ATM Cell Processor - Test Cell Error Count Register - Byte 0	RUR	0x00
0x1728	Receive ATM Cell Count Register - Byte 3	RUR	0x00
0x1729	Receive ATM Cell Count Register - Byte 2	RUR	0x00
0x172A	Receive ATM Cell Count Register - Byte 1	RUR	0x00
0x172B	Receive ATM Cell Count Register - Byte 0	RUR	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x172C	Receive ATM Cell - Discard Cell Count Register - Byte 3	RUR	0x00
0x172D	Receive ATM Cell - Discard Cell Count Register - Byte 2	RUR	0x00
0x172E	Receive ATM Cell - Discard Cell Count Register - Byte 1	RUR	0x00
0x172F	Receive ATM Cell - Discard Cell Count Register - Byte 0	RUR	0x00
0x1730	Receive ATM Correctable HEC Byte Error Count Register - Byte 3	RUR	0x00
0x1731	Receive ATM Correctable HEC Byte Error Count Register - Byte 2	RUR	0x00
0x1732	Receive ATM Correctable HEC Byte Error Count Register - Byte 1	RUR	0x00
0x1733	Receive ATM Correctable HEC Byte Error Count Register - Byte 0	RUR	0x00
0x1734	Receive ATM Uncorrectable HEC Byte Error Count Register - Byte 3	RUR	0x00
0x1735	Receive ATM Uncorrectable HEC Byte Error Count Register - Byte 2	RUR	0x00
0x1736	Receive ATM Uncorrectable HEC Byte Error Count Register - Byte 1	RUR	0x00
0x1737	Receive ATM Uncorrectable HEC Byte Error Count Register - Byte 0	RUR	0x00
0x1738 - 0x1742	Reserved		
0x1743	Receive ATM - User Cell Filter # 0 - Filter Control Register	R/W	0x00
0x1744	Receive ATM - User Cell Filter # 0 - Header Byte # 1 Pattern Register	R/W	0x00
0x1745	Receive ATM - User Cell Filter # 0 - Header Byte # 2 Pattern Register	R/W	0x00
0x1746	Receive ATM - User Cell Filter # 0 - Header Byte # 3 Pattern Register	R/W	0x00
0x1747	Receive ATM - User Cell Filter # 0 - Header Byte # 4 Pattern Register	R/W	0x00
0x1748	Receive ATM - User Cell Filter # 0 - Header Byte # 1 Check Register	R/W	0x00
0x1749	Receive ATM - User Cell Filter # 0 - Header Byte # 2 Check Register	R/W	0x00
0x174A	Receive ATM - User Cell Filter # 0 - Header Byte # 3 Check Register	R/W	0x00
0x174B	Receive ATM - User Cell Filter # 0 - Header Byte # 4 Check Register	R/W	0x00
0x174C	Receive ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x174D	Receive ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x174E	Receive ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x174F	Receive ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1750 - 0x1752	Reserved		
0x1753	Receive ATM - User Cell Filter # 1 - Filter Control Register	R/W	0x00
0x1754	Receive ATM - User Cell Filter # 1 - Header Byte # 1 Pattern Register	R/W	0x00
0x1755	Receive ATM - User Cell Filter # 1 - Header Byte # 2 Pattern Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1756	Receive ATM - User Cell Filter # 1 - Header Byte # 3 Pattern Register	R/W	0x00
0x1757	Receive ATM - User Cell Filter # 1 - Header Byte # 4 Pattern Register	R/W	0x00
0x1758	Receive ATM - User Cell Filter # 1 - Header Byte # 1 Check Register	R/W	0x00
0x1759	Receive ATM - User Cell Filter # 1 - Header Byte # 2 Check Register	R/W	0x00
0x175A	Receive ATM - User Cell Filter # 1 - Header Byte # 3 Check Register	R/W	0x00
0x175B	Receive ATM - User Cell Filter # 1 - Header Byte # 4 Check Register	R/W	0x00
0x175C	Receive ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x175D	Receive ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x175E	Receive ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x175F	Receive ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1760 - 0x1762	Reserved		
0x1763	Receive ATM - User Cell Filter # 2 - Filter Control Register	R/W	0x00
0x1764	Receive ATM - User Cell Filter # 2 - Header Byte # 1 Pattern Register	R/W	0x00
0x1765	Receive ATM - User Cell Filter # 2 - Header Byte # 2 Pattern Register	R/W	0x00
0x1766	Receive ATM - User Cell Filter # 2 - Header Byte # 3 Pattern Register	R/W	0x00
0x1767	Receive ATM - User Cell Filter # 2 - Header Byte # 4 Pattern Register	R/W	0x00
0x1768	Receive ATM - User Cell Filter # 2 - Header Byte # 1 Check Register	R/W	0x00
0x1769	Receive ATM - User Cell Filter # 2 - Header Byte # 2 Check Register	R/W	0x00
0x176A	Receive ATM - User Cell Filter # 2 - Header Byte # 3 Check Register	R/W	0x00
0x176B	Receive ATM - User Cell Filter # 2 - Header Byte # 4 Check Register	R/W	0x00
0x176C	Receive ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x176D	Receive ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x176E	Receive ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x176F	Receive ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1770 - 0x1772	Reserved		
0x1773	Receive ATM - User Cell Filter # 3 - Filter Control Register	R/W	0x00
0x1774	Receive ATM - User Cell Filter # 3 - Header Byte # 1 Pattern Register	R/W	0x00
0x1775	Receive ATM - User Cell Filter # 3 - Header Byte # 2 Pattern Register	R/W	0x00
0x1776	Receive ATM - User Cell Filter # 3 - Header Byte # 3 Pattern Register	R/W	0x00
0x1777	Receive ATM - User Cell Filter # 3 - Header Byte # 4 Pattern Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1778	Receive ATM - User Cell Filter # 3 - Header Byte # 1 Check Register	R/W	0x00
0x1779	Receive ATM - User Cell Filter # 3 - Header Byte # 2 Check Register	R/W	0x00
0x177A	Receive ATM - User Cell Filter # 3 - Header Byte # 3 Check Register	R/W	0x00
0x177B	Receive ATM - User Cell Filter # 3 - Header Byte # 4 Check Register	R/W	0x00
0x177C	Receive ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x177D	Receive ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x177E	Receive ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x177F	Receive ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1780 - 0x1EFF	Reserved		
0x1F00	Transmit ATM Control Register - Byte 3	R/W	0x00
0x1F01	Transmit ATM Control Register - Byte 2	R/W	0x00
0x1F02	Transmit ATM Control Register - Byte 1	R/W	0x00
0x1F03	Transmit ATM Control Register - Byte 0 Transmit PPP Packet Processor - Transmit PPP Control Register - Byte 2	R/W	0x00
0x1F04	Transmit ATM Status Register - Byte 3	R/O	0x00
0x1F05	Transmit ATM Status Register - Byte 2	R/O	0x00
0x1F06	Transmit ATM Status Register - Byte 1	R/O	0x00
0x1F07	Transmit ATM Status Register - Byte 0	R/O	0x00
0x1F08 - 0x1F0A	Reserved		
0x1F0B	Transmit ATM Cell Processor Interrupt Status Register Transmit PPP Packet Processor - Interrupt Status Register	RUR	0x00
0x1F0C - 0x1F0E	Reserved		
0x1F0F	Transmit ATM Cell Processor Interrupt Enable Register Transmit PPP Packet Processor - Interrupt Enable Register	R/W	0x00
0x1F10 - 0x1F12	Reserved		
0x1F13	Transmit ATM Cell Insertion/Extraction Memory Control Register	R/O & R/W	0x00
0x1F14	Transmit ATM Cell Insertion/Extraction Data Register - Byte 3	R/O & R/W	0x00
0x1F15	Transmit ATM Cell Insertion/Extraction Data Register - Byte 2	R/O & R/W	0x00
0x1F16	Transmit ATM Cell Insertion/Extraction Data Register - Byte 1	R/O & R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1F17	Transmit ATM Cell Insertion/Extraction Data Register - Byte 0	R/O & R/W	0x00
0x1F18	Transmit ATM - Idle Cell Header Byte # 1 Register	R/W	0x00
0x1F19	Transmit ATM - Idle Cell Header Byte # 2 Register	R/W	0x00
0x1F1A	Transmit ATM - Idle Cell Header Byte # 3 Register	R/W	0x00
0x1F1B	Transmit ATM - Idle Cell Header Byte # 4 Register	R/W	0x00
0x1F1C - 0x1F1E	Reserved		
0x1F1F	Transmit ATM - Idle Cell Payload Byte Register	R/W	0x00
0x1F20	Transmit ATM - Test Cell Header Byte # 1 Register	R/W	0x00
0x1F21	Transmit ATM - Test Cell Header Byte # 2 Register	R/W	0x00
0x1F22	Transmit ATM - Test Cell Header Byte # 3 Register	R/W	0x00
0x1F23	Transmit ATM - Test Cell Header Byte # 4 Register	R/W	0x00
0x1F24 - 0x1F27	Reserved		
0x1F28	Transmit ATM Cell Count Register - Byte 3	RUR	0x00
0x1F29	Transmit ATM Cell Count Register - Byte 2	RUR	0x00
0x1F2A	Transmit ATM Cell Count Register - Byte 1	RUR	0x00
0x1F2B	Transmit ATM Cell Count Register - Byte 0	RUR	0x00
0x1F2C	Transmit ATM - Discarded Cell Count Register - Byte 3	RUR	0x00
0x1F2D	Transmit ATM - Discarded Cell Count Register - Byte 2	RUR	0x00
0x1F2E	Transmit ATM - Discarded Cell Count Register - Byte 1	RUR	0x00
0x1F2F	Transmit ATM - Discarded Cell Count Register - Byte 0	RUR	0x00
0x1F30	Transmit ATM HEC Byte Error Count Register - Byte 3	RUR	0x00
0x1F31	Transmit ATM HEC Byte Error Count Register - Byte 2	RUR	0x00
0x1F32	Transmit ATM HEC Byte Error Count Register - Byte 1	RUR	0x00
0x1F33	Transmit ATM HEC Byte Error Count Register - Byte 0	RUR	0x00
0x1F34	Transmit ATM Cell Processor - Parity Error Count Register - Byte 3	RUR	0x00
0x1F35	Transmit ATM Cell Processor - Parity Error Count Register - Byte 2	RUR	0x00
0x1F36	Transmit ATM Cell Processor - Parity Error Count Register - Byte 1	RUR	0x00
0x1F37	Transmit ATM Cell Processor - Parity Error Count Register - Byte 0	RUR	0x00
0x1F38 - 0x1F42	Reserved		
0x1F43	Transmit ATM - User Cell Filter # 0 - Filter Control Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1F44	Transmit ATM - User Cell Filter # 0 - Header Byte # 1 Pattern Register	R/W	0x00
0x1F45	Transmit ATM - User Cell Filter # 0 - Header Byte # 2 Pattern Register	R/W	0x00
0x1F46	Transmit ATM - User Cell Filter # 0 - Header Byte # 3 Pattern Register	R/W	0x00
0x1F47	Transmit ATM - User Cell Filter # 0 - Header Byte # 4 Pattern Register	R/W	0x00
0x1F48	Transmit ATM - User Cell Filter # 0 - Header Byte # 1 Check Register	R/W	0x00
0x1F49	Transmit ATM - User Cell Filter # 0 - Header Byte # 2 Check Register	R/W	0x00
0x1F4A	Transmit ATM - User Cell Filter # 0 - Header Byte # 3 Check Register	R/W	0x00
0x1F4B	Transmit ATM - User Cell Filter # 0 - Header Byte # 4 Check Register	R/W	0x00
0x1F4C	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x1F4D	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x1F4E	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x1F4F	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1F50 - 0x1F52	Reserved		
0x1F53	Transmit ATM - User Cell Filter # 1 - Filter Control Register	R/W	0x00
0x1F54	Transmit ATM - User Cell Filter # 1 - Header Byte # 1 Pattern Register	R/W	0x00
0x1F55	Transmit ATM - User Cell Filter # 1 - Header Byte # 2 Pattern Register	R/W	0x00
0x1F56	Transmit ATM - User Cell Filter # 1 - Header Byte # 3 Pattern Register	R/W	0x00
0x1F57	Transmit ATM - User Cell Filter # 1 - Header Byte # 4 Pattern Register	R/W	0x00
0x1F58	Transmit ATM - User Cell Filter # 1 - Header Byte # 1 Check Register	R/W	0x00
0x1F59	Transmit ATM - User Cell Filter # 1 - Header Byte # 2 Check Register	R/W	0x00
0x1F5A	Transmit ATM - User Cell Filter # 1 - Header Byte # 3 Check Register	R/W	0x00
0x1F5B	Transmit ATM - User Cell Filter # 1 - Header Byte # 4 Check Register	R/W	0x00
0x1F5C	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x1F5D	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x1F5E	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x1F5F	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1F60 - 0x1F62	Reserved		
0x1F63	Transmit ATM - User Cell Filter # 2 - Filter Control Register	R/W	0x00
0x1F64	Transmit ATM - User Cell Filter # 2 - Header Byte # 1 Pattern Register	R/W	0x00
0x1F65	Transmit ATM - User Cell Filter # 2 - Header Byte # 2 Pattern Register	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
RECEIVE ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1F66	Transmit ATM - User Cell Filter # 2 - Header Byte # 3 Pattern Register	R/W	0x00
0x1F67	Transmit ATM - User Cell Filter # 2 - Header Byte # 4 Pattern Register	R/W	0x00
0x1F68	Transmit ATM - User Cell Filter # 2 - Header Byte # 1 Check Register	R/W	0x00
0x1F69	Transmit ATM - User Cell Filter # 2 - Header Byte # 2 Check Register	R/W	0x00
0x1F6A	Transmit ATM - User Cell Filter # 2 - Header Byte # 3 Check Register	R/W	0x00
0x1F6B	Transmit ATM - User Cell Filter # 2 - Header Byte # 4 Check Register	R/W	0x00
0x1F6C	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x1F6D	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x1F6E	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x1F6F	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1F70 - 0x1F72	Reserved		
0x1F73	Transmit ATM - User Cell Filter # 3 - Filter Control Register	R/W	0x00
0x1F74	Transmit ATM - User Cell Filter # 3 - Header Byte # 1 Pattern Register	R/W	0x00
0x1F75	Transmit ATM - User Cell Filter # 3 - Header Byte # 2 Pattern Register	R/W	0x00
0x1F76	Transmit ATM - User Cell Filter # 3 - Header Byte # 3 Pattern Register	R/W	0x00
0x1F77	Transmit ATM - User Cell Filter # 3 - Header Byte # 4 Pattern Register	R/W	0x00
0x1F78	Transmit ATM - User Cell Filter # 3 - Header Byte # 1 Check Register	R/W	0x00
0x1F79	Transmit ATM - User Cell Filter # 3 - Header Byte # 2 Check Register	R/W	0x00
0x1F7A	Transmit ATM - User Cell Filter # 3 - Header Byte # 3 Check Register	R/W	0x00
0x1F7B	Transmit ATM - User Cell Filter # 3 - Header Byte # 4 Check Register	R/W	0x00
0x1F7C	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x1F7D	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x1F7E	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x1F7F	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1F80 - 0x1FFF	Reserved		

TRANSMIT ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
TRANSMIT ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1F00	Transmit ATM Control Register - Byte 3	R/W	0x00
0x1F01	Transmit ATM Control Register - Byte 2	R/W	0x00
0x1F02	Transmit ATM Control Register - Byte 1	R/W	0x00
0x1F03	Transmit ATM Control Register - Byte 0 Transmit PPP Packet Processor - Transmit PPP Control Register - Byte 2	R/W	0x00
0x1F04	Transmit ATM Status Register - Byte 3	R/O	0x00
0x1F05	Transmit ATM Status Register - Byte 2	R/O	0x00
0x1F06	Transmit ATM Status Register - Byte 1	R/O	0x00
0x1F07	Transmit ATM Status Register - Byte 0	R/O	0x00
0x1F08 - 0x1F0A	Reserved		
0x1F0B	Transmit ATM Cell Processor Interrupt Status Register Transmit PPP Packet Processor - Interrupt Status Register	RUR	0x00
0x1F0C - 0x1F0E	Reserved		
0x1F0F	Transmit ATM Cell Processor Interrupt Enable Register Transmit PPP Packet Processor - Interrupt Enable Register	R/W	0x00
0x1F10 - 0x1F12	Reserved		
0x1F13	Transmit ATM Cell Insertion/Extraction Memory Control Register	R/O & R/W	0x00
0x1F14	Transmit ATM Cell Insertion/Extraction Data Register - Byte 3	R/O & R/W	0x00
0x1F15	Transmit ATM Cell Insertion/Extraction Data Register - Byte 2	R/O & R/W	0x00
0x1F16	Transmit ATM Cell Insertion/Extraction Data Register - Byte 1	R/O & R/W	0x00
0x1F17	Transmit ATM Cell Insertion/Extraction Data Register - Byte 0	R/O & R/W	0x00
0x1F18	Transmit ATM - Idle Cell Header Byte # 1 Register	R/W	0x00
0x1F19	Transmit ATM - Idle Cell Header Byte # 2 Register	R/W	0x00
0x1F1A	Transmit ATM - Idle Cell Header Byte # 3 Register	R/W	0x00
0x1F1B	Transmit ATM - Idle Cell Header Byte # 4 Register	R/W	0x00
0x1F1C - 0x1F1E	Reserved		
0x1F1F	Transmit ATM - Idle Cell Payload Byte Register	R/W	0x00
0x1F20	Transmit ATM - Test Cell Header Byte # 1 Register	R/W	0x00

TRANSMIT ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
TRANSMIT ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1F21	Transmit ATM - Test Cell Header Byte # 2 Register	R/W	0x00
0x1F22	Transmit ATM - Test Cell Header Byte # 3 Register	R/W	0x00
0x1F23	Transmit ATM - Test Cell Header Byte # 4 Register	R/W	0x00
0x1F24 - 0x1F27	Reserved		
0x1F28	Transmit ATM Cell Count Register - Byte 3	RUR	0x00
0x1F29	Transmit ATM Cell Count Register - Byte 2	RUR	0x00
0x1F2A	Transmit ATM Cell Count Register - Byte 1	RUR	0x00
0x1F2B	Transmit ATM Cell Count Register - Byte 0	RUR	0x00
0x1F2C	Transmit ATM - Discarded Cell Count Register - Byte 3	RUR	0x00
0x1F2D	Transmit ATM - Discarded Cell Count Register - Byte 2	RUR	0x00
0x1F2E	Transmit ATM - Discarded Cell Count Register - Byte 1	RUR	0x00
0x1F2F	Transmit ATM - Discarded Cell Count Register - Byte 0	RUR	0x00
0x1F30	Transmit ATM HEC Byte Error Count Register - Byte 3	RUR	0x00
0x1F31	Transmit ATM HEC Byte Error Count Register - Byte 2	RUR	0x00
0x1F32	Transmit ATM HEC Byte Error Count Register - Byte 1	RUR	0x00
0x1F33	Transmit ATM HEC Byte Error Count Register - Byte 0	RUR	0x00
0x1F34	Transmit ATM Cell Processor - Parity Error Count Register - Byte 3	RUR	0x00
0x1F35	Transmit ATM Cell Processor - Parity Error Count Register - Byte 2	RUR	0x00
0x1F36	Transmit ATM Cell Processor - Parity Error Count Register - Byte 1	RUR	0x00
0x1F37	Transmit ATM Cell Processor - Parity Error Count Register - Byte 0	RUR	0x00
0x1F38 - 0x1F42	Reserved		
0x1F43	Transmit ATM - User Cell Filter # 0 - Filter Control Register	R/W	0x00
0x1F44	Transmit ATM - User Cell Filter # 0 - Header Byte # 1 Pattern Register	R/W	0x00
0x1F45	Transmit ATM - User Cell Filter # 0 - Header Byte # 2 Pattern Register	R/W	0x00
0x1F46	Transmit ATM - User Cell Filter # 0 - Header Byte # 3 Pattern Register	R/W	0x00
0x1F47	Transmit ATM - User Cell Filter # 0 - Header Byte # 4 Pattern Register	R/W	0x00
0x1F48	Transmit ATM - User Cell Filter # 0 - Header Byte # 1 Check Register	R/W	0x00
0x1F49	Transmit ATM - User Cell Filter # 0 - Header Byte # 2 Check Register	R/W	0x00
0x1F4A	Transmit ATM - User Cell Filter # 0 - Header Byte # 3 Check Register	R/W	0x00
0x1F4B	Transmit ATM - User Cell Filter # 0 - Header Byte # 4 Check Register	R/W	0x00

TRANSMIT ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
TRANSMIT ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1F4C	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x1F4D	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x1F4E	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x1F4F	Transmit ATM - User Cell Filter # 0 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1F50 - 0x1F52	Reserved		
0x1F53	Transmit ATM - User Cell Filter # 1 - Filter Control Register	R/W	0x00
0x1F54	Transmit ATM - User Cell Filter # 1 - Header Byte # 1 Pattern Register	R/W	0x00
0x1F55	Transmit ATM - User Cell Filter # 1 - Header Byte # 2 Pattern Register	R/W	0x00
0x1F56	Transmit ATM - User Cell Filter # 1 - Header Byte # 3 Pattern Register	R/W	0x00
0x1F57	Transmit ATM - User Cell Filter # 1 - Header Byte # 4 Pattern Register	R/W	0x00
0x1F58	Transmit ATM - User Cell Filter # 1 - Header Byte # 1 Check Register	R/W	0x00
0x1F59	Transmit ATM - User Cell Filter # 1 - Header Byte # 2 Check Register	R/W	0x00
0x1F5A	Transmit ATM - User Cell Filter # 1 - Header Byte # 3 Check Register	R/W	0x00
0x1F5B	Transmit ATM - User Cell Filter # 1 - Header Byte # 4 Check Register	R/W	0x00
0x1F5C	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x1F5D	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x1F5E	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x1F5F	Transmit ATM - User Cell Filter # 1 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1F60 - 0x1F62	Reserved		
0x1F63	Transmit ATM - User Cell Filter # 2 - Filter Control Register	R/W	0x00
0x1F64	Transmit ATM - User Cell Filter # 2 - Header Byte # 1 Pattern Register	R/W	0x00
0x1F65	Transmit ATM - User Cell Filter # 2 - Header Byte # 2 Pattern Register	R/W	0x00
0x1F66	Transmit ATM - User Cell Filter # 2 - Header Byte # 3 Pattern Register	R/W	0x00
0x1F67	Transmit ATM - User Cell Filter # 2 - Header Byte # 4 Pattern Register	R/W	0x00
0x1F68	Transmit ATM - User Cell Filter # 2 - Header Byte # 1 Check Register	R/W	0x00
0x1F69	Transmit ATM - User Cell Filter # 2 - Header Byte # 2 Check Register	R/W	0x00
0x1F6A	Transmit ATM - User Cell Filter # 2 - Header Byte # 3 Check Register	R/W	0x00
0x1F6B	Transmit ATM - User Cell Filter # 2 - Header Byte # 4 Check Register	R/W	0x00
0x1F6C	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x1F6D	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 2	RUR	0x00

TRANSMIT ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
CHANNEL CONTROL REGISTERS			
TRANSMIT ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK CONTROL REGISTERS			
0x1F6E	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x1F6F	Transmit ATM - User Cell Filter # 2 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1F70 - 0x1F72	Reserved		
0x1F73	Transmit ATM - User Cell Filter # 3 - Filter Control Register	R/W	0x00
0x1F74	Transmit ATM - User Cell Filter # 3 - Header Byte # 1 Pattern Register	R/W	0x00
0x1F75	Transmit ATM - User Cell Filter # 3 - Header Byte # 2 Pattern Register	R/W	0x00
0x1F76	Transmit ATM - User Cell Filter # 3 - Header Byte # 3 Pattern Register	R/W	0x00
0x1F77	Transmit ATM - User Cell Filter # 3 - Header Byte # 4 Pattern Register	R/W	0x00
0x1F78	Transmit ATM - User Cell Filter # 3 - Header Byte # 1 Check Register	R/W	0x00
0x1F79	Transmit ATM - User Cell Filter # 3 - Header Byte # 2 Check Register	R/W	0x00
0x1F7A	Transmit ATM - User Cell Filter # 3 - Header Byte # 3 Check Register	R/W	0x00
0x1F7B	Transmit ATM - User Cell Filter # 3 - Header Byte # 4 Check Register	R/W	0x00
0x1F7C	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 3	RUR	0x00
0x1F7D	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 2	RUR	0x00
0x1F7E	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 1	RUR	0x00
0x1F7F	Transmit ATM - User Cell Filter # 3 - Filtered Cell Count Register - Byte 0	RUR	0x00
0x1F80 - 0x1FFF	Reserved		

OPERATION BLOCK INTERRUPT REGISTER BIT FORMATS

Operation Control Register - Byte 3 (Address = 0x0100)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Configura-tion Control
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
0	Configuration Control	R/W	**Configuration Control:** This READ/WRITE bit-field permits the user to configure the XRT79L71 to support any of the following configurations. • ATM/PPP • Clear Channel/HDLC The following table presents the relationship between the value written into these register bits and the corresponding Mode of operation.

Configuration Control	Mode
0	ATM/PPP
1	Clear Channel/HDLC

Operation Control Register - Byte 2 (Address = 0x0101)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Interrupt WC/INT*	Enable Interrupt Auto-Clear	Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 3	Unused	R/O	Please set to "0" for normal operation.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Interrupt Write to Clear/ RUR	R/W	**Interrupt - Write to Clear/RUR Select:** This READ/WRITE bit-field permits the user to configure all of the Source-Level Interrupt Status bits (within the XRT79L71) to either be Write to Clear (WTC) or Reset-upon-Read (RUR) bits. 0 - Configures all Source-Level Interrupt Status register bits to function as Reset-upon-Read (RUR). 1 - Configures all Source-Level Interrupt Status register bits to function as Write-to-Clear (WTC).
1	Enable Interrupt Clear	R/W	**Enable Auto-Clear of Interrupts Select:** This READ/WRITE bit-field permits the user to configure the XRT79L71 to automatically disable all interrupts that are activated. 0 - Configures the chip to NOT automatically disable any Interrupts following their activation. 1 - Configures the chip to automatically disable all Interrupts following their activation.
0	Interrupt Enable	R/W	**Interrupt Enable:** This READ/WRITE bit-field permits the user to configure the XRT79L71 to generate interrupt requests to the Microprocessor. 0 - Configures the chip to NOT generate interrupt to the Microprocessor. All interrupts are disabled and the Microprocessor must poll the register bits. 1 - Configures the chip to generate interrupts to the Microprocessor.

Operation Control - Loop-back Control Register (Address = 0x0102)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Loop-back Control [3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
3 - 0	Loop-back Control [3:0]	R/W	**Loop-back Mode Select:** These READ/WRITE bit-fields permit the user to configure the XRT79L71 to operate in any of the following loop-back modes. • Local Medium Loop-back • Remote Host Loop-back The following table presents the contents of these bit-fields and the corresponding Loop-back Modes. **Loop-back Control [3:0]** / **Resulting Loop-back Mode** 0000 - 0011 / Reserved 0100 / Local Medium Loop-back Mode 0101 / Remote Host Loop-back Mode 0101 - 1111 / Reserved ***NOTE:*** *The Local Medium Loop-back Mode is only available if the XRT79L71 has been configured to operate in the ATM UNI or in the PPP Modes*

Operation Control Register - Byte 0 (Address = 0x0103)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Reserved			PPP/ATM*	Reserved	Software RESET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-6	Reserved	R/W	Set to "1" for Normal Operation.
5 - 3	Reserved	R/O	
2	PPP/ATM*	R/W	**PPP/ATM UNI Mode Select:** This READ-WRITE bit-field permits the user to configure the XRT79L71 to operate in either the ATM UNI or PPP Mode. If Bit 3 (Dual Bus), within the Operation Control Register - Byte 3 is set to "0", then this bit-field will then dictate the operating mode of the XRT79L71. 0 - Configures the XRT79L71 to operate in the ATM UNI Mode. 1 - Configures the XRT79L71 to operate in the PPP Mode. ***NOTE:*** *This bit-field is ignored if Bit 0 (Configuration Control) within the Operation Control Register - Byte 3 is is set to "1".*
1	Reserved	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Software RESET	R/W	**Software RESET:** This READ-WRITE bit-field permits the user to reset the XRT79L71. 0 - Normal Operation. 1 - Configure the XRT79L71 into RESET Mode.

Device ID Register (Address = 0x0104)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE_ID_VALUE [7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Device ID Value	R/O	**Device ID Value:** This READ-ONLY bit-field is set to the value "0x7A" and permits the user's software code to uniquely identify this device as the XRT79L71.

Revision ID Register (Address = 0x0105)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Revision Number Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Revision Number Value	R/O	**Revision Number Value:** This READ-ONLY bit-field is set to the value that corresponds to its revision number. Revision A silicon will be set to the value "0x01". This register permits the user's software code to uniquely identify the revision number of the XRT79L71.

Operation Interrupt Status Register - Byte 1 (Address = 0x0112)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS3/E3 LIU/JA Block Interrupt Status	DS3/E3 Framer Block Interrupt Status	Unused	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	DS3/E3 LIU/JA Block Interrupt Status	R/O	**DS3/E3 LIU/JA Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a DS3/E3 LIU/JA Block interrupt is awaiting service. 0 - No DS3/E3 LIU/Jitter Attenuator block interrupt is awaiting service. 1 - At least one DS3/E3 LIU/Jitter Attenuator block interrupt is awaiting service.
2	DS3/E3 Framer Block Interrupt Status	R/O	**DS3/E3 Framer Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a DS3/E3 Framer Block interrupt is awaiting service. 0 - No DS3/E3 Framer block interrupt is awaiting service. 1 - At least one DS3/E3 Framer block interrupt is awaiting service.
1 - 0	Unused	R/O	

Operation Interrupt Status Register - Byte 0 (Address = 0x0113)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive ATM Cell/ PPP Processor Block Interrupt Status	Unused			Transmit ATM Cell/ PPP Processor Block Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 -5	Unused	R/O	
4	Receive ATM Cell/PPP Processor Block Interrupt Status	R/O	**Receive ATM Cell/PPP Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a Receive ATM Cell/PPP Processor Block Interrupt is awaiting service. 0 - No Receive ATM Cell/PPP Processor block interrupt is awaiting service. 1 - At least one Receive ATM Cell/PPP Processor block interrupt is awaiting service.
3 - 1	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Transmit ATM Cell/PPP Processor Block Interrupt Status	R/O	**Receive ATM Cell/PPP Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a Receive ATM Cell/PPP Processor Block Interrupt is awaiting service. 0 - No Receive ATM Cell/PPP Processor block interrupt is awaiting service. 1 - At least one Receive ATM Cell/PPP Processor block interrupt is awaiting service.

Operation Interrupt Enable Register - Byte 1 (Address = 0x0116)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS3/E3 LIU/JA Block Interrupt Enable	DS3/E3 Framer Block Interrupt Enable	Unused	
R/O	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused		
3	DS3/E3 LIU/JA Block Interrupt Enable	R/W	**DS3/E3 LIU/Jitter Attenuator Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the DS3/E3 LIU/JA Block for interrupt generation. If the user writes a "0" to this register bit and disables the DS3/E3 LIU/JA Block (for interrupt generation), then all DS3/E3 LIU/JA Block interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, the user will still need to enable the individual DS3/E3 LIU/JA Block interrupt(s) at the Source Level in order to enable that particular interrupt. 0 - Disable all DS3/E3 LIU/JA Block interrupts within the device. 1 - Enables the DS3/E3 LIU/JA Block at the Block-Level.
2	DS3/E3 Framer Block Interrupt Enable	R/W	**DS3/E3 Framer Block Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the DS3/E3 Framer Block for interrupt generation. If the user writes a "0" to this register bit and disables the DS3/E3 Framer Block (for interrupt generation), then all DS3/E3 Framer Block interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, the user will still need to enable the individual DS3/E3 Framer Block interrupt(s) at the Source Level in order to enable that particular interrupt. 0 - Disable all DS3/E3 Framer Block interrupts within the device. 1 - Enables the DS3/E3 Framer Block at the Block-Level.
1 - 0	Unused		

Operation Interrupt Enable Register - Byte 0 (Address = 0x0117)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive ATM Cell/ PPP Proces-sor Block Interrupt Enable	Unused			Transmit ATM Cell/ PPP Proces-sor Block Interrupt Enable
R/W	R/O	R/O	R/W	R/W	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	Receive ATM Cell/PPP Processor Block Interrupt Enable	R/W	**Receive ATM Cell/PPP Packet Processor Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the Receive ATM Cell/PPP Packet Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the Receive ATM Cell/PPP Packet Processor Block (for interrupt generation), then all Receive ATM Cell/PPP Packet Processor Block interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, the user will still need to enable the individual Receive ATM Cell/PPP Packet Processor Block interrupt(s) at the Source Level in order to enable that particular interrupt. 0 - Disable all Receive ATM Cell/PPP Packet Processor Block interrupts within the device. 1 - Enables the Receive ATM Cell/PPP Packet Processor Block for interrupt generation at the Block-Level.
3	Transmit UTOPIA/POS-PHY Interface Block Interrupt Enable	R/W	**Transmit UTOPIA/POS-PHY Interface Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the Transmit UTOPIA/POS-PHY Interface Block for interrupt generation. If the user writes a "0" to this register bit and disables the Transmit UTOPIA/POS-PHY Interface Block (for interrupt generation), then all Transmit UTOPIA/POS-PHY Interface Block interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, the user will still need to enable the individual Transmit UTOPIA/POS-PHY Interface Block interrupt(s) at the Source Level in order to enable that particular interrupt. 0 - Disable all Transmit UTOPIA/POS-PHY Interface Block interrupts within the device. 1 - Enables the Transmit UTOPIA/POS-PHY Interface Block at the Block-Level.
2 - 1	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Transmit ATM Cell/PPP Processor Block Interrupt Enable	R/W	**Transmit ATM Cell/PPP Packet Processor Block Interrupt Enable:** This READ/WRITE bit permit the user to either enable or disable the Transmit ATM Cell/PPP Packet Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the Transmit ATM Cell/PPP Packet Processor Block (for interrupt generation), then all Transmit ATM Cell/PPP Packet Processor Block interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, the user will still need to enable the individual Transmit ATM Cell/PPP Packet Processor Block interrupt(s) at the Source Level in order to enable that particular interrupt. 0 - Disable all Transmit ATM Cell/PPP Packet Processor Block interrupts within the device. 1 - Enables the Transmit ATM Cell/PPP Packet Processor Block for interrupt generation at the Block-Level.

CHANNEL INTERRUPT INDICATION REGISTERS

Channel Interrupt Indicator - Receive Cell Processor/PPP Processor Block (Address = 0x0119)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Receive ATM Cell/PPP Packet Processor Block Interrupt
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	Receive ATM Cell/PPP Packet Processor Block Interrupt	R/O	**Receive ATM Cell/PPP Packet Processor Block Interrupt - XRT79L71:** This READ/ONLY bit-field indicates whether or not the Receive ATM Cell Processor block, associated with the XRT79L71 is declaring an Interrupt, as described below. 0 - The Receive ATM Cell/PPP Packet Processor block, associated with the XRT79L71 is NOT declaring an Interrupt. 1 - The Receive ATM Cell/PPP Packet Processor block, associated with the XRT79L71 is currently declaring an interrupt.

Channel Interrupt Indicator - LIU/Jitter Attenuator Block (Address = 0x011D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							LIU/JA Block Interrupt-Channel 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	LIU/JA Block Interrupt - Channel 0	R/O	**LIU/JA Block Interrupt - Channel 0:** This READ/ONLY bit-field indicates whether or not the LIU/JA block, associated with XRT79L71 is declaring an Interrupt, as described below. 0 - The LIU/JA block, associated with XRT79L71 is NOT declaring an Interrupt. 1 - The LIU/JA block, associated with XRT79L71 is currently declaring an interrupt.

Channel Interrupt Indicator - Transmit Cell Processor/PPP Processor Block (Address = 0x0121)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Transmit ATM Cell/PPP Packet Processor Block Interrupt
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	Transmit ATM Cell/PPP Packet Processor Block Interrupt	R/O	**Transmit ATM Cell/PPP Packet Processor Block Interrupt - XRT79L71:** This READ/ONLY bit-field indicates whether or not the Transmit ATM Cell/PPP Packet Processor block, associated with XRT79L71 is declaring an Interrupt, as described below. 0 - The Transmit ATM Cell/PPP Packet Processor block, associated with XRT79L71 is NOT declaring an Interrupt. 1 - The Transmit ATM Cell/PPP Packet Processor block, associated with XRT79L71 is currently declaring an interrupt.

Channel Interrupt Indicator - DS3/E3 Framer Block (Address = 0x0127)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							DS3/E3 Framer Block Interrupt
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	DS3/E3 Framer Block Interrupt - XRT79L71	R/O	**DS3/E3 Framer Block Interrupt - XRT79L71:** This READ/ONLY bit-field indicates whether or not the DS3/E3 Framer block, associated with XRT79L71 is declaring an Interrupt, as described below. 0 - The DS3/E3 Framer block, associated with XRT79L71 is NOT declaring an Interrupt. 1 - The DS3/E3 Framer block, associated with XRT79L71 is currently declaring an interrupt.

Operation General Purpose Pin Data Register (Address = 0x0147)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				General Purpose Data [3]	General Purpose Data [2]	General Purpose Data [1]	General Purpose Data [0]
R/O				R/W	R/W	R/W	R/W
0				0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	General Purpose Data[3]	R/W	**General Purpose Data - GPIO_3:** The exact function of this bit-field depends upon whether General Purpose I/O Pin, GPIO_3 (Pin R8) has been configured to function as an input or an output pin, as described below. **If GPIO_3 is configured to function as an input pin** If GPIO_3 is configured to function as an input pin, then the user can monitor the state of this particular input pin by reading out the state of this bit-field. If this bit-field is set to "0" then it means that GPIO_3 is currently pulled to a logic "Low" level. Conversely, if this bit-field is set to "1", then it means that GPIO_3 is currently pulled to a logic "High" level. ***NOTE:*** *If GPIO_3 is configured to function as an input pin, then writing to this particular register will have no affect on the state of this pin.* **If GPIO_3 is configured to function as an output pin.** If GPIO_3 is configured to function as an output pin, then the user can control the state of this particular output pin by writing the appropriate value to this bit-field. Setting this bit-field to "0" will cause GPIO_3 to be driven to a logic "Low" level. Conversely, setting this bit-field to "1" will cause GPIO_3 to be driven to a logic "High" level. ***NOTE:*** *GPIO_3 can be configured to function as either an input or output pin, by writing the appropriate value to Bit 3 (General Purpose Pin Direction[3]) within the Operation General Purpose Pin Direction Control Register (Address = 0x014B).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	General Purpose Data[2]	R/W	**General Purpose Data - GPIO_2:** The exact function of this bit-field depends upon whether General Purpose I/O Pin, GPIO_2 (Pin P8) has been configured to function as an input or an output pin, as described below. **If GPIO_2 is configured to function as an input pin** If GPIO_2 is configured to function as an input pin, then the user can monitor the state of this particular input pin by reading out the state of this bit-field.If this bit-field is set to "0" then it means that GPIO_2 is currently pulled to a logic "Low" level. Conversely, if this bit-field is set to "1", then it means that GPIO_2 is currently pulled to a logic "High" level. ***NOTE:*** *If GPIO_2 is configured to function as an input pin, then writing to this particular register will have no affect on the state of this pin.* **If GPIO_2 is configured to function as an output pin** If GPIO_2 is configured to function as an output pin, then the user can control the state of this particular output pin by writing the appropriate value to this bit-field. Setting this bit-field to "0" will cause GPIO_2 to be driven to a logic "Low" level. Conversely, setting this bit-field to "1" will cause GPIO_2 to be driven to a logic "High" level. ***NOTE:*** *GPIO_2 can be configured to function as either an input or output pin, by writing the appropriate value to Bit 2 (General Purpose Pin Direction[2]) within the Operation General Purpose Pin Direction Control Register (Address = 0x014B).*
1	General Purpose Data[1]	R/W	**General Purpose Data - GPIO_1:** The exact function of this bit-field depends upon whether General Purpose I/O Pin, GPIO_1 (Pin N8) has been configured to function as an input or an output pin, as described below. **If GPIO_1 is configured to function as an input pin** If GPIO_1 is configured to function as an input pin, then the user can monitor the state of this particular input pin by reading out the state of this bit-field.If this bit-field is set to "0" then it means that GPIO_1 is currently pulled to a logic "Low" level. Conversely, if this bit-field is set to "1", then it means that GPIO_1 is currently pulled to a logic "High" level. ***NOTE:*** *If GPIO_1 is configured to function as an input pin, then writing to this particular register will have no affect on the state of this pin.* **If GPIO_1 is configured to function as an output pin** If GPIO_1 is configured to function as an output pin, then the user can control the state of this particular output pin by writing the appropriate value to this bit-field.Setting this bit-field to "0" will cause GPIO_1 to be driven to a logic "Low" level. Conversely, setting this bit-field to "1" will cause GPIO_1 to be driven to a logic "High" level. ***NOTE:*** *GPIO_1 can be configured to function as either an input or output pin, by writing the appropriate value to Bit 1 (General Purpose Pin Direction[1]) within the Operation General Purpose Pin Direction Control Register (Address = 0x014B).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	General Purpose Data[0]	R/W	**General Purpose Data - GPIO_0:** The exact function of this bit-field depends upon whether General Purpose I/O Pin, GPIO_0 (Pin T7) has been configured to function as an input or an output pin, as described below. **If GPIO_0 is configured to function as an input pin** If GPIO_0 is configured to function as an input pin, then the user can monitor the state of this particular input pin by reading out the state of this bit-field. If this bit-field is set to "0" then it means that GPIO_0 is currently pulled to a logic "Low" level. Conversely, if this bit-field is set to "1", then it means that GPIO_0 is currently pulled to a logic "High" level. ***NOTE:*** *If GPIO_0 is configured to function as an input pin, then writing to this particular register will have no affect on the state of this pin.* **If GPIO_0 is configured to function as an output pin** If GPIO_0 is configured to function as an output pin, then the user can control the state of this particular output pin by writing the appropriate value to this bit-field. Setting this bit-field to "0" will cause GPIO_0 to be driven to a logic "Low" level. Conversely, setting this bit-field to "1" will cause GPIO_0 to be driven to a logic "High" level. ***NOTE:*** *GPIO_0 can be configured to function as either an input or output pin, by writing the appropriate value to Bit 0 (General Purpose Pin Direction[0]) within the "Operation General Purpose Pin Direction Control" Register (Address = 0x014B).*

Operation General Purpose Pin Direction Control Register (Address = 0x014B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				General Purpose Pin Direction [3]	General Purpose Pin Direction [2]	General Purpose Pin Direction [1]	General Purpose Pin Direction [0]
R/O				R/W	R/W	R/W	R/W
0				0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 -4	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	General Purpose Pin Direction - GPIO_3	R/W	**General Purpose Pin Direction - GPIO_3:** This READ/WRITE bit-field permits the user to define the General Purpose I/O Pin, GPIO_3 (Pin R8) as either in Input pin or an Output pin, as described below.0 - Configures GPIO_3 (Pin R8) to function as an input pin.1 - Configures GPIO_3 (Pin R8) to function as an output pin. ***NOTES:*** 1. *If GPIO_3 is configured to function as an input pin, then the user can monitor the state of this input pin by reading out the state of Bit 3 (General Purpose Data[3]) within the Operation General Purpose Pin Data Register (Address = 0x0147).* 2. *If GPIO_3 is configured to function as an output pin, then the user can control the state of this output pin by writing the appropriate value into Bit 3 (General Purpose Data[3]) within the Operation General Purpose Pin Data Register (Address =0x0147).*
2	General Purpose Pin Direction - GPIO_2	R/W	**General Purpose Pin Direction - GPIO_2:** This READ/WRITE bit-field permits the user to define the General Purpose I/O Pin, GPIO_2 (Pin P8) as either in Input pin or an Output pin, as described below.0 - Configures GPIO_2 (Pin P8) to function as an input pin.1 - Configures GPIO_2 (Pin P8) to function as an output pin. ***NOTES:*** 1. *If GPIO_2 is configured to function as an input pin, then the user can monitor the state of this input pin by reading out the state of Bit 2 (General Purpose Data[2]) within the Operation General Purpose Pin Data Register (Address = 0x0147).* 2. *If GPIO_2 is configured to function as an output pin, then the user can control the state of this output pin by writing the appropriate value into Bit 2 (General Purpose Data[2]) within the Operation General Purpose Pin Data Register (Address =0x0147).*
1	General Purpose Pin Direction - GPIO_1	R/W	**General Purpose Pin Direction - GPIO_1:** This READ/WRITE bit-field permits the user to define the General Purpose I/O Pin, GPIO_1 (Pin N8) as either in Input pin or an Output pin, as described below.0 - Configures GPIO_1 (Pin N8) to function as an input pin.1 - Configures GPIO_1 (Pin N8) to function as an output pin. ***NOTES:*** 1. *If GPIO_1 is configured to function as an input pin, then the user can monitor the state of this input pin by reading out the state of Bit 1 (General Purpose Data[1]) within the Operation General Purpose Pin Data Register (Address = 0x0147).* 2. *If GPIO_1 is configured to function as an output pin, then the user can control the state of this output pin by writing the appropriate value into Bit 1 (General Purpose Data[1]) within the Operation General Purpose Pin Data Register (Address =0x0147).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	General Purpose Pin Direction - GPIO_0	R/W	**General Purpose Pin Direction - GPIO_0:** This READ/WRITE bit-field permits the user to define the General Purpose I/O Pin, GPIO_0 (Pin T7) as either in Input pin or an Output pin, as described below.0 - Configures GPIO_0 (Pin T7) to function as an input pin.1 - Configures GPIO_0 (Pin T7) to function as an output pin. ***NOTES:*** 1. *If GPIO_0 is configured to function as an input pin, then the user can monitor the state of this input pin by reading out the state of Bit 0 (General Purpose Data[0]) within the Operation General Purpose Pin Data Register (Address = 0x0147).* 2. *If GPIO_0 is configured to function as an output pin, then the user can control the state of this output pin by writing the appropriate value into Bit 0 (General Purpose Data[0]) within the Operation General Purpose Pin Data Register (Address =0x0147).*

RECEIVE UTOPIA INTERFACE BLOCK - ATM UNI APPLICATIONS

This section presents the Register Description/Address Map of the control registers associated with the Receive UTOPIA Interface block for ATM UNI Applications. The Register Description/Address Map of these control registers for PPP Applications will be presented in the next sectionfor ATM UNI Applications. The Register Description/Address Map of these control registers for PPP Applications will be presented in the next section.

TABLE 2: RECEIVE UTOPIA INTERFACE BLOCK - REGISTER/ADDRESS MAP - ATM UNI APPLICATIONS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
RECEIVE UTOPIA INTERFACE - CONTROL REGISTERS			
0x0500	Reserved	R/O	0x00
0x0501	Receive UTOPIA Interface - Receive Control Register	R/W	0x00
0x0502	Receive UTOPIA Interface - Receive Control Register - Byte 1	R/W	0x00
0x0503	Receive UTOPIA Interface - Receive Control Register - Byte 0	R/W	0x00
0x0504 - 0x0512	Reserved	R/O	0x00
0x0513	Receive UTOPA Interface - Port Address Register	R/W	0x00
0x0514 - 0x0516	Reserved	R/O	0x00
0x0517	Receive UTOPIA Interface - Port Number Register	R/W	0x00
0x0518 - 0x057F	Reserved	R/O	0x00

Receive UTOPIA Interface - Receive Control Register - Byte 0 (Address = 0x0503)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive UTOPIA Level 3 Enable	Multi-PHY Polling Enable	Back to Back Polling Enable	Direct Status Indication Enable	Receive UTOPIA Data Bus Width [1:0]		Cell Size[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive UTOPIA Level 3 Enable	R/W	**Receive UTOPIA Level 3 Enable:** This READ/WRITE bit-field permits the user to configure the Receive UTOPIA Interface block to operate in either the UTOPIA Level 1 or 2 or UTOPIA Level 3 Modes, as described below. 0 - Configures the Receive UTOPIA Interface block to operate in the UTOPIA Level 1 or 2 Mode. 1 - Configures the Receive UTOPIA Interface block to operate in the UTOPIA Level 3 Mode. ***NOTE:*** *This particular bit-field only configures the Receive UTOPIA Interface block. The user must set Bit 7 (UTOPIA Level 3 Enable) within the Transmit UTOPIA Control Register - Byte 0 (Address = 0x0583) in order to configure the Transmit UTOPIA Interface block into the appropriate UTOPIA Level).*
6	Multi-PHY Polling Enable	R/W	**Multi-PHY Polling Enable:** This READ/WRITE bit-field permits the user to either enable or disable Multi-PHY Polling for the Receive UTOPIA Interface block. If the user implements this feature (and configures the XRT79L71 to operate in the Multi-PHY Mode) then the RxUClav output pin will be driven (either "High" or "Low") based upon the fill-status of the Receive FIFO within the Channel that corresponds to the Receive UTOPIA Address that is currently being applied to the RxUAddr[4:0] input pins. If the user does not implement this feature (and then configures the XRT79L71 to operate in the Single-PHY Mode), then the RxUClav output pin will unconditionally reflect the Receive FIFO fill-status for Channel 0. No attention will be paid to the address values placed upon the RxUAddr[4:0] input pins. 0 - Configures the Receive UTOPIA Interface block to operate in the Single-PHY Mode. 1 - Configures the Receive UTOPIA Interface block to operate in the Multi-PHY Mode.

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>5</td><td>Back-to-Back Polling Enable</td><td>R/W</td><td>Back-to-Back Polling Enable:
This READ/WRITE bit-field permits the user to configure the Receive UTOPIA Interface block to support Back-to-Back Polling.
Ordinarily, for Multi-PHY polling, the user is required to interleave all UTOPIA Address values (that are to be placed on the RxUAddr[4:0] input pins) with the NULL Address (e.g., 0x1F). However, if the user configures the Receive UTOPIA Interface block to operate in the UTOPIA Level 3 Mode, and if the user also enables Back-to-Back Polling, then the user does not need interleave the UTOPIA Addresses with the NULL Address. In this case, the user can simply apply a back-to-back stream of relevant UTOPIA Addresses to the RxUAddr[4:0] input pins, and the XRT79L71 will respond by driving the RxUClav output pins to the appropriate states (depending upon the Receive FIFO fill-status).
0 - Disables Back-to-Back Polling. In this mode, the user must interleave all UTOPIA Addresses (that are to be applied to the RxUAddr[4:0] input pins) with the NULL Address.
1 - Enables Back-to-Back Polling. In this mode, the user does not need to interleave all UTOPIA Addresses (that are to be applied to the RxUAddr[4:0] input pins) with the NULL Address.
NOTE: In order to configure the Receive UTOPIA Interface block to operate in the Back-to-Back Polling Mode, the user must also do the following.
a. Configure the Receive UTOPIA Interface to operate in the UTOPIA Level 3 Mode. This is accomplished by setting Bit 7 (UTOPIA Level 3 Disable) within this Register to "0".
b. Configure the Receive UTOPIA Interface to support Multi-PHY Polling. This is accomplished by setting Bit 6 (Multi-PHY Polling Enable) within this register to "1".</td></tr>
<tr><td>4</td><td>Direct Status Indication Enable</td><td>R/W</td><td></td></tr>
<tr><td>3 - 2</td><td>Receive UTOPIA Data Bus Width[1:0]</td><td>R/W</td><td>Receive UTOPIA Data Bus Width[1:0]:
These READ/WRITE bit-fields permit the user to select the width of the Receive UTOPIA Interface Data Buses. The relationship between the contents of these bit-fields and the corresponding widths of the Receive UTOPIA Interface Data Bus is tabulated below.
<table>
<tr><th colspan="2">Receive UTOPIA Data Bus Width[1:0]</th><th>Corresponding Receive UTOPIA Data Bus Width</th></tr>
<tr><td>0</td><td>0</td><td>Not Valid</td></tr>
<tr><td>0</td><td>1</td><td>8 bits</td></tr>
<tr><td>1</td><td>0</td><td>16 bits</td></tr>
<tr><td>1</td><td>1</td><td>Not Valid</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>1 - 0</td><td>Cell Size[1:0]</td><td></td><td>Cell Size[1:0]:
These two READ/WRITE bit-fields permit the user to specify the size of the ATM cell that will be handled by the Receive UTOPIA Interface blocks. The relationship between the contents of these bit-fields and the corresponding Cell Sizes are tabulated below.

<table>
<tr><th colspan="2">Cell Size[1:0]</th><th>Resulting Cell Size (Bytes)</th></tr>
<tr><td>0</td><td>0</td><td>52 bytes</td></tr>
<tr><td>0</td><td>1</td><td>53 bytes (Only valid for UTOPIA Level 1, and if the UTOPIA Data Bus Width is set to 8 bits)</td></tr>
<tr><td>1</td><td>0</td><td>54 bytes (Only valid for UTOPIA Levels 1 and 2)</td></tr>
<tr><td>1</td><td>1</td><td>56 bytes</td></tr>
</table>

NOTE: The user must bear in mind the UTOPIA Level and the UTOPIA Data Bus width selected, when selecting the Cell Size.</td></tr>
</table>

Receive UTOPIA Interface - Port Address Register (Address = 0x0513)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive UTOPIA Port Address[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4 - 0	Receive UTOPIA Port Address[4:0]	R/W	**Receive UTOPIA Port Address[4:0]:** These READ/WRITE register bits, along with the Receive UTOPIA Port Number[4:0] bits (within the Receive UTOPIA Port Number Register (Address = 0x0517) permit the user to assign a unique Receive UTOPIA address to each of the XRT79L71 devices. For UTOPIA Level 2/3 applications, the user can write in any value, ranging from 0x00 through 0x1E into this register. **The Receive UTOPIA Address Assignment Procedure:** In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT79L71, the user must do the following. **a.** Write the value corresponding to a given XRT79L71 Channel into the Receive UTOPIA Port Number Register (Address = 0x0517). **b.** Write the corresponding UTOPIA Address value into this register. Once this two-step procedure has been executed, then the XRT79L71 Channel (as specified during step a) will be assigned the Receive UTOPIA Address value (as specified during step b).

Receive UTOPIA Interface - Port Number Register (Address = 0x0517)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive UTOPIA Port Number[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4 - 0	Receive UTOPIA Port Number[4:0]	R/W	**Receive UTOPIA Port Number[4:0]:** These READ/WRITE register bits, along with the Receive UTOPIA Port Address[4:0] bits (within the Receive UTOPIA Port Address Register (Address = 0x0513) permit the user to assign a unique Receive UTOPIA address to the XRT79L71. **The Receive UTOPIA Address Assignment Procedure:** In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT79L71, the user must do the following. **a.** Write the value corresponding to a given XRT79L71 Channel into this register. **b.** Write the corresponding UTOPIA Address value into the Receive UTOPIA Port Address Register (Address = 0x0513). Once this two-step procedure has been executed, then the XRT79L71 Channel (as specified during step a) will be assigned the Receive UTOPIA Address value (as specified during step b).

THE RECEIVE POS-PHY INTERFACE BLOCK - PPP APPLICATIONS

This section presents the Register Description/Address Map of the control registers associated with the Receive POS-PHY Interface block for PPP Applications. The Register Description/Address Map of these control registers for ATM Applications are presented in the previous section.

RECEIVE POS-PHY INTERFACE BLOCK - REGISTER/ADDRESS MAP - PPP APPLICATIONS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
RECEIVE POS-PHY INTERFACE CONTROL REGISTERS			
0x0500	Receive POS-PHY Interface - Receive Control Register - Byte 2	R/W	0x00
0x0501	Receive POS-PHY Interface - Receive Control Register - Byte 1	R/W	0x00
0x0502	Receive POS-PHY Interface - Receive Control Register - Byte 0	R/W	0x00
0x0503 - 0x057F	Reserved	R/O	0x00

Receive POS-PHY Interface - Receive Control Register Byte - 2 (Address = 0x0500)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Receive Level 2 Packet Mode
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Receive Level 2 Mode</td><td>R/W</td><td>
Receive POS-PHY Level 2, Packet Mode:
This READ/WRITE bit-field along with Bits 1 and 0 (Receive_Mode[1:0]) within the Receive POS-PHY Interface - Receive Control Register - Byte 1 (Address 0x0501) permits the user to configure the Receive POS-PHY Interface block to operate in any of the following modes.
• The Level 2, Packet Mode
• The Level 2, Chunk Mode
• The Level 3, Packet Mode
• The Level 3
• Chunk Mode
The following table presents the relationship between these three bits, and the corresponding operating mode of the Receive POS-PHY Interface block.
<table>
<tr><th>Receive Mode[1:0]</th><th>Receive Level 2 Mode</th><th>Resulting Mode of Operation</th></tr>
<tr><td>00</td><td>X</td><td>Level 2, Chunk Mode</td></tr>
<tr><td>01</td><td>X</td><td>Level 3, Chunk Mode</td></tr>
<tr><td>10</td><td>0</td><td>Level 3, Packet Mode</td></tr>
<tr><td>XX</td><td>1</td><td>Level 2, Packet Mode</td></tr>
</table>
A brief description of the Receive POS-PHY Level 2 and Level 3 Modes are presented below.
If the Receive POS-PHY Interface block is configured to operate in the POS-PHY Level 2 Mode
If the Receive POS-PHY Interface block is configured to operate in the POS-PHY Level 2 Mode, then all of the following are true.
• When polling, the Receive POS-PHY Interface block will drive the RxPPA output pin to the appropriate level (reflecting the RxFIFO fill-status) within ONE RxPClk period (in lieu of two RxPClk periods) after sampling a given POS-PHY Port Address via the RxPAddr[4:0] input pins.
• The Link Layer Processor must employ Out-of-Band Addressing whenever it wishes to perform a Select to READ operation with the Receive POS-PHY Interface block. In contrast to the POS-PHY Level 3 Mode, this means that the Link Layer Processor will function as the POS-PHY Bus Master for all operations (including Select to READ).
</td></tr>
</table>

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Receive Level 2 Mode (CONTINUED)	R/W	**If the Receive POS-PHY Interface block is configured to operate in the Receive POS-PHY Level 3 Mode** If the Receive POS-PHY Interface block is configured to operate in the POS-PHY Level 3 Mode, then all of the following are true.· When polling, the Receive POS-PHY Interface block will drive the RxPPA output pin to the appropriate level (reflecting the RxFIFO fill-status) within TWO RxPClk periods (in lieu of one RxPClk periods) after sampling a given POS-PHY Port Address via the RxPAddr[4:0] input pins.· The Link Layer Processor must be responsive to In-Band Addressing signals from the Receive POS-PHY Interface block, anytime it (the Receive POS-PHY Interface block) wishes to perform Select to READ operations with the Link Layer Processor. This means that for Select to READ operations, the Receive POS-PHY Interface (and NOT the Link Layer Processor) will function as the POS-PHY Bus Master. ***NOTE:*** *If the user configures the Receive POS-PHY Interface block to operate in the POS-PHY Level 3 Mode, then (for Multi-PHY Applications) the Receive POS-PHY Interface (and NOT the Link Layer Processor) will function as the POS-PHY Bus Master, particular during Select to READ Operations. As a consequence, if the user plans to design the XRT79L71 in a PPP Applications, in which multiple PHY-Layer devices will share a common POS-PHY Bus, then the user is strongly advised to ONLY configure the Receive POS-PHY Interface (within the XRT79L71) to operate in the POS-PHY Level 2 Mode. The XRT79L71 does not contain any hooks to support any sort of POS-PHY Arbitration Scheme if it is configured to operate in the POS-PHY Level 3 Mode.*

Receive POS-PHY Interface - Receive Control Register Byte - 1 (Address = 0x0501)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Chunk_Size[2:0]/ RxFIFO_Packet_Fill_Level[2:0]			Receive POS-PHY Data Bus Width[1:0]		Receive Mode[1:0]	
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>6 - 4</td><td>Chunk_Size[2:0]/RxFIFO Packet Fill Level[2:0]</td><td>R/W</td><td>
Chunk_Size[2:0]/RxFIFO Packet Fill Level[2:0]:
The exact function of these three READ/WRITE bit-fields depends upon whether the Receive POS-PHY Interface block has been configured to operate in the Packet or Chunk Mode, as described below.
If the Receive POS-PHY Interface block is operating in the Chunk Mode
If the user has configured the Receive POS-PHY Interface block to operate in the Chunk Mode, then these three bit-fields permit the user to define the size of Chunks within the incoming Packet data-stream. The following table presents the relationship between the contents of these three bit-fields and the corresponding size of the fix-sized chunks that exist within the incoming PPP packet data-stream.
<table>
<tr><th>Chunk_Size[2:0]</th><th>Number of Bytes/Chunk</th></tr>
<tr><td>000</td><td>4 Bytes</td></tr>
<tr><td>001</td><td>8 Bytes</td></tr>
<tr><td>010</td><td>16 Bytes</td></tr>
<tr><td>011</td><td>32 Bytes</td></tr>
<tr><td>100</td><td>64 Bytes</td></tr>
<tr><td>101</td><td>128 Bytes</td></tr>
<tr><td>11X</td><td>Not Valid</td></tr>
</table>
If the Receive POS-PHY Interface block is operating in the Packet Mode
If the user has configured the Receive POS-PHY Interface block to operate in the Packet Mode, then these three bit-fields permit the user to specify the minimum number of bytes (of Packet data) that MUST exist within the RxFIFO before the Receive POS-PHY Interface block will drive the RxPPA output pin "High", when polled. The following table presents the relationship between the contents of these three bit-fields and the corresponding number of packet data bytes (within the RxFIFO) that are required to assert the RxPPA output pin.
<table>
<tr><th>RxFIFO Packet Fill Level[2:0]</th><th>Number of Packet Bytes required (within RxFIFO) to Assert RxPPA</th></tr>
<tr><td>000</td><td>1 Bytes</td></tr>
<tr><td>001</td><td>2 Bytes</td></tr>
<tr><td>010</td><td>4 Bytes</td></tr>
<tr><td>011</td><td>8 Bytes</td></tr>
<tr><td>100</td><td>16 Bytes</td></tr>
<tr><td>101</td><td>32 Bytes</td></tr>
<tr><td>110</td><td>64 Bytes</td></tr>
<tr><td>111</td><td>128 Bytes</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>3 - 2</td><td>Receive POS-PHY Data Bus Width[1:0]</td><td>R/W</td><td>Receive POS-PHY Data Bus Width[1:0]:
These two READ/WRITE bit-fields permit the user to select/ specify the width of the Receive POS-PHY Data Bus. The following table presents the relationship between the contents within these two bit-fields and the corresponding width of the Receive POS-PHY Data Bus.
<table><tr><th>Receive POS-PHY Data Bus Width[1:0]</th><th>Width of Receive POS-PHY Data Bus</th></tr><tr><td>000</td><td>Inactive</td></tr><tr><td>001</td><td>Unused</td></tr><tr><td>010</td><td>16 - bits</td></tr><tr><td>011</td><td>8 - bits</td></tr></table>
NOTE: This configuration setting only applies to the Receive POS-PHY Interface block, and does not apply to the Transmit POS-PHY Interface block.</td></tr>
<tr><td>1 - 0</td><td>Receive Mode[1:0]</td><td>R/W</td><td>Receive POS-PHY Interface Mode[1:0]:
These two READ/WRITE bit-fields, along with Bit 0 (Receive POS-PHY Level 2 Packet Mode) within the Receive POS-PHY Interface - Receive Control Register Byte 2 (Address = 0x0500) permit the user to configure the Receive POS-PHY Interface block to operate in any of the following modes.
• Level 2 Packet Mode
• Level 2, Chunk Mode
• Level 3, Packet Mode
• Level 3, Chunk Mode
The following table presents the relationship between these three bits and the corresponding operating mode of the Receive POS-PHY Interface block.
<table><tr><th>Receive Mode[1:0]</th><th>Receive Level 2 Mode</th><th>Resulting Mode of Operation</th></tr><tr><td>00</td><td>X</td><td>Level 2, Chunk Mode</td></tr><tr><td>01</td><td>X</td><td>Level 3, Chunk Mode</td></tr><tr><td>10</td><td>0</td><td>Level 3, Packet Mode</td></tr><tr><td>10</td><td>1</td><td>Level 2, Packet Mode</td></tr></table>
A brief description of the Receive POS-PHY Level 2 and Level 3 Modes are presented below.</td></tr>
</table>

BIT NUMBER	NAME	TYPE	DESCRIPTION
1 - 0	Receive Mode[1:0] **Continued**	R/W	**If the Receive POS-PHY Interface block is configured to operate in the POS-PHY Level 2 Mode** If the Receive POS-PHY Interface block is configured to operate in the POS-PHY Level 2 Mode, then all of the following are true. • When polling, the Receive POS-PHY Interface block will drive the RxPPA output pin to the appropriate level (reflecting the RxFIFO fill-status) within ONE RxPClk period (in lieu of two RxPClk periods) after sampling a given POS-PHY Port Address via the RxPAddr[4:0] input pins. • The Link Layer Processor must employ Out-of-Band Addressing whenever it wishes to perform a Select to READ operation with the Receive POS-PHY Interface block. In contrast to the POS-PHY Level 3 Mode, this means that the Link Layer Processor will function as the POS-PHY Bus Master for all operations (including Select to READ). If the Receive POS-PHY Interface block is configured to operate in the Receive POS-PHY Level 3 Mode **If the Receive POS-PHY Interface block is configured to operate in the POS-PHY Level 3 Mode, then all of the following are true.** • When polling, the Receive POS-PHY Interface block will drive the RxPPA output pin to the appropriate level (reflecting the RxFIFO fill-status) within TWO RxPClk periods (in lieu of one RxPClk periods) after sampling a given POS-PHY Port Address via the RxPAddr[4:0] input pins. • The Link Layer Processor must be responsive to In-Band Addressing signals from the Receive POS-PHY Interface block, anytime it (the Receive POS-PHY Interface block) wishes to perform Select to READ operations with the Link Layer Processor. This means that for Select to READ operations, the Receive POS-PHY Interface (and NOT the Link Layer Processor) will function as the POS-PHY Bus Master. ***NOTE:*** *If the user configures the Receive POS-PHY Interface block to operate in the POS-PHY Level 3 Mode, then (for Multi-PHY Applications) the Receive POS-PHY Interface (and NOT the Link Layer Processor) will function as the POS-PHY Bus Master, particular during Select to READ Operations. As a consequence, if the user plans to design the XRT79L71 in a PPP Applications, in which multiple PHY-Layer devices will share a common POS-PHY Bus, then the user is strongly advised to ONLY configure the Receive POS-PHY Interface (within the XRT79L71) to operate in the POS-PHY Level 2 Mode. The XRT79L71 does not contain any hooks to support any sort of POS-PHY Arbitration Scheme if it is configured to operate in the POS-PHY Level 3 Mode.*

Receive POS-PHY Interface - Receive Control Register Byte - 0 (Address = 0x0502)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	AUTO Stop Enable	Receive_POS_PHY_Addr[4:0]					
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	X	X	X	X	X	X

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/W	
5	AUTO Stop Enable	R/W	**Receive POS-PHY Interface - AUTO STOP Enable:** This READ/WRITE bit-field permits the user to either enable or disable the AUTO-STOP feature within the Receive POS-PHY Interface block. If the AUTO-STOP feature is enabled, then the Receive POS-PHY Interface block will automatically terminate its transmission of data (to the Link Layer Processor) once it has reached the end of the Packet (even if the Link Layer Processor block continues to assert the RxPEnb* signal. The Link Layer Processor block has to re-assert the RxPEnb* input pin in order to begin the process of reading out the next packet. 0 - Disable the AUTO-STOP feature. 1 - Enables the AUTO-STOP feature.
4 - 0	Receive POS-PHY Addr[4:0]	R/W	**Receive POS-PHY Interface - Port Address:** These five READ/WRITE bit-fields permit the user to assign a Receive POS-PHY Port Address to the Receive POS-PHY Interface block. ***NOTE:*** *The Saturn POS-PHY Level 2 and 3 specifications permit the user to assign a Receive POS-PHY Port Address of any five-bit value other than 0x1F (the NULL Address).*

TRANSMIT UTOPIA INTERFACE BLOCK - ATM UNI APPLICATIONS

This section presents the Register Description/Address Map of the control registers associated with the Transmit UTOPIA Interface blocks for ATM UNI Applications. The Register Description/Address Map of these control registers for PPP Applications will be presented in the next section.

TABLE 3: TRANSMIT UTOPIA INTERFACE BLOCK - REGISTER/ADDRESS MAP - ATM UNI APPLICATIONS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
TRANSMIT UTOPIA INTERFACE CONTROL REGISTERS			
00x580	Reserved	R/O	0x00
0x0581	Transmit UTOPIA Interface - Transmit Control Register - Byte 2	R/W	0x38
0x0582	Transmit UTOPIA Interface - Transmit Control Register - Byte 1	R/W	0x00
0x0583	Transmit UTOPIA Interface - Transmit Control Register - Byte 0	R/W	0x00
0x0584 - 0x0592	Reserved	R/O	0x00
0x0593	Transmit UTOPIA Interface - Port Address Register	R/W	0x00
0x0594 - 0x0596	Reserved	R/O	0x00
0x0597	Transmit UTOPIA Interface - Port Number Register	R/W	0x00
0x0598 - 0x10FF	Reserved	R/O	0x00

Transmit UTOPIA Interface - Transmit Control Register - Byte 0 (Address = 0x0583)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit UTOPIA Level 3 Enable	Multi-PHY Polling Enable	Back to Back Polling Enable	Direct Status Indication Enable	Transmit UTOPIA Data Bus Width		Cell Size[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Transmit UTOPIA Level 3 Enable	R/W	**Transmit UTOPIA Level 3 Enable:** This READ/WRITE bit-field configures the Transmit UTOPIA Interface block to operate in either the UTOPIA Level 1 or 2 or UTOPIA Level 3 Mode as described below. 0 - Configures the Transmit UTOPIA Interface block to operate in the UTOPIA Level 1 or 2 Mode. 1 - Configures the Transmit UTOPIA Interface block to operate in the UTOPIA Level 3 Mode. ***NOTE:*** *This particular bit-field only configures the Transmit UTOPIA Interface block. The user must set Bit 7 (UTOPIA Level 3 Enable) within the Receive UTOPIA Control Register - Byte 0 (Address = 0x0503) in order to configure the Receive UTOPIA Interface block into the appropriate UTOPIA Level).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	Multi-PHY Polling Enable	R/W	**Multi-PHY Polling Enable:** This READ/WRITE bit-field permits the user to either enable or disable Multi-PHY Polling for the Transmit UTOPIA Interface block. If the user implements this feature (and configures the XRT79L71 to operate in the Multi-PHY Mode) then the TxUClav output pin will be driven (either "High" or "Low") based upon the fill-status of the Transmit FIFO within the Channel that corresponds to the Transmit UTOPIA Address that is currently being applied to the TxUAddr[4:0] input pins. If the user does not implement this feature (and then configures the XRT79L71 to operate in the Single-PHY Mode), then the TxUClav output pin will unconditionally reflect the Transmit FIFO fill-status for Channel 0. No attention will be paid to the address values placed upon the TxUAddr[4:0] input pins. 0 - Configures the Transmit UTOPIA Interface block to operate in the Single-PHY Mode. 1 - Configures the Transmit UTOPIA Interface block to operate in the Multi-PHY Mode.
5	Back-to-Back Polling Enable	R/W	**Back-to-Back Polling Enable:** This READ/WRITE bit-field permits the user to configure the Transmit UTOPIA Interface block to support Back-to-Back Polling. Ordinarily, for Multi-PHY polling, the user is required to interleave all UTOPIA Address values (that are to be placed on the TxUAddr[4:0] input pins) with the NULL Address (e.g., 0x1F). However, if the user configures the Transmit UTOPIA Interface block to operate in the UTOPIA Level 3 Mode, and if the user also enables Back-to-Back Polling, then the user does not need interleave the UTOPIA Addresses with the NULL Address. In this case, the user can simply apply a back-to-back stream of relevant UTOPIA Addresses to the TxUAddr[4:0] input pins, and the XRT79L71 will respond by driving the TxUClav output pins to the appropriate states (depending upon the Transmit FIFO fill-status). 0 - Disables Back-to-Back Polling. In this mode, the user must interleave all UTOPIA Addresses (that are to be applied to the TxUAddr[4:0] input pins) with the NULL Address. 1 - Enables Back-to-Back Polling. In this mode, the user does not need to interleave all UTOPIA Addresses (that are to be applied to the TxUAddr[4:0] input pins) with the NULL Address. ***NOTE:*** *In order to configure the Transmit UTOPIA Interface block to operate in the Back-to-Back Polling Mode, the user must also do the following.* **a.** Configure the Transmit UTOPIA Interface to operate in the UTOPIA Level 3 Mode. This is accomplished by setting Bit 7 (UTOPIA Level 3 Disable) within this Register to "0". **b.** Configure the Transmit UTOPIA Interface to support Multi-PHY Polling. This is accomplished by setting Bit 6 (Multi-PHY Polling Enable) within this register to "1".
4	Direct Status Indication Enable	R/W	

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>3 - 2</td><td>Transmit UTOPIA Data Bus Width[1:0]</td><td>R/W</td><td>Transmit UTOPIA Data Bus Width[1:0]:
These READ/WRITE bit-fields permit the user to select the width of the Transmit UTOPIA and POS-PHY Data Buses. The relationship between the contents of these bit-fields and the corresponding widths of the Transmit UTOPIA and POS-PHY Data Bus is tabulated below.
<table><tr><th colspan="2">Transmit UTOPIA Data Bus Width[1:0]</th><th>Corresponding Transmit UTOPIA Data Bus Width</th></tr><tr><td>0</td><td>0</td><td>Not Valid</td></tr><tr><td>0</td><td>1</td><td>8 bits</td></tr><tr><td>1</td><td>0</td><td>16 bits</td></tr><tr><td>1</td><td>1</td><td>Not Valid</td></tr></table></td></tr>
<tr><td>1 - 0</td><td>Cell Size[1:0]</td><td></td><td>Cell Size[1:0]:
These two READ/WRITE bit-fields permit the user to specify the size of the ATM cell that will be handled by the Transmit UTOPIA Interface blocks. The relationship between the contents of these bit-fields and the corresponding Cell Sizes are tabulated below.
<table><tr><th colspan="2">Cell Size[1:0]</th><th>Resulting Cell Size (Bytes)</th></tr><tr><td>0</td><td>0</td><td>52 bytes</td></tr><tr><td>0</td><td>1</td><td>53 bytes (Only valid for UTOPIA Level 1, and if the UTOPIA Data Bus Width is set to 8 bits)</td></tr><tr><td>1</td><td>0</td><td>54 bytes (Only valid for UTOPIA Levels 1 and 2)</td></tr><tr><td>1</td><td>1</td><td>56 bytes</td></tr></table>
NOTE: The user must bear in mind the UTOPIA Level and the UTOPIA Data Bus width selected, when selecting the Cell Size.</td></tr>
</table>

Transmit UTOPIA Interface - Port Address Register (Address = 0x0593)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Transmit UTOPIA Port Address[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4 - 0	Transmit UTOPIA Port Address[4:0]	R/W	**Transmit UTOPIA Port Address[4:0]:** These READ/WRITE register bits, along with the Transmit UTOPIA Port Number[4:0] bits (within the Trasnmit UTOPIA Port Number Register (Address = 0x0597) permit the user to assign a unique Transmit UTOPIA address the XRT79L71. For UTOPIA Level 2/3 applications, the user can write in any value, ranging from 0x00 through 0x1E into this register. **The Transmit UTOPIA Address Assignment Procedure:** In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT79L71, the user must do the following. **a.** Write the value corresponding to a given XRT79L71 Channel into the Transmit UTOPIA Port Number Register (Address = 0x0597). **b.** Write the corresponding UTOPIA Address value into this register. Once this two-step procedure has been executed, then the XRT79L71 Channel (as specified during step a) will be assigned the Transmit UTOPIA Address value (as specified during step b).

Transmit UTOPIA Interface - Port Number Register (Address = 0x0597)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Transmit UTOPIA Port Number[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4 - 0	Transmit UTOPIA Port Number[4:0]	R/W	**Transmit UTOPIA Port Number[4:0]:** These READ/WRITE register bits, along with the Transmit UTOPIA Port Address[4:0] bits (within the Transmit UTOPIA Port Address Register (Address = 0x0593) permit the user to assign a unique Transmit UTOPIA address to each XRT79L71. **The Transmit UTOPIA Address Assignment Procedure:** In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT79L71, the user must do the following. **a.** Write the value corresponding to a given XRT79L71 Channel into this register. **b.** Write the corresponding UTOPIA Address value into the Transmit UTOPIA Port Address Register (Address = 0x0593). Once this two-step procedure has been executed, then the XRT79L71 Channel (as specified during step a) will be assigned the Transmit UTOPIA Address value (as specified during step b).

THE TRANSMIT POS-PHY INTERFACE - PPP APPLICATIONS

This section presents the Register Description/Address Map of the control registers associated with the Transmit POS-PHY Interface block for PPP Applications. The Register Description/Address Map of these control registers for ATM Applications are presented in the previous section.

TABLE 4: TRANSMIT POS-PHY INTERFACE BLOCK - REGISTER/ADDRESS MAP - PPP APPLICATIONS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUES
0x0580	Transmit POS-PHY Interface - Transmit Control Register - Byte 2	R/W	0x00
0x0581	Transmit POS-PHY Interface - Transmit Control Register - Byte 1	R/W	0x00
0x0582	Transmit POS-PHY Interface - Transmit Control Register - Byte 0	R/W	0x00
0x0583 - 0x0FFF	Reserved	R/O	0x00

Transmit POS-PHY Interface - Transmit Control Register Byte - 2 (Address = 0x0580)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Transmit Level 2 Mode
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	X

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Transmit Level 2 Mode	R/W	**Transmit POS-PHY Level 2, Packet Mode:** This READ/WRITE bit-field along with Bits 1 and 0 (Transmit_Mode[1:0]) within the Transmit POS-PHY Interface - Transmit Control Register - Byte 1 permits the user to configure the Transmit POS-PHY Interface block to operate in any of the following modes.· The Level 2, Packet Mode· The Level 2, Chunk Mode· The Level 3, Packet Mode· The Level 3, Out-of-Band, Chunk Mode· The Level 3, In-Band, Chunk ModeThe following table presents the relationship between these three bits, and the corresponding operating mode of the Transmit POS-PHY Interface block.

Transmit Mode[1:0]	Transmit Level 2 Mode	Resulting Mode of Operation
00	0	Level 2, Chunk Mode
01	0	Level 3, Out-of-Band Chunk Mode
10	0	Level 3, In-Band Chunk Mode
11	0	Level 3, Packet Mode
11	1	Level 2, Packet Mode

A brief description of the Transmit POS-PHY Level 2 and 3 Modes are presented below.

If the Transmit POS-PHY Interface block is configured to operate in the POS-PHY Level 2 Mode

If the Transmit POS-PHY Interface block is configured to operate in the POS-PHY Level 2 Mode, then all of the following is true.

- When polling, the Receive POS-PHY Interface block will drive the TxPPA output pin to the appropriate level (reflecting the TxFIFO fill-status) within ONE TxPClk period (in lieu of two TxPClk periods) after sampling a given POS-PHY Port Address via the TxPAddr[4:0] input pins.

If the Transmit POS-PHY Interface block is configured to operate in the POS-PHY Level 3 Mode

If the Transmit POS-PHY Interface block is configured to operate in the POS-PHY Level 3 Mode, then all of the following are true.

- When polling, the Transmit POS-PHY Interface block will drive the TxPPA output pin to the appropriate level (reflecting the TxFIFO fill-status) within TWO TxPClk periods (in lieu of one TxPClk periods) after sampling a given POS-PHY Port Address via the TxPAddr[4:0] input pins.

Transmit POS-PHY Interface - Transmit Control Register Byte - 1 (Address = 0x0581)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Chunk_Size[2:0]/ TxFIFO_Packet_Fill_Level[2:0]			Transmit POS-PHY Data Bus Width[1:0]		Transmit Mode[1:0]	
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	X	X

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>Unused</td><td>R/O</td><td></td></tr>
<tr><td>6 - 4</td><td>Chunk_Size[2:0]/ TxFIFOPacket Fill Level[2:0]</td><td>R/W</td><td>Chunk_Size[2:0]/TxFIFO Packet Fill Level[2:0]:
The exact function of these three READ/WRITE bit-fields depends upon whether the Transmit POS-PHY Interface block has been configured to operate in the Packet or Chunk Mode, as described below.
If the Transmit POS-PHY Interface block is operating in the Chunk Mode
If the user has configured the Transmit POS-PHY Interface block to operate in the Chunk Mode, then these three bit-fields permit the user to define the size of the fixed-size Chunks that the Transmit POS-PHY Interface block will handle as it accepts PPP packet data from the Link Layer Processor. The following table presents the relationship between the contents of these three bit-fields and the corresponding size of the fixed-size chunks that the Transmit POS-PHY Interface block will accept from the Link Layer Processor.
<table>
<tr><th>Chunk_Size[2:0]</th><th>Number of Bytes/Chunk</th></tr>
<tr><td>000</td><td>4 Bytes</td></tr>
<tr><td>001</td><td>8 Bytes</td></tr>
<tr><td>010</td><td>16 Bytes</td></tr>
<tr><td>011</td><td>32 Bytes</td></tr>
<tr><td>100</td><td>64 Bytes</td></tr>
<tr><td>101</td><td>128 Bytes</td></tr>
<tr><td>11X</td><td>Not Valid</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>6 - 4</td><td>Chunk_Size[2:0]/ TxFIFOPacket Fill Level[2:0]
Continued</td><td>R/W</td><td>If the Transmit POS-PHY Interface block is operating in the Packet Mode
If the user has configured the Transmit POS-PHY Interface block to operate in the Packet Mode, then these three bit-fields permit the user to specify the minimum amount of empty space that must exist (within the TxFIFO) before the Transmit POS-PHY Interface block will drive the TxPPA output pin "High" when polled. The following table presents the relationship between the contents of these three bit-fields and the corresponding amount of empty space (in terms of bytes) that must exist within the TxFIFO in order to assert the TxPPA output pin.
<table>
<tr><th>TxFIFO Packet Fill Level[2:0]</th><th>Amount of Empty Space Required (within the TxFIFO) to Assert TxPPA</th></tr>
<tr><td>000</td><td>4 Bytes</td></tr>
<tr><td>001</td><td>8 Bytes</td></tr>
<tr><td>010</td><td>16 Bytes</td></tr>
<tr><td>011</td><td>32 Bytes</td></tr>
<tr><td>100</td><td>64 Bytes</td></tr>
<tr><td>101</td><td>128 Bytes</td></tr>
<tr><td>11X</td><td>Do Not Use</td></tr>
</table></td></tr>
<tr><td>3 -2</td><td>Transmit POS-PHY Data Bus Width[1:0]</td><td>R/W</td><td>Transmit POS-PHY Data Bus Width[1:0]:
These two READ/WRITE bit-fields permit the user to select/ specify the width of the Transmit POS-PHY Data Bus. The following table presents the relationship between the contents within these two bit-fields and the corresponding width of the Transmit POS-PHY Data Bus.
<table>
<tr><th>Transmit POS-PHY Data Bus Width[1:0]</th><th>Width of Transmit POS-PHY Data Bus</th></tr>
<tr><td>00</td><td>Inactive</td></tr>
<tr><td>01</td><td>Unused</td></tr>
<tr><td>10</td><td>16 - bits</td></tr>
<tr><td>11</td><td>8 - bits</td></tr>
</table></td></tr>
</table>

BIT NUMBER	NAME	TYPE	DESCRIPTION
1 - 0	Transmit Mode[1:0]	R/W	**Transmit POS-PHY Interface Mode[1:0]:** These two READ/WRITE bit-fields, along with Bit 0 (Transmit POS-PHY Level 2 Packet Mode) within the Transmit POS-PHY Interface - Transmit Control Register Byte 2 permit the user to configure the Transmit POS-PHY Interface block to operate in any of the following modes. • The Level 2, Packet Mode • The Level 2, Chunk Mode • The Level 3, Packet Mode • The Level 3, Out-of-Band, Chunk Mode • The Level 3, In-Band, Chunk Mode The following table presents the relationship between these three bits that the corresponding mode of the Transmit POS-PHY Interface block.

Transmit Mode[1:0]	Transmit Level 2 Mode	Resulting Mode of Operation
00	X	Level 2, Chunk Mode
01	X	Level 3, Out-of-Band Chunk Mode
10	X	Level 3, In-Band Chunk Mode
11	0	Level 3, Packet Mode
11	1	Level 2, Packet Mode

A brief description of the Transmit POS-PHY Level 2 and 3 Modes are presented below.

If the Transmit POS-PHY Interface block is configured to operate in the POS-PHY Level 2 Mode

If the Transmit POS-PHY Interface block is configured to operate in the POS-PHY Level 2 Mode, then all of the following is true.

- When polling, the Receive POS-PHY Interface block will drive the TxPPA output pin to the appropriate level (reflecting the TxFIFO fill-status) within ONE TxPClk period (in lieu of two TxPClk periods) after sampling a given POS-PHY Port Address via the TxPAddr[4:0] input pins.

If the Transmit POS-PHY Interface block is configured to operate in the POS-PHY Level 3 Mode

If the Transmit POS-PHY Interface block is configured to operate in the POS-PHY Level 3 Mode, then all of the following are true.

- When polling, the Transmit POS-PHY Interface block will drive the TxPPA output pin to the appropriate level (reflecting the TxFIFO fill-status) within TWO TxPClk periods (in lieu of one TxPClk periods) after sampling a given POS-PHY Port Address via the TxPAddr[4:0] input pins.

Transmit POS-PHY Interface - Transmit Control Register Byte - 0 (Address = 0x0582)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Runt Packet ABORT	Parity Check Enable	ODD Parity	Transmit_POS_PHY_Addr[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Runt Packet ABORT	R/W	**Runt Packet ABORT:** This READ/WRITE bit-field permits the user to either enable or disable the RUNT Packet Abort feature. If the user enables this feature, then anytime the Transmit POS-PHY Interface block receives a RUNT packet from the Link Layer Processor, this packet will be transmitted to the remote terminal as an Aborted Packet. ***NOTE:*** *An example of a RUNT packet being accepted by the Transmit POS-PHY Interface block is whenever the Link Layer Processor asserts the TxPSoP [Start of Packet) indicator multiple times without asserting the TxPEOP (End of Packet) indicator.* 0 - Disables the RUNT Packet Abort feature. 1 - Enables the RUNT Packet Abort feature.
6	Parity Check Enable	R/W	**Parity Check Enable** This READ/WRITE bit-field permits the user to either enable or disable parity checking of all data that is accepted by the Transmit POS-PHY Interface. If the user enables this feature, then the XRT79L71 will compute either the EVEN or ODD parity value (depending upon the setting of Bit 5, within this register) of each byte or word that is accepted by the Transmit POS-PHY Interface - Data Bus. The Transmit POS-PHY Interface block will then compare this locally calculated parity value with the state of the TxPPrty input pin. If these two values match, then the Transmit POS-PHY Interface block will presume that it has accepted PPP data from the Link Layer Processor in an un-erred manner. Conversely, if these two values do not match, then the Transmit POS-PHY Interface block will presume that it has accepted PPP data from the Link Layer Processor in an erred manner and it will transmit this PPP Packet as an Aborted Packet. 0 - Disables Parity Checking via the Transmit POS-PHY Interface. 1 - Enables Parity Checking via the Transmit POS-PHY Interface.

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	ODD Parity	R/W	**ODD Parity** This READ/WRITE bit-field permits the user to configure the Transmit POS-PHY Interface block to compute and verify either the EVEN or ODD parity of all bytes or 16-bit words that are accepted via the Transmit POS-PHY Interface, as described below. 0 - Configures the Transmit POS-PHY Interface block to verify EVEN Parity. 1 - Configures the Transmit POS-PHY Interface block to verify ODD Parity. ***NOTE:*** *This bit-field is only active if Bit 6 (Parity Check Enable) within this register is set to "1".*
4 - 0	Transmit POS-PHY Addr[4:0]	R/W	**Transmit POS-PHY Interface - Port Address:** These five READ/WRITE bit-fields permit the user to assign a Transmit POS-PHY Port Address to the Transmit POS-PHY Interface block. ***NOTE:*** *The Saturn POS-PHY Level 2 and 3 specifications permit the user to assign a Transmit POS-PHY Port Address of any five-bit value other than 0x1F (the NULL Address).*

DS3/E3 FRAMER AND PLCP PROCESSOR BLOCK REGISTERS

DS/E3 FRAMER BLOCK REGISTERS

The register map for the DS3/E3 Framer Block is presented in the Table below. Additionally, a detailed description of each of the ?DS3/E3 Framer? block registers is presented below

Framer Operating Mode Register (Address = 0x1100)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framer Local Loop Back	IsDS3	Interna lLOS Enable	RESET	Direct Map ATM	Frame For-mat	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Framer Local Loop Back	R/W	**Framer Block Local Loop-back Mode:** This READ/WRITE bit field configures the XRT79L71 to operate in the Framer Local Loop-back Mode. If the XRT79L71 has been configured to operate in the Framer Local Loop-back Mode, then the signal that is generated by the Transmit DS3/E3 Framer block will be internally looped back into the receive input of the Receive DS3/E3 Framer block. ***NOTE:*** *Whenever the XRT79L71 has been configured into the Framer Local Loop-back Mode, then the Transmit DS3/E3 LIU and Receive DS3/E3 LIU Blocks will NOT be operating in the Signal Path.* 0 - Configures the XRT79L71 to operate in the Normal Operating (e.g., Non-Framer Local Loop-back) Mode 1 - Configures the XRT79L71 to operate in the Framer Local Loop-back Mode
6	IsDS3	R/W	**Is DS3 Mode:** This READ/WRITE bit-field, along with Bit 2 (Frame Format), permits the user to configure both the Transmit and Receive DS3/E3 Framer blocks to operate in the appropriate framing for-mat. The relationship between the state of this bit-field, Bit 2 and the resulting framing format is presented below. **Bit 6 (IsDS3) / Bit 2 (Frame Format) / Framing Format** 0 / 0 / E3, ITU-T G.751 0 / 1 / E3, ITU-T G.832 1 / 0 / DS3, C-bit Parity 1 / 1 / DS3, M13 ***NOTE:*** *These bit settings also configure the Transmit DS3/E3 LIU and Receive DS3/E3 LIU Blocks into either the DS3 or E3 Modes.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	Internal LOS Enable	R/W	**Internal LOS Enable:** This READ/WRITE bit-field permits the user to enable or disable the Internal LOS Detector, within the Receive DS3/E3 Framer block. If the user disables the Internal LOS Detector then the Receive Section of the XRT79L71 will only declare the LOS defect condition, whenever the Receive DS3/E3 LIU block declares the LOS defect condition. 0 - Internal LOS Detector is disabled. 1 - Internal LOS Detector is enabled.
4	RESET	R/W	Software RESET Input: A "0" to "1" transition in this bit-field commands a Software RESET to the XRT79L71. Once the user executes a Software reset to the frame, all of the internal state machines will be reset and the Receive DS3/E3 Framer block will execute a Reframe operation. ***NOTE:*** *For a Software Reset, the contents of the Command Register will not be reset to their default values.*
3	Direct Map ATM	R/W	**Direct Map ATM:** This READ/WRITE bit-field permits the user to configure the XRT79L71 to operate in either the Direct Map ATM mode or in the PLCP Mode. If the user configures the XRT79L71 to operate in the Direct Map ATM Mode, then both the Transmit PLCP Processor and the Receive PLCP Processor blocks will be bypassed and will not process any ATM cell traffic. In this case, ATM cells will be DIRECTIY mapped into the payload bits within each outbound DS3 or E3 frame, without first being mapped into PLCP frames. If the user configures the XRT79L71 to operate in the Direct Map ATM Mode, then both the Transmit PLCP Processor and Receive PLCP Processor blocks will be enabled and will be processing ATM cell traffic. 0 - Configures the XRT79L71 to operate in the PLCP Mode. 1 - Configures the XRT79L71 to operate in the Direct Map ATM Mode. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the ATM UNI Mode.*

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>2</td><td>Frame Format</td><td>R/W</td><td>Frame Format:
This READ/WRITE bit-field, along with Bit 6 (IsDS3), permits the user to configure the both the Receive DS3/E3 Framer and the Transmit DS3/E3 Framer blocks to operate in the appropriate framing format. The relationship between the state of this bit-field, Bit 2 and the resulting framing format is presented below.
<table>
<tr><th>Bit 6 (IsDS3)</th><th>Bit 2 (Frame Format)</th><th>Framing Format</th></tr>
<tr><td>0</td><td>0</td><td>E3, ITU-T G.751</td></tr>
<tr><td>0</td><td>1</td><td>E3, ITU-T G.832</td></tr>
<tr><td>1</td><td>0</td><td>DS3, C-bit Parity</td></tr>
<tr><td>1</td><td>1</td><td>DS3, M13</td></tr>
</table>
NOTE: These bit settings also configure the Transmit DS3/E3 LIU and Receive DS3/E3 LIU Blocks into either the DS3 or E3 Modes.</td></tr>
<tr><td>1 - 0</td><td>TimRefSel[1:0]</td><td>R/W</td><td>Time Reference Select:
These two READ/WRITE bit-fields permit the user to define both the timing source and the framing-alignment source for the Transmit DS3/E3 Framer block, as presented below.
<table>
<tr><th>TimRefSel[1:0]</th><th>Timing Reference</th><th>Framing Reference</th></tr>
<tr><td>00</td><td>Loop-Timing (Transmit DS3/E3 Framer block timing is taken from the Receive DS3/E3 LIU block)</td><td>The Transmit DS3/E3 Framer block will initiate the generation of a given "outbound" DS3/E3 frame, based upon a clock signal that is asynchronous with respect to any externally supplied signal</td></tr>
<tr><td>01</td><td>The TxInClk input pin will function as the Timing Source for the Transmit DS3/E3 Framer block The Transmit DS3/E3 Framer block will generate a new DS3/E3 frame upon the rising edge of the TxFrameRef Input</td><td>The Transmit DS3/E3 Framer block will generate a new DS3/E3 frame upon the rising edge of the TxFrameRef Input</td></tr>
<tr><td>10</td><td>The TxInClk input pin will function as the Timing Source for the Transmit DS3/E3 Framer block</td><td>Asynchronous</td></tr>
<tr><td>11</td><td>The TxInClk input pin will function as the Timing Source for the Transmit DS3/E3 Framer block</td><td>Asynchronous</td></tr>
</table></td></tr>
</table>

I/O Control Register (Address = 0x1101)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	Reserved				Reframe
R/W	R/O	R/W	R/O	R/O	R/O	R/O	R/W
1	0	1	0	0	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Disable TxLOC	R/W	**Disable Transmit Loss of Clock Feature:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit Loss of Clock feature. If this feature is enabled, then the DS3/E3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a Loss of Transmit (or Frame Generator) Clock Event were to occur. The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3/E3 Framer block) from hanging in the event of a Loss of Clock event. 0 - Enables the Transmit Loss of Clock feature. 1 - Disables the Transmit Loss of Clock feature.
6	LOC	R/O	**Loss of Clock Indicator:** This READ-ONLY bit-field indicates that the Channel has experiences a Loss of Clock event.
5	Disable RxLOC	R/W	**Disable Receive Loss of Clock Feature:** This READ/WRITE bit-field permits the user to either enable or disable the Receive Loss of Clock feature. If this feature is enabled, then the DS3/E3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a Loss of Receiver Clock Event were to occur. The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3/E3 Framer block) from hanging in the event of a Loss of Clock event. 0 - Enables the Receive Loss of Clock feature. 1 - Disables the Receive Loss of Clock feature.
4 - 1	Reserved		the User must make sure that each of these bits are set to "0" in order to ensure proper operation.
0	Reframe	R/W	Receive DS3/E3 Framer Block - Reframe Command: A "0" to "1" transition, within this bit-field commands the Receive DS3/E3 Framer block to exit the Frame Maintenance Mode, and go back and enter the Frame Acquisition Mode ***NOTE:*** *The user should go back and set this bit-field to "0" following execution of the Reframe Command.*

Framer Block Interrupt Enable Register (Address = 0x1104)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive DS3/E3 Framer Block Interrupt Enable	Receive PLCP Processor Block Interrupt Enable	Unused				Transmit DS3/E3 Framer Block Interrupt Enable	One Second Interrupt
R/W	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive DS3/E3 Framer Block Interrupt Enable	R/W	**Receive DS3/E3 Framer Block Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the Receive DS3/E3 Framer block for Interrupt Generation. If the user enables the Receive DS3/E3 Framer block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the Source level, in order for these interrupts to be enabled. However, if the user disables the Receive DS3/E3 Framer block (for Interrupt Generation) at the Block Level, then ALL Receive DS3/E3 Framer block-related interrupts are disabled. 0 - The Receive DS3/E3 Framer block is Disabled for Interrupt Generation. 1 - The Receive DS3/E3 Framer block is enabled (at the Block level) for Interrupt Generation.
6	Receive PLCP Processor Block Interrupt Enable	R/W	**Receive PLCP Processor Block Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the Receive PLCP Processor block for Interrupt Generation. If the user enables the Receive PLCP Processor block (for Interrupt Generation) at the block level, the user will still need to enable the individual interrupts at the Source Level, as well, in order for these interrupts to be enabled. However, if the user disables the Receive PLCP Processor block (for Interrupt Generation) at the Block Level, then ALL Receive PLCP Processor block-related interrupts are disabled. 0 - The Receive PLCP Processor block is disabled for Interrupt Generation. 1 - The Receive PLCP Processor block is enabled for Interrupt Generation. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the ATM/PLCP Mode.*
5 - 2	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Transmit DS3/E3 Framer Block Interrupt Enable	R/W	**Transmit DS3/E3 Framer Block Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the Transmit DS3/E3 Framer block for Interrupt Generation. If the user enables the Transmit DS3/E3 Framer block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the Source level, in order for these interrupts to be enabled However, if the user disables the Transmit DS3/E3 Framer block (for Interrupt Generation) at the Block Level, then ALL Transmit DS3/E3 Framer block -related interrupts are disabled. 0 - Transmit DS3/E3 Framer block is Disabled for Interrupt Generation. 1 - Transmit DS3/E3 Framer block is Enabled (at the Block Level) for Interrupt Generation.
0	One Second Interrupt	R/W	**One Second Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the One-Second Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt at one second intervals. 0 - One Second Interrupt is disabled. 1 - One Second Interrupt is enabled.

Framer Block Interrupt Status Register (Address = 0x1105)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive DS3/E3 Framer Block Interrupt Status	Receive PLCP Processor Block Interrupt Status	Unused				Transmit DS3/E3 Framer Block Interrupt Status	One Second Interrupt
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive DS3/E3 Framer Block Interrupt Status	R/O	**Receive DS3/E3 Framer Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a Receive DS3/E3 Framer Block-related interrupt is requesting interrupt service. 0 - The Receive DS3/E3 Framer block is NOT requesting any interrupt service. 1 - The Receive DS3/E3 Framer block is requesting interrupt service.

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	Receive PLCP Processor Block Interrupt Status	R/O	**Receive PLCP Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a Receive PLCP Processor Block related interrupt is requesting interrupt service. 0 - The Receive PLCP Processor block is NOT requesting any interrupt service. 1 - The Receive PLCP Processor block is requesting interrupt service. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the ATM/PLCP Mode.*
6 - 2	Unused	R/O	
1	Transmit DS3/E3 Framer Block Interrupt Status	R/O	**Transmit DS3/E3 Framer Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a Transmit DS3/E3 Framer block -related interrupt is requesting interrupt service. 0 - The Transmit DS3/E3 Framer block is NOT requesting any interrupt service. 1 - The Transmit DS3/E3 Framer block is requesting interrupt service.
0	One Second Interrupt Status	RUR	**One Second Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not a One second Interrupt has occurred since the last read of this register. 0 - The One Second Interrupt has NOT occurred since the last read of this register. 1 - The One Second Interrupt has occurred since the last read of this register.

Test Register (Address = 0x110C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxOHSrc	R/W	**Transmit Overhead Bit Source:** This READ/WRITE bit-field permits the user to configure the Transmit DS3/E3 Framer block to accept and insert overhead bits/bytes which are input via the Transmit Payload Data Input Interface block, as indicated below .0 - No overhead bit insertion will occur. Overhead bits/bytes are internally generated by the Transmit DS3/E3 Framer block. 1 - Overhead bit insertion will occur. In this case, the overhead bits/byte data is accepted from the Transmit Payload Data Input Interface block. ***NOTE:*** *This register bit applies to all framing formats that are supported by the Transmit DS3/E3 Framer block.*
6 - 5	Unused	R/O	
4	RxPRBS Lock	R/O	**PRBS Lock Indicator:** This READ-ONLY bit-field indicates whether or not the PRBS Receiver (within the XRT79L71) has acquired PRBS Lock with the payload data of the incoming DS3 or E3 data stream. 0 - PRBS Receiver does not have PRBS Lock with the incoming data stream. 1 - PRBS Receiver does have PRBS Lock with the incoming data stream.
3	RxPRBS Enable	R/W	**Receive PRBS Enable:** This READ/WRITE bit-field permits the user to either enable or disable the PRBS Receiver within the Receive DS3/E3 Framer block. Once the user enables the PRBS Receiver, then it will proceed to attempt to acquire and maintain pattern (or PRBS Lock) within the payload bits, within the incoming DS3 or E3 data stream. 0 - Disables the PRBS Receiver. 1 - Enables the PRBS Receiver.
2	TxPRBS Enable	R/W	**Transmit PRBS Enable:** This READ/WRITE bit-field permits the user to either enable or disable the PRBS Generator within the Transmit DS3/E3 Framer block. Once the user enables the PRBS Generator block, then it will proceed to insert a PRBS pattern into the payload bits, within the outbound DS3 or E3 data stream. 0 - Disables the PRBS Generator. 1 - Enables the PRBS Generator.
1 - 0	Unused	R/O	

Payload HDLC Control Register, Address = 0x110D

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framer By-Pass	HDLC Controller Enable	HDLC CRC-32	Unused	HDLC Loop-back	Unused		
R/W	R/W	R/W	R/O	R/W	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Framer By-Pass	R/W	
6	HDLC Controller Enable	R/W	**HDLC Controller Enable:** This READ/WRITE bit-field configures the XRT79L71 to operate in either the High-Speed HDLC Controller Mode, or in the Clear-Channel Framer Mode. If the user configures the XRT79L71 to operate in the High-Speed HDLC Controller Mode, then all of the following will be true **In the Transmit Direction** Some of the Transmit Payload Data Input Interface pins will change function, and will present a byte-wide Transmit High-Speed HDLC Controller input interface to the System-Side Terminal Equipment. This Transmit High-Speed HDLC Controller input interface will also present the System-Side Terminal Equipment with a demand output clock signal (which is approximately one-eight of the either the E3 or DS3 rates, depending which rate is being used). This Transmit High-Speed HDLC Controller Input Interface will accept data (from the System-Side Terminal Equipment) in a byte-wide manner. As the Transmit High-Speed HDLC Controller Input Interface accepts this data, it will route this data to the Transmit High-Speed HDLC Controller block where it will encapsulate this data into a variable-length HDLC frame. The Transmit High-Speed HDLC Controller block will also take on the responsibility of zero-stuffing the payload data, within each of these outbound HDLC frames. Finally, the Transmit High-Speed HDLC Controller circuitry will optionally append either a CRC-32 or CRC-16 value to the back-end of any Outbound HDLC frame. Anytime the System-Side Terminal Equipment is NOT providing any data to the Transmit High-Speed HDLC Controller Input Interface, then the Transmit High-Speed HDLC Controller block will generate a string of repeating Flag Sequence octets (0x7E), in order to (1) denote the boundaries of all outbound HDLC frames and (2) to indicate that no HDLC frames are currently being transported across the DS3/E3 transport medium. This composite Outbound data-stream (consisting of HDLC frames and Flag Sequence octets) will be routed to the Transmit DS3/E3 Framer block. In this case, the Transmit DS3/E3 Framer block will insert this composite Outbound data-stream into the payload bits within each outbound DS3 or E3 data-stream.

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	HDLC Controller Enable Continued	R/W	**In the Receive Direction** In the Receive Direction, the Receive High-Speed HDLC Controller block will accept the payload data (within the incoming DS3/E3 data-stream) from the Receive DS3/E3 Framer block. As the Receive High-Speed HDLC Controller block receives this incoming data, it will perform the following functions. • It will flag any occurrence of the Flag Sequence octet, within the incoming data-stream.. • It will locate the boundaries of the incoming HDLC frames.· It will perform zero-unstuffing on the payload data (within each incoming HDLC frame). • It will compute and verify either the CRC-16 or CRC-32 value (that is appended at the back-end of the outbound HDLC Frame). • It will output this incoming HDLC data to the System-Side Terminal Equipment via a byte-wide output interface. 0 - Configures the XRT79L71 to operate in the Clear-Channel Framer Mode (e.g., disables the Transmit and Receive High-Speed HDLC Controller blocks). 1- Configures the XRT79L71 to operate in the High-Speed HDLC Controller (e.g., enables the Transmit and Receive High-Speed HDLC Controller blocks).
5	HDLC CRC-32	R/W	**HDLC CRC-32:** This READ/WRITE bit-field permits the user to configure the Transmit and Receive High-Speed HDLC Controller blocks to handle either CRC-16 or CRC-32 values (at the back-end of each HDLC frame), as described below. **If configured to handle CRC-16 values** If the XRT79L71 is configured to handle CRC-16 Values then all of the following is true. • The Transmit High-Speed HDLC Controller block will compute and append a CRC-16 (2-byte) value to the back-end of each Outbound HDLC frame. • The Receive High-Speed HDLC Controller block will compute and verify the CRC-16 value (which has been appended to the back-end) of each incoming HDLC frame. **If configured to handle CRC-32 values:** If the XRT79L71 is configured to handle CRC-32 Values then all of the following is true. • The Transmit High-Speed HDLC Controller block will compute and append a CRC-32 (4-byte) value to the back-end of each Outbound HDLC frame. • The Receive High-Speed HDLC Controller block will compute and verify the CRC-32 value (which has been appended to the back-end) of each incoming HDLC frame. 0 - Configures the XRT79L71 to handle CRC-16 values. 1 - Configures the XRT79L71 to handle CRC-32 values. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	Unused	R/O	
3	HDLC Loop-back	R/W	
2 - 0	Unused	R/O	

RECEIVE DS3 RELATED REGISTERS

Receive DS3 Configuration and Status Register (Address = 0x1110)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AIS Defect Condition Declared	LOS Defect Condition Declared	DS3 Idle Condition Declared	OOF Defect Condition Declared	Unused	Framing with Valid P-Bits	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	1	0	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	AIS Defect Condition Declared	R/O	**AIS Defect Condition Declared Indicator:** This READ-ONLY bit-field indicates whether or not the Receive DS3/E3 Framer block is currently declaring the AIS defect condition within the incoming DS3 data-stream, as described below. 0 - The Receive DS3/E3 Framer block is NOT currently declaring the AIS defect condition. 1 - The Receive DS3/E3 Framer block is currently declaring the AIS defect condition.
6	LOS Defect Condition Declared	R/O	**LOS Defect Condition Declared Indicator:** This READ-ONLY bit-field indicates whether or not the Receive Section of the XRT79L71 (e.g., either the Receive DS3/E3 LIU or the Receive DS3/E3 Framer block) is currently detecting the LOS defect condition, as described below. 0 - Indicates that the Receive Section of the XRT79L71 is NOT currently declaring the LOS defect condition. 1 - Indicates that the Receive Section of the XRT79L71 is currently declaring the LOS defect condition.
5	DS3 Idle Condition Declared	R/O	**DS3 Idle Condition Declared Indicator:** This READ-ONLY bit-field indicates whether or not the Receive DS3/E3 Framer block is currently detecting the DS3 Idle pattern, in its incoming path, as described below. 0 - Indicates that the Receive DS3/E3 Framer block is NOT currently declaring the DS3 Idle Condition. 1 - Indicates that the Receive DS3/E3 Framer block is currently declaring the DS3 Idle Condition. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3 Mode.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	OOF Defect Condition Declared	R/O	**OOF (Out of Frame) Defect Condition Declared Indicator:** This READ-ONLY bit-field indicates whether or not the Receive DS3/E3 Framer block is currently declaring the OOF (Out of Frame) defect condition. 0 - Indicates that the Receive DS3/E3 Framer block is NOT currently declaring the OOF defect condition. 1 - Indicates that the Receive DS3/E3 Framer block is currently declaring the OOF defect condition.
3	Unused	R/O	
2	Framing with Valid P Bits	R/W	**Framing with Valid P-Bit Select:** This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Frame Acquisition/Maintenance criteria that the Receive DS3/E3 Framer block will use to (1) acquire and declare Frame Synchronization, and (2) to declare the OOF Defect condition .0 - Normal Framing Acquisition/Maintenance Criteria (without P-bit Checking) In this mode, the Receive DS3/E3 Framer block will declare the In-frame state, one it has successfully completed both the F-Bit Search and the M-Bit Search states 1 - Framing Acquisition/Maintenance with P-bit CheckingIn this mode, the Receive DS3/E3 Framer block will (in addition to passing through the F-Bit Search and M-Bit Search states) also verify valid P-bits, prior to declaring the In-Frame state. ***NOTE:*** *This bit-field is ignored if the XRT79L71 has been configured to operate in the E3 Mode.*
1	F-Sync Algo	R/W	**F-Bit Search State Criteria Select:** This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Out of Frame (OOF) Defect Declaration criteria. 0 - The OOF defect condition will be declared when 6 out of 15 F-bits are erred. 1 - The OOF defect condition will be declared when 3 out of 15 F-bits are erred. ***NOTE:*** *This bit-field is ignored if the XRT79L71 has been configured to operate in the E3 Mode.*
0	M-Sync Algo	R/W	**M-Bit Search State Criteria Select:** This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Out of Frame (OOF) Defect Declaration criteria. 0 - M-bit Errors do not result in the Receive DS3/E3 Framer block declaring the OOF defect condition. 1 - The OOF defect condition will be declared when all M-bits, within 3 out of 4 consecutive DS3 frames are in error. ***NOTE:*** *This bit-field is ignored if the XRT79L71 has been configured to operate in the E3 Mode.*

Receive DS3 Status Register (Address = 0x1111)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			FERF/RDI Defect Declared	RxAIC	RxFEBE[2:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	FERF/RDI Defect Declared	R/O	**FERF/RDI (Far-End Receive Failure/Remote Defect Indicator) Defect Declared Indicator:** This READ-ONLY bit-field indicates whether or not the Receive DS3/E3 Framer block is currently declaring the FERF/RDI defect condition, as described below. 0 - The Receive DS3/E3 Framer block is NOT currently declaring the FERF/RDI defect condition. 1 - The Receive DS3/E3 Framer block is currently declaring the FERF/RDI defect condition. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3 Mode.*
3	RxAIC	R/O	**Receive AIC State:** This READ-ONLY bit-field indicates the current state of the AIC bit-field within the incoming DS3 data-stream. 0 - Indicates that the Receive DS3/E3 Framer block has received at least 2 consecutive M-frames that have the AIC bit-field set to "0". 1 - Indicates that the Receive DS3/E3 Framer block has received at least 63 consecutive M-frames that have the AIC bit-field set to "1". ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3 Mode.*
2 - 0	RxFEBE[2:0]	R/O	**Receive FEBE (Far-End Block Error) Value:** These READ-ONLY bit-fields reflect the FEBE value within the most recently received DS3 frame. RxFEBE[2:0] = [1, 1, 1] indicates a normal condition. All other values for RxFEBE[2:0] indicates an erred condition at the remote terminal equipment. ***NOTE:*** *These bit-fields are only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*

Receive DS3 Interrupt Enable Register (Address = 0x1112)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP Bit Error Interrupt Enable	Change of LOS Defect Condition Interrupt Enable	Change of AIS Defect Condition Interrupt Enable	Change of Idle Condition Interrupt Enable	Change of FERF Defect Condition Interrupt Enable	Change of AIC State Interrupt Enable	Change of OOF Defect Condition Interrupt Enable	Detection of P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of CP Bit Error Interrupt Enable	R/W	**Detection of CP-Bit Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of CP-Bit Error Interrupt, within the Channel. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt anytime it detects CP bit errors. 0 - Disables the Detection of CP Bit Error Interrupt. 1 - Enables the Detection of CP-Bit Error Interrupt. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing Format.*
6	Change of LOS Defect Condition Interrupt Enable	R/W	**Change in LOS Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in LOS (Loss of Signal) Defect Condition Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt in response to either of the following conditions.· • The instant that the Receive DS3/E3 Framer block declares the LOS defect condition. • The instant that the Receive DS3/E3 Framer block clears the LOS defect condition. 0 - Disables the Change in LOS Defect Condition Interrupt. 1 - Enables the Change in LOS Defect Condition Interrupt.
5	Change of AIS Defect Condition Interrupt Enable	R/W	**Change in AIS Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in AIS (Alarm Indication Signal) Defect Condition Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt in response to either of the following conditions.· • The instant that the Receive DS3/E3 Framer block declares the AIS defect condition. • The instant that the Receive DS3/E3 Framer block clears the AIS defect condition. 0 - Disables the Change in AIS Defect Condition Interrupt. 1 - Enables the Change in AIS Defect Condition Interrupt.

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	Change of DS3 Idle Condition Interrupt Enable	R/W	**Change in DS3 Idle Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in DS3 Idle Condition Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt in response to either of the following conditions. • The instant that the Receive DS3/E3 Framer block declares the DS3 Idle condition. • The instant that the Receive DS3/E3 Framer block clears the DS3 Idle condition .0 - Disables the Change in DS3 Idle Condition Interrupt. 1 - Enables the Change in DS3 Idle Condition Interrupt.
3	Change of FERF/RDI Defect Condition Interrupt Enable	R/W	**Change in FERF/RDI Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in FERF/RDI (Far-End Receive Failure/ Remote Defect Indicator) Defect Condition Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt in response to either of the following conditions. • The instant that the Receive DS3/E3 Framer block declares the FERF/RDI defect condition.· • The instant that the Receive DS3/E3 Framer block clears the FERF/RDI defect condition. 0 - Disables the Change in FERF/RDI Defect Condition Interrupt. 1 - Enables the Change in FERF/RDI Defect Condition Interrupt.
2	Change of AIC State Interrupt Enable	R/W	**Change in AIC State Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in AIC State Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt in response to it detecting a change in the AIC bit-field, within the incoming DS3 data stream. 0 - Disables the Change in AIC State Interrupt 1 - Enables the Change in AIC State Interrupt
1	Change of OOF Defect Condition Interrupt Enable	R/W	**Change in OOF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in OOF (Out of Frame) Defect Condition Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt in response to either of the following conditions.· • The instant that the Receive DS3/E3 Framer block declares the OOF defect condition. • The instant that the Receive DS3/E3 Framer block clears the OOF defect condition. 0 - Disables the Change in OOF Defect Condition Interrupt. 1 - Enables the Change in OOF Defect Condition Interrupt.

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Detection of P-Bit Error Interrupt Enable	R/W	**Detection of P-Bit Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of CP-Bit Error Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt anytime it detects CP bit errors. 0 - Disables the Detection of CP Bit Error Interrupt. 1 - Enables the Detection of CP-Bit Error Interrupt.

Receive DS3 Interrupt Status Register (Address = 0x1113)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP Bit Error Interrupt Status	Change of LOS Defect Condition Interrupt Status	Change of AIS Defect Condition Interrupt Status	Change of DS3 Idle Condition Interrupt Status	Change of FERF/RDI Defect Condition Interrupt Status	Change of AIC State Interrupt Status	Change of OOF Defect Condition Interrupt Status	Detection of P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of CP Bit Error Interrupt Status	RUR	**Detection of CP-Bit Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Detection of CP-Bit Error Interrupt has occurred since the last read of this register as depicted below. 0 - The Detection of CP-Bit Error Interrupt has not occurred since the last read of this register. 1 - The Detection of CP-Bit Error Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing Format.*
6	Change of LOS Defect Condition Interrupt Status	RUR	**Change in LOS Defect Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the Change in LOS Defect Condition Interrupt has occurred since the last read of this register as debicted below. 0 - The Change in LOS Defect Condition Interrupt has not occurred since the last read of this register. 1 - The Change in LOS Defect Condition Interrupt has occurred since the last read of this register.

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	Change of AIS Defect Condition Interrupt Status	RUR	**Change in AIS Defect Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the Change in AIS Defect Condition Interrupt has occurred since the last read of this register as depicted below. 0 - The Change in AIS Defect Condition Interrupt has not occurred since the last read of this register. 1 - The Change in AIS Defect Condition Interrupt has occurred since the last read of this register.
4	Change of DS3 Idle Condition Interrupt Status	RUR	**Change in DS3 Idle Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the Change in DS3 Idle Condition interrupt has occurred since the last read of this register. 0 - The Change in DS3 Idle Condition Interrupt has not occurred since the last read of this register. 1 - The Change in DS3 Idle Condition Interrupt has occurred since the last read of this register.
3	Change of FERF/RDI Defect Condition Interrupt Status	RUR	**Change in FERF/RDI Defect Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the Change in FERF/RDI Defect Condition Interrupt has occurred since the last read of this register. 0 - The Change in FERF/RDI Defect Condition Interrupt has not occurred since the last read of this register. 1 - The Change in FERF/RDI Defect Condition Interrupt has occurred since the last read of this register.
2	Change of AIC State Interrupt Status	RUR	**Change in AIC State Interrupt Status:** This RESET-upon-READ register bit indicates whether or not the Change in AIC State interrupt has occurred since the last read of this register. 0 - The Change in AIC State Interrupt has not occurred since the last read of this register. 1 - The Change in AIC State Interrupt has occurred since the last read of this register.
1	Change of OOF Defect Condition Interrupt Status	RUR	**Change in OOF Defect Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the Change in OOF Defect Condition Interrupt has occurred since the last read of this register. 0 - The Change in OOF Defect Condition Interrupt has not occurred since the last read of this register. 1 - The Change in OOF Defect Condition Interrupt has occurred since the last read of this register.
0	Detection of P-Bit Error Interrupt Status	RUR	**Detection of P-Bit Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Detection of CP-Bit Error Interrupt has occurred since the last read of this register. 0 - The Detection of CP-Bit Error Interrupt has not occurred since the last read of this register. 1 - The Detection of CP-Bit Error Interrupt has occurred since the last read of this register.

Receive DS3 Sync Detect Register (Address = 0x1114)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					P-Bit Correct	F Algorithm	One and Only
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 3	Reserved	R/O	
2	P-Bit Correct	R/W	**P-Bit Correct:** This READ/WRITE bit-field permits the user to enable or disable the P-Bit Correct feature within the Receive DS3/E3 Framer block. If the user enables this feature, then the Receive DS3/E3 Framer block will automatically invert the state of any P-bits, whenever it detects P-bit errors within the incoming DS3 data-stream. 0 - Disables the P-Bit Correct feature. 1 - Enables the P-Bit Correct feature
1	F Algorithm	R/W	**F-Bit Search Algorithm Select:** This READ/WRITE bit-field permits the user to select the F-bit acquisition criteria that the Receive DS3/E3 Framer block will use whenever it is operating in the F-Bit Search state. 0 - Configures the Receive DS3/E3 Framer block to move on to the M-Bit Search state whenever it has properly located 10 consecutive F-bits within the incoming DS3 data-stream. 1 -Configures the DS3/E3 Framer block to move on to the M-Bit Search state whenever it has properly located 16 consecutive F-bits within the incoming DS3 data-stream. ***NOTE:*** *This bit-field is only active if the user has configured the XRT79L71 to operate in the DS3 Mode.*
0	One and Only	R/W	**F-Bit Search/Mimic-Handling Algorithm Select:** This READ/WRITE bit-field permits the user to select the F-bit acquisition criteria that the Receive DS3/E3 Framer block will use whenever it is operating in the F-Bit Search state. 0 - Configures the Receive DS3/E3 Framer block to move on to the M-Bit Search state whenever it has properly located 10 (or 16) consecutive F-bits (as configured in Bit 1 of this register). 1 - Configures the Receive DS3/E3 Framer block to move on to the M-Bit Search state, when (1) it has properly located 10 (or 16) consecutive F-bits and (2) when it has located and identified only one viable F-Bit Alignment candidate. ***NOTE:*** *If this bit is set to "1", then the Receive DS3/E3 Framer block will NOT transition into the M-Bit Search state, as long as at least two viable candidate set of bits appear to function as the F-bits.*

Receive DS3 FEAC Register (Address = 0x1116)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxFEAC_Code[5:0]						Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	1	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6 - 1	RxFEAC_Code[5:0]	R/O	**Receive FEAC Code Word:** These READ-ONLY bit-fields contain the value of the most recently validated FEAC Code word. ***NOTE:*** *These bit-fields are only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*
0	Unused	R/O	

Receive DS3 FEAC Interrupt Enable/Status Register (Address = 0x1117)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
R/O	R/O	R/O	R/O	R/W	RUR	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	Please set to "0" (the default value) for normal operation.
4	FEAC Valid	R/O	**FEAC Message Validation Indicator:** This READ-ONLY bit-field indicates that the FEAC Code (which resides within the RxDS3 FEAC Register) has been validated by the Receive FEAC Controller block. The Receive FEAC Controller block will validate a FEAC codeword if it has received this codeword in 8 out of the last 10 FEAC Messages. Polled systems can monitor this bit-field, when checking for a newly validated FEAC codeword. 0 - FEAC Message is not (or no longer) validated. 1 - FEAC Message has been validated. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	RxFEACRemove Interrupt Enable	R/W	**FEAC Message Remove Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive FEAC Remove Interrupt. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt anytime the most recently validated FEAC Message has been removed. The Receive FEAC Controller will remove a validated FEAC codeword, if it has received a different codeword in 3 out of the last 10 FEAC Messages .0 - Receive FEAC Remove Interrupt is disabled. 1 - Receive FEAC Remove Interrupt is enabled. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*
2	RxFEAC Remove Interrupt Status	RUR	**FEAC Message Remove Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the FEAC Message Remove Interrupt has occurred since the last read of this register. 0 - FEAC Message Remove Interrupt has NOT occurred since the last read of this register. 1 - FEAC Message Remove Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*
1	RxFEAC Valid Interrupt Enable	R/W	**FEAC Message Validation Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the FEAC Message Validation Interrupt. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt anytime a new FEAC Codeword has been validated by the Receive FEAC Controller block. 0 - FEAC Message Validation Interrupt is NOT enabled. 1 - FEAC Message Validation Interrupt is enabled. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*
0	RxFEAC Valid Interrupt Status	RUR	**FEAC Message Validation Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the FEAC Message Validation Interrupt has occurred since the last read of this register. 0 - FEAC Message Validation Interrupt has not occurred since the last read of this register. 1 - FEAC Message Validation Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*

Receive DS3 LAPD Control Register (Address = 0x1118)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLAPD Any	Unused				Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive APD Interrupt Status
R/W	R/O	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLAPD Any	R/W	**Receive LAPD - Any kind:** This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller block to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes. 0 - Does not invoke this Any Kind of HDLC Message feature. In this case, the Receive LAPD Controller block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI. 1 - Invokes this Any Kind of HDLC Message feature. In this case, the Receive LAPD Controller block will be able to receive HDLC Messages that contain any header byte values. ***NOTE:*** *The user can determine the size (or byte-count) of the most recently received LAPD/PMDL Message, by reading the contents of the RxLAPD Byte Count Register (Address = 0x1184)*
6 - 3	Unused	R/O	
2	Receive LAPD Enable	R/W	**Receive LAPD Controller Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Controller block within the XRT79L71. If the user enables the Receive LAPD Controller block, then it will immediately begin extracting out and monitoring the data (being carried via the DL bits) within the incoming DS3 data stream. 0 - Enables the Receive LAPD Controller block. 1 - Disables the Receive LAPD Controller block. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Receive LAPD Interrupt Enable	R/W	**Receive LAPD Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Message Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the Receive LAPD Controller block receives a new PMDL Message. 0 - Disables the Receive LAPD Message Interrupt. 1 - Enables the Receive LAPD Message Interrupt. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*
0	Receive LAPD Interrupt Status	RUR	**Receive LAPD Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive LAPD Message Interrupt has occurred since the last read of this register. 0 - Receive LAPD Message Interrupt has NOT occurred since the last read of this register. 1 - Receive LAPD Message Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*

Receive DS3 LAPD Status Register (Address = 0x1119)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxABORT	RxLAPDType[1:0]		RxCRType	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>RxABORT</td><td>R/O</td><td>Receive ABORT Sequence Indicator:
This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block has received an ABORT sequence (e.g., a string of seven consecutive "0s"), as described below.
0 - Indicates that the Receive LAPD Controller block has NOT received an ABORT sequence.
1 - Indicates that the Receive LAPD Controller block has received an ABORT sequence.
NOTES:
1. Once the Receive LAPD Controller block receives an ABORT sequence, it will set this bit-field "High", until it receives another LAPD Message.
2. This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.</td></tr>
<tr><td>5 - 4</td><td>RxLAPDType[1:0]</td><td>R/O</td><td>Receive LAPD Message Type Indicator:
These two READ-ONLY bits indicate the type of LAPD Message that is residing within the Receive LAPD Message buffer. The relationship between the content of these two bit-fields and the corresponding message type is presented below.
<table><tr><th colspan="2">RxLAPDType[1:0]</th><th>Message Type</th></tr><tr><td>0</td><td>0</td><td>CL Path Identification</td></tr><tr><td>0</td><td>1</td><td>Idle Signal Identification</td></tr><tr><td>1</td><td>0</td><td>Test Signal Identification</td></tr><tr><td>1</td><td>1</td><td>ITU-T Path Identification</td></tr></table>NOTE: These bit-fields are only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.</td></tr>
<tr><td>3</td><td>RxCR Type</td><td>R/O</td><td>Received C/R Value:
This READ-ONLY bit-field indicates the value of the C/R bit (within one of the header bytes) of the most recently received LAPD Message.
NOTE: This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.</td></tr>
<tr><td>2</td><td>RxFCS Error</td><td>R/O</td><td>Receive Frame Check Sequence (FCS) Error Indicator:
This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error.
0 - The most recently received LAPD Message frame does not contain an FCS error.
1 - The most recently received LAPD Message frame does contain an FCS error.
NOTE: This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.</td></tr>
</table>

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	End of Message	R/O	**End of Message Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block has received a complete LAPD Message, as described below. 0 - Receive LAPD Controller block is currently receiving a LAPD Message, but has not received the complete message. 1 - Receive LAPD Controller block has received a complete LAPD Message. ***NOTES:*** *1. Once the Receive LAPD Controller block sets this bit-field "High", this bit-field will remain high, until the Receive LAPD Controller block begins to receive a new LAPD Message.* *2. This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*
0	Flag Present	R/O	**Receive Flag Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel), as described below .0 - Indicates that the Receive LAPD Controller block is NOT currently receiving the Flag Sequence octet. 1 - Indicates that the Receive LAPD Controller block is currently receiving the Flag Sequence octet. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*

Receive DS3 Pattern Register (Address = 0x112F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS3 AIS-Unframed "All-Ones"	DS3 AIS Non Stuck Stuff	Unused	Receive LOS Pattern	Receive DS3 Idle Pattern[3:0]			
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	DS3 AIS - Unframed "All-Ones"	R/W	**DS3 AIS - Unframed "All-Ones" - AIS Pattern:** This READ/WRITE bit-field, (along with the Non-Stuck-Stuff bit) permits the user specify the AIS Declaration criteria for the Receive DS3 Framer block, as described below. 0 - Configures the Receive DS3 Framer block to declare the AIS defect condition, when receiving a DS3 signal carrying a framed 1010.. pattern. 1 - Configures the Receive DS3 Framer block to declare an AIS condition, when receiving either an unframed, "All-Ones" pattern or a framed 1010.. pattern.
6	DS3 AIS -Non-Stuck Stuff	R/W	**DS3 AIS -Non-Stuck-Stuff Option - AIS Pattern:** This READ/WRITE bit-field (along with the Unframed "All-Ones" - AIS Pattern bit-field) permits the user to define the AIS Defect Declaration criteria for the Receive DS3 Framer block, as described below. 0 - Configures the Receive DS3 Framer block to require that all C bits are set to "0" before it will declare the AIS defect condition. 1 - Configures the Receive DS3 Framer block to NOT require that all C bits are set to "0" before it will declare the AIS defect condition. In this mode, no attention will be paid to the state of the "C" bits within the incoming DS3 data-stream.
5	Unused	R/O	
4	Receive LOS Pattern	R/W	**Receive LOS Pattern:** This READ/WRITE bit-field permits the user to define the LOS Defect Declaration criteria for the Receive DS3 Framer block, as described below. 0 - Configures the Receive DS3 Framer block to declare the LOS defect condition if it receives a string of a specific length of consecutive zeros. 1 - Configures the Receive DS3 Framer block to declare the LOS defect condition if it receives a string (of a specific length) of consecutive ones. ***NOTE:*** *This bit-field is only enabled if the "Internal LOS Enable" feature has been enabled within the Receive DS3/E3 Framer block.*
3 - 0	Receive DS3 Idle Pattern[3:0]	R/W	**Receive DS3 Idle Pattern:** These READ/WRITE bit-fields permit the user to specify the pattern in which the Receive DS3 Framer block will recognize as the DS3 Idle Pattern. ***NOTE:*** *The Bellcore GR-499-CORE specified value for the Idle Pattern is a framed repeating "1, 1, 0, 0…" pattern. Therefore, if the user wishes to configure the Receive DS3 Framer block to declare an Idle Pattern when it receives this pattern, then the user write the value [1100] into these bit-fields.*

RECEIVE E3, ITU-T G.751 RELATED REGISTERS

Receive E3 Configuration and Status Register # 1 - G.751 (Address = 0x1110)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			RxFERF Algo	Unused			RxBIP-4 Enable
R/O	R/O	R/O	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	RxFERF Algo	R/W	**Receive FERF Algorithm Select:** This READ/WRITE bit-field permits the user to select the FERF Defect Declaration and Clearance criteria that will be used by the Receive E3 Framer block. 0 - The FERF/RDI defect is declared if the "A" bit-field (within the incoming E3 data-stream) is set to "1" for 3 consecutive frames. The FERF/RDI defect is cleared if the "A" bit-field is set to "0" for 3 consecutive frames. 1 - The FERF/RDI defect is declared if the "A" bit-field is set to "1" for 5 consecutive frames. The FERF/RDI defect is cleared if the "A" bit-field is set to "0" for 5 consecutive frames. ***NOTE:*** *This bit-field is ignored if Bit 0 (RxBIP-4 Enable) is set to "1".*
3 - 1	Unused	R/O	
0	RxBIP4 Enable	R/W	**Enable BIP-4 Verification:** This READ/WRITE bit-field permits the user to configure the Receive E3 Framer block to verify the BIP-4 value, within the incoming E3 data-stream. If the user implements this configuration selection, then all of the following will be true. **a.** The Receive E3 Framer block will detect and flag occurrences of BIP-4 errors within the incoming E3 data-stream. **b.** The Receive E3 Framer block will never declare the FERF/RDI indicator. **c.** The Receive E3 Framer block will interpret the "A" bit, being set "High" to indicate a FEBE/REI event (in lieu of a FERF/RDI condition). The user can enable or disable BIP-4 verification as depicted below.0 - BIP-4 Verification is NOT performed.1 - BIP-4 Verification is performed.

Receive E3 Configuration and Status Register # 2 - G.751 (Address = 0x1111)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	LOF Defect Condition Declared	OOF Defect Condition Declared	LOS Defect Condition Declared	AIS Defect Condition Declared	Unused		FERF/RDI Defect Condition Declared
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	0	0	0	0	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLOF Algo	R/W	**Receive LOF (Loss of Frame) Defect Declaration/Clearance Criteria Select:** This READ/WRITE bit-field permits the user to select the Loss of Frame (LOF) Defect Declaration and Clearance Criteria. 0 - The Receive E3 Framer block declares the LOF defect condition if the Receive E3 Framer block resides within the OOF (Out-of-Frame) state for 24 E3 frame periods. The Receive E3 Framer block clears the LOF defect condition once the Receive E3 Framer block resides within the In-Frame state for 24 E3 frame period. 1 - The Receive E3 Framer block declares the LOF defect condition if the Receive E3 Framer block resides within the OOF state for 8 E3 frame periods. The Receive E3 Framer block clears the LOF defect condition once the Receive DS3/E3 Framer block resides within the In-Frame state for 8 E3 frame periods.
6	LOF Defect Condition Declared	R/O	**LOF (Loss of Frame) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the LOF defect condition, as described below. 0 - Indicates that the Receive E3 Framer block is NOT currently declaring the LOF defect condition with the incoming data stream. 1 - Indicates that the Receive E3 Framer block is currently declaring the LOF defect condition with the incoming data stream.
5	OOF Defect Condition Declared	R/O	**OOF (Out of Frame) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive DS3/E3 Framer block is currently declaring the OOF defect condition, as described below. 0 - Indicates that the Receive E3 Framer block is NOT declaring the OOF defect condition with the incoming data stream. 1 - Indicates that the Receive E3 Framer block is currently declaring the OOF defect condition with the incoming data stream.

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	LOS Defect Condition Declared	R/O	**LOS (Loss of Signal) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the LOS defect condition, as described below. 0 - Indicates that the Receive E3 Framer block is NOT currently declaring the LOS defect condition in the incoming data stream. 1 - Indicates that the Receive E3 Framer block is currently declaring the LOS defect condition in the incoming data stream.
3	AIS Defect Condition Declared	R/O	**AIS Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the AIS defect condition within the incoming E3 data-stream, as described below. 0 - Indicates that the Receive E3 Framer block is NOT declaring the AIS defect condition with the incoming E3 data stream. 1 - Indicates that the Receive E3 Framer block is currently declaring the AIS defect condition with the incoming data stream.
2 - 1	Unused	R/O	
0	FERF/RDI Defect Condition Declared	R/O	**FERF/RDI (Far-End-Receive Failure/Remote Defect Indicator) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the FERF/RDI defect condition, as described below. 0 - Indicates that the Receive E3 Framer block is NOT declaring the FERF/RDI defect condition. 1 - Indicates that the Receive E3 Framer block is declaring the FERF/RDI defect condition. ***NOTE:*** *This bit-field is ignored if the user has configured the Receive E3 Framer block to compute and verify the BIP-4 value within the incoming E3 data-stream.*

Receive E3 Interrupt Enable Register # 1 - G.751 (Address = 0x1112)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			COFA Interrupt Enable	Change in OOF Defect Condition Interrupt Enable	Change in LOF Defect Condition Interrupt Enable	Change in LOS Defect Condition Interrupt Enable	Change in AIS Defect Condition Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	COFA Interrupt Enable	R/W	**Change of Framing Alignment Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of Framing Alignment Interrupt, within the Channel. If the user enables this interrupt, then the Receive E3 Framer block will generate an interrupt anytime it detects a Change in Frame Alignment (e.g., the FAS bits have appeared to move to a different location in the E3 data stream). 0 - Disables the Change of Framing Alignment Interrupt. 1 - Enables the Change of Framing Alignment Interrupt.
3	Change in OOF Defect Condition Interrupt Enable	R/W	**Change in OOF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in OOF (Out of Frame) Defect Condition Interrupt, within the XRT79L71 If the user enables this interrupt, then the Receive E3 Framer block will generate an interrupt in response to either of the following conditions. • The instant that the Receive E3 Framer block declares the OOF defect condition. • The instant that the Receive E3 Framer block clears the OOF defect condition. The Change in OOF Defect Condition Interrupt can be enabled or disabled, as described below. 0 - Disables the Change in OOF Defect Condition Interrupt. 1 - Enables the Change in OOF Defect Condition Interrupt.
2	Change in LOF Defect Condition Interrupt Enable	R/W	**Change in LOF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in LOF (Loss of Frame) Defect Condition Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive E3 Framer block will generate an interrupt in response to either of the following conditions. • The instant that the Receive E3 Framer block declares the LOF defect condition. • The instant that the Receive E3 Framer block clears the LOF defect condition. The Change in LOF Defect Condition Interrupt can be enabled or disabled, as described below. 0 - Disables the Change in LOF Defect Condition Interrupt. 1 - Enables the Change in LOF Defect Condition Interrupt.

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Change in LOS Defect Condition Interrupt Enable	R/W	**Change in LOS Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in LOS (Loss of Signal) Defect Condition Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive E3 Framer block will generate an interrupt in response to either of the following conditions. • The instant that the Receive E3 Framer block declares the LOS defect condition. • The instant that the Receive E3 Framer block clears the LOS defect condition. The Change in LOS Defect Condition Interrupt can be enabled or disabled, as described below. 0 - Disables the Change in LOS Defect Condition Interrupt. 1 - Enables the Change in LOS Defect Condition Interrupt.
0	Change in AIS Defect Condition Interrupt Enable	R/W	**Change in AIS Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in AIS (Alarm Indication Signal) Defect Condition Interrupt, within the XRT79L71. If the user enables this interrupt, then the Receive E3 Framer block will generate an interrupt in response to either of the following conditions. • The instant that the Receive E3 Framer block declares the AIS defect condition. • The instant that the Receive E3 Framer block clears the AIS defect condition. The Change in AIS Defect Condition Interrupt can be enabled or disabled, as described below. 0 - Disables the Change in AIS Defect Condition Interrupt. 1 - Enables the Change in AIS Defect Condition Interrupt.

Receive E3 Interrupt Enable Register # 2 - G.751 (Address = 0x1113)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change in FERF/RDI Defect Condition Interrupt Enable	Detection of BIP-4 Error Interrupt Enable	Detection of FAS Bit Error Interrupt Enable	Reserved
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	Please set to "0" (the default value) for normal operation

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	Change in FERF/RDI Defect Condition Interrupt Enable	R/W	**Change in FERF/RDI Defect Condition Interrupt:** Enable:This READ/WRITE bit-field permits the user to either enable or disable the Change in FERF/RDI Defect Condition Interrupt. If the user enables this interrupt, then the Receive DS3/E3 Framer block will generate an interrupt in response to either of the following events. • Whenever the Receive E3 Framer block declares the FERF/RDI Defect condition. • Whenever the Receive E3 Framer block clears the FERF/RDI Defect condition. The user can enable or disable this particular interrupt as described below. 0 - Disables the Change in FERF/RDI Defect Condition Interrupt. 1 - Enables the Change in FERF/RDI Condition Interrupt. ***NOTE:*** *This bit-field is ignored if the Receive E3 Framer block is configured to verify BIP-4 values within each incoming E3 frame.*
2	Detection of BIP-4 Error Interrupt Enable	R/W	**Detection of BIP-4 Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of BIP-4 Error Interrupt. If the user enables this interrupt, then the Receive E3 Framer block will generate an interrupt anytime it detects a BIP-4 error, within the incoming E3 data stream. The user can enable or disable this interrupt as described below. 0 - Disables the Detection of BIP-4 Error Interrupt. 1 - Enables the Detection of BIP-4 Error Interrupt. ***NOTE:*** *This bit-field is only active, if the Receive E3 Framer block has been configured to compute and verify the BIP-4 values within each incoming E3 frame.*
1	Detection of FAS Bit Error Interrupt Enable	R/W	**Detection of FAS (Framing Alignment Signal) Bit Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the FAS Bit Error Interrupt. If the user enables this interrupt, then the Receive E3 Framer block will generate an interrupt anytime it detects an FAS error within the incoming E3 data stream. 0 - Disables the Detection of FAS Bit Error Interrupt. 1 - Enables the Detection of FAS Bit Error Interrupt.
0	Unused	R/O	Please set to "0" (the default value) for normal operation.

Receive E3 Interrupt Status Register # 1 - G.751 (Address = 0x1114)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			COFA Interrupt Status	Change in OOF Defect Condition Interrupt Status	Change in LOF Defect Condition Interrupt Status	Change in LOS Defect Condition Interrupt Status	Change in AIS Defect Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	COFA Interrupt Status	RUR	**Change of Framing Alignment (COFA) Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of Framing Alignment (COFA) interrupt has occurred since the last read of this register. 0 - The COFA Interrupt has NOT occurred since the last read of this register. 1 - The COFA Interrupt has occurred since the last read of this register.
3	Change in OOF Defect Condition Interrupt Status	RUR	**Change of OOF (Out of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of OOF Defect Condition Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block generates an interrupt in response to either of the following condition. • Whenever the Receive E3 Framer block declares the OOF Defect Condition. • Whenever the Receive E3 Framer block clears the OOF Defect Condition. 0 - Indicates that the Change in OOF Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change in OOF Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can obtain the current OOF defect condition of the Receive E3 Framer block by reading out the state of Bit 5 (OOF Defect Condition Declared) within the Receive E3 Configuration and Status # 2 - G.751 (Address = 0x1111).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Change in LOF Defect Condition Interrupt Status	RUR	**Change of LOF (Loss of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of LOF Defect Condition Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block generates an interrupt in response to either of the following condition.· • Whenever the Receive E3 Framer block declares the LOF Defect Condition. • Whenever the Receive E3 Framer block clears the LOF Defect Condition. 0 - Indicates that the Change in LOF Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change in LOF Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can obtain the current LOF defect condition of the Receive E3 Framer block by reading out the state of Bit 6 (LOF Defect Condition Declared) within the Receive E3 Configuration and Status # 2 - G.751 (Address = 0x1111).*
1	Change in LOS Defect Condition Interrupt Status	RUR	**Change of LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of LOS Defect Condition Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block generates an interrupt in response to either of the following condition. • Whenever the Receive E3 Framer block declares the LOS Defect Condition. • Whenever the Receive E3 Framer block clears the LOS Defect Condition. 0 - Indicates that the Change of LOS Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of LOS Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can obtain the current LOS defect condition of the Receive E3 Framer block by reading out the state of Bit 4 (LOS Defect Condition Declared) within the Receive E3 Configuration and Status # 2 - G.751 (Address = 0x1111).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Change in AIS Defect Condition Interrupt Status	RUR	**Change of AIS Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of AIS Defect Condition Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block generates an interrupt in response to either of the following condition. • Whenever the Receive E3 Framer block declares the AIS Defect Condition. • Whenever the Receive E3 Framer block clears the AIS Defect Condition. 0 - Indicates that the Change of AIS Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of AIS Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can obtain the current AIS defect condition of the Receive E3 Framer block by reading out the state of Bit 3 (AIS Defect Condition Declared) within the Receive E3 Configuration and Status # 2 - G.751 (Address = 0x1111).*

Receive E3 Interrupt Status Register # 2 - G.751 (Address = 0x1115)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change of FERF/RDI Defect Condition Interrupt Status	Detection of BIP-4 Error Interrupt Status	Detection of FAS Bit Error Interrupt Status	Reserved
R/O	R/O	R/O	R/O	RUR	RUR	RUR	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	Change of FERF/RDI Defect Condition Interrupt Status	RUR	**Change of FERF/RDI Defect Condition Interrupt:** This RESET-upon-READ bit-field indicates whether or not the Change in FERF/RDI Defect Condition interrupt has occurred since the last read of this register. The Receive DS3/E3 Framer block generates this interrupt in response to either of the following events. • Whenever the Receive DS3/E3 Framer block declares the FERF/RDI Defect condition. • Whenever the Receive DS3/E3 Framer block clears the FERF/RDI Defect condition. 0 - Indicates that the Change in FERF/RDI Defect Condition interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change in FERF/RDI Defect Condition interrupt has occurred since the last read of this register.
2	Detection of BIP-4 Error Interrupt Status	RUR	**Detection of BIP-4 Error Interrupt:** This RESET-upon-READ bit-field indicates whether or not the Detection of BIP-4 Error interrupt has occurred since the last read of this register. The Receive DS3/E3 Framer block generates this interrupt anytime it detects BIP-4 errors within the incoming E3 data-stream. 0 - Indicates that the Detection of BIP-4 Error Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Detection of BIP-4 Error Interrupt has occurred since the last read of this register.
1	Detection of FAS Bit Error Interrupt Status	RUR	**Detection of FAS Bit Error Interrupt:** This RESET-upon-READ bit-field indicates whether or not the Detection of FAS Bit Error interrupt has occurred since the last read of this register. The Receive DS3/E3 Framer block generates this interrupt anytime it detects FAS bit errors within the incoming E3 data-stream. 0 - Indicates that the Detection of FAS Bit Error Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Detection of FAS Bit Error Interrupt has occurred since the last read of this register.
0	Unused	R/O	

Receive E3 LAPD Control Register - G.751 (Address = 0x1118)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLAPD Any	Unused				Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive LAPD Interrupt Status
R/W	R/O	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLAPD Any	R/W	**Receive LAPD - Any kind:** This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller block to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes. 0 - Does not invoke this Any Kind of HDLC Message feature. In this case, the Receive LAPD Controller block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI. 1 - Invokes this Any Kind of HDLC Message feature. In this case, the Receive LAPD Controller block will be able to receive HDLC Messages that contain any header byte values. ***NOTE:*** *The user can determine the size (or byte count) of the most recently received LAPD/PMDL Message, by reading the contents of the Receive LAPD Byte Count Register (Address = 0x1184).*
6 - 3	Unused	R/O	
2	Receive LAPD Enable	R/W	**Receive LAPD Controller Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Controller block within the XRT79L71. If the user enables the Receive LAPD Controller block, then it will immediately begin extracting out and monitoring the data (being carried via the N bits) within the incoming E3 data stream. 0 - Enables the Receive LAPD Controller block. 1 - Disables the Receive LAPD Controller block.
1	Receive LAPD Interrupt Enable	R/W	**Receive LAPD Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Message Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the Receive LAPD Controller block receives a new PMDL Message. 0 - Disables the Receive LAPD Message Interrupt. 1 - Enables the Receive LAPD Message Interrupt.
0	Receive LAPD Interrupt Status	RUR	**Receive LAPD Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive LAPD Message Interrupt has occurred since the last read of this register. 0 - Receive LAPD Message Interrupt has NOT occurred since the last read of this register. 1 - Receive LAPD Message Interrupt has occurred since the last read of this register.

Receive E3 LAPD Status Register - G.751 (Address = 0x1119)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	RxABORT	R/O	**Receive ABORT Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block has received an ABORT sequence (e.g., a string of seven consecutive "0s"), as described below. 0 - Indicates that the Receive LAPD Controller block has NOT received an ABORT sequence. 1 - Indicates that the Receive LAPD Controller block has received an ABORT sequence. ***NOTE:*** *Once the Receive LAPD Controller block receives an ABORT sequence, it will set this bit-field "High", until it receives another LAPD Message.*
5 - 4	RxLAPDType[1:0]	R/O	**Receive LAPD Message Type Indicator:** These two READ-ONLY bits indicate the type of LAPD Message that is residing within the Receive LAPD Message buffer. The relationship between the content of these two bit-fields and the corresponding message type is presented below.
3	RxCR Type	R/O	**Received C/R Value:** This READ-ONLY bit-field indicates the value of the C/R bit (within one of the header bytes) of the most recently received LAPD Message.
2	RxFCS Error	R/O	**Receive Frame Check Sequence (FCS) Error Indicator:** This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error. 0 - Indicates that the most recently received LAPD Message frame does not contain an FCS error. 1 - Indicates that the most recently received LAPD Message frame does contain an FCS error.

RxLAPDType[1:0]		Message Type
0	0	CL Path Identification
0	1	Idle Signal Identification
1	0	Test Signal Identification
1	1	ITU-T Path Identification

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	End of Message	R/O	**End of Message Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block has received a complete LAPD Message, as described below. 0 - Receive LAPD Controller block is currently receiving a LAPD Message, but has not received the complete message. 1 - Receive LAPD Controller block has received a complete LAPD Message. ***NOTE:*** *Once the Receive LAPD Controller block sets this bit-field "High", this bit-field will remain high, until the Receive LAPD Controller block begins to receive a new LAPD Message.*
0	Flag Present	R/O	**Receive Flag Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel) .0 - Indicates that the Receive LAPD Controller block is NOT currently receiving the Flag Sequence octet. 1 - Indicates that the Receive LAPD Controller block is currently receiving the Flag Sequence octet.

Receive E3 Service Bits Register - G.751 (Address = 0x111A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						RxA	RxN
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	RxA	R/O	**Received A Bit Value:** This READ-ONLY bit-field reflects the value of the "A" bit, within the most recently received E3 frame.
0	RxN	R/O	**Received N Bit Value:** This READ-ONLY bit-field reflects the value of the "N" bit, within the most recently received E3 frames.

RECEIVE E3, ITU-T G.832 RELATED REGISTERS

Receive E3 Configuration and Status Register # 1 - G.832 (Address = 0x1110)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxPLDType[2:0]			RxFERF Algo.	RxTMark Algo	RxPLDTypeExp[2:0]		
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	RxPLDType[2:0]	R/O	**Received PLD (Payload) Type[2:0]:** These three READ-ONLY bit-fields reflect the value of the Payload Type bits, within the MA byte of the most recently received E3 frame.
4	RxFERF Algo	R/W	**Receive FERF/RDI Defect Declaration/Clearance Algorithm:** This READ/WRITE bit-field permits the user to select a FERF/RDI Defect Declaration and Clearance Algorithm, as indicated below. 0 - Configures the Receive E3 Framer block to declare the FERF/RDI defect condition anytime it receives the FERF/RDI indicator (within the incoming E3 data-stream) in 3 consecutive E3 frames. Additionally, this same setting will also configure the Receive E3 Framer block to clear the FERF/RDI defect condition anytime it ceases to receive the FERF/RDI indicator (within the E3 data-stream) for 3 consecutive E3 frames. 1 - Configures the Receive E3 Framer block to declare the FERF/RDI defect condition anytime it receives the FERF indicator (within the incoming E3 data-stream) in 5 consecutive E3 frames. Additionally, this same setting will also configure the Receive E3 Framer block to clear the FERF/RDI defect condition anytime it ceases to receive the FERF indicator for 5 consecutive E3 frames.
3	RxTMark Algo	R/W	**Receive Timing Marker Validation Algorithm:** This READ/WRITE bit-field permits the user to select the Receive Timing Marker Validation algorithm, as indicated below. 0 - The Timing Marker will be validated if it is of the same state for three (3) consecutive E3 frames. 1 - The Timing Marker will be validated if it is of the same state for five (5) consecutive E3 frames.
2 - 0	RxPLDTypExp[2:0]	R/W	**Receive PLD (Payload) Type - Expected:** This READ/WRITE bit-field permits the user to specify the expected value for the Payload Type, within the MA bytes of each incoming E3 frame. If the Receive E3 Framer block receives a Payload Type that differs then what has been written into these register bits, then it will generate the Payload Type Mismatch Interrupt.

Receive E3 Configuration and Status Register # 2 - G.832 (Address = 0x1111)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	LOF Defect Condition Declared	OOF Defect Condition Declared	LOS Defect Condition Declared	AIS Defect Condition Declared	RxPLD Unstab	RxT Mark	FERF/RDI Defect Condition Declared
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	0	0	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLOF Algo	R/W	**Receive LOF (Loss of Frame) Defect Declaration Algorithm:** This READ/WRITE bit-field permits the user to select a Receive LOF Defect Declaration Algorithm, as indicated below. 0 - Configures the Receive E3 Framer block to declare the LOF defect condition after it has resided within the OOF (Out of Frame) condition for 24 E3 frame periods. 1 - Configure the Receive E3 Framer block will declare the LOF defect condition after it has resided within the OOF condition for 8 E3 frame periods.
6	LOF Defect Condition Declared	R/O	**LOF (Loss of Frame) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the LOF defect condition, as described below. 0 - Indicates that the Receive E3 Framer block is NOT currently declaring the LOF defect condition with the incoming data stream. 1 - Indicates that the Receive E3 Framer block is currently declaring the LOF defect condition with the incoming data stream.
5	OOF Defect Condition Declared	R/O	**OOF (Out of Frame) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the Out of Frame (OOF) defect condition, as indicated below. 0 - Indicates that the Receive E3 Framer block is NOT currently declaring the OOF defect condition within the incoming data-stream. 1 - Indicates that the Receive E3 Framer block is currently declaring the OOF defect condition within the incoming data-stream. ***NOTE:*** *The Receive E3 Framer block will declare the OOF defect condition anytime it detects FA1 or FA2 byte errors in four (4) consecutive incoming E3 frames.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	LOS Defect Condition Declared	R/O	**LOS (Loss of Signal) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the LOS (Loss of Signal) defect condition, as indicated below. 0 - Indicates that the Receive E3 Framer block is NOT currently declaring the LOS defect condition. 1 - Indicates that the Receive E3 Framer block is currently declaring the LOS defect condition.
3	AIS Defect Condition Declared	R/O	**AIS Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the AIS defect condition, in the incoming E3 data stream, as indicated below. 0 - Indicates that the Receive E3 Framer block is NOT currently declaring the AIS defect condition in the incoming E3 data stream. 1 - Indicates that the Receive E3 Framer block is currently declaring the AIS defect condition in the incoming E3 data stream. ***NOTE:*** *The Receive E3 Framer block will declare the AIS defect condition if it detects 7 or less "0s" within two consecutive incoming E3 frames.*
2	RxPLD Unstab	R/O	**Receive Payload-Type Unstable Indicator:** This READ-ONLY bit-field indicates whether or not the Payload Type (within the MA bytes of each incoming E3 frame) has been consistent in the last 5 frames, as indicated below. 0 - The Payload Type value has been consistent for at least 5 consecutive E3 frames. 1 - The Payload Type value has NOT been consistence for the last 5 E3 frames.
1	RxTMark	R/O	**Received (Validated) Timing Marker:** This READ-ONLY bit-field indicates the value of the most recently validated Timing Marker.
0	FERF/RDI Defect Condition Declared	R/O	**FERF/RDI (Far-End-Receive Failure) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Receive E3 Framer block is currently declaring the FERF/RDI defect condition, as indicated below. 0 - Indicates that the Receive E3 Framer block is NOT currently declaring the FERF/RDI defect condition. 1 - Indicates that the Receive E3 Framer block is currently declaring the FERF/RDI defect condition.

Receive E3 Interrupt Enable Register # 1 - G.832 (Address = 0x1112)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in SSM MSG Interrupt Enable	Change in SSM OOS Interrupt Enable	COFA Interrupt Enable	Change in OOF Defect Condition Interrupt Enable	Change in LOF Defect Condition Interrupt Enable	Change in LOS Defect Condition Interrupt Enable	Change in AIS Defect Condition Interrupt Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change in SSM MSG Interrupt Enable	R/W	**Change of Synchronization Status Message (SSM) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in SSM Message Interrupt, as indicated below. 0 - Disables the Change in SSM Message Interrupt. 1 - Enables the Change of SSM Message Interrupt. In this configuration, the Receive E3 Framer block will generate an interrupt anytime it receives a new (or different) SSM Message in the incoming E3 data-stream.
5	Change in SSM OOS State Interrupt Enable	R/W	**Change of SSM OOS (Out of Sequence) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of SSM OOS Condition Interrupt, as indicated below. 0 - Disables the Change of SSM OOS Condition Interrupt. 1 - Enables the Change of SSM OOS Condition Interrupt. In this configuration, the Receive E3 Framer block will generate an interrupt under the following conditions. **a.** When the Receive SSM Controller block declares an SSM OOS condition. **b.** When the Receive SSM Controller block clears the SSM OOS condition.
4	COFA Interrupt Enable	R/W	**Change of Framing Alignment Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of Framing Alignment condition interrupt, as indicated below. 0 - Disables the Change of Framing Alignment Interrupt. 1 - Enables the Change of Framing Alignment Interrupt.

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	Change in OOF Defect Condition Interrupt Enable	R/W	**Change of OOF (Out of Frame) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of OOF Defect Condition Interrupt, as indicated below. 0 - Disables the Change of OOF Defect Condition Interrupt. 1 - Enables the Change of OOF Defect Condition Interrupt. In this configuration, the Receive E3 Framer block will generate an interrupt under the following conditions. **a.** When the Receive E3 Framer block declares the OOF defect condition **b.** When the Receive E3 Framer block clears the OOF defect condition.
2	Change in LOF Defect Condition Interrupt Enable	R/W	**Change of LOF (Loss of Frame) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of LOF Defect Condition Interrupt, as indicated below. 0 - Disables the Change of LOF Defect Condition Interrupt. 1 - Enables the Change of LOF Defect Condition Interrupt. In this configuration, the Receive E3 Framer block will generate an interrupt under the following conditions. **a.** When the Receive E3 Framer block declares the LOF defect condition **b.** When the Receive E3 Framer block clears the LOF defect condition.
1	Change in LOS Defect Condition Interrupt Enable	R/W	**Change of LOS (Loss of Signal) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of LOS Defect Condition Interrupt, as indicated below. 0 - Disables the Change of LOS Defect Condition Interrupt. 1 - Enables the Change of LOS Defect Condition Interrupt. In this configuration, the Receive E3 Framer block will generate an interrupt under the following conditions. **a.** When the Receive E3 Framer block declares an LOS defect condition. **b.** When the Receive E3 Framer block clears the LOS defect condition.

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Change of AIS Defect Condition Interrupt Enable	R/W	**Change of AIS (Alarm Indication Signal) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of AIS Defect Condition Interrupt, as indicated below. 0 - Disables the Change of AIS Defect Condition Interrupt. 1 - Enables the Change of AIS Defect Condition Interrupt. In this configuration, the Receive E3 Framer block will generate an interrupt under the following conditions. **a.** When the Receive E3 Framer block declares an AIS defect condition. **b.** When the Receive E3 Framer block clears the AIS defect condition.

Receive E3 Interrupt Enable Register # 2 - G.832 (Address = 0x1113)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in Receive Trail-Trace Message Interrupt Enable	Reserved	Detection of FEBE Event Interrupt Enable	Change in FERF/RDI Defect Condition Interrupt Enable	Detection of BIP-8 Error Interrupt Enable	Detection of Framing Byte Error Interrupt Enable	RxPLD Mismatch Interrupt Enable
R/O	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change in Receive Trail-Trace Message Interrupt Enable	R/W	**Change in Receive Trail-Trace Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in Receive Trail-Trace Message Interrupt, as indicated below. 0 - Disables the Change in Receive Trail-Trace Message Interrupt. 1 - Enables the Change in Receive Trail-Trace Message Interrupt. In this mode, the Receive E3 Framer block will generate an interrupt anytime it receives a different Trail-Trace message, then what it had been receiving.
5	Unused	R/W	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	Detection of FEBE Event Interrupt Enable	R/W	**Detection of FEBE Event Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of FEBE Event Interrupt, as indicated below. 0 - Disables the Detection of FEBE Event Interrupt. 1 - Enables the Detection of FEBE Event Interrupt. In this mode, the Receive E3 Framer block will generate an interrupt anytime it detects a FEBE (Far-End Block Error) indicator in the incoming E3 data-stream.
3	Change in FERF/RDI Defect Condition Interrupt Enable	R/W	**Change of FERF/RDI Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of FERF/RDI Defect Condition Interrupt, as indicated below. 0 - Disables the Change in FERF/RDI Defect Condition Interrupt. 1 - Enables the Change in FERF/RDI Defect Condition Interrupt. In this mode, the Receive E3 Framer block will generate an interrupt, in response to either of the following conditions. **a.** Whenever the Receive E3 Framer block declares the FERF/RDI defect condition. **b.** Whenever the Receive E3 Framer block clears the FERF/RDI defect condition.
2	Detection of BIP-8 Error Interrupt Enable	R/W	**Detection of BIP-8 Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of BIP-8 Error Interrupt, as indicated below. 0 - Disables the Detection of BIP-8 Error Interrupt. 1 - Enables the Detection of BIP-8 Error Interrupt. In this mode, the Receive E3 Framer block will generate an interrupt anytime it detects a BIP-8 error in the incoming E3 data-stream.
1	Detection of Framing Byte Error Interrupt Enable	R/W	**Detection of Framing Byte Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of Framing Byte Error Interrupt, as indicated below. 0 - Disables the Detection of Framing Byte Error Interrupt. 1 - Enables the Detection of Framing Byte Error Interrupt. In this mode, the Receive E3 Framer block will generate an interrupt anytime it detects a FA1 or FA2 byte error in the incoming E3 data stream.
0	RxPLD Mis Interrupt Enable		**Received Payload Type Mismatch Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive Payload Type Mismatch interrupt, as indicated below. 0 - Disables the Received Payload Type Mismatch Interrupt. 1 - Enables the Received Payload Type Mismatch Interrupt. In this mode, the Receive E3 Framer block will generate an interrupt anytime it receives a Payload Type value (within the MA byte) that differs from that written into the RxPLDExp[2:0] bit-fields.

Receive E3 Interrupt Status Register # 1 - G.832 (Address = 0x1114)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in SSM MSG Interrupt Status	Change in SSM OOS Interrupt Status	COFA Interrupt Status	Change in OOF Defect Condition Interrupt Status	Change in LOF Defect Condition Interrupt Status	Change in LOS Defect Condition Interrupt Status	Change in AIS Defect Condition Interrupt Status
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change in SSM MSG Interrupt Status	RUR	**Change in SSM (Synchronization Status Message) Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in SSM Message Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SSM Controller block will generate an interrupt, anytime it detects a change in the SSM[3:0] value that it has received via the incoming E3 data-stream. 0 - Indicates that the Change in SSM Message Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change in SSM Message Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can obtain the newly received value for SSM by reading out the contents of Bits 3 through 1 (RxSSM[3:0]) within the Receive E3 SSM Register - G.832 (Address = 0x112C).*
5	Change in SSM OOS State Interrupt Status	RUR	**Change in SSM OOS (Out of Sequence) State Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in SSM OOS State Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SSM Controller block will generate the Change in SSM OOS State Interrupt will response to the following events. • Whenever the Receive SSM Controller block declares the SSM OOS Condition. • Whenever the Receive SSM Controller block clears the SSM OOS condition. 0 - Indicates that the Change in SSM OOS Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change in SSM OOS Condition Interrupt has occurred since the last read of this register.

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	COFA Interrupt Status	RUR	**COFA Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the COFA (Change of Framing Alignment) Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block will generate an interrupt anytime it detects a new Framing Alignment with the incoming E3 data-stream. 0 - Indicates that the COFA Interrupt has not occurred since the last of this register. 1 - Indicates that the COFA Interrupt has occurred since the last read of this register.
3	Change in OOF Defect Condition Interrupt Status	RUR	**Change in OOF (Out of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in OOF Defect Condition Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block will generate the Change in OOF Defect Condition Interrupt in response to the following events. • When the Receive E3 Framer block declares the OOF Defect Condition • When the Receive E3 Framer block clears the OOF Defect Condition. 0 - Indicates that the Change in OOF Defect Condition Interrupt has not occurred since the last of this register. 1 - Indicates that the Change in OOF Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the OOF Defect Condition by reading out the contents of Bit 5 (OOF Defect Condition Declared) within the Receive E3 Configuration and Status Register # 2 - G.832 (Address = 0x1111).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Change in LOF Defect Condition Interrupt Status	RUR	**Change in LOF (Loss of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in LOF Defect Condition Interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive E3 Framer block will generate the Change in LOF Defect Condition Interrupt will occur in response to the following events. • Whenever the Receive E3 Framer block declares the LOF Defect Condition. • Whenever the Receive E3 Framer block clears the LOF Defect Condition. 0 - Indicates that the Change in LOF Defect Condition Interrupt has not occurred since the last of this register. 1 - Indicates that the Change in LOF Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the LOF Defect Condition by reading out the contents of Bit 6 (LOF Defect Condition Declared) within the Receive E3 Configuration and Status Register # 2 - G.832 (Address = 0x1111).*
1	Change in LOS Defect Condition Interrupt Status	RUR	**Change in LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in LOS Defect Condition Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block will generate the Change in LOS Defect Condition Interrupt will occur in response to the following events. • Whenever the Receive E3 Framer block declares the LOS Defect Condition. • Whenever the Receive E3 Framer block clears the LOS Defect Condition. 0 - Indicates that the Change in LOS Defect Condition Interrupt has not occurred since the last of this register. 1 - Indicates that the Change in LOS Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the LOS Defect Condition by reading out the contents of Bit 4 (LOS Defect Condition Declared) within the Receive E3 Configuration and Status Register # 2 - G.832 (Address = 0x1111).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Change in AIS Defect Condition Interrupt Status	RUR	**Change in AIS Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in AIS Defect Condition Interrupt has occurred since the last read of this register. f this interrupt is enabled, then the Receive E3 Framer block will generate the Change in AIS State Interrupt will occur in response to the following events. • When the Receive E3 Framer block declares the AIS Defect Condition. • When the Receive E3 Framer block clears the AIS Defect Condition. 0 - Indicates that the Change in AIS Defect Condition Interrupt has not occurred since the last of this register. 1 - Indicates that the Change in AIS Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the AIS Defect Condition by reading out the contents of Bit 3 (AIS Defect Condition Declared) within the Receive E3 Configuration and Status Register # 2 - G.832 (Address = 0x1111).*

Receive E3 Interrupt Status Register # 2 - G.832 (Address = 0x1115)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in Receive Trail-Trace Message Interrupt Status	Reserved	Detection of FEBE/REI Event Interrupt Status	Change in FERF/RDI Defect Condition Interrupt Status	Detection of BIP-8 Error Interrupt Status	Detection of Framing Byte Error Interrupt Status	RxPLD Mismatch Interrupt Status
R/O	RUR	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	Change in Receive Trail-Trace Message Interrupt Status	RUR	**Change in Receive Trail-Trace Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in Receive Trail-Trace Message Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive Trail-Trace Message Controller block will generate an interrupt anytime it receives a Trail-Trace Message, that is different from that of the previously received message. 0 - Indicates that the Change in Receive Trail-Trace Message Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change in Receive Trail-Trace Message Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can obtain the value of the most recently received Trail-Trace Message by reading out the contents of the Receive E3 Trail-Trace Message Register Byte -0 through Receive E3 Trail-Trace Message Byte -15 registers (Address = 0x111C through 0x112B).*
5	Unused	R/O	
4	Detection of FEBE/REI Event Interrupt Status	RUR	**Detection of FEBE/REI Event Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Detection of FEBE Event Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block will generate an interrupt anytime is detects a FEBE event in the incoming E3 data-stream. 0 - Indicates that the Detection of FEBE Event Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Detection of FEBE Event Interrupt has occurred since the last read of this register.
3	Change in FERF/RDI Defect Condition Interrupt Status	RUR	**Change in FERF/RDI (Far-End Receive Failure) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in FERF/RDI Defect Condition Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block will generate an interrupt in response to the following events. • Whenever the Receive E3 Framer block declares the FERF/RDI defect condition. • Whenever the Receive E3 Framer block clears the FERF/RDI defect condition. 0 - Indicates that the Change in FERF/RDI Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change in FERF/RDI Defect Condition Interrupt has occurred since the last read of the register. ***NOTE:*** *The user can obtain the state of the FERF/RDI condition, by reading out the contents of Bit 0 (FERF/RDI Defect Condition Declared) within the Receive E3 Configuration and Status Register # 2 - G.832 (Address = 0x1111).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Detection of BIP-8 Error Interrupt Status	RUR	**Detection of BIP-8 Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Detection of BIP-8 Error Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block will generate an interrupt anytime is detects a BIP-8 Error in the incoming E3 data-stream. 0 - Indicates that the Detection of BIP-8 Error Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Detection of BIP-8 Error Interrupt has occurred since the last read of this register.
1	Detection of Framing Byte Error Interrupt Status	RUR	**Detection of Framing Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Detection of Framing Byte Error Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block will generate an interrupt anytime is detects an error in either the FA1 or FA2 byte, within the incoming E3 data-stream. 0 - Indicates that the Detection of Framing Byte Error Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Detection of Framing Byte Error Interrupt has occurred since the last read of this register.
0	Detection of PLD Type Mismatch Interrupt Status	RUR	**Detection of Payload Type Mismatch Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Detection of Payload Type Mismatch Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E3 Framer block will generate an interrupt anytime it receives an E3 data-stream that contains a RxPLDType[2:0] that is different from the RxPLD-TypeExp[2:0] value. 0 - Indicates that the Detection of Payload Type Mismatch Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Detection of Payload Type Mismatch Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can obtain the contents of the most recently received Payload Type by reading out the contents of Bits 7 through 5 (RxPLDType[2:0]) within the Receive E3 Configuration and Status Register # 1 - G.832 (Address = 0x1110).*

Receive E3 LAPD Control Register - G.832 (Address = 0x1118)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLAPD Any	Unused			Receive LAPD from NR Byte	Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive LAPD Interrupt Status
R/W	R/O	R/O	R/O	R/W	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLAPD Any	R/W	**Receive LAPD - Any kind:** This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller block to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes. 0 - Does not invoke this Any Kind of HDLC Message feature. In this case, the Receive LAPD Controller block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI. 1-Invokes this Any Kind of HDLC Message feature. In this case, the Receive LAPD Controller block will be able to receive HDLC Messages that contain any header byte values. ***NOTE:*** *The user can determine the size (or byte count) of the most recently received LAPD/PMDL Message, by reading the contents of the Receive LAPD Byte Count Register (Address = 0x1184).*
6 - 4	Unused	R/O	
3	Receive LAPD from NR Byte	R/W	**Receive LAPD Message from NR Byte Select:** This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller block to extract out the PMDL data from the NR or GC byte, within the incoming E3 data stream. 0 - The Receive LAPD Controller block will extract PMDL information from the GC byte, within the incoming E3 data stream. 1 - The Receive LAPD Controller block will extract PMDL information from the NR byte, within the incoming E3 data stream.
2	Receive LAPD Enable	R/W	**Receive LAPD Controller Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Controller block within the XRT79L71. If the user enables the Receive LAPD Controller block then it will immediately begin extracting out and monitoring the data that is being carried by either the NR or GC bytes (depending upon user configuration) within the incoming E3 data stream. 0 - Disables the Receive LAPD Controller Block. 1 - Enables the Receive LAPD Controller Block for operation.
1	Receive LAPD Interrupt Enable	R/W	**Receive LAPD Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Message Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt, anytime the Receive LAPD Controller block receives a new LAPD/PMDL Message. 0 - Disables the Receive LAPD Message Interrupt. 1 - Enables the Receive LAPD Message Interrupt. ***NOTE:*** *This bit-field is ignored if the Receive LAPD Controller block is disabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Receive LAPD Interrupt Status	RUR	**Receive LAPD Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive LAPD Message Interrupt has occurred since the last read of this register as described below. 0 - Indicates that the Receive LAPD Message Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Receive LAPD Message Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is ignored if the Receive LAPD Controller block or the Receive LAPD Message Interrupt are disabled.*

Receive E3 LAPD Status Register - G.832 (Address = 0x1119)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	RxABORT	R/O	**Receive ABORT Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the most recently received LAPD/PMDL message was interrupted by an ABORT Sequence (e.g., a string of seven or more consecutive "1s") as described below. 0 - Indicates that the Receive LAPD Controller block has NOT received an ABORT sequence within the most recently received LAPD/PMDL Message. 1 - Indicates that the Receive LAPD Controller block has received an ABORT sequence within the most recently received LAPD/PMDL Message. ***NOTE:*** *Once the Receive LAPD Controller block receives an ABORT sequence, it will set this bit-field "High", until it receives another LAPD/PMDL Messages.*

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>5 - 4</td><td>RxLAPDType[1:0]</td><td>R/O</td><td>Receive LAPD Message Type Indicator [1:0]:
These two READ-ONLY bits indicate the type of LAPD Message that is residing within the Receive LAPD Message buffer. The relationship between the content of these two bit-fields and the corresponding message type is presented below.
<table>
<tr><th colspan="2">RxLAPDType[1:0]</th><th>Message Type</th></tr>
<tr><td>0</td><td>0</td><td>CL Path Identification</td></tr>
<tr><td>0</td><td>1</td><td>Idle Signal Identification</td></tr>
<tr><td>1</td><td>0</td><td>Test Signal Identification</td></tr>
<tr><td>1</td><td>1</td><td>ITU-T Path Identification</td></tr>
</table></td></tr>
<tr><td>3</td><td>RxCR Type</td><td>R/O</td><td>Received C/R Value:
This READ-ONLY bit-field indicates the value of the C/R bit (within one of the header bytes) of the most recently received LAPD Message.</td></tr>
<tr><td>2</td><td>RxFCS Error</td><td>R/O</td><td>Receive Frame Check Sequence (FCS) Error Indicator:
This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error, as described below.
0 - Indicates that the most recently received LAPD Message frame does not contain an FCS error.
1 - Indicates that the most recently received LAPD Message frame does contain an FCS error.</td></tr>
<tr><td>1</td><td>End of Message</td><td>R/O</td><td>End of Message Indicator:
This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block has received a complete LAPD Message.
0 - Indicates that the Receive LAPD Controller block is still currently receiving a LAPD Message, but has not received the complete message.
1 - Indicates that the Receive LAPD Controller block has received a completed LAPD Message.
NOTE: Once the Receive LAPD Controller block sets this bit-field "High", this bit-field will remain high, until the Receive LAPD Controller block begins to receive a new LAPD Message.</td></tr>
<tr><td>0</td><td>Flag Present</td><td>R/O</td><td>Receive Flag Sequence Indicator:
This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets) within the Data Link channel.
0 - Indicates that the Receive LAPD Controller block is NOT currently receiving the Flag Sequence octet.
1 - Indicates that the Receive LAPD Controller block is currently receiving the Flag Sequence octet.</td></tr>
</table>

Receive E3 NR Byte Register - G.832 (Address = 0x111A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxNR_Byte[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxNR_Byte[7:0]	R/O	**Receive NR Byte Value:** These READ-ONLY bit-fields contain the value of the NR byte, within the most recently received E3 frame.

Receive E3 GC Byte Register - G.832 (Address = 0x111B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxGC_Byte[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxGC_Byte[7:0]	R/O	**Receive GC Byte Value:** These READ-ONLY bit-fields contain the value of the GC byte, within the most recently received E3 frame.

Receive E3 Trail-Trace - 0 Register - G.832 (Address = 0x111C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_0[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_0[7:0]	R/O	**Receive Trail-Trace Message - Byte 0:** These READ-ONLY bit-fields contain the contents of Byte 0 (e.g., the Marker Byte), within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 1 Register - G.832 (Address = 0x111D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_1[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_1[7:0]	R/O	**Receive Trail-Trace Message - Byte 1:** These READ-ONLY bit-fields contain the contents of Byte 1, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 2 Register - G.832 (Address = 0x111E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_2[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_2[7:0]	R/O	**Receive Trail-Trace Message - Byte 2:** These READ-ONLY bit-fields contain the contents of Byte 2, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 3 Register - G.832 (Address = 0x111F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_3[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_3[7:0]	R/O	**Receive Trail-Trace Message - Byte 3:** These READ-ONLY bit-fields contain the contents of Byte 3, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 4 Register - G.832 (Address = 0x1120)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_4[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_4[7:0]	R/O	**Receive Trail-Trace Message - Byte 4:** These READ-ONLY bit-fields contain the contents of Byte 4, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 5 Register - G.832 (Address = 0x1121)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_5[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_5[7:0]	R/O	**Receive Trail-Trace Message - Byte 5:** These READ-ONLY bit-fields contain the contents of Byte 5, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 6 Register - G.832 (Address = 0x1122)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_6[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_6[7:0]	R/O	**Receive Trail-Trace Message - Byte 6:** These READ-ONLY bit-fields contain the contents of Byte 6, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 7 Register - G.832 (Address = 0x1123)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_7[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_7[7:0]	R/O	**Receive Trail-Trace Message - Byte 7:** These READ-ONLY bit-fields contain the contents of Byte 7, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 8 Register - G.832 (Address = 0x1124)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_8[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_8[7:0]	R/O	**Receive Trail-Trace Message - Byte 8:** These READ-ONLY bit-fields contain the contents of Byte 8, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 9 Register - G.832 (Address = 0x1125)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_9[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_9[7:0]	R/O	**Receive Trail-Trace Message - Byte 9:** These READ-ONLY bit-fields contain the contents of Byte 9, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 10 Register - G.832 (Address = 0x1126)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_10[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_10[7:0]	R/O	**Receive Trail-Trace Message - Byte 10:** These READ-ONLY bit-fields contain the contents of Byte 10, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 11 Register - G.832 (Address = 0x1127)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_11[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_11[7:0]	R/O	**Receive Trail-Trace Message - Byte 11:** These READ-ONLY bit-fields contain the contents of Byte 11, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 12 Register - G.832 (Address = 0x1128)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_12[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_12[7:0]	R/O	**Receive Trail-Trace Message - Byte 12:** These READ-ONLY bit-fields contain the contents of Byte 12, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 13 Register - G.832 (Address = 0x1129)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_13[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_13[7:0]	R/O	**Receive Trail-Trace Message - Byte 13:** These READ-ONLY bit-fields contain the contents of Byte 13, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 14 Register - G.832 (Address = 0x112A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_14[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_14[7:0]	R/O	**Receive Trail-Trace Message - Byte 14:** These READ-ONLY bit-fields contain the contents of Byte 14, within the most recently received Trail-Trace Message.

Receive E3 Trail-Trace - 15 Register - G.832 (Address = 0x112B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_15[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_15[7:0]	R/O	**Receive Trail-Trace Message - Byte 15:** These READ-ONLY bit-fields contain the contents of Byte 15, within the most recently received Trail-Trace Message.

Receive E3 SSM Register - G.832 (Address = 0x112C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxSSM Enable	MF[1:0]		Reserved	RxSSM[3:0]			
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxSSM Enable	R/W	**Receive SSM Enable:** This READ/WRITE bit-field permits the user to configure the Receive E3 Framer block to operate in either the Old ITU-T G.832 Framing format or in the New ITU-T G.832 Framing format. 0 - Configures the Receive E3 Framer block to support the Pre October 1998 version of the E3, ITU-T G.832 Framing format. 1 - Configures the Receive E3 Framer block to support the October 1998 version of the E3, ITU-T G.832 framing format. ***NOTE:*** *If the user configures the Receive E3 Framer block to support the October 1998 Version of the E3, ITU-T G.832 Framing format, then the Receive SSM Controller block will be enabled.*
6 - 5	MF[1:0]	R/O	**Multi-Frame Identification:** These READ-ONLY bit-fields reflect the current frame number, within the Received Multi-Frame. ***NOTE:*** *These bit-fields are only active if the Receive SSM Controller block is active, and if Bit 7 (RxSSM Enable) of this register is set to "1".*
4	Unused	R/O	
3 - 0	RxSSM[3:0]	R/O	**Receive Synchronization Status Message[3:0]:** These READ-ONLY bit-fields reflect the content of the SSM bits, within the most recently received SSM Multi-frame. ***NOTE:*** *These bit-fields are only active if the Receive SSM Controller block is active, and if Bit 7 (RxSSM Enable) of this register is set to "1".*

TRANSMIT DS3 RELATED REGISTERS

Transmit DS3 Configuration Register (Address = 0x1130)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force TxFERF/RDI	Tx X-Bits	TxIdle	TxAIS	TxLOS	TxFERF/RDI upon LOS	TxFERF/RDI upon OOF	TxFERF/RDI upon AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Force TxFERF/RDI	R/W	**Force Transmit Yellow Alarm (FERF/RDI) indicator:** This READ/WRITE bit-field permits the user to force the Transmit DS3 Framer block to transmit the FERF/RDI indicator to the remote terminal equipment by setting both of the X-bits (within each outbound DS3 frame) to "0". 0 - Does not force the Transmit DS3/E3 Framer block to transmit the FERF/RDI indicator. In this case, the Transmit DS3/E3 Framer block will set the X bits (within each outbound DS3 frame) to the appropriate value, depending upon receive conditions (as detected by the Receive DS3 Framer block). 1 - Forces the Transmit DS3/E3 Framer block to transmit the FERF/RDI indicator. In this case, the Transmit DS3/E3 Framer block will force the X bits (within each outbound DS3 frame) to "0". Thereby transmitting the FERF/RDI indicator to the remote terminal equipment. ***NOTE:*** *For normal operation (e.g., where the Transmit DS3/E3 Framer block will automatically transmit the FERF/RDI indicator whenever the Receive DS3/E3 Framer block declares either the LOS, AIS or LOF/OOF defect condition), the user MUST set this bit-field to "0".*
6	Tx X-Bits	R/W	**Force X bits to "1":** This READ/WRITE bit-field permits the user to force the Transmit DS3 Framer block to set the X-bits (within each outbound DS3 frame) to "1". 0 - Configures the Transmit DS3/E3 Framer block to automatically set the X bits to the appropriate value, depending upon the receive conditions (as detected by the Receive DS3 Framer block). 1 - Configures the Transmit DS3/E3 Framer block to force all of the "X" bits (within the outbound DS3 data-stream) to "1". In this configuration setting the Transmit DS3/E3 Framer block sets all X bits to "1" independent of whether the Receive DS3/E3 Framer block is currently declaring any defect conditions. ***NOTE:*** *For normal operation (e.g., where the Transmit DS3/E3 Framer block automatically transmits the FERF/RDI indicator whenever the Receive DS3/E3 Framer block declares the LOS, AIS or LOF/OOF defect condition) the user must set this bit-field to "0".*

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	TxIdle	R/W	**Transmit DS3 Idle Signal:** This READ/WRITE bit-field permits the user to force the Transmit DS3 Framer block to transmit the DS3 Idle signal pattern to the remote terminal equipment, as described below. 0 - Configures the Transmit DS3/E3 Framer block to transmit normal traffic to the remote terminal equipment. 1 - Configures the Transmit DS3/E3 Framer block to transmit the DS3 Idle Pattern to the remote terminal equipment ***NOTES:*** 1. *This bit-field is ignored if TxAIS or TxLOS bit-fields are set to "1".* 2. *The exact pattern that the Transmit DS3 Framer block transmits (whenever this bit-field is set to "1") depends upon the contents within Bits 3 through 0 (Tx_Idle_Pattern[3:0]) within the Transmit DS3 Pattern Register (Address = 0x114C).*
4	TxAIS	R/W	**Transmit AIS Pattern:** This READ/WRITE bit-field permits the user to force the Transmit DS3 Framer block to transmit the AIS indicator to the remote terminal equipment, as described below. 0 - Configures the Transmit DS3/E3 Framer block to transmit normal traffic to remote terminal equipment. 1 - Configures the Transmit DS3/E3 Framer block to transmit the DS3 AIS indicator to the remote terminal equipment. ***NOTES:*** 1. *This bit-field is ignored if the TxLOS bit-field is set to "1".* 2. *When this bit-field is set to "1", it will transmit either a "Framed, repeating "1, 0, 1, 0, …" pattern, or an Unframed, "All-Ones" pattern, depending upon the state of Bit 7 (TxAIS Unframed "All-Ones"), within the Transmit DS3 Pattern Register (Address = 0x114C).*
3	TxLOS	R/W	**Transmit LOS Pattern:** This READ/WRITE bit-field permits the user to force the Transmit DS3 Framer block to transmit an LOS signal pattern to the remote terminal equipment, as described below. 0 - Configures the Transmit DS3/E3 Framer block to transmit normal traffic to the remote terminal equipment. 1 - Configures the Transmit DS3/E3 Framer block to transmit the LOS Pattern (e.g., All Zeros or an All Ones Pattern, depending upon user configuration). ***NOTES:*** 1. *This bit-field is ignored if TxAIS or TxLOS are set to "1".* 2. *When this bit-field is set to "1", it will transmit either an "All Zeros" pattern, or an "*All-Ones*" pattern, depending upon the state of Bit 4 (TxLOS Pattern) within the "Transmit DS3 Pattern Register (Address =0x114C).*

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	TxFERF/RDI upon LOS	R/W	**Transmit FERF/RDI upon Declaration of the LOS defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the corresponding (Near-End) Receive DS3 Framer block declares the LOS defect condition, as described below. 0 - The Transmit DS3 Framer block will NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Receive DS3 Framer block declares the LOS defect condition. 1 - The Transmit DS3 Framer block will automatically transmit the FERF/RDI indicator whenever (and for the duration that) the Receive DS3 Framer block declares the LOS defect condition.
1	TxFERF/RDI upon OOF	R/W	**Transmit FERF/RDI upon Declaration of the OOF Defect Condition:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the corresponding (Near-End) Receive DS3 Framer block declares the OOF defect condition, as described below. 0 - The Transmit DS3 Framer block will NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the corresponding (Near-End) Receive DS3 Framer block declares the OOF defect condition.1 - The Transmit DS3 Framer block will automatically transmit the FERF/RDI indicator whenever (and for the duration that) the Receive DS3 Framer block declares the OOF defect condition.
0	TxFERF/RDI upon AIS	R/W	**Transmit FERF/RDI upon Declaration of the AIS Defect Condition:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the corresponding (Near-End) Receive DS3 Framer block declares the AIS defect condition, as described below. 0 - The Transmit DS3 Framer block will NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the corresponding (Near-End) Receive DS3 Framer block declares the AIS defect condition. 1 - The Transmit DS3 Framer block will automatically transmit the FERF/RDI indicator whenever (and for the duration that) the Receive DS3 Framer block declares the AIS defect condition.

Transmit DS3 FEAC Configuration and Status Register (Address = 0x1131)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxFEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
R/O	R/O	R/O	R/W	RUR	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	Please set to "0" for normal operation.
4	TxFEAC Interrupt Enable	R/W	**Transmit FEAC Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit FEAC Interrupt. If the user enables this interrupt, then the Transmit FEAC Controller block will generate an interrupt, once it has completed its 10th transmission of a given FEAC Message to the remote terminal equipment. 0 - Disables the Transmit FEAC Interrupt. In this configuration setting, the Transmit FEAC Controller block will NOT generate an interrupt after it has completed its 10th transmission of a given FEAC Message. 1 - Enables the Transmit FEAC Interrupt. In this configuration setting, the Transmit FEAC Controller block will generate an interrupt after it has completed its 10th transmission of a given FEAC Message. ***NOTE:*** *This bit-field is only active if Bit 2 (TxFEAC Enable) within this register is set to "1".*
3	TxFEACInterrupt Status	RUR	**Transmit FEAC Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit FEAC Interrupt has occurred since the last read of this register, as described below. 0 - Indicates that the Transmit FEAC Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Transmit FEAC Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if Bit 2 (TxFEAC Enable) within this register is set to "1".*
2	TxFEACEnable	R/W	**Transmit FEAC Controller Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit FEAC Controller block, as described below. 0 - Disables the Transmit FEAC Controller block. 1 - Enables the Transmit FEAC Controller block.

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	TxFEAC Go	R/W	**Transmit FEAC Message Command:** A "0" to "1" transition, within this bit-field configures the Transmit FEAC Controller block to begin its transmission of the FEAC Message (which consists of the FEAC code, as specified within the TxDS3 FEAC Register). ***NOTES:*** *1. The user is advised to perform a write operation that resets this bit-field back to "0", following execution of the command to transmit a FEAC Message.* *2. This bit-field is only active if Bit 2 (TxFEAC Enable) within this register is set to "1".*
0	TxFEAC Busy	R/O	**Transmit FEAC Controller BUSY Indicator:** This READ-ONLY bit-field indicates whether or not the Transmit FEAC Controller block is currently busy transmitting a FEAC Message to the remote terminal, as described below. 0 - Indicates that the Transmit FEAC Controller block is NOT busy. 1 - Indicates that the Transmit FEAC Controller block is currently transmitting the FEAC Message to the remote terminal. ***NOTE:*** *This bit-field is only active if Bit 2 (TxFEAC Enable) within this register is set to "1".*

Transmit DS3 FEAC Register (Address = 0x1132)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	TxFEACCode[5:0]						Unused
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/O
0	1	1	1	1	1	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6 - 1	TxFEACCode[5:0]	R/W	**Transmit FEAC Code Word[5:0]:** These six (6) READ/WRITE bit-fields permit the user to specify the FEAC Code word that the Transmit FEAC Controller block should transmit to the remote terminal equipment. Once the user enables the Transmit FEAC Controller block and commands it to begin its transmission, the Transmit FEAC Controller block will then (1) encapsulate this six-bit code word into a 16-bit structure, (2) proceed to transmit this 16-bit structure 10 times, repeatedly, and then halt. ***NOTE:*** *These bit-fields are ignored if the user does not enable and use the Transmit FEAC Controller block.*
0	Unused	R/O	

Transmit DS3 LAPD Configuration Register (Address = 0x1133)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit LAPD Any	Unused			Auto Retransmit	Reserved	Transmit LAPD Message Length	Transmit LAPD Enable
R/W	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Transmit LAPD Any	R/W	Transmit LAPD - Any kind: This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller block to transmit any kind of LAPD Message (or HDLC Message) with a size of 82 byte or less. If the user implements this option, then the Transmit LAPD Controller block will be capable of transmitting any kind of HDLC frame (with any value of header bytes). The only restriction is that the size of the HDLC frame must not exceed 82 bytes. 0 - Does not invoke this Any Kind of HDLC Message feature. In this case, the Transmit LAPD Controller block will only transmit HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI. 1- Invokes this Any Kind of HDLC Message feature. In this case, the Transmit LAPD Controller block will be able to transmit HDLC Messages that contain any header byte values. ***NOTE:*** *If the user invokes the Any Kind of HDLC Message feature, then the user must indicate the size of the information payload (in terms of bytes) within the Transmit LAPD Byte Count Register (Address =0x1183).*
6 - 4	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	Auto Retransmit	R/W	**Auto-Retransmit of LAPD Message:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller block to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature and then commands the Transmit LAPD Controller block to transmit a given PMDL Message, the Transmit LAPD Controller block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. 0 - Disables the Auto-Retransmit Feature. In this case, the PMDL Message will only be transmitted once, afterwards the Transmit LAPD Controller block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission. 1 - Enables the Auto-Retransmit Feature.In this case, the Transmit LAPD Controller block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. ***NOTE:*** *This bit-field is ignored if the Transmit LAPD Controller block is disabled.*
2	Reserved	R/O	
1	Transmit LAPD Message Length	R/W	**Transmit LAPD Message Length Select:** This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below. 0 - Configures the Transmit LAPD Controller block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes. 1 - Configures the Transmit LAPD Controller block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes. This bit-field is ignored if the Transmit LAPD Controller block is disabled.
0	Transmit LAPD Enable	R/W	**Transmit LAPD Controller Block Enable:** This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller block, within the XRT79L7l device. Once the user enables the Transmit LAPD Controller block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the outbound "DL" bits, within each DS3 data stream. The Transmit LAPD Controller block will continue to repeatedly transmit the Flag Sequence octet until the user commands the Transmit LAPD Controller block to transmit a PMDL Message. 0 - Disables the Transmit LAPD Controller block. 1 - Enables the Transmit LAPD Controller block.

Transmit DS3 LAPD Status/Interrupt Register (Address = 0x1134)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Initiate Transmis-sion of LAPD/ PMDL Message	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Initiate Transmission of LAPD/PMDL Message	R/W	**Transmit LAPD Message Command:** A "0" to "1" transition, within this bit-field commands the Transmit LAPD Controller block to begin the following activities: • Reading out the contents of the Transmit LAPD Message Buffer • Zero-Stuffing of this data • FCS Calculation and Insertion· • Fragmentation of this composite PMDL Message, and insertion into the "DL" bit-fields, within each outbound DS3 frame. ***NOTE:*** *This bit-field is only active if the Transmit LAPD Controller block has been enabled.*
2	Transmit LAPD Controller Busy	R/O	**Transmit LAPD Controller Busy Indicator:** This READ-ONLY bit-field indicates whether or not the Transmit LAPD Controller block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can con-tinuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message. 0 - Indicates that the Transmit LAPD Controller block is NOT busy transmitting a PMDL Message. 1 - Indicates that the Transmit LAPD Controller block is currently busy transmitting a PMDL Message. ***NOTE:*** *This bit-field is only active if the Transmit LAPD Controller block has been enabled.*
1	Transmit LAPD Interrupt Enable	R/W	**Transmit LAPD Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit LAPD Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt anytime the Transmit LAPD Controller block has completed its transmis-sion of a given LAPD/PMDL Message to the remote terminal. 0 - Disables the Transmit LAPD Interrupt. 1 - Enables the Transmit LAPD Interrupt.

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Transmit LAPD Interrupt Status	RUR	**Transmit LAPD Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit LAPD Interrupt has occurred since the last read of this register. 0 - Indicates that the Transmit LAPD Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Transmit LAPD Interrupt has occurred since the last read of this register.

Transmit DS3 M-Bit Mask Register (Address = 0x1135)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFEBEDat[2:0]			FEBE Register Enable	Tx P-Bit Error	TxM_Bit_Mask[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DECRIPTION
7 - 5	TxFEBEDat[2:0]	R/W	**Transmit FEBE Value:** These READ/WRITE bit-fields, along with FEBE Register Enable permit the user to configure the Transmit DS3 Framer block to transmit user specified FEBE values (to the remote terminal) based upon the contents of these bit-fields. If the user sets the FEBE Register Enable bit-field to "1", then the Transmit DS3 Framer block will write the contents of these bit-fields into the FEBE bits, within each outbound DS3 frame. If the user sets the FEBE Register Enable bit-field to "0" then these register bits will be ignored.
4	FEBE Register Enable	R/W	**Transmit FEBE (by Software) Enable:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit user specified FEBE values (to the remote terminal) per register setting via the TxFEBEDat[2:0] bit-field. This option provides the user with software control over the Outbound FEBE values, within the DS3 data stream. 0 - Configures the Transmit DS3 Framer block to set the FEBE bit-fields (within each outbound DS3 frame) to the appropriate values based upon receive conditions, as determined by the companion Receive DS3 Framer block. 1 - Configures the Transmit DS3 Framer block to write the contents of the TxFEBEDat[2:0] bit-fields into the FEBE bits, within each Outbound DS3 frame.

BIT NUMBER	NAME	TYPE	DECRIPTION
3	Tx P-Bit Error	R/W	**Transmit P-Bit Error:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with erred P-bits, as indicated below. 0 - Configures the Transmit DS3/E3 Framer block to generate and transmit DS3 frames with correct P-bits, to the remote terminal equipment. 1 - Configures the Transmit DS3/E3 Framer block to generate and transmit DS3 frames with erred P-bits, to the remote terminal equipment.
2 - 0	TxM_Bit_Mask[2:0]	R/W	**Transmit M-Bit Error:** These READ/WRITE bit-fields permit the user to configure the Transmit DS3 Framer block to transmit DS3 frames with erred M-bits. These three (3) bit-fields correspond to the three M-bits, within each outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of these bit-fields and the value of the three M-bits. The results of this calculation will be written back into the M-bit positions within each outbound DS3 frame. The user should set these bit-fields to "0, 0, 0" for normal (e.g., un-erred) operation.

Transmit DS3 F-Bit Mask # 1 Register (Address = 0x1136)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				F_Bit Mask[27]/ UDL Bit # 9 (C73)	F_Bit Mask [26]/ UDL Bit # 8 (C72)	F_Bit Mask [25]/ UDL Bit# 7 (C71)	F_Bit Mask [24]/
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	F Bit Mask[27]/UDL Bit # 9 (C73)	R/W	**Transmit F-Bit Error - Bit 28/UDL Bit # 9 (C73):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 28:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 28th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 28th F-bit. The results of this calculation will be written back into the 28th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the "Clear-Channel Framer Mode", AND if "TxOHSrc" = "1" - Insert Enable for UDL Bit # 9 or C73 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit #9 (or C73) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1 - Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	F Bit Mask [26]/UDL Bit #8 (C72)	R/W	**Transmit F-Bit Error - Bit 27/UDL Bit # 8 (C72):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0" **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 27** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 27th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 27th F-bit. The results of this calculation will be written back into the 27th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode AND if TxOHSrc = "1" - Insert Enable for UDL Bit # 8 or C72 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit #8 (or C72) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1 - Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	F Bit Mask [25]/UDL Bit # 7 (C71)	R/W	**Transmit F-Bit Error - Bit 26/UDL Bit # 7 (C71):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 26:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 26th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 26th F-bit. The results of this calculation will be written back into the 26th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode AND if TxOHSrc = "1" - Insert Enable for UDL Bit # 7 or C71 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit #7 (or C71) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1 - Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [24]	R/W	**Transmit F-Bit Error - Bit 25:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 25th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 25th F-bit. The results of this calculation will be written back into the 25th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

Transmit DS3 F-Bit Mask # 2 Register (Address = 0x1137)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F_Bit Mask [23]/ UDL Bit# 6 (C63)	F_Bit Mask [22]/ UDL Bit# 5 (C62)	F_Bit Mask [21]/ UDL Bit # 4 (C61)	F_Bit Mask [20]	F_Bit Mask [19]/DL Bit # 3 (C53)	F_Bit Mask [18]/DL Bit # 2 (C52)	F_Bit Mask [17]/DL Bit# 1 (C51)	F_Bit Mask [16]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F Bit Mask[23]/UDL Bit # 6 (C63)	R/W	**Transmit F-Bit Error - Bit 24/UDL Bit # 6 (C63):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 24:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 24th F-bit, within a given out-bound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 24th F-bit. The results of this calculation will be written back into the 24th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for UDL Bit # 6 or C63 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit # 6 (or C63) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	F Bit Mask [22]/UDL Bit # 5 (C62)	R/W	**Transmit F-Bit Error - Bit 23/UDL Bit # 5 (C62):** The exact function of this register bit depends upon the following parameters.· • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 23:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 23rd F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 23rd F-bit. The results of this calculation will be written back into the 23rd F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for UDL Bit # 5 or C62 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit # 5 (or C62) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	F Bit Mask [21]/UDL Bit # 4 (C61)	R/W	**Transmit F-Bit Error - Bit 22/UDL Bit # 4 (C61):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 22:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 22nd F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 22nd F-bit. The results of this calculation will be written back into the 22nd F-bit position, within each outbound DS3 frame.The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for UDL Bit # 4 or C61 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit # 4 (or C61) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.
4	F Bit Mask [20]	R/W	**Transmit F-Bit Error - Bit 21:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 21st F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 21st F-bit. The results of this calculation will be written back into the 21st F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	F Bit Mask [19]/DL Bit # 3 (C53)	R/W	**Transmit F-Bit Error - Bit 20/DL Bit # 3 (C53):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 20:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 20th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 20th F-bit. The results of this calculation will be written back into the 20th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for DL Bit # 3 or C53 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the DL Bit # 3 (or C53) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	F Bit Mask [18]/DL Bit # 2 (C52)	R/W	**Transmit F-Bit Error - Bit 19/DL Bit # 2 (C52):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 19:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 19th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 19th F-bit. The results of this calculation will be written back into the 19th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for DL Bit # 2 or C52 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the DL Bit # 2 (or C52) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	F Bit Mask [17]/DL Bit # 1 (C51)	R/W	**Transmit F-Bit Error - Bit 18/DL Bit # 1 (C51):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 18:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 18th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 18th F-bit. The results of this calculation will be written back into the 18th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for DL Bit # 1 or C51 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the DL Bit # 1 (or C51) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [16]	R/W	**Transmit F-Bit Error - Bit 17:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 17th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 17th F-bit. The results of this calculation will be written back into the 17th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

Transmit DS3 F-Bit Mask # 3 Register (Address = 0x1138)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F_Bit Mask [15]/ FEBE Bit 3 (C43)	F_Bit Mask [14]/ FEBE Bit 2 (C42)	F_Bit Mask [13]/ FEBE Bit 1 (C41)	F_Bit Mask [12]	F_Bit Mask [11]/ CP Bit # 3(C33)	F_Bit Mask [10]/ CP Bit # 2(C32)	F_Bit Mask [9]/CP Bit # 1(C31)	F_Bit Mask [8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F Bit Mask[15]/FEBE Bit # 3 (C43)	R/W	**Transmit F-Bit Error - Bit 16/FEBE Bit # 3 (C43):** The exact function of this register bit depends upon the following parameters.· • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 16:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 16th F-bit, within a given out-bound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 16th F-bit. The results of this calculation will be written back into the 16th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for FEBE Bit # 3 or C43 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the FEBE Bit # 3 (or C43) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	F Bit Mask [14]/FEBE Bit # 2 (C42)	R/W	**Transmit F-Bit Error - Bit 15/FEBE Bit # 2 (C42):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 15:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 15th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 15th F-bit. The results of this calculation will be written back into the 15th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for FEBE Bit # 2 or C42 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the FEBE Bit # 2 (or C42) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	F Bit Mask [13]/FEBE Bit 1 (C41)	R/W	**Transmit F-Bit Error - Bit 14/FEBE Bit # 1 C41):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 14:T** his READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 14th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 14th F-bit. The results of this calculation will be written back into the 14th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for FEBE Bit # 1 or C41 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the FEBE Bit # 1 (or C41) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.
4	F Bit Mask [12]	R/W	**Transmit F-Bit Error - Bit 13:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 13th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 13th F-bit. The results of this calculation will be written back into the 13th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	F Bit Mask [11]/CP Bit # 3 (C33)	R/W	**Transmit F-Bit Error - Bit 12/CP Bit # 3 (C33):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 12:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 12th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 12th F-bit. The results of this calculation will be written back into the 12th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for CP Bit # 3 or C33 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the CP Bit # 3 (or C33) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	F Bit Mask [10]/CP Bit # 2 (C32)	R/W	**Transmit F-Bit Error - Bit 11/CP Bit # 2 (C32):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 11: This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 11th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 11th F-bit. The results of this calculation will be written back into the 11th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for CP Bit # 2 or C32 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the CP Bit # 2 (or C32) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	F Bit Mask [9]/CP Bit # 1 (C31)	R/W	**Transmit F-Bit Error - Bit 10/CP Bit # 1 (C31):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 10:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 10th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 10th F-bit. The results of this calculation will be written back into the 10th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for CP Bit # 1 or C31 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the CP Bit # 1 (or C31) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [8]	R/W	**Transmit F-Bit Error - Bit 9:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 9th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 9th F-bit. The results of this calculation will be written back into the 9th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

Transmit DS3 F-Bit Mask # 4 Register (Address = 0x1139)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F_Bit Mask [7]/ UDL Bit # 3 (C23)	F_Bit Mask [6]/ UDL Bit # 2 (C22)	F_Bit Mask [5]/ UDL Bit # 1 (C21)	F_Bit Mask [4]/X Bit # 2	F_Bit Mask [3]/ FEAC Bit (C13)	F_Bit Mask [2]/NA Bit (C12)	F_Bit Mask [1]/AIC Bit (C11)	F_Bit Mask [0]/X Bit # 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F Bit Mask[7]/UDL Bit # 3 (C23)	R/W	**Transmit F-Bit Error - Bit 8/UDL Bit # 3 (C23):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 8:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 8th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 8th F-bit. The results of this calculation will be written back into the 8th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for UDL Bit # 3 or C23 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit # 3 (or C23) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	F Bit Mask [6]/UDL Bit # 2 (C22)	R/W	**Transmit F-Bit Error - Bit 7/UDL Bit # 2 (C22):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 7:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 7th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 7th F-bit. The results of this calculation will be written back into the 7th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for UDL Bit # 2 or C22 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit # 2 (or C22) bit-fields, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	F Bit Mask [5]/UDL Bit # 1 (C21)	R/W	**Transmit F-Bit Error - Bit 6/UDL Bit # 1 (C21):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 6:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 6th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 6th F-bit. The results of this calculation will be written back into the 6th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for UDL Bit # 1 or C21 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the UDL Bit # 1 (or C21) bit-field, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	F Bit Mask [4]/X Bit # 2	R/W	**Transmit F-Bit Error - Bit 5/X Bit # 2:** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 5:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 5th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 5th F-bit. The results of this calculation will be written back into the 5th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for X Bit # 2:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the X-Bit # 2 bit-field, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	F Bit Mask [3]/FEAC Bit (C13)	R/W	**Transmit F-Bit Error - Bit 4/FEAC Bit (C13):** The exact function of this register bit depends upon the following parameters.· Whenever the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not.· Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 4:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 4th F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 4th F-bit. The results of this calculation will be written back into the 4th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for FEAC or C13 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the FEAC (or C13) bit-field, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	F Bit Mask [2]/NA Bit (C12)	R/W	**Transmit F-Bit Error - Bit 3/NA Bit (C12):** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 3:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 3rd F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 3rd F-bit. The results of this calculation will be written back into the 3rd F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for NA or C12 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the NA (or C12) bit-field, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	F Bit Mask [1]/AIC Bit (C11)	R/W	**Transmit F-Bit Error - Bit 2/AIC Bit (C11):** The exact function of this register bit depends upon the following parameters.· • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 2: This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 2nd F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 2nd F-bit. The results of this calculation will be written back into the 2nd F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for AIC or C11 bit:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the AIC (or C11) bit-field, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	F Bit Mask [0]/X Bit # 1	R/W	**Transmit F-Bit Error - Bit 1/X Bit # 1:** The exact function of this register bit depends upon the following parameters. • Whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, or not. • Whether Bit 7 (TxOHSrc), within the Test Register (Address = 0x110C) is set to "1" or "0". **If the XRT79L71 is NOT configured to operate in the Clear-Channel Framer Mode, OR if TxOHSrc = "0" - Transmit F-Bit Error - Bit 1:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit DS3 frames with an erred F bit. This F-bit corresponds with the 1st F-bit, within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and value of the 1st F-bit. The results of this calculation will be written back into the 1st F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, AND if TxOHSrc = "1" - Insert Enable for X Bit # 1:** This READ/WRITE bit-field permits the user to configure the Transmit Payload Data Input Interface block to externally accept an overhead bit and insert it into the X-Bit # 1 bit-field, within the outbound DS3 data-stream. 0 - Configures the Transmit Direction circuitry to externally accept and insert data into this overhead bit-field. 1- Configures the Transmit Direction circuitry to NOT externally accept and insert data into this overhead bit-field.

Transmit DS3 Pattern Register (Address = 0x114C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxAIS Unframed "All-Ones"	DS3 AIS Non-Stuck Stuff	Unused	TxLOS Pattern Select	Transmit_Idle_Pattern[3:0]			
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxAIS - Unframed "All-Ones"	R/W	**Transmit AIS - Unframed "All-Ones":** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit either of the following patterns, anytime it is configured to transmit the AIS indicator. **1.** A Framed, repeating "1, 0, 1, 0…" pattern (per Bellcore GR-499-CORE) or **2.** An Unframed "All-Ones" pattern. 0 - Configures the Transmit DS3 Framer block to transmit the Framed, Repeating "1, 0, 1, 0, …" pattern whenever it is configured to transmit the AIS indicator. 1- Configures the Transmit DS3 Framer block to transmit an Unframed, "All-Ones" pattern, whenever it is configured to transmit an AIS signal.
6	DS3 AIS-Non-Stuck Stuff	R/W	**DS3 AIS - Non-Stuck Stuff Option - AIS Pattern:** This READ/WRITE bit-field (along with the TxAIS - Unframed "All-Ones" bit-field) permits the user to define the type of AIS data-stream that the Transmit DS3 Framer block will transmit, as described below. 0 - Configures the Transmit DS3 Framer block to force all of the C bits to "0", when it is configured to transmit a Framed AIS signal. 1 - Configures the Transmit DS3 Framer block to NOT force all of the C bits to "0", when it is configured to transmit an Framed AIS signal. In this case, the C bits can be used to transport FEAC or PMDL messages. ***NOTE:*** *This bit-field is ignored if the Transmit DS3 Framer block has been configured to transmit an Unframed - "All-Ones" type of AIS signal.*
5	Unused	R/W	
4	TxLOS Pattern Select	R/W	**Transmit LOS Pattern Select:** This READ/WRITE bit-field permits the user to configure the Transmit DS3 Framer block to transmit either an "All Zeros" or an "All-Ones" pattern, anytime it is configured to transmit the LOS Pattern to the remote terminal equipment, as described below. 0 - Configures the Transmit DS3 Framer block to transmit an "All Zeros" pattern, whenever it is configured to transmit the LOS pattern. 1 - Configures the Transmit DS3 Framer block to transmit an "All-Ones" pattern, whenever it is configured to transmit the LOS pattern.
3 - 0	Tx_Idle Pattern[3:0]	R/W	**Transmit DS3 Idle Signal Pattern:** These READ/WRITE bit-fields permit the user to specify the type of framed, repetitive four-bit pattern that the Transmit DS3 Framer block should generate and transmit, whenever it is configured to transmit the "DS3 Idle" pattern. ***NOTE:*** *Setting these bit-fields to "[1, 1, 0, 0]" configures the Transmit DS3 Framer block to transmit the standard Framed, repeating "1, 1, 0, 0, …" pattern (per Bellcore GR-499-CORE) requirements.*

TRANSMIT E3, ITU-T G.751 RELATED REGISTERS

Transmit E3 Configuration Register - G.751 (Address = 0x1130)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxBIP-4 Enable	TxASrcSel[1:0]		TxNSrcSel[1:0]		TxAIS Enable	TxLOS Enable	TxFAS Source Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxBIP-4 Enable	R/W	**Transmit BIP-4 Enable:** This READ/WRITE bit-field permits the user to configure the Transmit E3 Framer block to do the following: **a.** To compute the BIP-4 value over a given E3 frame. **b.** To insert this BIP-4 value into the last nibble-field within the very next E3 frame. 0 - Does not configure this option. In this case, the last nibble of each Outbound E3 frame will contain payload data. 1 - Configures the Transmit E3 Framer block to compute and insert the BIP-4 value.
6 - 5	TxASrcSel[1:0]	R/W	**Transmit A Bit Source Select[1:0]:** These two READ/WRITE bit-fields permit the user to specify the source or type of data that is being carried via the A bits, within each Outbound E3 data stream, as indicated below.

TxASrcSel[1:0]		Resulting Source of A Bit
0	0	The "TxA" bit-field, within the "Transmit E3 Service Bit" register (Address = 0x1135).
0	1	Not Valid - Do not use
1	0	The "A" bit is sourced via the "Transmit Payload Data Input Interface" block. This is discussed in greater detail in Section _.
1	1	The Receive E3 Framer block. In this case, the A bit will transmit the FEBE indicator to the remote terminal equipment. The A bit will be set to "1" when the Receive E3 Framer block detects a BIP-4 error, and will be set to "0" when the Receive E3 Framer block detects un-erred E3 frames.

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>4 - 3</td><td>TxNSrcSel[1:0]</td><td>R/W</td><td>Transmit N Bit Source Select[1:0]:
These two READ/WRITE bit-fields permit the user to specify the source or type of data that is being carried via the N bits, within each Outbound E3 data stream, as indicated below.
<table>
<tr><th colspan="2">TxNSrcSel[1:0]</th><th>Resulting Source of A Bit</th></tr>
<tr><td>0</td><td>0</td><td>The "TxN" bit-field, within the "Transmit E3 Service Bit" register (Address = 0x1135).</td></tr>
<tr><td>0</td><td>1</td><td>Not Valid - Do not use</td></tr>
<tr><td>1</td><td>0</td><td>The Transmit LAPD Controller block In this case, the N bit, will function as the LAPD/ PMDL channel.</td></tr>
<tr><td>1</td><td>1</td><td>The "N" bit is sourced via the "Transmit Payload Data Input Interface" block.This is discussed in greater detail in Section _.</td></tr>
</table></td></tr>
<tr><td>2</td><td>TxAIS Enable</td><td>R/W</td><td>Transmit AIS Indicator:
This READ/WRITE bit-field permits the user to (by software control) force the Transmit E3 Framer block to generate and transmit the AIS indicator to the remote terminal equipment.
0 - Does not configure the Transmit E3 Framer block to generate and transmit the AIS indicator. In this case, the Transmit E3 Framer block will transmit normal E3 traffic.
1 - Configures the Transmit E3 Framer block to generate and transmit the AIS indicator. In this case, the Transmit E3 Framer block will force all bits (within the Outbound E3 data stream) to an Unframed "All-Ones" pattern.
NOTE: This bit-field is ignored if the Transmit E3 Framer block has been configured to transmit the LOS pattern.</td></tr>
<tr><td>1</td><td>TxLOS Enable</td><td>R/W</td><td>Transmit LOS (Pattern) Enable:
This READ/WRITE bit-field permits the user to (by software control) force the Transmit E3 Framer block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment, as described below.
0 - Does not configure the Transmit E3 Framer block to generate and transmit the LOS pattern. In this case, the Transmit E3 Framer block will be transmitting normal E3 traffic.
1 - Configures the Transmit E3 Framer block to generate and transmit the LOS pattern. In this case, the Transmit E3 Framer block will force all bits (within the Outbound E3 data stream) to an "All Zeros" pattern.</td></tr>
</table>

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	TxFAS Source Sel	R/W	**Transmit FAS Source Select:** This READ/WRITE bit-field permits the user to specify the source of the FAS (Framing Alignment Signal), to be used in the Outbound E3 data-stream, as indicated below. 0 - Configures the Transmit E3 Framer block to internally generate and insert the FAS bits within the outbound E3 data-stream. 1 - Configures the Transmit E3 Framer block to accept the FAS bits from "up-stream" circuitry (via the Transmit Payload Data Input Interface block) and to insert this data into the outbound E3 data-stream. This is discussed in greater detail in Section _.

Transmit E3 LAPD Configuration Register - G.751 (Address = 0x1133)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Auto Retransmit	Reserved	Transmit LAPD Message Length	Transmit LAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Auto Retransmit	R/W	**Auto-Retransmit of LAPD Message:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller block to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller block to transmit a given PMDL Message, the Transmit LAPD Controller block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. 0 - Disables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller block will transmit this PMDL Message will only be transmitted once, afterwards the Transmit LAPD Controller block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission. 1 - Enables the Auto-Retransmit Feature.In this case, the Transmit LAPD Controller block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. ***NOTE:*** *This bit-field is ignored if the Transmit LAPD Controller block is disabled.*
2	Reserved	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	TransmitLAPD Message Length	R/W	**Transmit LAPD Message Length Select:** This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below. 0 - Configures the Transmit LAPD Controller block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes. 1 - Configures the Transmit LAPD Controller block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes.
0	Transmit LAPD Enable	R/W	**Transmit LAPD Controller Block Enable:** This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller block, within the XRT79L71. Once the user enables the Transmit LAPD Controller block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the outbound DL bits, within each DS3 data stream. The Transmit LAPD Controller block will continue to do this until the user commands the Transmit LAPD Controller block to transmit a PMDL Message. 0 - Disables the Transmit LAPD Controller block. 1 - Enables the Transmit LAPD Controller block.

Transmit E3 LAPD Status/Interrupt Register - G.751 (Address = 0x1134)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Initiate Transmission of LAPD/PMDL Message	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Initiate Transmission of LAPD/PMDL Message	R/W	**Transmit LAPD Message Command:** A "0" to "1" transition, within this bit-field commands the Transmit LAPD Controller block to begin the following activities: • Reading out the contents of the Transmit LAPD Message Buffer.· Zero-Stuffing of this data • FCS Calculation and Insertion • Fragmentation of this composite PMDL Message, and insertion into the N bit-field, within each outbound E3 frame. ***NOTE:*** *This bit-field is only active if the Transmit LAPD Controller block has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Transmit LAPD Controller Busy	R/O	**Transmit LAPD Controller Busy Indicator:** This READ-ONLY bit-field indicates whether or not the Transmit LAPD Controller block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message. 0 - Indicates that the Transmit LAPD Controller block is NOT busy transmitting a PMDL Message. 1 - Indicates that the Transmit LAPD Controller block is currently busy transmitting a PMDL Message. ***NOTE:*** *This bit-field is only active if the Transmit LAPD Controller block has been enabled.*
1	Transmit LAPD Interrupt Enable	R/W	**Transmit LAPD Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit LAPD Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt anytime the Transmit LAPD Controller block has completed its transmission of a given LAPD/PMDL Message to the remote terminal. 0 - Disables Transmit LAPD Interrupt. 1 - Enables Transmit LAPD Interrupt.
0	Transmit LAPD Interrupt Status	RUR	**Transmit LAPD Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit LAPD Interrupt has occurred since the last read of this register. 0 - Transmit LAPD Interrupt has NOT occurred since the last read of this register. 1 - Transmit LAPD Interrupt has occurred since the last read of this register.

Transmit E3 Service Bits Register - G.751 (Address = 0x1135)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						TxA	TxN
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	TxA	R/W	**Transmit A Bit:** This READ/WRITE bit-field permits the user to control the state of the A bit, within each Outbound E3 frame, as indicated below. 0 - Forces each A bit (within the Outbound E3 frame) to "0". 1 - Forces each A bit (within the Outbound E3 frame) to "1". ***NOTE:*** *This bit-field is only valid if the Transmit E3 Framer block has been configured to use this bit-field as the source of the A bit (e.g., if TxASrcSel[1:0] = "0, 0").*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	TxN	R/W	**Transmit N Bit:** This READ/WRITE bit-field permits the user to control the state of the N bit, within each Outbound E3 frame, as indicated below. 0 - Forces each N bit (within the Outbound E3 frame) to "0". 1 - Forces each N bit (within the Outbound E3 frame) to "1". ***NOTE:*** *This bit-field is only valid if the Transmit E3 Framer block has been configured to use this bit-field as the source of the N bit (e.g., if TxNSrcSel[1:0] = "0, 0").*

Transmit E3 FAS Error Mask Upper Register - G.751 (Address = 0x1148)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxFAS_Error_Mask_Upper[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4 - 0	TxFAS_Error_Mask_Upper[4:0]	R/W	**TxFAS Error Mask Upper[4:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the upper five bits, within the FAS (Framing Alignment Signal), within the outbound E3 data stream. The Transmit E3 Framer block will perform an XOR operation with the contents of these FAS bits, and this register. The results of this calculation will be inserted into the upper 5 FAS bit positions within the Outbound E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FAS will be in error. ***NOTE:*** *For normal operation, the user should set this register to 0x00.*

Transmit E3 FAS Error Mask Lower Register - G.751 (Address = 0x1149)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxFAS_Error_Mask_Lower[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4 - 0	TxFAS_Error_Mask_Lower[4:0]	R/W	**TxFAS Error Mask Lower[4:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the lower five bits, within the FAS (Framing Alignment Signal), within the outbound E3 data stream. The Transmit E3 Framer block will perform an XOR operation with the contents of these FAS bits, and this register. The results of this calculation will be inserted into the lower 5 FAS bit positions within the Outbound E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FAS will be in error. ***NOTE:*** *For normal operation, the user should set this register to 0x00.*

Transmit E3 BIP-4 Mask Register - G.751 (Address = 0x114A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxBIP-4_Mask[3:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	TxBIP-4_Mask_[3:0]	R/W	**TxBIP-4 Error Mask[3:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the BIP-4 bits, within the outbound E3 data stream. The Transmit E3 Framer block will perform an XOR operation with the contents of the BIP-4 bits, and this register. The results of this calculation will be inserted into the BIP-4 bit positions within the Outbound E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the BIP-4 will be in error ***NOTE:*** *For normal operation, the user should set this register to 0x00.*

TRANSMIT E3, ITU-T G.832 RELATED REGISTERS

Transmit E3 Configuration Register - G.832 (Address = 0x1130)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	TxDL in NR	Reserved	TxAIS Enable	TxLOS Enable	TxMA Rx		
R/O	R/O	R/O	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	TxDL in NR	R/W	**Transmit DL (Data Link Channel) in NR Byte:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller block to use either the NR or the GC byte as the LAPD/PMDL channel, as described below. 0 - Configures the Transmit LAPD Controller block to transmit all Outbound LAPD/PMDL Messages via the GC byte. 1 - Configures the Transmit LAPD Controller block to transmit all Outbound LAPD/PMDL Messages via the NR byte.
3	Unused	R/O	
2	TxAIS Enable	R/W	**Transmit AIS Indicator:** This READ/WRITE bit-field permits the user to (by software control) force the Transmit E3 Framer block to generate and transmit the AIS indicator to the remote terminal equipment, as described below. 0 - Does not configure the Transmit E3 Framer block to generate and transmit the AIS indicator. In this case, the Transmit E3 Framer block will transmit normal E3 traffic. 1 - Configures the Transmit E3 Framer block to generate and transmit the AIS indicator. In this case, the Transmit E3 Framer will force all bits (within the Outbound E3 data stream) to an Unframed "All-Ones" pattern.N ***NOTE:*** *This bit-field is ignored if the Transmit E3 Framer block has been configured to transmit the LOS pattern.*
1	TxLOS Enable	R/W	**Transmit LOS (Pattern) Enable:** This READ/WRITE bit-field permits the user to (by software control) force the Transmit E3 Framer block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment. 0 - Does not configure the Transmit E3 Framer block to generate and transmit the LOS pattern. 1 - Configures the Transmit E3 Framer block to generate and transmit the LOS pattern. In this case, the Transmit E3 Framer block will force all bits (within the Outbound E3 data stream) to an "All Zeros" pattern.
0	TxMA Rx	R/W	**Transmit MA Byte from Receiver E3 Framer Block Select:** This READ/WRITE bit-field permits the user to configure the Transmit E3 Framer block to use either the Receive E3 Framer block or the Tx MA Byte Register as the source of the FERF/RDI and FEBE/REI bit-fields (within the MA byte-field of the Outbound E3 data stream), as indicated below. 0 - Configures the Transmit E3 Framer to read in the contents of the Transmit MA Byte register (Address = 0x1136), and write it into the MA byte-field within each Outbound E3 frame. ***NOTE:*** *This option permits the user to send FERF and FEBE indicators, under software control.* 1 - Configures the Transmit E3 Framer block to set the FERF and FEBE bit-fields to values, based upon conditions detected by the corresponding Receive E3 Framer block.

Transmit E3 LAPD Configuration Register - G.832 (Address = 0x1133)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Auto Retransmit	Reserved	Transmit LAPD Message Length	Transmit LAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Auto Retransmit	R/W	**Auto-Retransmit of LAPD Message:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller block to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller block to transmit a given PMDL Message, the Transmit LAPD Controller block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one second intervals. 0 - Disables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller block will only transmit this PMDL Message once. Afterwards the Transmit LAPD Controller block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via either the NR or GC bytes, within each output E3 frame. The Transmit LAPD Controller block will not transmit any more PMDL Messages until the user commands another transmission. 1 - Enables the Auto-Retransmit Feature.In this case, the Transmit LAPD Controller block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. ***NOTE:*** *This bit-field is ignored if the Transmit LAPD Controller block is disabled.*
2	Reserved	R/O	
1	Transmit LAPD Message Length	R/W	**Transmit LAPD Message Length Select:** This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below. 0 - Configures the Transmit LAPD Controller block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes. 1 - Configures the Transmit LAPD Controller block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes. ***NOTE:*** *This bit-field is ignored if the Transmit LAPD Controller block is disabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Transmit LAPD Enable	R/W	**Transmit LAPD Controller Block Enable:** This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller block, within the XRT79L71. Once the user enables the Transmit LAPD Controller block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via either the NR or the GC bytes, within the outbound E3 data stream. The Transmit LAPD Controller block will continue to do this until the user commands the Transmit LAPD Controller block to transmit a PMDL Message. 0 - Disables the Transmit LAPD Controller block. 1 - Enables the Transmit LAPD Controller block.

Transmit E3 LAPD Status/Interrupt Register - G.832 (Address = 0x1134)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Initiate Transmission of LAPD/PMDL Message	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Initiate Transmission of LAPD/PMDL Message	R/W	**Transmit LAPD Message Command:** A "0" to "1" transition, within this bit-field commands the Transmit LAPD Controller block to begin the following activities: • Reading out the contents of the Transmit LAPD Message Buffer.· • Zero-Stuffing of this data· FCS Calculation and Insertion • Fragmentation of this composite PMDL Message, and insertion into either the NR or GC byte-fields, within each outbound E3 frame. ***NOTE:*** *This bit-field is only active if the Transmit LAPD Controller block has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Transmit LAPD Controller Busy	R/O	**Transmit LAPD Controller Busy Indicator:** This READ-ONLY bit-field indicates whether or not the Transmit LAPD Controller block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message. 0 - Indicates that the Transmit LAPD Controller block is NOT busy transmitting a PMDL Message. 1 - Indicates that the Transmit LAPD Controller block is currently busy transmitting a PMDL Message. ***NOTE:*** *This bit-field is only active if the Transmit LAPD Controller block has been enabled.*
1	Transmit LAPD Interrupt Enable	R/W	**Transmit LAPD Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit LAPD Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt anytime the Transmit LAPD Controller block has completed its transmission of a given LAPD/PMDL Message to the remote terminal. 0 - Disables Transmit LAPD Interrupt. 1 - Enables Transmit LAPD Interrupt.
0	Transmit LAPD Interrupt Status	RUR	**Transmit LAPD Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit LAPD Interrupt has occurred since the last read of this register. 0 - Indicates that the Transmit LAPD Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Transmit LAPD Interrupt has occurred since the last read of this register.

Transmit E3 GC Byte Register - G.832 (Address = 0x1135)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxGC_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxGC_Byte[7:0]	R/W	**Transmit GC Byte:** This READ/WRITE bit-field permits the user to specify the contents of the GC byte, within the Outbound E3 data stream. The Transmit E3 Framer block will load the contents of this register in the GC byte-field, within each outbound E3 frame. This register is ignored if the GC byte is configured to be the LAPD/PMDL channel.

Transmit E3 MA Byte Register - G.832 (Address = 0x1136)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxMA Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxMA_Byte[7:0]	R/W	**Transmit MA Byte:** This READ/WRITE bit-field permits the user to specify the contents of the MA byte, within the Outbound E3 data stream. The Transmit E3 Framer block will load the contents of this register in the MA byte-field, within each outbound E3 frame. ***NOTES:*** *1. This register is ignored if the Transmit MA Byte - from Receiver option is selected (e.g., by setting TxMA Rx = "1".* *2. This feature permits the user to transmit FERF/RDI and FEBE/REI indicators upon software command.*

Transmit E3 NR Byte Register - G.832 (Address = 0x1137)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxNR_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxNR_Byte[7:0]	R/W	**Transmit NR Byte:** This READ/WRITE bit-field permits the user to specify the contents of the NR byte, within the Outbound E3 data stream. The Transmit E3 Framer block will load the contents of this register in the NR byte-field, within each outbound E3 frame. This register is ignored if the NR byte is configured to be the LAPD/PMDL channel.

Transmit E3 Trail-Trace - 0 Register - G.832 (Address = 0x1138)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_0[7:0]	R/W	**Transmit TTB (Trail-Trace Buffer) Byte 0:** These READ/WRITE bits permit the user to specify the contents of byte 0, within the Outbound Trail-Trace Message which is to be transmitted via the outbound E3 data stream. By default, the MSB (Most Significant Bit) of this register bit will be set to "1" in order to permit the remote terminal to be able to identify this particular byte, as being the first byte of the Trail-Trace Buffer Message.

Transmit E3 Trail-Trace - 1 Register - G.832 (Address = 0x1139)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_1[7:0]	R/W	**Transmit Trail-Trace Message - Byte 1:** These READ/WRITE bits permit the user to specify the contents of the second byte (Byte 1) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 2 Register - G.832 (Address = 0x113A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_2[7:0]	R/W	**Transmit Trail-Trace Message - Byte 2:** These READ/WRITE bits permit the user to specify the contents of the third byte (Byte 2) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 3 Register - G.832 (Address = 0x113B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_3[7:0]	R/W	**Transmit Trail-Trace Message - Byte 3:** These READ/WRITE bits permit the user to specify the contents of the fourth byte (Byte 3) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 4 Register - G.832 (Address = 0x113C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_4							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_4[7:0]	R/W	**Transmit Trail-Trace Message - Byte 4:** These READ/WRITE bits permit the user to specify the contents of the fifth byte (Byte 4) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

Transmit E3 Trail-Trace - 5 Register - G.832 (Address = 0x113D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_5							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_5[7:0]	R/W	**Transmit Trail-Trace Message - Byte 5:** These READ/WRITE bits permit the user to specify the contents of the sixth byte (Byte 5) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 6 Register - G.832 (Address = 0x113E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_6							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_6[7:0]	R/W	**Transmit Trail-Trace Message - Byte 6:** These READ/WRITE bits permit the user to specify the contents of the seventh byte (Byte 6) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 7 Register - G.832 (Address = 0x113F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_7							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_7[7:0]	R/W	**Transmit Trail-Trace Message - Byte 7:** These READ/WRITE bits permit the user to specify the contents of the eighth byte (Byte 7) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 8 Register - G.832 (Address = 0x1140)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_8							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_8[7:0]	R/W	**Transmit Trail-Trace Message - Byte 8:** These READ/WRITE bits permit the user to specify the contents of the ninth byte (Byte 8) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 9 Register - G.832 (Address = 0x1141)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_9							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_9[7:0]	R/W	**Transmit Trail-Trace Message - Byte 9:** These READ/WRITE bits permit the user to specify the contents of the tenth byte (Byte 9) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 10 Register - G.832 (Address = 0x1142)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_10							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_10[7:0]	R/W	**Transmit Trail-Trace Message - Byte 10:** These READ/WRITE bits permit the user to specify the contents of the eleventh byte (Byte 10) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 11 Register - G.832 (Address = 0x1143)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_11							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_11[7:0]	R/W	**Transmit Trail-Trace Message - Byte 11:** These READ/WRITE bits permit the user to specify the contents of the twelfth byte (Byte 11) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 12 Register - G.832 (Address = 0x1144)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_12							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_12[7:0]	R/W	**Transmit Trail-Trace Message - Byte 12:** These READ/WRITE bits permit the user to specify the contents of the 13th byte (Byte 12) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 13 Register - G.832 (Address = 0x1145)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_13							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_13[7:0]	R/W	**Transmit Trail-Trace Message - Byte 13:** hese READ/WRITE bits permit the user to specify the contents of the 14th byte (Byte 13) within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 14 Register - G.832 (Address = 0x1146)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_14							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_14[7:0]	R/W	**Transmit Trail-Trace Message - Byte 14:** These READ/WRITE bits permit the user to specify the contents of the 15th byte (Byte 14)within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 Trail-Trace - 15 Register - G.832 (Address = 0x1147)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_15							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxTTB_Byte_15[7:0]	R/W	**Transmit Trail-Trace Message - Byte 15:** These READ/WRITE bits permit the user to specify the contents of the 16th (and last) byte within the Trail-Trace Message that is to be transported via the outbound E3 data stream. ***NOTE:*** *In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".*

Transmit E3 FA1 Byte Error Mask Register - G.832 (Address = 0x1148)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFA1_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxFA1_Mask_Byte[7:0]	R/W	**TxFA1 Error Mask Byte[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the FA1 bytes, within the outbound E3 data stream. The Transmit E3 Framer block will perform an XOR operation with the contents of the FA1 byte, and this register. The results of this calculation will be inserted into the FA1 byte position within the Outbound E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FA1 byte will be in error. ***NOTE:*** *For normal operation, the user should set this register to 0x00.*

Transmit E3 FA2 Byte Error Mask Register - G.832 (Address = 0x1149)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFA2_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxFA2_Mask_Byte[7:0]	R/W	**TxFA2 Error Mask Byte[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the FA2 bytes, within the outbound E3 data stream. The Transmit E3 Framer block will perform an XOR operation with the contents of the FA2 byte, and this register. The results of this calculation will be inserted into the FA2 byte position within the Outbound E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FA2 byte will be in error. ***NOTE:*** *For normal operation, the user should set this register to 0x00.*

Transmit E3 BIP-8 Error Mask Register - G.832 (Address = 0x114A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxBIP-8_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxBIP-8_Mask_Byte[7:0]	R/W	**TxBIP-8 (B1) Error Mask[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound E3 data stream. The Transmit E3 Framer block will perform an XOR operation with the contents of the B1 byte, and this register. The results of this calculation will be inserted into the B1 byte position within the Outbound E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. For normal operation, the user should set this register to 0x00.

Transmit E3 SSM Register - G.832 (Address = 0x114B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxSSM Enable	Unused			TxSSM[3:0]			
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxSSM Enable	R/W	**Transmit SSM Enable:** This READ/WRITE bit-field permits the user to configure the Transmit E3 Framer block to operate in either the Old ITU-T G.832 Framing format or in the New ITU-T G.832 Framing format, as described below. 0 - Configures the Transmit E3 Framer block to support the Pre October 1998 version of the E3, ITU-T G.832 framing format. In this particular setting, the Transmit SSM Controller block will be disabled. 1 - Configures the Transmit E3 Framer block to support the October 1998 version of the E3, ITU-T G.832 framing format. In this particular setting, the Transmit SSM Controller block will be enabled.
6 - 4	Unused	R/O	
3 - 0	TxSSM[3:0]	R/W	**Transmit (or Outbound) Synchronization Status Message[3:0]:** These READ/WRITE bit-fields permit the user to specify the contents of the Outbound Synchronization Status Message (SSM) that is to be transported via the Outbound E3 data-stream. The Transmit SSM Controller block will then proceed to transport this SSM via the outbound E3 data-stream. ***NOTE:*** *These bit-fields are only active if Bit 7 (TxSSM Enable) within this register is set to "1".*

DS3/E3 FRAMER BLOCK PERFORMANCE MONITOR REGISTERS

A NOTE ABOUT READING OUT THE CONTENTS OF THE DS3/E3 FRAMER BLOCK PERFORMANCE MONITOR REGISTERS

These particular PMON Registers (below) are 16-bit RESET-upon-READ registers. However, the manner in which these PMON Registers are to be read is listed below.

As mentioned earlier, these PMON Registers are 16-bits in length. More specifically each of these PMON Registers will consist of a MSB (Most Significant Byte) 8-bit register, and a LSB (Least Significant Byte) register. Since the Microprocessor Interface of the XRT79L71 contains an eight-bit wide bi-directional data bus, the user will have to execute two consecutive read operations in order to obtain the full 16-bit content of a given PMON register. As the user reads out the contents of these PMON Registers, the user must be aware of the following restrictions.

- During the first (of the two) read operations (to a given PMON Register), the user can read out either the MSB or the LSB Register.
- However, as the user executes this first read operation, the entire 16-bit contents of this particular PMON register will be cleared to "0x0000". The XRT79L71 will store the contents of the un-read register into the PMON Holding Register (Address = 0x116C).
- Therefore, during the second (of the two) read operations (to a given PMON Register), the user MUST obtain the contents of the un-read byte, from the PMON Holding Register.
- This method for reading out the PMON Registers, applies to the following PMON Registers.
  - **a.** PMON Excessive Zero Count Registers
  - **b.** PMON Line Code Violation Count Registers
  - **c.** PMON Framing Bit/Byte Error Count Registers
  - **d.** PMON Parity/P-Bit Count Registers

e. PMON FEBE Event Count Registers

f. PMON CP-Bit Error Count Registers

g. PRBS Error Count Registers

- This method for reading out the DS3/E3 Framer PMON Register does not apply to the PLCP Processor, Transmit ATM Cell Processor or Receive ATM Cell Processor PMON registers.

PMON Excessive Zero Count Registers - MSB (Address = 0x114E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_EXZ_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_EXZ_Count_Upper_Byte[7:0]	RUR	**Performance Monitor - Excessive Zero Event Count - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON Excessive Zero Count Register - LSB combine to reflect the cumulative number of instances that a string of three or more consecutive zeros (for DS3 applications) or four or more consecutive zeros (for E3 applications) has been detected by the Receive DS3/E3 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

PMON Excessive Zero Count Registers - LSB (Address = 0x114F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_EXZ_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_EXZ_Count_Upper_Byte[7:0]	RUR	**Performance Monitor - Excessive Zero Event Count - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON Excessive Zero Count Register - MSB combine to reflect the cumulative number of instances that a string of three or more consecutive zeros (for DS3 applications) or four or more consecutive zeros (for E3 applications) has been detected by the Receive DS3/E3 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

PMON Line Code Violation Count Registers - MSB (Address = 0x1150)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_LCV_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON LCV Count Upper Byte[7:0]	RUR	**Performance Monitor- Line Code Violation Count Register - Upper Byte:** These RESET-upon-READ bits along with that within the PMON Line Code Violation Count - LSB combine to reflect the cumulative number of Line Code Violations that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

PMON Line Code Violation Count Registers - LSB (Address = 0x1151)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_LCV_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON LCV Count Lower Byte[7:0]	RUR	**Performance Monitor- Line Code Violation Count Register - Lower Byte:** These RESET-upon-READ bits along with that within the PMON Line Code Violation Count - MSB combine to reflect the cumulative number of Line Code Violations that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

PMON Framing Bit/Byte Error Count Register - MSB (Address = 0x1152)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Framing_Bit/Byte_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_Framing Bit/Byte Error_Count_Upper Byte[7:0]	RUR	**Performance Monitor - Framing Bit/Byte Error Count - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON Framing Bit/Byte Error Count Register - LSB combine to reflect the cumulative number of Framing bit (or byte) errors that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. ***NOTES:*** *1. For DS3 applications, this register will increment for each F or M bit error detected.* *2. For E3, ITU-T G.751 applications, this register will increment for each FAS error detected.* *3. For E3, ITU-T G.832 applications, this register will increment for each FA1 or FA2 byte error detected.*

PMON Framing Bit/Byte Error Count Register - LSB (Address = 0x1153)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Framing_Bit/Byte_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_Framing Bit/Byte Error_Count_Lower Byte[7:0]	RUR	**Performance Monitor - Framing Bit/Byte Error Count - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON Framing Bit/Byte Error Count Register - MSB combine to reflect the cumulative number of Framing bit (or byte) errors that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. ***NOTES:*** *1. For DS3 applications, this register will increment for each F or M bit error detected.* *2. For E3, ITU-T G.751 applications, this register will increment for each FAS error detected.* *3. For E3, ITU-T G.832 applications, this register will increment for each FA1 or FA2 byte error detected.*

PMON Parity/P-Bit Error Count Register - MSB (Address = 0x1154)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Parity_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_P-Bit/Parity Bit Error_Count_Upper Byte[7:0]	RUR	**Performance Monitor - P Bit/Parity Bit Error Count - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON P-Bit/Parity Bit Error Count Register - LSB combine to reflect the cumulative number of P bit errors (for DS3 applications) or BIP-8/BIP-4 errors (for E3 applications) that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

PMON Parity/P-Bit Error Count Register - LSB (Address = 0x1155)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Parity_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_P-Bit/Parity Bit Error_Count_Lower Byte[7:0]	RUR	**Performance Monitor - P Bit/Parity Bit Error Count - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON P-Bit/Parity Bit Error Count Register - MSB combine to reflect the cumulative number of P bit errors (for DS3 applications) or BIP-8/BIP-4 errors (for E3 applications) that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

PMON FEBE Event Count Register - MSB (Address = 0x1156)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_FEBE_Event_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_FEBE Event_Count_Upper Byte[7:0]	RUR	**Performance Monitor - FEBE Event Count - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON FEBE Event Count Register - LSB combine to reflect the cumulative number of erred FEBE events that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

PMON FEBE Event Count Register - LSB (Address = 0x1157)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_FEBE_Event_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_FEBE Event_Count_Lower Byte[7:0]	RUR	**Performance Monitor - FEBE Event Count - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON FEBE Event Count Register - MSB combine to reflect the cumulative number of erred FEBE events that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

PMON CP-Bit Error Count Register - MSB (Address = 0x1158)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_CP-Bit_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_CP-Bit Error_Count_Upper Byte[7:0]	RUR	**Performance Monitor - CP Bit Error Count - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON CP-Bit Error Count Register - LSB combine to reflect the cumulative number of CP bit errors that have been detected by the Receive DS3 Framer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. ***NOTE:*** *These register bits are only active if the XRT79L71 has been configured to operate in the DS3 C-Bit Parity Framing format.*

PMON CP-Bit Error Count Register - LSB (Address = 0x1159)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_CP-Bit_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_CP-Bit Error_Count_Lower Byte[7:0]	RUR	**Performance Monitor - CP Bit Error Count - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON CP-Bit Error Count Register - MSB combine to reflect the cumulative number of CP bit errors that have been detected by the Receive DS3 Framer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. **NOTE:** *These register bits are only active if the XRT79L71 has been configured to operate in the DS3 C-Bit Parity Framing Format.*

PLCP PROCESSOR BLOCK PERFORMANCE MONITOR REGISTERS

A NOTE ABOUT READING OUT THE CONTENTS OF THE PLCP PROCESSOR BLOCK PERFORMANCE MONITOR REGISTERS

These particular PMON Registers (below) are 16-bit RESET-upon-READ registers. However, the manner in which these PMON Registers are to be read is listed below.

As mentioned earlier, these PMON Registers are 16-bits in length. More specifically each of these PMON Registers will consist of a MSB (Most Significant Byte) 8-bit register, and a LSB (Least Significant Byte) register. Since the Microprocessor Interface of the XRT79L71 contains an eight-bit wide bi-directional data bus, the user will have to execute two consecutive read operations in order to obtain the full 16-bit content of a given PMON register. As the user reads out the contents of these PMON Registers, the user must be aware of the following restrictions.

- During the first (of the two) read operations (to a given PMON Register), the user MUST read out the MSB Register.
- During the second (of the two) read operations (to a given PMON Register), the user MUST read out the LSB Register.

NOTE: *In contrast to the DS3/E3 Framer Block PMON Registers, the PMON Holding Register is NOT used when reading out the PLCP Processor Block PMON Registers.*

- This method for reading out the PLCP Processor Block PMON Registers, applies to the following PMON Registers.
  - **a.** PMON PLCP BIP-8 Error Count Registers
  - **b.** PMON PLCP Framing Byte Error Count Registers
  - **c.** PMON PLCP FEBE Event Count Register

PMON PLCP BIP-8 Error Count Register - MSB (Address = 0x115A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_PLCP - BIP-8 Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_PLCP - BIP-8_Error_Count_Upper_Byte[7:0]	RUR	**Performance Monitor - PLCP BIP-8 Error Count Register - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON PLCP BIP-8 Error Count Register - LSB combine to reflect the cumulative number of PLCP BIP-8 bit errors that have been detected by the Receive PLCP Processor block, since the last reads of this register. This register contains the Most Significant byte of this 16-bit expression. ***NOTE:*** *These register bits are only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.*

PMON PLCP BIP-8 Error Count Register - LSB (Address = 0x115B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_PLCP - BIP-8 Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_PLCP - BIP-8_Error_Count_Lower_Byte[7:0]	RUR	**Performance Monitor - PLCP BIP-8 Error Count Register - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON PLCP BIP-8 Error Count Register - MSB combine to reflect the cumulative number of PLCP BIP-8 bit errors that have been detected by the Receive PLCP Processor block, since the last reads of this register. This register contains the Least Significant byte of this 16-bit expression. These register bits are only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.

PMON PLCP Framing Byte Error Count Register - MSB (Address = 0x115C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_PLCP - Framing Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_PLCP - Framing_Byte_Error_Count_Upper _Byte[7:0]	RUR	**Performance Monitor - PLCP Framing Byte Error Count Register - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON PLCP Framing Byte Error Count Register - LSB combine to reflect the cumulative number of PLCP Framing byte errors that have been detected by the Receive PLCP Processor block, since the last reads of this register. This register contains the Most Significant byte of this 16-bit expression. ***NOTE:*** *These register bits are only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.*

PMON PLCP Framing Byte Error Count Register - LSB (Address = 0x115D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_PLCP - Framing Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_PLCP - Framing_Byte_Error_Count_Upper _Byte[7:0]	RUR	**Performance Monitor - PLCP Framing Byte Error Count Register - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON PLCP Framing Byte Error Count Register - MSB combine to reflect the cumulative number of PLCP Framing byte errors that have been detected by the Receive PLCP Processor block, since the last reads of this register. This register contains the Least Significant byte of this 16-bit expression. ***NOTE:*** *These register bits are only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.*

PMON PLCP FEBE Event Count Register - MSB (Address = 0x115E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_PLCP - FEBE_Event_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_PLCP - FEBE_Event_Count_Upper _Byte[7:0]	RUR	**Performance Monitor - PLCP FEBE Event Count Register - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON PLCP FEBE Event Count Register - LSB combine to reflect the cumulative number of PLCP FEBE events that have been detected by the Receive PLCP Processor block, since the last reads of this register. This register contains the Most Significant byte of this 16-bit expression. ***NOTE:*** *These register bits are only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.*

PMON PLCP FEBE Event Count Register - LSB (Address = 0x115F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_PLCP - FEBE_Event_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_PLCP - FEBE_Event_Count_Lower _Byte[7:0]	RUR	**Performance Monitor - PLCP FEBE Event Count Register - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON PLCP FEBE Event Count Register - MSB combine to reflect the cumulative number of PLCP FEBE events that have been detected by the Receive PLCP Processor block, since the last reads of this register. This register contains the Least Significant byte of this 16-bit expression. These register bits are only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.

THE PRBS ERROR COUNT REGISTERS

A NOTE ABOUT READING OUT THE CONTENTS OF THE PRBS ERROR COUNT REGISTERS

The PRBS Error Count Registers (below) are 16-bit RESET-upon-READ registers. However, the manner in which these registers are to be read is listed below.

As mentioned earlier, these Registers are 16-bits in length. More specifically these registers will consist of a MSB (Most Significant Byte) 8-bit register, and a LSB (Least Significant Byte) register. Since the Microprocessor Interface of the XRT79L71 contains an eight-bit wide bi-directional data bus, the user will have to execute two consecutive read operations in order to obtain the full 16-bit contents of these PRBS Error Count Registers. As the user reads out the contents of these Registers, the user must be aware of the following restrictions.

- During the first (of the two) read operations (to the PRBS Error Count Registers), the user read out either the MSB or the LSB Register.
- However, as the user executes this first read operation, the entire 16-bit contents of this particular PRBS Error Count Register will be cleared to "0x0000". The XRT79L71 will store the contents of the un-read register into the PMON Holding Register (Address = 0x116C).

- Therefore, during the second (of the two) read operations (to the PRBS Error Count Register), the user MUST obtain the contents of the un-read byte, from the PMON Holding Register.

PRBS Error Count Register - MSB (Address = 0x1168)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PRBS Error_Count_Upper Byte[7:0]	RUR	**PRBS Error Count - Upper Byte:** These RESET-upon-READ bits, along with that within the PRBS Error Count Register - LSB combine to reflect the cumulative number of PRBS bit errors that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. ***NOTE:*** *These register bits are not active if the PRBS Receiver has not been enabled.*

PRBS Error Count Register - LSB (Address = 0x1169)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PRBS Error_Count_Lower Byte[7:0]	RUR	**PRBS Error Count - Lower Byte:** These RESET-upon-READ bits, along with that within the PRBS Error Count Register - MSB combine to reflect the cumulative number of PRBS bit errors that have been detected by the Receive DS3/E3 Framer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. ***NOTE:*** *These register bits are not active if the PRBS Receiver has not been enabled.*

PMON Holding Register (Address = 0x116C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Hold_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON Holding Value	R/O	**PMON Holding Value:** These READ-ONLY bit-fields were specifically allocated to support READ operations to the PMON (Performance Monitor) Registers, within the Receive DS3/E3 Framer block. Since the PMON Register (within the Receive DS3/E3 Framer block) are 16-bit registers. Therefore, given that the bi-directional data bus of the XRT79L71 is only 8-bits wide, it will require two read operations in order to read out the entire 16 bit content of these registers. The other thing to note is that the PMON Registers (within the DS3/E3 Framer blocks) are RESET-upon-READ type registers. As consequence, the entire 16-bit contents of a given PMON Register will be cleared to "0x0000" immediately after the user has executed the first (of two) read operations to this register. In order to avoid losing the contents of the other byte, the contents of the un-read byte is automatically loaded into this register. Hence, once the user reads a register, from a given PMON Register, the user is suppose to obtain the contents of the other byte, by reading the contents of this register.

One Second Error Status Register (Address = 0x116D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Errored Second	Severe Errored Second
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Errored Second	R/O	**Errored Second Indicator:** This READ-ONLY bit-field indicates whether or not the DS3/E3 Framer block has declared the last one-second accumulation period as a Errored Second. The DS3/E3 Framer block will declare a errored second if it detects any of the following events. **For DS3 Applications** • P-Bit Errors • CP Bit Errors • Framing Bit (F or M bit) Errors **For E3 Applications** • BIP-4/BIP-8 Errors • FAS or Framing Byte (FA1, FA2) Errors 0 - Indicates that the DS3/E3 Framer block has NOT declared the last one-second accumulation period as being an errored second. 1 - Indicates that the DS3/E3 Framer block has declared the last one-second accumulation period as being an errored second.
0	Severely Errored Second	R/O	**Severely Errored Second Indicator:** This READ-ONLY bit-field indicates whether or not the DS3/E3 Framer block has declared the last one second accumulation period as being a Severely Errored Second. The DS3/E3 Framer block will declare a given second as being a severely errored second if it determines that the BER (Bit Error Rate) during this One-second accumulation period is greater than 10^{-3} errors/second. 0 - Indicates that the DS3/E3 Framer block has not declared the last one-second accumulation period as being a severely-errored second. 1 - Indicates that the DS3/E3 Framer block has declared the last one-second accumulation period as being a severely-errored second.

One Second - LCV Count Accumulator Register - MSB (Address = 0x116E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_LCV_Count_Accum_MSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_LCV_Count Accum_LSB[7:0]	R/O	**One Second LCV Count Accumulator Register - MSB:** These READ-ONLY bits, along with that within the One Second LCV Count Accumulator Register - MSB combine to reflect the cumulative number of Line Code Violations that have been detected by the Receive DS3/E3 Framer block, in the last One second accumulation period. This register contains the Most Significant byte of this 16-bit expression.

One Second - LCV Count Accumulator Register - LSB (Address = 0x116F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_LCV_Count_Accum_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_LCV_Count Accum_LSB[7:0]	R/O	**One Second LCV Count Accumulator Register - LSB:** These READ-ONLY bits, along with that within the One Second LCV Count Accumulator Register - LSB combine to reflect the cumulative number of Line Code Violations that have been detected by the Receive DS3/E3 Framer block, in the last One second accumulation period. This register contains the Least Significant byte of this 16-bit expression.

One Second - Parity Error Accumulator Register - MSB (Address = 0x1170)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_Parity_Error_Accum_MSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_Parity Error Accum_MSB[7:0]	R/O	**One Second Parity Error Accumulator Register - MSB:** These READ-ONLY bits, along with that within the One Second Parity Error Accumulator Register - LSB combine to reflect the cumulative number of Parity Errors that have been detected by the Receive DS3/E3 Framer block, in the last One second accumulation period. This register contains the Most Significant byte of this 16-bit expression. ***NOTES:*** 1. *For DS3 applications, the register will reflect the number of P-bit errors, detected within the last One second accumulation period.* 2. *For E3, ITU-T G.751 applications, this register will reflect the number of BIP-4 errors, detected within the last One second accumulation period.* 3. *For E3, ITU-T G.832 applications, this register will reflect the number of BIP-8 (B1 Byte) errors detected within the last One second accumulation period.*

One Second - Parity Error Accumulator Register - LSB (Address = 0x1171)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_Parity_Error_Accum_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_Parity Error Accum_LSB[7:0]	R/O	**One Second Parity Error Accumulator Register - LSB:** These READ-ONLY bits, along with that within the One Second Parity Error Accumulator Register - MSB combine to reflect the cumulative number of Parity Errors that have been detected by the Receive DS3/E3 Framer block, in the last One second accumulation period. This register contains the Least Significant byte of this 16-bit expression. ***NOTES:*** 1. *For DS3 applications, the register will reflect the number of P-bit errors, detected within the last One second accumulation period.* 2. *For E3, ITU-T G.751 applications, this register will reflect the number of BIP-4 errors, detected within the last One second accumulation period.* 3. *For E3, ITU-T G.832 applications, this register will reflect the number of BIP-8 (B1 Byte) errors detected within the last One second accumulation period.*

One Second - CP Bit Error Accumulator Register - MSB (Address = 0x1172)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_CP_Bit_Error_Accum_MSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_CP Bit Error Accum_MSB[7:0]	R/O	**One Second CP Bit Error Accumulator Register - MSB:** These READ-ONLY bits, along with that within the One Second CP-Bit Error Accumulator Register - LSB combine to reflect the cumulative number of CP Bit Errors that have been detected by the Receive DS3 Framer block, in the last One second accumulation period. This register contains the Most Significant byte of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT79L71 has been configured to operate in the DS3, C-Bit Parity framing format.*

One Second - CP Bit Error Accumulator Register - LSB (Address = 0x1173)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_CP_Bit_Error_Accum_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_CP Bit Error Accum_LSB[7:0]	R/O	**One Second CP Bit Error Accumulator Register - LSB:** These READ-ONLY bits, along with that within the One Second CP-Bit Error Accumulator Register - MSB combine to reflect the cumulative number of CP Bit Errors that have been detected by the Receive DS3 Framer block, in the last One second accumulation period. This register contains the Least Significant byte of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT79L71 has been configured to operate in the DS3, C-bit Parity Framing format.*

LAPD CONTROLLER BYTE COUNT REGISTERS

Payload HDLC Control Register, Address = 0x1182

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framer By-Pass	HDLC Controller Enable	HDLC CRC-32	Unused	HDLC Loop-back	Unused		
R/W	R/W	R/W	R/O	R/W	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Framer By-Pass	R/W	

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	HDLC Controller Enable	R/W	**HDLC Controller Enable:** This READ/WRITE bit-field configures the XRT79L71 to operate in either the High-Speed HDLC Controller Mode, or in the Clear-Channel Framer Mode. If the user configures the XRT79L71 to operate in the High-Speed HDLC Controller Mode, then all of the following will be true. **In the Transmit Direction** Some of the Transmit Payload Data Input Interface pins will change function, and will present a byte-wide Transmit High-Speed HDLC Controller input interface to the System-Side Terminal Equipment. This Transmit High-Speed HDLC Controller input interface will also present the System-Side Terminal Equipment with a demand output clock signal (which is approximately one-eight of the either the E3 or DS3 rates, depending which rate is being used). This Transmit High-Speed HDLC Controller Input Interface will accept data (from the System-Side Terminal Equipment) in a byte-wide manner. As the Transmit High-Speed HDLC Controller Input Interface accepts this data, it will route this data to the Transmit High-Speed HDLC Controller block where it will encapsulate this data into a variable-length HDLC frame. The Transmit High-Speed HDLC Controller block will also take on the responsibility of zero-stuffing the payload data, within each of these outbound HDLC frames. Finally, the Transmit High-Speed HDLC Controller circuitry will optionally append either a CRC-32 or CRC-16 value to the back-end of any outbound HDLC frame. Anytime the System-Side Terminal Equipment is NOT providing any data to the Transmit High-Speed HDLC Controller Input Interface, then the Transmit High-Speed HDLC Controller block will generate a string of repeating Flag Sequence octets (0x7E), in order to (1) denote the boundaries of all outbound HDLC frames and (2) to indicate that no HDLC frames are currently being transported across the DS3/E3 transport medium. This composite outbound data-stream (consisting of HDLC frames and Flag Sequence octets) will be routed to the Transmit DS3/E3 Framer block. In this case, the Transmit DS3/E3 Framer block will insert this composite outbound data-stream into the payload bits within each outbound DS3 or E3 data-stream. **In the Receive Direction** In the Receive Direction, the Receive High-Speed HDLC Controller block will accept the payload data (within the incoming DS3/E3 data-stream) from the Receive DS3/E3 Framer block. As the Receive High-Speed HDLC Controller block receives this incoming data, it will perform the following functions. • It will flag any occurrence of the Flag Sequence octet, within the incoming data-stream.. • It will locate the boundaries of the incoming HDLC frames. • It will perform zero-unstuffing on the payload data (within each incoming HDLC frame). • It will compute and verify either the CRC-16 or CRC-32 value (that is appended at the back-end of the outbound HDLC Frame). • It will output this incoming HDLC data to the System-Side Terminal Equipment via a byte-wide output interface. 0 - Configures the XRT79L71 to operate in the Clear-Channel Framer Mode (e.g., disables the Transmit and Receive High-Speed HDLC Controller blocks). 1 - Configures the XRT79L71 to operate in the High-Speed HDLC Controller (e.g., enables the Transmit and Receive High-Speed HDLC Controller blocks).

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	HDLC CRC-32	R/W	**HDLC CRC-32:** This READ/WRITE bit-field permits the user to configure the Transmit and Receive High-Speed HDLC Controller blocks to handle either CRC-16 or CRC-32 values (at the back-end of each HDLC frame), as described below. **If configured to handle CRC-16 values** If the XRT79L71 is configured to handle CRC-16 Values then all of the following is true. • The Transmit High-Speed HDLC Controller block will compute and append a CRC-16 (2-byte) value to the back-end of each outbound HDLC frame. • The Receive High-Speed HDLC Controller block will compute and verify the CRC-16 value (which has been appended to the back-end) of each incoming HDLC frame. **If configured to handle CRC-32 values:** If the XRT79L71 is configured to handle CRC-32 Values then all of the following is true. • The Transmit High-Speed HDLC Controller block will compute and append a CRC-32 (4-byte) value to the back-end of each outbound HDLC frame. • The Receive High-Speed HDLC Controller block will compute and verify the CRC-32 value (which has been appended to the back-end) of each incoming HDLC frame. 0 - Configures the XRT79L71 to handle CRC-16 values. 1 - Configures the XRT79L71 to handle CRC-32 values. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode.*
4	Unused	R/O	
3	HDLC Loop-back	R/W	
2 - 0	Unused	R/O	

LAPD CONTROLLER BYTE COUNT REGISTERS

Transmit LAPD Byte Count Register (Address = 0x1183)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxLAPD_MESSAGE_SIZE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxLAPD_MESSAGE_SIZE[7:0]	R/W	**Transmit LAPD Message Size:** These READ/WRITE bit-fields permit the user to specify the size of the information payload (in terms of bytes) within the very next outbound LAPD/PMDL Message, whenever Bit 7 (TxLAPD Any) within the Transmit Tx LAPD Configuration Register has been set to "1".

Receive LAPD Byte Count Register (Address = 0x1184)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLAPD_MESSAGE_SIZE[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxLAPD_MESSAGE_SIZE[7:0]	R/O	**Receive LAPD Message Size:** These READ-ONLY bit-fields indicate the size of the most recently received LAPD/PMDL Message, whenever Bit 7 (RxLAPD Any) within the Rx LAPD Control Register has been set to "1". The contents of these register bits, reflects the Received LAPD Message size, in terms of bytes.

Receive PLCP Processor - Configuration and Status Register (Address = 0x1190)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					PLCP OOF Defect Declared	PLCP LOF Defect Declared	PLCP FERF/RAI Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	1	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 3	Unused	R/O	
2	PLCP OOF Defect Declared	R/O	**PLCP OOF (Out of Frame) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive PLCP Processor block is currently declaring the OOF (Out of Frame) defect condition, as described below. 0 - Indicates that the Receive PLCP Processor block is currently NOT declaring the PLCP OOF Defect Condition. 1 - Indicates that the Receive PLCP Processor block is currently declaring the PLCP OOF Defect Condition. ***NOTE:*** *This bit-field is ONLY ACTIVE if the XRT79L71 has been configured to operate in BOTH the ATM UNI and the PLCP Modes.*
1	PLCP LOF Defect Declared	R/O	**PLCP LOF (Loss of Frame) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive PLCP Processor block is currently declaring the LOF (Loss of Frame) defect condition, as described below. 0 - Indicates that the Receive PLCP Processor block is currently NOT declaring the PLCP LOF Defect Condition. 1 - Indicates that the Receive PLCP Processor block is currently declaring the PLCP LOF Defect Condition. ***NOTE:*** *This bit-field is ONLY ACTIVE if the XRT79L71 has been configured to operate in BOTH the ATM UNI and the PLCP Modes.*
0	PLCP FERF/RAI Defect Declared	R/O	**PLCP FERF/RAI Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive PLCP Processor block is currently declaring the FERF/RAI (Far-End Receive Failure/Remote Alarm Indicator) defect condition, as described below. 0 - Indicates that the Receive PLCP Processor block is currently NOT declaring the PLCP FERF/RAI Defect Condition. 1 - Indicates that the Receive PLCP Processor block is currently declaring the PLCP FERF/RAI Defect Condition. ***NOTE:*** *This bit-field is ONLY ACTIVE if the XRT79L71 has been configured to operate in BOTH the ATM UNI and the PLCP Modes.*

Receive PLCP Processor - Interrupt Enable Register (Address = 0x1191)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change in PLCP OOF Defect Condition Interrupt Enable	Change in PLCP LOF Defect Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	Change in PLCP OOF Defect Condition Interrupt Enable	R/W	**Change in PLCP OOF (Out of Frame) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in PLCP OOF Defect Condition Interrupt within the XRT79L71. If the user enables this particular interrupt, then the XRT79L71 will generate this interrupt, anytime any of the following conditions are met. **a.** Whenever the Receive PLCP Processor block declares the PLCP OOF defect condition. **b.** Whenever the Receive PLCP Processor block clears the PLCP OOF defect condition. The user can enable or disable the Change in PLCP OOF Defect Condition Interrupt, as described below. 0 - Disables the Change in PLCP OOF Defect Condition Interrupt. 1 - Enables the Change in PLCP OOF Defect Condition Interrupt. ***NOTE:*** *This bit-field is ONLY ACTIVE if the XRT79L71 has been configured to operate in BOTH the ATM UNI and the PLCP Modes.*
0	Change in PLCP LOF Defect Condition Interrupt	R/O	**Change in PLCP LOF (Loss of Frame) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in PLCP LOF Defect Condition Interrupt within the XRT79L71. If the user enables this particular interrupt, then the XRT79L71 will generate this interrupt, anytime any of the following conditions are met. **a.** Whenever the Receive PLCP Processor block declares the PLCP LOF defect condition. **b.** Whenever the Receive PLCP Processor block clears the PLCP LOF defect condition. The user can enable or disable the Change in PLCP LOF Defect Condition Interrupt, as described below. 0 - Disables the Change in PLCP LOF Defect Condition Interrupt. 1 - Enables the Change in PLCP LOF Defect Condition Interrupt. ***NOTE:*** *This bit-field is ONLY ACTIVE if the XRT79L71 has been configured to operate in BOTH the ATM UNI and the PLCP Modes.*

Receive PLCP Processor - Interrupt Status Register (Address = 0x1192)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change in PLCP OOF Defect Condition Interrupt Status	Change in PLCP LOF Defect Condition Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	Change in PLCP OOF Defect Condition Interrupt Status	RUR	**Change in PLCP OOF (Out of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in PLCP OOF Defect Condition Interrupt has occurred since the last read of this register, as described below. 0 - The Change in PLCP OOF Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - The Change in PLCP OOF Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is ONLY ACTIVE if the XRT79L71 has been configured to operate in BOTH the ATM UNI and the PLCP Modes.*
0	Change in PLCP LOF Defect Condition Interrupt Status	RUR	**Change in PLCP LOF (Loss of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change in PLCP LOF Defect Condition Interrupt has occurred since the last read of this register, as described below. 0 - The Change in PLCP LOF Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - The Change in PLCP LOF Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is ONLY ACTIVE if the XRT79L71 has been configured to operate in BOTH the ATM UNI and the PLCP Modes.*

Transmit PLCP Processor - A1 Byte Error Mask Register (Address = 0x1198)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxPLCP_A1_Byte_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	TxPLCP_A1_Byte_Mask[7:0]	R/W	**TxPLCP A1 Byte Error Mask Byte[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the A1 bytes, within the outbound PLCP data stream. The Transmit PLCP Processor block will perform an XOR operation with the contents of the A1 byte, and this register. The results of this calculation will be inserted into the A1 byte position within each outbound PLCP frame. For each bit-field (within this register) that is set to "1", the corresponding bit, within the A1 byte will be in error. ***NOTE:*** *For normal operation, the user should set this register to 0x00.*

Transmit PLCP Processor - A2 Byte Error Mask Register (Address = 0x1199)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxPLCP_A2_Byte_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	TxPLCP_A2_Byte_Mask[7:0]	R/W	**TxPLCP A2 Byte Error Mask Byte[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the A2 bytes, within the outbound PLCP data stream. The Transmit PLCP Processor block will perform an XOR operation with the contents of the A2 byte, and this register. The results of this calculation will be inserted into the A2 byte position within each outbound PLCP frame. For each bit-field (within this register) that is set to "1", the corresponding bit, within the A2 byte will be in error. ***NOTE:*** *For normal operation, the user should set this register to 0x00.*

Transmit PLCP Processor - B1 Byte Error Mask Register (Address = 0x119A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxPLCP_B1_Byte_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	TxPLCP_B1_Byte_Mask[7:0]	R/W	**TxPLCP B1 Byte Error Mask Byte[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound PLCP data stream. The Transmit PLCP Processor block will perform an XOR operation with the contents of the B1 byte, and this register. The results of this calculation will be inserted into the B1 byte position within each outbound PLCP frame. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. ***NOTE:*** *For normal operation, the user should set this register to 0x00.*

Transmit PLCP Processor - G1 Byte Control Register (Address = 0x119B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Force Tx PLCP FEBE to 0	Force PLCP FERF/RDI	LSS[2:0]		
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	Force TxPLCP FEBE to 0	R/W	**Force Transmit PLCP FEBE to 0:** This READ/WRITE bit-field permits the user to configure the Transmit PLCP Processor block to do either of the following. **a.** Generate and transmit PLCP FEBE values, based upon the number of B1 bit errors that are detected by the corresponding Receive PLCP Processor block. **b.** To set the PLCP FEBE bit-fields (within each outbound PLCP frame) to "[0, 0, 0, 0]. 0 - Configures the Transmit PLCP Processor block to generate and transmit PLCP FEBE based upon the number of B1 bit errors that have been detected by the corresponding Receive PLCP Processor block. 1 - Configures the Transmit PLCP Processor block to force the PLCP FEBE bits (within the G1 byte of each Outbound PLCP frame to [0, 0, 0, 0], independent of the number of B1 bit errors that have been detected by the Receive PLCP Processor block. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.*
3	Force PLCP FERF/RDI	R/W	**Force Transmit PLCP FERF/RDI:** This READ/WRITE bit-field permits the user to configure the Transmit PLCP Processor block to do either of the following. **a.** To generate and transmit the PLCP FERF/RDI indicator based upon defect conditions that are declared by the corresponding Receive PLCP Processor block. **b.** To force the transmission of the PLCP FERF/RDI indicator. (In this case, the Transmit PLCP Processor block will transmit the PLCP FERF/RDI indicator independent of the conditions that are being declared by the corresponding Receive PLCP Processor block). 0 - Configures the Transmit PLCP Processor block to generate and transmit the PLCP FERF/RDI indicator based upon defect conditions as declared by the corresponding Receive PLCP Processor block. 1 - Commands the Transmit PLCP Processor block to transmit the FERF/RDI indicator to the remote terminal. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in both the ATM UNI and PLCP Modes.*
2 - 0	LSS[2:0]	R/W	

LIU/JITTER ATTENUATOR CONTROL REGISTER BIT-FORMAT

LIU Transmit APS/Redundancy Control Register (Address = 0x1300)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							TxON
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 1	Reserved	R/O	0	
0	TxON	R/W	0	**Transmit Section ON:** This READ/WRITE bit-field permits the user to either turn on or turn off the Transmit Driver of XRT79L71. If the user turns on the Transmit Driver, then XRT79L71 will begin to transmit DS3 or E3 (on the line) via the TTIP and TRING output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP and TRING output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with XRT79L71 and tri-states the TTIP and TRING0 output pins. 1 - Turns on (or enables) the Transmit Driver associated the XRT79L71. ***NOTE:*** *If the user wishes to exercise software control over the state of the Transmit Driver of the XRT79L71, then it is imperative that the user pull the TxON (pin R15) to a logic "Low" level.*

LIU Interrupt Enable Register (Address = 0x1301)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change of FL Condition Interrupt Enable	Change of LOL Condition Interrupt Enable	Change of LOS Condition Interrupt Enable	Change of DMO Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 4	Reserved	R/O	0	

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
3	Change of FL Condition Interrupt Enable	R/W	0	**Change of FL (FIFO Limit Alarm) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of FL Condition Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt any time any of the following events occur. • Whenever the Jitter Attenuator (within XRT79L71) declares the FL (FIFO Limit Alarm) condition. • Whenever the Jitter Attenuator (within XRT79L71) clears the FL (FIFO Limit Alarm) condition. 0 - Disables the Change in FL Condition Interrupt. 1 - Enables the Change in FL Condition Interrupt.
2	Change of LOL Condition Interrupt Enable	R/W	0	**Change of Receive LOL (Loss of Lock) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of Receive LOL Condition Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within XRT79L71) declares the Loss of Lock Condition. • Whenever the Receive Section (within XRT79L71) clears the Loss of Lock Condition. 0 - Disables the Change in Receive LOL Condition Interrupt. 1 - Enables the Change in Receive LOL Condition Interrupt.
1	Change of LOS Condition Interrupt Enable	R/W	0	**Change of the Receive LOS (Loss of Signal) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of the Receive LOS Defect Condition Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within XRT79L71) declares the LOS Defect Condition. • Whenever the Receive Section (within XRT79L71) clears the LOS Defect condition. 0 - Disables the Change in the LOS Defect Condition Interrupt. 1 - Enables the Change in the LOS Defect Condition Interrupt.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
0	Change of DMO Condition Interrupt Enable	R/W	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change of Transmit DMO Condition Interrupt. If the user enables this interrupt, then the XRT79L71 will generate an interrupt any time any of the following events occur. • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "1". • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "0". 0 - Disables the Change in the DMO Condition Interrupt. 1 - Enables the Change in the DMO Condition Interrupt.

LIU Interrupt Status Register (Address = 0x1302)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change of FL Condition Interrupt Status	Change of LOL Condition Interrupt Status	Change of LOS Condition Interrupt Status	Change of DMO Condition Interrupt Status
R/O	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 4	Unused	R/O	0	
3	Change of FL Condition Interrupt Status	RUR	0	**Change of FL (Jitter Attenuator FIFO Limit Alarm) Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of FL Condition Interrupt has occurred since the last read of this register. 0 - Indicates that the Change of FL Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of FL Condition Interrupt has occurred since the last read of this register. ***NOTES:*** *1. 1.This bit-field is only active if the user has enabled the Jitter Attenuator within the XRT79L71.* *2. The user can determine the current state of the FIFO Alarm condition by reading out the contents of Bit 3 (FL Alarm Declared) within the Alarm Status Register.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
2	Change of LOL Condition Interrupt Status	RUR	0	**Change of Receive LOL (Loss of Lock) Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of Receive LOL Condition Interrupt has occurred since the last read of this register. 0 - Indicates that the Change of Receive LOL Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of Receive LOL Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Receive LOL Defect condition by reading out the contents of Bit 2 (Receive LOL Defect Declared) within the Alarm Status Register.*
1	Change of LOS Condition Interrupt Status	RUR	0	**Change of Receive LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of the Receive LOS Defect Condition Interrupt has occurred since the last read of this register. 0 - Indicates that the Change of the Receive LOS Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of the Receive LOS Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Receive LOS Defect condition by reading out the contents of Bit 1 (Receive LOS Defect Declared) within the Alarm Status Register.*
0	Change of DMO Condition Interrupt Status	RUR	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of the Transmit DMO Condition Interrupt has occurred since the last read of this register. 0 - Indicates that the Change of the Transmit DMO Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of the Transmit DMO Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Transmit DMO Condition by reading out the contents of Bit 0 (Transmit DMO Condition) within the Alarm Status Register.*

LIU Alarm Status Register (Address = 0x1303)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Digital LOS Defect Declared	Analog LOS Defect Declared	FL (FIFO Limit) Alarm Declared	Receive LOL Defect Declared	Receive LOS Defect Declared	Transmit DMO Condition
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	Digital LOS Defect Declared	R/O	0	**Digital LOS Defect Declared:** This READ-ONLY bit-field indicates whether or not the Digital LOS (Loss of Signal) detector (within the Receive DS3/E3 LIU Block) is declaring the LOS Defect condition. For DS3 application, the Digital LOS Detector (within the Receive DS3/E3 LIU Block) will declare the LOS Defect condition whenever it detects an absence of pulses (within the incoming DS3 data-stream) for 160 consecutive bit-periods. Further, (again for DS3 applications) the Digital LOS Detector will clear the LOS Defect condition whenever it determines that the pulse density (within the incoming DS3 signal) is at least 33%. 0 - Indicates that the Digital LOS Detector (within the Receive DS3/E3 LIU Block) is NOT declaring the LOS Defect Condition. 1 - Indicates that the Digital LOS Detector (within the Receive DS3/E3 LIU Block) is currently declaring the LOS Defect condition. ***NOTES:*** 1. *LOS Detection (within the Receive DS3/E3 LIU Block) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the LOS Defect Declare states of these two detectors.2.* 2. *The current LOS Defect Condition (per the Receive DS3/E3 LIU Block) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.* 3. *This particular bit-field reflects the LOS condition, as declared by the Receive DS3/E3 LIU Block. The Receive DS3/E3 Framer block also has its own LOS Defect Declare bit-field as well.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
4	Analog LOS Defect Declared	R/O	0	**Analog LOS Defect Declared:** This READ-ONLY bit-field indicates whether or not the Analog LOS (Loss of Signal) detector is declaring the LOS Defect condition. For DS3 application, the Analog LOS Detector (within the Receive DS3/E3 LIU Block) will declare the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3 line signal) drops below a certain Analog LOS Defect Declaration threshold level. Conversely, (again for DS3 application) the Analog LOS Detector will clear the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3 line signal) has risen above a certain Analog LOS Defect Clearance threshold level. It should be noted that, in order to prevent chattering within the Analog LOS Detector output, there is some built-in hysteresis between the Analog LOS Defect Declaration and the Analog LOS Defect Clearance threshold levels. 0 - Indicates that the Analog LOS Detector is NOT declaring the LOS Defect Condition. 1 - Indicates that the Analog LOS Detector is currently declaring the LOS Defect condition. ***NOTES:*** *1. LOS Detection (within the Receive DS3/E3 LIU Block) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of the Receive DS3/E3 LIU Block is simply a WIRED-OR of the LOS Defect Declare states of these two detectors.2.* *2. The current LOS Defect Condition (per the Receive DS3/E3 LIU Block) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
3	FL Alarm Declared	R/O	0	**FL (FIFO Limit) Alarm Declared:** This READ-ONLY bit-field indicates whether or not the Jitter Attenuator block (within the XRT79L71) is currently declaring the FIFO Limit Alarm. The Jitter Attenuator block will declare the FIFO Limit Alarm anytime the Jitter Attenuator FIFO comes within two bit-periods of either overflowing or under-running. Conversely, the Jitter Attenuator block will clear the FIFO Limit Alarm anytime the Jitter Attenuator FIFO is NO longer within two bit-periods of either overflowing or under-running. Typically, this Alarm will only be declared whenever there is a very serious problem with timing or jitter in the system. 0 - Indicates that the Jitter Attenuator block (within the XRT79L71) is NOT currently declaring the FIFO Limit Alarm condition. 1 - Indicates that the Jitter Attenuator block (within the XRT79L71) is currently declaring the FIFO Limit Alarm condition. ***NOTE:*** *This bit-field is only active if the Jitter Attenuator (within the XRT79L71) has been enabled.*
2	Receive LOL Condition Declared	R/O	0	**Receive LOL (Loss of Lock) Condition Declared:** This READ-ONLY bit-field indicates whether or not the Receive Section (within the XRT79L71) is currently declaring the LOL (Loss of Lock) condition. The Receive Section (of XRT79L71) will declare the LOL Condition, if any one of the following conditions is met. • If the frequency of the Recovered Clock signal differs from that of the signal provided to the E3CLK input (for E3 applications) or the DS3CLK input (for DS3 applications) by 0.5% (or 5000ppm) or more. • If the frequency of the Recovered Clock signal differs from the line-rate clock signal (for XRT79L71) that has been generated by the SFM Clock Synthesizer PLL (for SFM Mode Operation) by 0.5% (or 5000ppm) or more. 0 - Indicates that the Receive Section of XRT79L71 is NOT currently declaring the LOL Condition. 1 - Indicates that the Receive Section of XRT79L71 is currently declaring the LOL Condition.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	Receive LOS Defect Condition Declared	R/O	0	**Receive LOS (Loss of Signal) Defect Condition Declared:** This READ-ONLY bit-field indicates whether or not the Receive Section (within the XRT79L71) is currently declaring the LOS defect condition. The Receive Section (of XRT79L71) will declare the LOS defect condition, if any one of the following conditions is met. • If the Digital LOS Detector declares the LOS defect condition (for DS3 application)· If the Analog LOS Detector declares the LOS defect condition (for DS3 application) • If the ITU-T G.775 LOS Detector declares the LOS defect condition (for E3 application). 0 - Indicates that the Receive Section is NOT currently declaring the LOS Defect Condition. 1 - Indicates that the Receive Section is currently declaring the LOS Defect condition.
0	Transmit DMO Condition Declared	R/O	0	**Transmit DMO (Drive Monitor Output) Condition Declared:** This READ-ONLY bit-field indicates whether or not the Transmit Section is currently declaring the DMO Alarm condition. If configured accordingly, the Transmit Section will either internally or externally check the Transmit Output DS3/E3 Line signal for bipolar pulses via the TTIP and TRING output signals. If the Transmit Section were to detect no bipolar for 128 consecutive bit-periods, then it will declare the Transmit DMO Alarm condition. This particular alarm can be used to check for fault conditions on the Transmit Output Line Signal path. The Transmit Section will clear the Transmit DMO Alarm condition the instant that it detects some bipolar activity on the Transmit Output Line signal. 0 - Indicates that the Transmit Section of XRT79L71 is NOT currently declaring the Transmit DMO Alarm condition. 1 - Indicates that the Transmit Section of XRT79L71 is currently declaring the Transmit DMO Alarm condition.

LIU Transmit Control Register (Address = 0x1304)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Internal Transmit Drive Monitor	Unused		TAOS	Unused	TxLEV
R/O	R/O	R/W	R/O	R/O	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	Internal Transmit Drive Monitor	R/W	0	**Internal Transmit Drive Monitor Enable:** This READ/WRITE bit-field permits the user to configure the Transmit Section of XRT79L71 to either internally or externally monitor the TTIP and TRING output pins for bipolar pulses, in order to determine whether to declare the Transmit DMO Alarm condition. If the user configures the Transmit Section to externally monitor the TTIP and TRING output pins (for bipolar pulses) then the user must make sure that the user has connected the MTIP and MRING input pins to their corresponding TTIP and TRING output pins (via a 274 ohm series resistor). If the user configures the Transmit Section to internally monitor the TTIP and TRING output pins (for bipolar pulses) then the user does NOT need to make sure that the MTIP and MRING input pins are connected to the TTIP and TRING output pins (via series resistors). This monitoring will be performed right at the TTIP and TRING output pads. 0 - Configures the Transmit Drive Monitor to externally monitor the TTIP and TRING output pins for bipolar pulses. 1 - Configures the Transmit Drive Monitor to internally monitor the TTIP and TRING output pins for bipolar pulses.
4	Unused	R/O	0	
3	Unused	R/O	0	
2	TAOS	R/W	0	**Transmit "All-Ones" Pattern:** This READ/WRITE bit-field permits the user to command the Transmit DS3/E3 LIU Block, within the XRT79L71 to generate and transmit an unframed, "All-Ones" pattern via the DS3 or E3 line signal (to the remote terminal equipment). Whenever the user implements this configuration setting the Transmit DS3/E3 LIU Block will ignore the data that it is accepting from the Transmit DS3/E3 Framer block (as well as the upstream system-side terminal equipment) and overwrite this data with the "All-Ones" Pattern. 0 - Configures the Transmit DS3/E3 LIU Block to transmit the data that it accepts from the Transmit DS3/E3 Framer block. 1 - Configures the Transmit DS3/E3 Framer block to generate and transmit the Unframed, "All-Ones" pattern.
1	Unused	R/O	0	

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
0	TxLEV	R/W	0	**Transmit Line Build-Out Select:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit Line Build-Out (e.g., pulse-shaping) circuit within the Transmit DS3/E3 LIU Block. The user should set this bit-field to either "0" or to "1" based upon the following guidelines. 0 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is 225 feet or less. 1 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is 225 feet or more. The user must follow these guidelines in order to insure that the Transmit Transmit DS3/E3 Framer block (of XRT79L71) will always generate a DS3 pulse that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE. ***NOTE:*** *This bit-field is ignored if the XRT79L71 has been configured to operate in the E3 Mode.*

LIU Receive Control Register (Address = 0x1305)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Disable DLOS Detector	Disable ALOS Detector	Unused	LOSMUT Enable	Receive Monitor Mode Enable	Receive Equalizer Enable
R/O	R/O	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	Disable DLOS Detector	R/W	0	**Disable Digital LOS Detector:** This READ/WRITE bit-field permits the user to either enable or disable the Digital LOS (Loss of Signal) Detector within the Receive DS3/E3 LIU Block, of the XRT79L71, as described below. 0 - Enables the Digital LOS Detector within the Receive DS3/E3 LIU Block. ***NOTE:*** *This is the default condition.* 1 - Disables the Digital LOS Detector within the Receive DS3/E3 LIU Block. ***NOTE:*** *This bit-field is only active if XRT79L71 has been configured to operate in the DS3 Mode.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
4	Disable ALOS Detector	R/W	0	**Disable Analog LOS Detector:** This READ/WRITE bit-field permits the user to either enable or disable the Analog LOS (Loss of Signal) Detector within the Receive DS3/E3 LIU Block, as described below. 0 - Enables the Analog LOS Detector within Receive DS3/E3 LIU Block. ***NOTE:*** *This is the default condition).* 1 - Disables the Analog LOS Detector within Receive DS3/E3 LIU Block. ***NOTE:*** *This bit-field is only active if XRT79L71 has been configured to operate in the DS3 Modes.*
3	Unused	R/O	0	
2	LOSMUT Enable	R/W	0	**Muting (Recovered Data) upon LOS Enable:** This READ/WRITE bit-field permits the user to configure the Receive DS3/E3 LIU Block (within the XRT79L71) to automatically internally pull its Recovered Data Output pins (e.g., RPOS and RNEG) to GND anytime (and for the duration that) the Receive DS3/E3 LIU Block declares the LOS defect condition. In other words, this feature (if enabled) will cause the Receive DS3/E3 LIU Block to automatically mute the Recovered data (thst is being routed to the Receive DS3/E3 Framer Block) anytime (and for the duration that) the Receive DS3/E3 LIU Block declares the LOS defect condition. 0 - Disables the Muting upon LOS feature. In this setting the Receive DS3/E3 LIU Block will NOT automatically mute the Recovered Data whenever it is declaring the LOS defect condition. 1 - Enables the Muting upon LOS feature. In this setting the Receive DS3/E3 LIU Block will automatically mute the Recovered Data whenever it is declaring the LOS defect condition. ***NOTE:*** *Invoking the Muting upon LOS feature will NOT configure the Receive Payload Data Output Interface, Receive UTOPIA Interface or Receive POS-PHY Interface blocks to mute their outputs to the System-Side Terminal equipment. This setting only causes the Receive DS3/E3 LIU Block to internally mute its recovered data output (that it routes to the Receive DS3/E3 Framer block) whenever it (the Receive DS3/E3 LIU Block) declares the LOS defect condition.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	Receive Monitor Mode Enable	R/W	0	**Receive Monitor Mode Enable:** This READ/WRITE bit-field permits the user to configure the Receive DS3/E3 LIU Block of the XRT79L71 to operate in the Receive Monitor Mode. If the user configures the Receive DS3/E3 LIU Block to operate in the Receive Monitor Mode, then it will be able to receive a nominal DSX-3/STSX-1 signal that has been attenuator by 20dB of flat loss along with 6dB of cable loss, in an error-free manner, and without declaring the LOS defect condition. 0 - Configures the Receive DS3/E3 LIU Block to operate in the Normal Mode. 1 - Configure the Receive DS3/E3 LIU Block to operate in the Receive Monitor Mode.
0	Receive Equalizer Enable	R/W	0	**Receive Equalizer Enable - XRT79L71:** This READ/WRITE register bit permits the user to either enable or disable the Receive Equalizer block within the Receive DS3/E3 LIU Block of the XRT79L71, as listed below. 0 - Disables the Receive Equalizer within the Receive DS3/E3 LIU Block. 1 - Enables the Receive Equalizer within the Receive DS3/E3 LIU Block. ***NOTE:*** *For virtually all applications, we recommend that the user set this bit-field to "1" and enable the Receive Equalizer.*

LIU Channel Control Register (Address = 0x1306)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	SFM Clock Out Enable	SFM Enable	LIU Remote Loop-back Mode	LIU Local Loop-back Mode	Unused		
R/O	R/O	R/O	R/W	R/W	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7	Unused	R/O	0	

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
6	SFM Clock Out Enable	R/W	0	**Single-Frequency Mode - Clock Output Enable:** This READ/WRITE bit-field permits the user to either enable or disable the CLKOUT output pin (Ball K16) of the XRT79L71. If the CLKOUT output pin is enabled, then it will output a replicate of the Reference Clock signal that is currently being used by the Clock Recovery and Jitter Attenuator PLL's within the Receive DS3/E3 LIU Block. If the XRT79L71 is operating in the DS3 Mode, then a 44.736MHz clock signal will be output via the CLKOUT output pin. Conversely, if the XRT79L71 is operating in the E3 Mode, then a 34.368MHz clock signal will be output via the CLKOUT output pin. If the XRT79L71 has been configured to operate in the SFM (Single-Frequency) Mode, then the Reference Clock signal (that is ultimately synthesized by the SFM Synthesizer circuitry) will be output via the CLKOUT signal (if enabled). If the XRT79L71 has NOT been configured to operate in the SFM Mode, then the Receive DS3/E3 LIU Block will simply output a replicate of the signal that it is using as an internal reference. If the XRT79L71 is operating in the DS3 Mode, then the CLKOUT signal will ultimately be a buffered version of the clock signal being applied at the DS3CLK input pin. Likewise, if the XRT79L71 is operate in the E3 Mode, then the CLKOUT signal will ultimately be a buffered version of the clock signal being applied at the E3CLK input pin. ***NOTES:*** 1. *The user does not need to configure the Receive DS3/E3 LIU Block to operate in the SFM Mode, in order to enable the CLKOUT output pin.* 2. *The CLKOUT signal is NOT derived from the LIU Recovered Clock signal.*
5	SFM Enable	R/W	0	**Single-Frequency Mode Enable:** This READ/WRITE bit-field permits the user to configure the Receive DS3/E3 LIU Block (within the XRT79L71) to operate in the Single-Frequency Mode. If the user configures the Receive DS3/E3 LIU Block to operate in the Single-Frequency Mode, then all of the following will be true. • The user only needs to supply a 12.288MHz clock signal to the DS3CLK input pin (Ball P16). • The Receive DS3/E3 LIU Block will internally synthesize the appropriate reference clock signal for itself, depending whether it has been configured to operate in the DS3 or E3 Mode.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
4	RLB	R/W	0	**Loop-Back Select - RLB Bit:** This READ/WRITE bit-field along with the corresponding LLB bit-field permits the user to configure the XRT79L71 into any of the following loop-back modes. • Normal (No-Loop-back) Mode· • LIU Remote Loop-back Mode • LIU Analog Local Loop-back Mode· • LIU Digital Local Loop-back Mode The relationship between the settings for this input pin, the corresponding LLB bit-field and the resulting Loop-back Mode is presented below.
3	LLB	R/W	0	**Loop-Back Select - LLB Bit-field:** Please see the description (above) for RLB.
2 - 0	Unused	R/O	0	

LLB	RLB	Loop-back Mode
0	0	Normal (No Loop-back) Mode
0	1	LIU Remote Loop-back Mode
1	0	LIU Analog Local Loop-back Mode
1	1	LIU Digital Local Loop-back Mode

Jitter Attenuator Control Register (Address = 0x1307)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			DFL	Jitter Attenuator FIFO Pointer RESET	Jitter Attenuator PLL/FIFO Operating Mode - Bit 1	Jitter Attenuator in Transmit Path	Jitter Attenuator PLL/FIFO Operating Mode - Bit 0
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 5	Unused	R/O	0	

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
3	Jitter Attenuator FIFO Pointer RESET	R/W	0	**Jitter Attenuator RESET:** Writing a "0" to "1" transition within this bit-field will configure the Jitter Attenuator (within the XRT79L71) to execute a RESET operation. Whenever the user executes a RESET operation, then all of the following will occur. • The READ and WRITE pointers (within the Jitter Attenuator FIFO) will be reset to their default values. • The contents of the Jitter Attenuator FIFO will be flushed. ***NOTE:*** *The user must follow up any "0" to "1" transition with the appropriate write operate to set this bit-field back to "0", in order to resume normal operation with the Jitter Attenuator.*
2	Jitter Attenuator PLL/ FIFO Operating Mode - Bit 1	R/W	0	**Jitter Attenuator Configuration Select Input - Bit 1:** This READ/WRITE bit-field, along with Bit 0 (JA0) permits the user to do any of the following. • To enable or disable the Jitter Attenuator within the XRT79L71. • To select the FIFO Depth for the Jitter Attenuator within the XRT79L71. The relationship between the settings of these two bit-fields and the Enable/Disable States, and FIFO Depths is presented below.
1	Jitter Attenuator in Transmit Path	R/W	0	**Jitter Attenuator in Transmit/Receive Path Select Bit:** This input pin permits the user to configure the Jitter Attenuator (within the XRT79L71) to operate in either the Transmit or Receive path, as described below. 0 - Configures the Jitter Attenuator (e.g., within the Receive DS3/E3 LIU Block) to operate in the Receive Path. 1 - Configures the Jitter Attenuator (e.g., within the Receive DS3/E3 LIU Block) to operate in the Transmit Path.
0	Jitter Attenuator PLL/ FIFO Operating Mode - Bit 0	R/W	0	**Jitter Attenuator Configuration Select Input - Bit 0:** Please see the description for Bit 2 (JA1) within this Register.

JA0	JA1	Jitter Attenuator Mode
0	0	Enabled FIFO Depth = 16 bits
0	1	Enabled FIFO Depth = 32 bits
1	0	Disabled
1	1	Disabled

LIU Receive APS/Redundancy Control Register (Address = 0x1308)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							RxON
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 1	Reserved	R/O	0	
0	RxON	R/W	0	**Receiver Section ON - XRT79L71:** This READ/WRITE bit-field permits the user to either turn on or turn off the Receive Section of XRT79L71. If the user turns on the Receive Section, then XRT79L71 will begin to receive the incoming DS3 or E3 data-stream via the RTIP and RRING input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section (e.g., AGC and Receive Equalizer Block, Clock Recovery PLL, etc) will be powered down. 0 - Shuts off the Receive Section of XRT79L71. 1 - Turns on the Receive Section of XRT79L71.

RECEIVE ATM CELL PROCESSOR BLOCK REGISTERS (ATM APPLICATIONS)

THE RECEIVE ATM CELL PROCESSOR BLOCK

This section presents the Register Description/Address Map of the control registers associated with the Receive ATM Cell Processor block.

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0x1700	Receive ATM Control - Receive ATM Control Register - Byte 3	R/W	0x00
0x1701	Receive ATM Control - Receive ATM Control Register - Byte 2	R/W	0x00
0x1702	Receive ATM Control - Receive ATM Control Register - Byte 1	R/W	0x00
0x1703	Receive ATM Cell/PPP Control - Receive ATM Control Register - Byte 0	R/W	0x00
0x1704 - 0x1706	Reserved	R/O	0x00
0x1707	Receive ATM Status Register- -1	R/O	0x00
0x1708 - 0x1709	Reserved	R/O	0x00
0x170A	Receive ATM Interrupt Status Register - Byte 1	RUR	0x00
0x170B	Receive ATM Cell/PPP Processor Interrupt Status Register - Byte 0	RUR	0x00
0x170C - 0x170D	Reserved	R/O	0x00
0x170E	Receive ATM Cell Processor Block Interrupt Enable Register - Byte 1	R/W	0x00
0x170F	Receive ATM Cell/PPP Processor Block Interrupt Enable Register - Byte 0	R/W	0x00
0x1710	Receive PPP Processor - Receive Good PPP Packet Count Register - Byte 3	RUR	0x00
0x1711	Receive PPP Processor - Receive Good PPP Packet Count Register - Byte 2	RUR	0x00
0x1712	Receive PPP Processor - Receive Good PPP Packet Count Register - Byte 1	RUR	0x00
0x1713	Receive ATM Cell Insertion/Extraction Memory Control Register Receive PPP Processor - Receive Good PPP Packet Count Register - Byte 0	R/W or RUR	0x00
0x1714	Receive ATM Cell Insertion/Extraction Memory Data Register - Byte 3 Receive PPP Processor - Receive FCS Error Count Register - Byte 3	R/W or RUR	0x00
0x1715	Receive ATM Cell Insertion/Extraction Memory Data Register - Byte 2 Receive PPP Processor - Receive FCS Error Count Register - Byte 2	R/W or RUR	0x00
0x1716	Receive ATM Cell Insertion/Extraction Memory Data Register - Byte 1 Receive PPP Processor - Receive FCS Error Count Register - Byte 1	R/W or RUR	0x00
0x1717	Receive ATM Cell Insertion/Extraction Memory Data Register - Byte 0 Receive PPP Processor - Receive FCS Error Count Register - Byte 0	R/W or RUR	0x00
0x1718	Receive ATM Programmable User Defined Field Register - Byte 3 Receive PPP Processor - Receive ABORT Count Register - Byte 3	R/W or RUR	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0x1719	Receive ATM Programmable User Defined Field Register - Byte 2 Receive PPP Processor - Receive ABORT Count Register - Byte 2	R/W or RUR	0x00
0x171A	Receive ATM Programmable User Defined Field Register - Byte 1 Receive PPP Processor - Receive ABORT Count Register - Byte 1	R/W or RUR	0x00
0x171B	Receive ATM Programmable User Defined Field Register - Byte 0 Receive PPP Processor - Receive ABORT Count Register - Byte 0	R/W or RUR	0x00
0x171C	Receive PPP Processor - Receive RUNT PPP Count Register - Byte 3	RUR	0x00
0x171D	Receive PPP Processor - Receive RUNT PPP Count Register - Byte 2	RUR	0x00
0x171E	Receive PPP Processor - Receive RUNT PPP Count Register - Byte 1	RUR	0x00
0x171F	Receive PPP Processor - Receive RUNT PPP Count Register - Byte 0	RUR	0x00
0x1720	Receive ATM Controller - Test Cell Header - Byte 1	R/W	0x00
0x1721	Receive ATM Controller - Test Cell Header - Byte 2	R/W	0x00
0x1722	Receive ATM Controller - Test Cell Header - Byte 3	R/W	0x00
0x1723	Receive ATM Controller - Test Cell Header - Byte 4	R/W	0x00
0x1724	Receive ATM Controller - Test Cell Error Counter - Byte 3	RUR	0x00
0x1725	Receive ATM Controller - Test Cell Error Counter - Byte 2	RUR	0x00
0x1726	Receive ATM Controller - Test Cell Error Counter - Byte 1	RUR	0x00
0x1727	Receive ATM Controller - Test Cell Error Counter - Byte 0	RUR	0x00
0x1728	Receive ATM Controller - Receive ATM Cell Count - Byte 3	RUR	0x00
0x1729	Receive ATM Controller - Receive ATM Cell Count - Byte 2	RUR	0x00
0x172A	Receive ATM Controller - Receive ATM Cell Count - Byte 1	RUR	0x00
0x172B	Receive ATM Controller - Receive ATM Cell Count - Byte 0	RUR	0x00
0x172C	Receive ATM Controller - Receive ATM Discard Cell Count - Byte 3	RUR	0x00
0x172D	Receive ATM Controller - Receive ATM Discard Cell Count - Byte 2	RUR	0x00
0x172E	Receive ATM Controller - Receive ATM Discard Cell Count - Byte 1	RUR	0x00
0x172F	Receive ATM Controller - Receive ATM Discard Cell Count - Byte 0	RUR	0x00
0x1730	Receive ATM Controller - Receive ATM Correctable HEC Cell Counter - Byte 3	RUR	0x00
0x1731	Receive ATM Controller - Receive ATM Correctable HEC Cell Counter - Byte 2	RUR	0x00
0x1732	Receive ATM Controller - Receive ATM Correctable HEC Cell Counter - Byte 1	RUR	0x00
0x1733	Receive ATM Controller - Receive ATM Correctable HEC Cell Counter - Byte 0	RUR	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0x1734	Receive ATM Controller - Receive ATM Uncorrectable HEC Cell Counter - Byte 3	RUR	0x00
0x1735	Receive ATM Controller - Receive ATM Uncorrectable HEC Cell Counter - Byte 2	RUR	0x00
0x1736	Receive ATM Controller - Receive ATM Uncorrectable HEC Cell Counter - Byte 1	RUR	0x00
0x1737	Receive ATM Controller - Receive ATM Uncorrectable HEC Cell Counter - Byte 0	RUR	0x00
0x1738 - 0x1742	Reserved	R/O	0x00
0x1743	Receive ATM Controller - Receive ATM Filter # 0 Control Register	R/W	0x00
0x1744	Receive ATM Controller - Receive ATM Filter # 0 Pattern - Header Byte 1	R/W	0x00
0x1745	Receive ATM Controller - Receive ATM Filter # 0 Pattern - Header Byte 2	R/W	0x00
0x1746	Receive ATM Controller - Receive ATM Filter # 0 Pattern - Header Byte 3	R/W	0x00
0x1747	Receive ATM Controller - Receive ATM Filter # 0 Pattern - Header Byte 4	R/W	0x00
0x1748	Receive ATM Controller - Receive ATM Filter # 0 Check - Header Byte 1	R/W	0x00
0x1749	Receive ATM Controller - Receive ATM Filter # 0 Check - Header Byte 2	R/W	0x00
0x174A	Receive ATM Controller - Receive ATM Filter # 0 Check - Header Byte 3	R/W	0x00
0x174B	Receive ATM Controller - Receive ATM Filter # 0 Check - Header Byte 4	R/W	0x00
0x174C	Receive ATM Controller - Filter # 0 - Filtered Cell Count Register - Byte 3	R/W	0x00
0x174D	Receive ATM Controller - Filter # 0 - Filtered Cell Count Register - Byte 2	R/W	0x00
0x174E	Receive ATM Controller - Filter # 0 - Filtered Cell Count Register - Byte 1	R/W	0x00
0x174F	Receive ATM Controller - Filter # 0 - Filtered Cell Count Register - Byte 0	R/W	0x00
0x1750 - 0x1752	Reserved	R/O	0x00
0x1753	Receive ATM Controller - Receive ATM Filter # 1 Control Register	R/W	0x00
0x1754	Receive ATM Controller - Receive ATM Filter # 1 Pattern - Header Byte 1	R/W	0x00
0x1755	Receive ATM Controller - Receive ATM Filter # 1 Pattern - Header Byte 2	R/W	0x00
0x1756	Receive ATM Controller - Receive ATM Filter # 1 Pattern - Header Byte 3	R/W	0x00
0x1757	Receive ATM Controller - Receive ATM Filter # 1 Pattern - Header Byte 4	R/W	0x00
0x1758	Receive ATM Controller - Receive ATM Filter # 1 Check - Header Byte 1	R/W	0x00
0x1759	Receive ATM Controller - Receive ATM Filter # 1 Check - Header Byte 2	R/W	0x00
0x175A	Receive ATM Controller - Receive ATM Filter # 1 Check - Header Byte 3	R/W	0x00
0x175B	Receive ATM Controller - Receive ATM Filter # 1 Check - Header Byte 4	R/W	0x00
0x175C	Receive ATM Controller - Filter # 1 - Filtered Cell Count Register - Byte 3	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0x175D	Receive ATM Controller - Filter # 1 - Filtered Cell Count Register - Byte 2	R/W	0x00
0x175E	Receive ATM Controller - Filter # 1 - Filtered Cell Count Register - Byte 1	R/W	0x00
0x175F	Receive ATM Controller - Filter # 1 - Filtered Cell Count Register - Byte 0	R/W	0x00
0x1760 - 0x1762	Reserved	R/O	0x00
0x1763	Receive ATM Controller - Receive ATM Filter # 2 Control Register	R/W	0x00
0x1764	Receive ATM Controller - Receive ATM Filter # 2 Pattern - Header Byte 1	R/W	0x00
0x1765	Receive ATM Controller - Receive ATM Filter # 2 Pattern - Header Byte 2	R/W	0x00
0x1766	Receive ATM Controller - Receive ATM Filter # 2 Pattern - Header Byte 3	R/W	0x00
0x1767	Receive ATM Controller - Receive ATM Filter # 2 Pattern - Header Byte 4	R/W	0x00
0x1768	Receive ATM Controller - Receive ATM Filter # 2 Check - Header Byte 1	R/W	0x00
0x1769	Receive ATM Controller - Receive ATM Filter # 2 Check - Header Byte 2	R/W	0x00
0x176A	Receive ATM Controller - Receive ATM Filter # 2 Check - Header Byte 3	R/W	0x00
0x176B	Receive ATM Controller - Receive ATM Filter # 2 Check - Header Byte 4	R/W	0x00
0x176C	Receive ATM Controller - Filter # 2 - Filtered Cell Count Register - Byte 3	R/W	0x00
0x176D	Receive ATM Controller - Filter # 2 - Filtered Cell Count Register - Byte 2	R/W	0x00
0x176E	Receive ATM Controller - Filter # 2 - Filtered Cell Count Register - Byte 1	R/W	0x00
0x176F	Receive ATM Controller - Filter # 2 - Filtered Cell Count Register - Byte 0	R/W	0x00
0x1770 - 0x1772	Reserved	R/O	0x00
0x1773	Receive ATM Controller - Receive ATM Filter # 3 Control Register	R/W	0x00
0x1774	Receive ATM Controller - Receive ATM Filter # 3 Pattern - Header Byte 1	R/W	0x00
0x1775	Receive ATM Controller - Receive ATM Filter # 3 Pattern - Header Byte 2	R/W	0x00
0x1776	Receive ATM Controller - Receive ATM Filter # 3 Pattern - Header Byte 3	R/W	0x00
0x1777	Receive ATM Controller - Receive ATM Filter # 3 Pattern - Header Byte 4	R/W	0x00
0x1778	Receive ATM Controller - Receive ATM Filter # 3 Check - Header Byte 1	R/W	0x00
0x1779	Receive ATM Controller - Receive ATM Filter # 3 Check - Header Byte 2	R/W	0x00
0x177A	Receive ATM Controller - Receive ATM Filter # 3 Check - Header Byte 3	R/W	0x00
0x177B	Receive ATM Controller - Receive ATM Filter # 3 Check - Header Byte 4	R/W	0x00
0x177C	Receive ATM Controller - Filter # 3 - Filtered Cell Count Register - Byte 3	R/W	0x00
0x177D	Receive ATM Controller - Filter # 3 - Filtered Cell Count Register - Byte 2	R/W	0x00
0x177E	Receive ATM Controller - Filter # 3 - Filtered Cell Count Register - Byte 1	R/W	0x00
0x177F	Receive ATM Controller - Filter # 3 - Filtered Cell Count Register - Byte 0	R/W	0x00

RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
RECEIVE ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0x1780 - 0x1901	Reserved	R/O	0x00

Receive ATM Cell Processor Block - Receive ATM Control Register - Byte 2 (Address = 0x1701)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Receive ATM Cell Processor Enable	Test Cell Receiver Mode Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	Receive ATM Cell Processor Enable	R/W	**Receive ATM Cell Processor Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive ATM Cell Processor block. To operate the XRT79L71 in the ATM Mode, enable the Receive ATM Cell Processor block. 0 - Disables the Receive ATM Cell Processor block. 1 - Enables the Receive ATM Cell Processor block.
0	Test Cell Receiver Mode Enable	R/W	**Test Cell Receiver Mode Enable:** This READ/WRITE bit-field permits the user to enable the Test Cell Receiver (within the Receive ATM Cell Processor block). The user must implement this configuration option in order to perform diagnostic operations with Test Cells. 0 - Disables the Test Cell Receiver. 1 - Enables the Test Cell Receiver. ***NOTE:*** *For normal operation, the user should set this bit-field to "0".*

Receive ATM Cell Processor Block - Receive ATM Control Register - Byte 1 (Address = 0x1702)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			GFC Extraction Enable	HEC Byte Correction Enable	Uncorrectable HEC Byte Error Retain	COSET Polynomial Addition	Regenerate HEC Byte Enable
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	GFC Extraction Enable	R/W	**GFC (Generic Flow Control) Extraction Enable:** This READ/WRITE bit-field permits the user to configure the Receive ATM Cell Processor block to output the contents of the GFC Nibble (within each incoming ATM Cell) via the Receive GFC Value Output port. 0 - Configures the Receive ATM Cell Processor block to NOT output the contents of the GFC Nibble (within each incoming ATM cell) via the Receive GFC Value Output port. 1 - Configures the Receive ATM Cell Processor block to output the contents of the GFC Nibble (within each incoming ATM cell) via the Receive GFC Value Output port.
3	HEC Byte Correction Enable	R/W	**HEC Byte Correction Enable:** This READ/WRITE bit-field permits the user to enable Correction Mode operation for the Receive ATM Cell Processor block. If the user implements this configuration option, then the Receive ATM Cell Processor block will transition into either the Correction Mode or the Detection Mode (as Receive Conditions warrant). If the Receive ATM Cell Processor block is operating in the Correction Mode then it will correct any cells that contain Single-Bit Header byte errors. In contrast, if the Receive ATM Cell Processor block is operating in the Detection Mode, then it will unconditionally discard any cells that contain Header byte errors (Single-Bit or Multi-Bit errors). If the user does not implement this feature, then the Receive ATM Cell Processor block will only be capable of operating in the Detection Mode. 0 - Disables the Correction Mode. In this setting, the Receive ATM Cell Processor block will only operate in the Detection Mode. 1 - Enables the Correction Mode. In this setting, the Receive ATM Cell Processor block will transition into and out of the Correction Mode or Detection Mode as receive conditions warrant.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Uncorrectable HEC Byte Retain	R/W	**Uncorrectable HEC Byte Retain:** This READ/WRITE bit-field permits the user to configure the Receive ATM Cell Processor block to either automatically discard or retain all incoming ATM cells that contain uncorrectable HEC byte errors. If the user implements this feature, then the Receive ATM Cell Processor block will automatically retain any cells that fit into any one of the following categories. • ATM cells that contain multi-bit HEC byte errors. • ATM cells that contain single-bit HEC byte errors, while the Receive ATM Cell Processor block is operating in the Detection Mode. If the user does NOT implement this feature, then the Receive ATM Cell Processor block will automatically discard any cells that fit into any one of the above-mentioned categories. These cells (along with un-erred or cells with correctable HEC byte errors) will be retains for further processing. 0 - Configures the Receive ATM Cell Processor block to automatically discard ALL incoming ATM cells that contain "uncorrectable" HEC byte errors. All remaining cells will be retained for further processing. 1 - Configures the Receive ATM Cell Processor block to retain ALL incoming ATM cells that contain uncorrectable HEC byte errors for further processing.
1	COSET Polynomial Addition	R/W	**COSET Polynomial Addition:** This READ/WRITE bit-field permits the user to configure the Receive ATM Cell Processor block to account for the fact that the HEC bytes (within the incoming ATM cell traffic) also include the Modulo-2 addition of the Coset Polynomial (e.g., x^6 + x^4 + x^2 + 1), when performing HEC Byte Verification. 0 - Configures the Receive ATM Cell Processor block to NOT account for the Coset Polynomial within the HEC bytes of the incoming ATM cells. 1 - Configures the Receive ATM Cell Processor block to account for the Coset Polynomial within the HEC bytes of the incoming ATM cells.
0	Regenerate HEC Byte Enable	R/W	**Regenerate HEC Byte Enable:** This READ/WRITE bit-field permits the user to configure the Receive ATM Cell Processor block to automatically re-compute and insert a new HEC byte into each incoming ATM cell that contains an uncorrectable HEC byte. 0 - Does not configure the Receive ATM Cell Processor block to compute and insert a new HEC byte into ATM cells that contains an uncorrectable HEC byte error. 1 - Configures the Receive ATM Cell Processor block to compute and insert a new HEC byte into any incoming ATM cell that contains an uncorrectable HEC byte error. ***NOTE:*** *If the user wishes to implement this feature, then the user must disable the Uncorrectable HEC Byte Discard feature, by setting Bit 2 (Uncorrectable HEC Byte Discard) within this register, to "0".*

Receive ATM Cell Processor Block - Receive ATM Control Register - Byte 0 (Address = 0x1703)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HEC Byte Insert into UDF1 Enable	HEC Status into UDF2 Enable	HEC Byte Correction Threshold[1:0]		Receive UTOPIA Parity - ODD	Unused		Descramble Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/O	R/W
1	1	0	0	1	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	HEC Byte Insert into UDF1	R/W	**HEC Byte Insert into UDF1 Enable:** This READ/WRITE bit-field permits the user to configure the Receive ATM Cell Processor block to compute and insert the HEC byte into the UDF1 byte position, within each cell it routes to the Receive FIFO (and then to the Receive UTOPIA Interface). 0 - Configures the Receive ATM Cell Processor block to NOT compute the HEC byte and insert it into the UDF1 byte position, within each cell that it routes the Receive FIFO. 1 - Configures the Receive ATM Cell Processor block to compute the HEC byte and insert it into the UDF1 byte position, within each cell that it routes to the Receive FIFO. ***NOTE:*** *This bit-field is only valid if the Receive UTOPIA Interface has been configured to handle 54 or 56 byte cells. As a consequence, the user must set Bits 1 and 0 (Cell Sizes[1:0]) within the Receive UTOPIA/POS-PHY Control Register (Address = 0x0503) to either [1, 0] or [1, 1].*

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>HEC Status into UDF2 Enable</td><td>R/W</td><td>
HEC Status into UDF2 Byte Enable:
This READ/WRITE bit-field permits the user to configure the Receive ATM Cell Processor block to insert the HEC Byte Status indicator into the UDF2 byte position, within each cell that it routes to the Receive FIFO (and then to the Receive UTOPIA Interface).
If the user implements this configuration option, then the Receive ATM Cell Processor block will insert some values into the UDF2 byte-field, that reflect the HEC Byte Verification results on this particular incoming ATM cell.
<table>
<tr><th>HEC Byte Status Value</th><th>Corresponding HEC Byte Verification Results</th></tr>
<tr><td>0x00</td><td>Error Free HEC Byte Value</td></tr>
<tr><td>0xFF</td><td>Uncorrectable HEC Byte Value</td></tr>
<tr><td>0xAA</td><td>Correctable HEC Byte Value</td></tr>
</table>
0 - Configures the Receive ATM Cell Processor block to NOT insert the HEC Byte Status value into the UDF2 byte of each ATM cell that it routes to the Receive FIFO.
1 - Configures the Receive ATM Cell Processor block to insert the HEC Byte Status value into the UDF2 byte of each ATM cell that it routes to the Receive FIFO.
NOTE: This bit-field is only valid if the Receive UTOPIA Interface block has been configured to handle 56 byte cells.
</td></tr>
<tr><td>5 - 4</td><td>HEC Byte Correction Threshold[1:0]</td><td>R/W</td><td>
HEC Byte Correction Threshold[1:0]:
These two READ/WRITE bit-fields permit the user to define the HEC Byte Correction Threshold for the Receive ATM Cell Processor block. The HEC Byte Correction threshold is defined as the minimum number of consecutive un-erred (no HEC byte errors) cells that the Receive ATM Cell Processor must receive before it will transition from the Detection Mode into the Correction Mode.
The relationship between the value of these bit-fields and the corresponding HEC Byte Correction thresholds is tabulated below.
<table>
<tr><th>HEC Byte</th><th>HEC Byte Correction</th></tr>
<tr><td>00</td><td>1 ATM Cell with a valid HEC Byte</td></tr>
<tr><td>01</td><td>2 consecutive ATM Cells each with a valid HEC Byte</td></tr>
<tr><td>10</td><td>4 consecutive ATM Cells each with a valid HEC Byte</td></tr>
<tr><td>11</td><td>8 consecutive ATM Cells each with a valid HEC Byte</td></tr>
</table>
</td></tr>
</table>

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	Receive UTOPIA Parity - ODD	R/W	**Receive UTOPIA Parity Value - ODD Parity:** This READ/WRITE bit-field permits the user to configure the Receive ATM Cell Processor block to compute either the EVEN or ODD parity value for each byte (or 16-bit word) within each cell that it processes. Each of these parity value will ultimately be output via the RxUPrty output pin (on the Receive UTOPIA Bus) coincident to when the corresponding byte (of ATM cell data) is output via the Receive UTOPIA Data Bus (RxU-Data[15:0]). 0 - Configures the Receive ATM Cell Processor block to compute the EVEN Parity value of each byte (or 16-bit word) of ATM cell data that it processes. 1 - Configures the Receive ATM Cell Processor block to compute the ODD Parity value of each byte of ATM cell data that is processes.
2 - 1	Unused	R/O	
0	Descramble Enable		**De-Scramble Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Cell De-Scrambler within the Receive ATM Cell Processor Block. 0 - Disables the Cell De-Scrambler. 1 - Enables the Cell De-Scrambler.

Receive ATM Cell Processor Block - Receive ATM Status Register (Address = 0x1707)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				PRBS Lock Indicator	Cell Delineation Status[1:0]		LCD Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBERS	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	PRBS Lock Indicator	R/O	**Test Cell - PRBS Lock Indicator:** This READ-ONLY bit-field indicates whether or not the Test Cell Receiver is declaring a PRBS Lock condition within the payload data within the incoming Test Cell data-stream. 0 - Indicates that the Test Cell Receiver is NOT declaring the PRBS Lock condition. 1 - Indicates that the Test Cell Receiver is currently declaring the PRBS Lock condition. ***NOTE:*** *This bit-field is only valid if the Test Cell Receiver has been enabled.*

BIT NUMBERS	NAME	TYPE	DESCRIPTION
2 - 1	Cell Delineation Status[1:0]	R/O	**Cell Delineation Status[1:0]:** These two READ-ONLY bit-fields indicate the current state (within the Cell Delineation State Machine) that the Receive ATM Cell Processor block is currently operating in. The relationship between the contents of these bit-fields and the corresponding Cell Delineation State Machine state that the Receive ATM Cell Processor block is operating in, is tabulated below. **Cell Delineation Status[1:0]** / **State of Receive ATM Cell Processor Block** 00 – SYNC State 01 – PRE-SYNC State 10 – Not Valid 11 – HUNT State
0	LCD Defect Declared	R/O	**LCD (Loss of Cell Delineation) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive ATM Cell Processor block is currently declaring the LCD defect condition. The Receive ATM Cell Processor block will declare the LCD defect condition anytime that the Receive ATM Cell Processor block is NOT operating in the SYNC State, within the Cell Delineation State Machine. 0 - Indicates that the Receive ATM Cell Processor block is NOT declaring the LCD Defect Condition. 1 - Indicates that the Receive ATM Cell Processor block is currently declaring the LCD Defect Condition.

Receive ATM Cell Processor Block - Receive ATM Interrupt Status Register - Byte 1 (Address = 0x170A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Receive Cel Extraction Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Receive Cell Extraction Interrupt Status	RUR	**Receive Cell Extraction Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive Cell Extraction Interrupt has occurred since the last read of this register. The Receive ATM Cell Processor block will generate the Receive Cell Extraction Interrupt anytime it receives an incoming ATM cell (from traffic) and loads an ATM cell into the Extraction Memory Buffer. 0 - Indicates that the Receive Cell Extraction Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Receive Cell Extraction Interrupt has occurred since the last read of this register.

Receive ATM Cell Processor Block - Receive ATM Interrupt Status Register - Byte 0 (Address = 0x170B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Cell Insertion Interrupt Status	Receive FIFO Overflow Interrupt Status	Receive Cell Extraction Memory Overflow Interrupt Status	Receive Cell Insertion Memory Overflow Interrupt Status	Detection of Correctable HEC Byte Error Interrupt Status	Detection of Uncorrect-able HEC Byte Error Interrupt Status	Clearance of LCD Interrupt Status	Declaration of LCD Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive Cell Insertion Interrupt Status	RUR	**Receive Cell Insertion Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive Cell Insertion Interrupt has occurred since the last read of this register. The Receive ATM Cell Processor block will generate the Receive Cell Insertion Interrupt anytime a cell (residing in the Receive Cell Insertion Buffer) is read out of the Receive Cell Insertion Buffer and is loaded into the incoming ATM cell traffic. 0 - Indicates that the Receive Cell Insertion Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Receive Cell Insertion Interrupt has occurred since the last read of this register.
6	Receive FIFO Overflow Interrupt Status	RUR	**Receive FIFO Overflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive FIFO Overflow Interrupt has occurred since the last read of this register, as described below. 0 - Indicates that the Receive FIFO Overflow Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Receive FIFO Overflow Interrupt has occurred since the last read of this register.

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	Receive Cell Extraction Memory Overflow Interrupt Status	RUR	**Receive Cell Extraction Memory Overflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive Cell Extraction Memory Overflow Interrupt has occurred since the last read of this register. The Receive ATM Cell Processor block will generate this interrupt anytime an overflow event has occurred in the Receive Cell Extraction Memory Buffer. 0 - Indicates that the Receive ATM Cell Processor block has NOT declared the Receive Cell Extraction Memory Overflow Interrupt since the last read of this register. 1 - Indicates that the Receive ATM Cell Processor block has declared the Receive Cell Extraction Memory Overflow interrupt since the last read of this register.
4	Receive Cell Insertion Memory Overflow Interrupt Status	RUR	**Receive Cell Insertion Memory Overflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive Cell Insertion Memory Overflow Interrupt has occurred since the last read of this register. The Receive ATM Cell Processor block will generate this interrupt anytime an overflow event has occurred in the Receive Cell Insertion Memory Buffer. 0 - Indicates that the Receive ATM Cell Processor block has NOT declared the Receive Cell Insertion Memory Overflow interrupt since the last read of this register. 1 - Indicates that the Receive ATM Cell Processor block has declared the Receive Cell Insertion Memory Overflow interrupt since the last read of this register.
3	Detection of Correctable HEC Byte Error Interrupt Status	RUR	**Detection of Correctable HEC Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive ATM Cell Processor block has declared the Detection of Correctable HEC Byte Error interrupt since the last read of this register. The Receive ATM Cell Processor block will generate this interrupt anytime it has received an ATM cell that contains a correctable HEC byte error .0 - Indicates that the Receive ATM Cell Processor block has NOT declared the Detection of Correctable HEC Byte Error Interrupt since the last read of this register. 1 - Indicates that the Receive ATM Cell Processor block has declared the Detection of Correctable HEC Byte Error Interrupt since the last read of this register.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Detection of Uncorrectable HEC Byte Error Interrupt Status	RUR	**Detection of Uncorrectable HEC Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive ATM Cell Processor block has declared the Detection of Uncorrectable HEC Byte Error Interrupt since the last read of this register. The Receive ATM Cell Processor block will generate this interrupt anytime it has received an ATM cell that contains an uncorrectable HEC byte error. 0 - Indicates that the Receive ATM Cell Processor block has NOT declared the Detection of Uncorrectable HEC Byte Error interrupt since the last read of this register. 1 - Indicates that the Receive ATM Cell Processor block has declared the Detection of Uncorrectable HEC Byte Error Interrupt since the last read of this register.
1	Clearance of LCD Interrupt Status	RUR	**Clearance of LCD (Loss of Cell Delineation) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive ATM Cell Processor block has cleared the LCD Defect condition since the last read of this register. ***NOTE:*** *If the Receive ATM Cell Processor block clears the LCD Defect, then this means that the Receive ATM Cell Processor block is currently properly delineating ATM cells that it receives from either the Receive DS3/E3 Framer or Receive PLCP Processor block.* 0 - Indicates that the Receive ATM Cell Processor block has NOT cleared the LCD Defect since the last read of this register. 1 - Indicates that the Receive ATM Cell Processor block has cleared the LCD Defect since the last read of this register.
0	Declaration of LCD Interrupt Status	RUR	**Declaration of LCD (Loss of Cell Delineation) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Receive ATM Cell Processor block has declared the LCD Defect condition since the last read of this register. ***NOTE:*** *If the Receive ATM Cell Processor block declares the LCD Defect, then this means that the Receive ATM Cell Processor block is NOT currently delineation ATM cells that it receives from either the Receive DS3/E3 Framer or Receive PLCP Processor block.* 0 - Indicates that the Receive ATM Cell Processor block has NOT declared the LCD Defect since the last read of this register. 1 - Indicates that the Receive ATM Cell Processor block has declared the LCD Defect since the last read of this register.

Receive ATM Cell Processor Block - Receive ATM Interrupt Enable Register - Byte 1 (Address = 0x170E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Receive Cell Extraction Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	Receive Cell Extraction Interrupt Enable	R/W	**Receive Cell Extraction Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive Cell Extraction Interrupt. If the user enables this interrupt, then the Receive ATM Cell Processor block will generate the Receive Cell Extraction Interrupt anytime it receives an incoming ATM cell (from traffic) and loads an ATM cell into the Extraction Memory Buffer. 0 - Disables the Receive Cell Extraction Interrupt. 1 - Enables the Receive Cell Extraction Interrupt.

Receive ATM Cell Processor Block - Receive ATM Interrupt Enable Register - Byte 0 (Address = 0x170F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Cell Insertion Interrupt Enable	Receive FIFO Overflow Interrupt Enable	Receive Cell Extraction Memory Overflow Interrupt Enable	Receive Cell Insertion Memory Overflow Interrupt Enable	Detection of Correctable HEC Byte Error Interrupt Enable	Detection of Uncorrectable HEC Byte Error Interrupt Enable	Clearance of LCD Interrupt Enable	Declaration of LCD Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive Cell Insertion Interrupt Enable	R/W	**Receive Cell Insertion Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive Cell Insertion Interrupt. If the user enables this feature, then the Receive ATM Cell Processor block will generate the Receive Cell Insertion Interrupt anytime a cell (residing in the Receive Cell Insertion Buffer) is read out of the Receive Cell Insertion Buffer and is loaded into the incoming ATM cell traffic. 0 - Disables the Receive Cell Insertion Interrupt. 1 - Enables the Receive Cell Insertion Interrupt

BIT NUMBER	NAME	TYPE	DESCRIPTION
6	Receive FIFO Overflow Interrupt Enable	R/W	**Receive FIFO Overflow Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive FIFO Overflow Interrupt. If the user enables this interrupt, then the Receive ATM Cell Processor block will generate an interrupt any time an overflow condition occurs within the RxFIFO. 0 - Disables the Receive FIFO Overflow Interrupt. 1 - Enables the Receive FIFO Overflow Interrupt.
5	Receive Cell Extraction Memory Overflow Interrupt Enable	R/W	**Receive Cell Extraction Memory Overflow Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive Cell Extraction Memory Overflow Interrupt. If the user enables this interrupt, then the Receive ATM Cell Processor block will generate an interrupt any time an overflow event has occurred in the Receive Cell Extraction Memory buffer. 0 - Disables the Receive Cell Extraction Memory Overflow Interrupt. 1 - Enables the Receive Cell Extraction Memory Overflow Interrupt.
4	Receive Cell Insertion Memory Overflow Interrupt Enable	R/W	**Receive Cell Insertion Memory Overflow Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive Cell Insertion Memory Overflow Interrupt. If the user enables this interrupt, then the Receive ATM Cell Processor block will generate an interrupt any time an overflow event has occurred in the Receive Cell Insertion Memory buffer. 0 - Disables the Receive Cell Insertion Memory Overflow Interrupt. 1 - Enables the Receive Cell Insertion Memory Overflow Interrupt.
3	Detection of Correctable HEC Byte Error Interrupt Enable	R/W	**Detection of Correctable HEC Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of Correctable HEC Byte Error Interrupt within the Receive ATM Cell Processor block. If the user enables this interrupt, then the Receive ATM Cell Processor block will generate an interrupt each time it receives an ATM cell (in incoming traffic) that contains a correctable HEC Byte error. 0 - Disables the Detection of Correctable HEC Byte Error Interrupt. 1 - Enables the Detection of Correctable HEC Byte Error Interrupt.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Detection of Uncorrectable HEC Byte Error Interrupt Enable	R/W	**Detection of Uncorrectable HEC Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of Uncorrectable HEC Byte Error Interrupt within the Receive ATM Cell Processor block. If the user enables this interrupt, then the Receive ATM Cell Processor block will generate an interrupt each time it receives an ATM cell (in incoming traffic) that contains an uncorrectable HEC Byte error. 0 - Disables the Detection of Uncorrectable HEC Byte Error Interrupt. 1 - Enables the Detection of Uncorrectable HEC Byte Error Interrupt.
1	Clearance of LCD Interrupt Enable	R/W	**Clearance of LCD (Loss of Cell Delineation) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Clearance of LCD Interrupt. If the user enables this interrupt, then the Receive ATM Cell Processor block will generate an interrupt, anytime it clears the LCD (Loss of Cell Delineation) defect condition. 0 - Disables the Clearance of LCD Defect Condition Interrupt. 1 - Enables the Clearance of LCD Defect Condition Interrupt.
0	Declaration of LCD Interrupt Enable	R/W	**Declaration of LCD (Loss of Cell Delineation) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Declaration of LCD Interrupt. If the user enables this interrupt, then the Receive ATM Cell Processor block will generate an interrupt, anytime it declares the LCD defect condition. 0 - Disables the Declaration of LCD Defect Condition Interrupt. 1 - Enables the Declaration of LCD Defect Condition Interrupt.

Receive ATM Cell Processor Block - Receive ATM Cell Insertion/Extraction Memory Control Register (Address = 0x1713)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive Cell Extraction Memory RESET*	Receive Cell Extraction Memory CLAV	Receive Cell Insertion Memory RESET*	Receive Cell Insertion Memory ROOM	Receive Cell Insertion Memory WSOC
R/O	R/O	R/O	R/W	R/O	R/W	R/O	W/O
0	0	0	1	0	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	Receive Cell Extraction Memory RESET*	R/W	**Receive Cell Extraction Memory RESET*:** This READ/WRITE bit-field permits the user to perform a RESET operation to the Receive Cell Extraction Memory. If the user writes a "1" to "0" transition into this bit-field, then the following events will occur. **a.** All of the contents of the Receive Cell Extraction Memory will be flushed. **b.** All READ and WRITE pointers will be reset to their default positions. ***NOTE:*** *Following this RESET event, the user must write the value "1" into this bit-field in order to enable normal operation within the Receive Cell Extraction Memory*
3	Receive Cell Extraction CLAV	R/O	**Receive Cell Extraction Memory - Cell Available Indicator:** This READ-ONLY bit-field indicates whether or not there is at least ATM cell of data (residing within the Receive Cell Extraction Memory) that needs to be read out via the Microprocessor Interface. 0 - Indicates that the Receive Cell Extraction Memory is empty and contains no ATM cell data. 1 - Indicates that the Receive Cell Extraction Memory contains at least one ATM cell of data that needs to be read out. ***NOTE:*** *The user should validate each ATM cell that is being read out from the Receive Cell Extraction memory by checking the state of this bit-field prior to reading out the contents of any ATM cell data residing within the Receive Cell Extraction Memory.*
2	Receive Cell Insertion Memory RESET*	R/W	**Receive Cell Insertion Memory RESET*:** This READ/WRITE bit-field permits the user to perform a RESET operation to the Receive Cell Insertion Memory. If the user writes a "1" to "0" transition into this bit-field, then the following events will occur. **a.** All of the contents of the Receive Cell Insertion Memory will be flushed. **b.** All READ and WRITE pointers will be reset to their default positions. ***NOTE:*** *Following this RESET event, the user must write the value "1" into this bit-field in order to enable normal operation of the Receive Cell Insertion Memory.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Receive Cell Insertion Memory ROOM	R/O	**Receive Cell Insertion Memory - ROOM Indicator:** This READ-ONLY bit-field indicates whether or not there is room (e.g., empty space) available for the contents of another ATM cell to be written into the Receive Cell Insertion Memory. 0 - Indicates that the Receive Cell Insertion Memory does not contain enough empty space to receive another ATM cell via the Microprocessor Interface. 1 - Indicates that the Receive Cell Insertion Memory does contain enough empty space to receive another ATM cell via the Microprocessor Interface. ***NOTE:*** *The user should verify that the Receive Cell Insertion Memory has sufficient empty space to accept another ATM cell of data (via the Microprocessor Interface) by polling the state of this bit-field prior to writing each cell into the Receive Cell Insertion Memory.*
0	Receive Cell Insertion Memory WSOC	W/O	**Receive Cell Insertion Memory - Write SOC (Start of Cell):** Whenever the users are writing the contents of an ATM cell into the Receive Cell Insertion Memory, then they are suppose to identify/designate the very first byte of this ATM cell by setting this bit-field to "1". Whenever the user does this, then the Receive Cell Insertion Memory will know that the next octet that is written into the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory Data Register - Byte 3 (Address = 0x1714) is designated as the first byte of the ATM cell currently being written into the Receive Cell Insertion Memory. This bit-field must be set to "0" during all other WRITE operations to the Receive ATM Cell Processor - Receive Cell Insertion/Extraction Memory Data Register.

Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory Data - Byte 3 (Address = 0x1714)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Cell Insertion/Extraction Memory Data[31:24]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive Cell Insertion/ Extraction Memory Data[31:24]	R/W	**Receive Cell Insertion/Extraction Memory Data[31:24]:** These READ/WRITE bit-fields, along with that in the Receive ATM Cell Processor Block -Receive Cell Insertion/Extraction Memory Data - Bytes 2 through 0 support the following functions. **a.** They function as the address location, for which the user to write the contents of an Outbound ATM cell into the Receive Cell Insertion Memory, via the Microprocessor Interface. **b.** They function as the address location, for which the user to read out the contents of an inbound ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. ***NOTES:*** *1. If the user performs a WRITE operation to this (and the other three address locations), then the user is writing ATM cell data into the Receive Cell Insertion Memory.* *2. If the user performs a READ operation to this (and the other three address locations), then the user is reading ATM cell data from the Receive Cell Extraction Memory.* *3. READ and WRITE operations must be performed in a 32-bit (4-byte word) manner. Hence, whenever a user performs a READ/WRITE operation to these address locations, the user must start by writing in or reading out the first byte (of this 4-byte word) of a given ATM cell, into/from this particular address location. Next, the user must perform the READ/WRITE operation (with the second of this 4-byte word) to the Receive ATM Cell Processor Block -Receive Cell Insertion/Extraction Memory - Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this 4-byte word) to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this 4-byte word) to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 0 register. When reading out (writing in) the next four bytes of a given ATM cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.* *4. Whenever the user is writing cell data into the Receive Cell Insertion Memory, the size of the Cell is always 56 bytes.* *5. Whenever the user is reading cell data from the Receive Cell Extraction Memory, the size of the Cell is always 56 bytes.*

Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory Data - Byte 2 (Address = 0x1715)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Cell Insertion/Extraction Memory Data[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive Cell Insertion/ Extraction Memory Data[23:16]	R/W	**Receive Cell Insertion/Extraction Memory Data[31:24]:** These READ/WRITE bit-fields, along with that in the Receive ATM Cell Processor Block- Receive Cell Insertion/Extraction Memory Data- Bytes 3, and Bytes 1, 0 support the following functions. **a.** They function as the address location for which the user to write the contents of an Outbound ATM cell into the Receive Cell Insertion Memory, via the Microprocessor Interface. **b.** They function as the address location, for which the user to read out the contents of an inbound ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. ***NOTES:*** *1. If the user performs a WRITE operation to this (and the other three address locations), then the user is writing ATM cell data into the Receive Cell Insertion Memory.* *2. If the user performs a READ operation to this (and the other three address locations, then the user is reading ATM cell data from the Receive Cell Extraction Memory.* *3. READ and WRITE operations must be performed in a 32-bit (4-byte chunk) manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, the user must start by writing in or reading out the first byte (of this 4-byte chunk) of a given ATM cell into/from the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 3. Next, the user must perform a READ/WRITE operation (with the second of this 4-byte words) to this particular address location. Afterwards, the user must perform a READ/WRITE operation (with the third of this 4-byte word) to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this 4-byte word) to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 0 register. When reading out (writing in) the next four bytes of a given ATM cell, the user must repeat this process with a READ or WRITE operation, to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 3 register, and so on.* *4. Whenever the user is writing cell data into the Receive Cell Insertion Memory, the size of the Cell is always 56 bytes.* *5. Whenever the user is reading cell data from the Receive Cell Extraction Memory, the size of the Cell is always 56 bytes.*

Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory Data - Byte 1 (Address = 0x1716)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Cell Insertion/Extraction Memory Data[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive Cell Insertion/ Extraction Memory Data[15:8]	R/W	**Receive Cell Insertion/Extraction Memory Data[15:8]:** These READ/WRITE bit-fields, along with that in the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory Data - Bytes 3, 2 and 0 support the following functions. **a.** They function as the address location, for which the user to write the contents of an Outbound ATM cell into the Receive Cell Insertion Memory, via the Microprocessor Interface. **b.** They function as the address location, for which the user to read out the contents of an inbound ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. ***NOTES:*** *1. If the user performs a WRITE operation to this (and the other three address locations), then the user is writing ATM cell data into the Receive Cell Insertion Memory.* *2. If the user performs a READ operation to this (and the other three address locations, then the user is reading ATM cell data from the Receive Cell Extraction Memory.* *3. READ and WRITE operations must be performed in a 32-bit (4-byte word) manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, the user must start by writing in or reading out the first byte (of this 4-byte word) of a given ATM cell, into/from the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 3 register. Next, the user must perform a READ/ WRITE operation (with the second of this 4-byte word) to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this 4-byte word) to this register. Finally, the user must perform a READ/WRITE operation (with the fourth of this 4-byte word) to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 0. When reading out (writing in) the next four bytes of a given ATM cell, the user must repeat this process with a READ or WRITE operation to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 3, and so on.* *4. Whenever the user is writing cell data into the Receive Cell Insertion Memory, the size of the Cell is always 56 bytes.* *5. Whenever the user is reading cell data from the Receive Cell Extraction Memory, the size of the Cell is always 56 bytes.*

Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory Data - Byte 0 (Address = 0x1717)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Cell Insertion/Extraction Memory Data[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive Cell Insertion/ Extraction Memory Data[7:0]	R/W	**Receive Cell Insertion/Extraction Memory Data[7:0]:** These READ/WRITE bit-fields, along with that in the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory Data - Bytes 3 through 1 support the following functions. They function as the address location, for which the user to write the contents of an Outbound ATM cell into the Receive Cell Insertion Memory, via the Microprocessor Interface. They function as the address location, for which the user to read out the contents of an inbound ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. ***NOTES:*** 1. *If the user performs a WRITE operation to this (and the other three address locations), then the user is writing ATM cell data into the Receive Cell Insertion Memory.* 2. *If the user performs a READ operation to this (and the other three address locations), then the user is writing ATM cell data into the Receive Cell Insertion Memory.* 3. *READ and WRITE operations must be performed in a 32-bit (4-byte word) manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, the user must start by writing in or reading out the first byte (of this 4-byte word) of a given ATM cell, into/from the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 3 register. Next, the user must perform a READ/ WRITE operation (with the second of this 4-byte word) to the Receive ATM Cell Processor block - Receive Cell Insertion/Extraction Memory - Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this 4-byte word) to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this 4-byte word) to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 0. When reading out (writing in) the next four bytes of a given ATM cell, the user must repeat this process with a READ or WRITE operation, to the Receive ATM Cell Processor Block - Receive Cell Insertion/Extraction Memory - Byte 3, and so on.* 4. *Whenever the user is writing cell data into the Receive Cell Insertion Memory, the size of the Cell is always 56 bytes.* 5. *Whenever the user is reading cell data from the Receive Cell Extraction Memory, the size of the Cell is always 56 bytes.*

Receive ATM Cell Processor Block - UDF1 Byte Value Register (Address = 0x1718)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive UDF1 Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive UDF1 Byte[7:0]	R/W	**Receive UDF1 Byte[7:0]:** These READ/WRITE bit-fields permit the user to specify the value of the UDF1 byte, within any ATM Cell data that is written to the Receive FIFO and is ultimately output via the Receive UTOPIA Interface block. ***NOTE:*** *These register bits are only valid if the Receive UTOPIA Interface has been configured to operate in the UTOPIA Level 3 Mode, and if the Cell Size (as processed via the Receive UTOPIA Interface) is configured to be 56 bytes.*

Receive ATM Cell Processor Block - UDF2 Byte Value Register (Address = 0x1719)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive UDF2 Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive UDF2 Byte[7:0]	R/W	**Receive UDF2 Byte[7:0]:** These READ/WRITE bit-fields permit the user to specify the value of the UDF2 byte, within any ATM Cell data that is written to the Receive FIFO and is ultimately output via the Receive UTOPIA Interface block. ***NOTE:*** *These register bits are only valid if the Receive UTOPIA Interface has been configured to operate in the UTOPIA Level 3 Mode, and if the Cell Size (as processed via the Receive UTOPIA Interface) is configured to be 56 bytes.*

Receive ATM Cell Processor Block - UDF3 Byte Value Register (Address = 0x171A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive UDF3 Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive UDF3 Byte[7:0]	R/W	**Receive UDF3 Byte[7:0]:** These READ/WRITE bit-fields permit the user to specify the value of the UDF3 byte, within any ATM Cell data that is written to the Receive FIFO and is ultimately output via the Receive UTOPIA Interface block. ***NOTE:*** *These register bits are only valid if the Receive UTOPIA Interface has been configured to operate in the UTOPIA Level 3 Mode, and if the Cell Size (as processed via the Receive UTOPIA Interface) is configured to be 56 bytes.*

Receive ATM Cell Processor Block - UDF4 Byte Value Register (Address = 0x171B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive UDF4 Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive UDF4 Byte[7:0]	R/W	**Receive UDF4 Byte[7:0]:** These READ/WRITE bit-fields permit the user to specify the value of the UDF4 byte, within any ATM Cell data that is written to the Receive FIFO and is ultimately output via the Receive UTOPIA Interface block. ***NOTE:*** *These register bits are only valid if the Receive UTOPIA Interface has been configured to operate in the UTOPIA Level 3 Mode, and if the Cell Size (as processed via the Receive UTOPIA Interface) is configured to be 56 bytes.*

Receive ATM Cell Processor Block - Receive Test Cell Header Byte - Byte 1 (Address = 0x1720)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Test Cell Header Byte 1[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive Test Cell Header Byte 1 [7:0]	R/W	**Receive Test Cell Header Byte 1:** These READ/WRITE register bits along with that in Receive ATM Cell Processor Block - Receive Test Cell Header Byte - Bytes 2 through 4 permit the user to define the header bytes of test cells that are being generated by the Transmit Test Cell Generator. These cells also permit the Receive Test Cell Receiver to identify the test cells within the incoming ATM cell data stream. This particular register byte permits the user to define the contents of Header byte # 1. ***NOTE:*** *These register bits are only valid if the Receive Test Cell Receiver has been enabled.*

Receive ATM Cell Processor Block - Receive Test Cell Header Byte - Byte 2 (Address = 0x1721)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Test Cell Header Byte 2[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive Test Cell Header Byte 2 [7:0]	R/W	**Receive Test Cell Header Byte 2:** These READ/WRITE register bits along with that in Receive ATM Cell Processor Block - Receive Test Cell Header Byte - Bytes 1, Bytes 3 and 4 permit the user to define the header bytes of test cells that are being generated by the Transmit Test Cell Generator. These cells also permit the Receive Test Cell Receiver to identify the test cells within the incoming ATM cell data stream. This particular register byte permits the user to define the contents of Header byte # 2. ***NOTE:*** *These register bits are only valid if the Receive Test Cell Receiver has been enabled.*

Receive ATM Cell Processor Block - Receive Test Cell Header Byte - Byte 3 (Address = 0x1722)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Test Cell Header Byte 3[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive Test Cell Header Byte 3 [7:0]	R/W	**Receive Test Cell Header Byte 3:** These READ/WRITE register bits along with that in Receive ATM Cell Processor Block - Receive Test Cell Header Byte - Bytes 1, 2 and 4 permit the user to define the header bytes of test cells that are being generated by the Transmit Test Cell Generator. These cells also permit the Receive Test Cell Receiver to identify the test cells within the incoming ATM cell data stream. This particular register byte permits the user to define the contents of Header byte # 3. ***NOTE:*** *These register bits are only valid if the Receive Test Cell Receiver has been enabled.*

Receive ATM Cell Processor Block - Receive Test Cell Header Byte - Byte 4 (Address = 0x1723)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Test Cell Header Byte 4[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive Test Cell Header Byte 4 [7:0]	R/W	**Receive Test Cell Header Byte 4:** These READ/WRITE register bits along with that in Receive ATM Cell Processor Block - Receive Test Cell Header Byte - Bytes 1 through 3 permit the user to define the header bytes of test cells that are being generated by the Transmit Test Cell Generator. These cells also permit the Receive Test Cell Receiver to identify the test cells within the incoming ATM cell data stream. This particular register byte permits the user to define the contents of Header byte # 4. ***NOTE:*** *These register bits are only valid if the Receive Test Cell Receiver has been enabled.*

Receive ATM Cell Processor Block - Test Cell Error Count Registers - Byte 3 (Address = 0x1724)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Cell Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Test Cell Error Count[31:24]	RUR	**Test Cell Error Count[31:24]:** These RESET-upon-READ bit-fields along with that within the Receive ATM Cell Processor Block - Test Cell Error Count Registers - Bytes 2 through 0 contains the 32-bit expression for the number of Test Cell Bit Errors that have been detected (by the Test Cell Receiver) since the last read of these registers. More specifically, these register bits reflect the number of bit errors that have been detected within the PRBS data that is transported via the Payload Bytes of these Test Cells, since the last read of these registers. This particular register byte contains the MSB (Most Significant Byte) of this 32-bit value for the number of Test Cell Bit Errors. ***NOTES:*** *1. This register byte is only valid if the Test Cell Receiver has been enabled.* *2. If the number of Test Cell Error Bits reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Test Cell Error Count Registers - Byte 2 (Address = 0x1725)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Cell Error Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Test Cell Error Count[23:16]	RUR	**Test Cell Error Count[23:16]:** These RESET-upon-READ bit-fields along with that within the Receive ATM Cell Processor Block - Test Cell Error Count Registers - Bytes 3, 1 and 0 contains the 32-bit expression for the number of Test Cell Bit Errors that have been detected (by the Test Cell Receiver) since the last read of these registers. More specifically, these register bits reflect the number of bit errors that have been detected within the PRBS data that is transported via the Payload Bytes of these Test Cells, since the last read of these registers. ***NOTES:*** *1. This register byte is only valid if the Test Cell Receiver has been enabled.* *2. If the number of Test Cell Error Bits reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Test Cell Error Count Registers - Byte 1 (Address = 0x1726)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Cell Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Test Cell Error Count[15:8]	RUR	**Test Cell Error Count[15:8]:** These RESET-upon-READ bit-fields along with that within the Receive ATM Cell Processor Block - Test Cell Error Count Registers - Bytes 3, 2 and 0 contains the 32-bit expression for the number of Test Cell Bit Errors that have been detected (by the Test Cell Receiver) since the last read of these registers. More specifically, these register bits reflect the number of bit errors that have been detected within the PRBS data that is transported via the Payload Bytes of these Test Cells, since the last read of these registers. ***NOTES:*** 1. *This register byte is only valid if the Test Cell Receiver has been enabled.* 2. *If the number of Test Cell Error Bits reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Test Cell Error Count Registers - Byte 0 (Address = 0x1727)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Cell Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Test Cell Error Count[7:0]	RUR	**Test Cell Error Count[7:0]:** These RESET-upon-READ bit-fields along with that within the Receive ATM Cell Processor Block - Test Cell Error Count Registers - Bytes 3, through 1 contains the 32-bit expression for the number of Test Cell Bit Errors that have been detected (by the Test Cell Receiver) since the last read of these registers. More specifically, these register bits reflect the number of bit errors that have been detected within the PRBS data that is transported via the Payload Bytes of these Test Cells, since the last read of these registers.This particular register byte contains the LSB (Least Significant Byte) of this 32-bit value for the number of Test Cell Bit Errors. ***NOTES:*** *1. This register byte is only valid if the Test Cell Receiver has been enabled.* *2. If the number of Test Cell Error Bits reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cell Count Register - Byte 3 (Address = 0x1728)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive ATM Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive ATM Cell Count[31:24]	RUR	**Receive ATM Cell Count [31:24]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive ATM Cell Count Registers - Bytes 2 through 0 contain the 32-bit expression for the number of cells that has been received by the Receive FIFO (e.g., where it can be read out via the Receive UTOPIA Interface Block) since the last read of these registers. This particular register byte contains the MSB (Most Significant Byte) of this 32-bit value for the number of Received ATM cells. ***NOTES:*** *1. The contents within these register bytes do not include Cells that have been discarded due to uncorrectable HEC byte errors, or those cells that have been discarded via the User Cell Filter.* *2. If the number of Received ATM Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cell Count Register - Byte 2 (Address = 0x1729)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive ATM Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive ATM Cell Count[23:16]	RUR	**Receive ATM Cell Count [23:16]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive ATM Cell Count Registers - Bytes 3, 1 and 0 contain the 32-bit expression for the number of cells that has been received by the Receive FIFO (e.g., where it can be read out via the Receive UTOPIA Interface Block) since the last read of these registers. ***NOTES:*** 1. *The contents within these register bytes do not include Cells that have been discarded due to uncorrectable HEC byte errors, or those cells that have been discarded via the User Cell Filter.* 2. *If the number of Received ATM Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cell Count Register - Byte 1 (Address = 0x172A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive ATM Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive ATM Cell Count[15:8]	RUR	**Receive ATM Cell Count [15:8]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive ATM Cell Count Registers - Bytes 3, 2 and 0 contain the 32-bit expression for the number of cells that has been received by the Receive FIFO (e.g., where it can be read out via the Receive UTOPIA Interface Block) since the last read of these registers. ***NOTES:*** 1. *The contents within these register bytes do not include Idle Cells, and Cells that have been discarded due to uncorrectable HEC byte errors, or those cells that have been discarded via the User Cell Filter.* 2. *If the number of Received ATM Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cell Count Register - Byte 0 (Address = 0x172B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive ATM Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive ATM Cell Count[7:0]	RUR	**Receive ATM Cell Count [7:0]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive ATM Cell Count Registers - Bytes 3 through 1 contain the 32-bit expression for the number of cells that has been received by the Receive FIFO (e.g., where it can be read out via the Receive UTOPIA Interface Block) since the last read of these registers. This particular register bytes contains the LSB (Least Significant Byte) of this 32-bit value for the number of Received ATM cells. ***NOTES:*** 1. *The contents within these register bytes do not include Cells that have been discarded due to uncorrectable HEC byte errors, or those cells that have been discarded via the User Cell Filter.* 2. *If the number of Received ATM Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive Discarded ATM Cell Count - Byte 3 (Address = 0x172C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive - Discarded ATM Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive -Discard ATM Cell Count[31:24]	RUR	**Receive - Discarded ATM Cell Count[31:24]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Discarded ATM Cell Count - Bytes 2 through 0 registers contain the 32-bit expression for the number of cells that have been discarded since the last read of these registers. This particular register byte contains the MSB (Most Significant Byte) of this 32-bit value for the number of Received ATM cells.N ***NOTES:*** 1. *The contents within these register bytes do include Idle Cells that have been discarded by one of the User Cell Filters.* 2. *The contents within these register bytes do include those cells that have been discarded due to uncorrectable HEC byte errors, User Cell Filtering, or improper writes into the Receive FIFO.3. If the number of Discarded ATM Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive Discarded ATM Cell Count - Byte 2 (Address = 0x172D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive - Discarded ATM Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive -Discard ATM Cell Count[23:16]	RUR	**Receive - Discarded ATM Cell Count[23:16]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Discarded ATM Cell Count - Bytes 3, 1 and 0 registers contain the 32-bit expression for the number of cells that have been discarded since the last read of these registers. ***NOTES:*** *1. The contents within these register bytes do include Idle Cells that have been discarded by one of the User Cell Filters.* *2. The contents within these register bytes do include those cells that have been discarded due to uncorrectable HEC byte errors, User Cell Filtering, or improper writes into the Receive FIFO.* *3. If the number of Discarded ATM Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive Discarded ATM Cell Count - Byte 1 (Address = 0x172E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive - Discarded ATM Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive -Discard ATM Cell Count[15:8]	RUR	**Receive - Discarded ATM Cell Count[15:8]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Discarded ATM Cell Count - Bytes 3, 2 and 0 registers contain the 32-bit expression for the number of cells that have been discarded since the last read of these registers. ***NOTES:*** *1. The contents within these register bytes do include Idle Cells that have been discarded by one of the User Cell Filters.* *2. The contents within these register bytes do include those cells that have been discarded due to uncorrectable HEC byte errors, User Cell Filtering, or improper writes into the Receive FIFO.* *3. If the number of Discarded ATM Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive Discarded ATM Cell Count - Byte 0 (Address = 0x172F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive - Discarded ATM Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive -Discard ATM Cell Count[7:0]	RUR	**Receive - Discarded ATM Cell Count[7:0]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Discarded ATM Cell Count - Bytes 3 through 1 registers contain the 32-bit expression for the number of cells that have been discarded since the last read of these registers.This particular register byte contains the LSB (Least Significant Byte) of this 32-bit value for the number of Received ATM cells. ***NOTES:*** 1. *The contents within these register bytes do include Idle Cells that have been discarded by one of the User Cell Filters.* 2. *The contents within these register bytes do include those cells that have been discarded due to uncorrectable HEC byte errors, User Cell Filtering, or improper writes into the Receive FIFO.* 3. *If the number of Discarded ATM Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cells with Correctable HEC Byte Error Count Register - Byte 3 (Address = 0x1730)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received Cells with Correctable HEC Byte Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Received Cells with Correctable HEC Byte Error Count[31:24]	RUR	**Received Cells with Correctable HEC Byte Error Count[31:24]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Cells with Correctable HEC Byte Error Count - Bytes 2 through 0 registers contain the 32-bit expression for the number of cells (containing correctable HEC byte errors) that have been received since the last read of these registers. This particular register byte contains the MSB (Most Significant Byte) of this 32-bit value for the number of Received ATM cells with Correctable HEC Byte Errors. ***NOTE:*** *If the number of cells with Correctable HEC Byte Errors reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cells with Correctable HEC Byte Error Count Register - Byte 2 (Address = 0x1731)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received Cells with Correctable HEC Byte Error Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Received Cells with Correctable HEC Byte Error Count[23:16]	RUR	**Received Cells with Correctable HEC Byte Error Count[23:16]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Cells with Correctable HEC Byte Error Count - Bytes 3, 1 and 0 registers contain the 32-bit expression for the number of cells (containing correctable HEC byte errors) that have been received since the last read of these registers. ***NOTE:*** *If the number of cells with Correctable HEC Byte Errors reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cells with Correctable HEC Byte Error Count Register - Byte 1 (Address = 0x1732)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received Cells with Correctable HEC Byte Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Received Cells with Correctable HEC Byte Error Count[15:8]	RUR	**Received Cells with Correctable HEC Byte Error Count[15:8]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Cells with Correctable HEC Byte Error Count - Bytes 3, 2 and 0 registers contain the 32-bit expression for the number of cells (containing correctable HEC byte errors) that have been received since the last read of these registers. If the number of cells with Correctable HEC Byte Errors reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

Receive ATM Cell Processor Block - Receive ATM Cells with Correctable HEC Byte Error Count Register - Byte 0 (Address = 0x1733)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received Cells with Correctable HEC Byte Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Received Cells with Correctable HEC Byte Error Count[7:0]	RUR	**Received Cells with Correctable HEC Byte Error Count[7:0]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Cells with Correctable HEC Byte Error Count - Bytes 3 through 1 registers contain the 32-bit expression for the number of cells (containing correctable HEC byte errors) that have been received since the last read of these registers. This particular register byte contains the LSB (Least Significant Byte) of this 32-bit value for the number of Received ATM cells with Correctable HEC Byte Errors. ***NOTE:*** *If the number of cells with Correctable HEC Byte Errors reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cells with Uncorrectable HEC Byte Error Count Register - Byte 3 (Address = 0x1734)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received Cells with Uncorrectable HEC Byte Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Received Cells with Uncorrectable HEC Byte Error Count[31:24]	RUR	**Received Cells with Uncorrectable HEC Byte Error Count[31:24]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Cells with Uncorrectable HEC Byte Error Count - Bytes 2 through 0 registers contain the 32-bit expression for the number of cells (containing Uncorrectable HEC byte errors) that have been received since the last read of these registers. This particular register byte contains the MSB (Most Significant Byte) of this 32-bit value for the number of Received ATM cells with Uncorrectable HEC Byte Errors. ***NOTE:*** *If the number of cells with Uncorrectable HEC Byte Errors reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cells with Uncorrectable HEC Byte Error Count Register - Byte 2 (Address = 0x1735)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received Cells with Uncorrectable HEC Byte Error Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Received Cells with Uncorrectable HEC Byte Error Count[23:16]	RUR	**Received Cells with Uncorrectable HEC Byte Error Count[23:16]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Cells with Uncorrectable HEC Byte Error Count - Bytes 3, 1 and 0 registers contain the 32-bit expression for the number of cells (containing Uncorrectable HEC byte errors) that have been received since the last read of these registers. ***NOTE:*** *If the number of cells with Uncorrectable HEC Byte Errors reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cells with Uncorrectable HEC Byte Error Count Register - Byte 1 (Address = 0x1736)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received Cells with Uncorrectable HEC Byte Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Received Cells with Uncorrectable HEC Byte Error Count[15:8]	RUR	**Received Cells with Uncorrectable HEC Byte Error Count[15:8]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Cells with Uncorrectable HEC Byte Error Count - Bytes 3, 2 and 0 registers contain the 32-bit expression for the number of cells (containing Uncorrectable HEC byte errors) that have been received since the last read of these registers. ***NOTE:*** *If the number of cells with Uncorrectable HEC Byte Errors reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive ATM Cells with Uncorrectable HEC Byte Error Count Register - Byte 0 (Address = 0x1737)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received Cells with Uncorrectable HEC Byte Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Received Cells with Uncorrectable HEC Byte Error Count[7:0]	RUR	**Received Cells with Uncorrectable HEC Byte Error Count[7:0]:** These RESET-upon-READ bit-fields, along with that within the Receive ATM Cell Processor Block - Receive Cells with Uncorrectable HEC Byte Error Count - Bytes 3 through 1 registers contain the 32-bit expression for the number of cells (containing Uncorrectable HEC byte errors) that have been received since the last read of these registers. This particular register byte contains the LSB (Least Significant Byte) of this 32-bit value for the number of Received ATM cells with Uncorrectable HEC Byte Errors. ***NOTE:*** *If the number of cells with Uncorrectable HEC Byte Errors reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter Control - Filter 0 (Address = 0x1743)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Receive User Cell Filter # 0 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Receive User Cell Filter # 0 Enable	R/W	**Receive User Cell Filter # 0 - Enable:** This READ/WRITE bit-field permits the user to either enable or disable Receive User Cell Filter # 0. If the user enables Receive User Cell Filter # 0, then User Cell Filter # 0 will function per the configuration settings in Bits 2 through 0, within this register. If the user disables Receive User Cell Filter # 0, then User Cell Filter # 0 then all cells that are applied to the input of Receive User Cell Filter # 0 will pass through to the output of Receive User Cell Filter # 0. 0 - Disables Receive User Cell Filter # 0. 1 - Enables Receive User Cell Filter # 0.
2	Copy Cell Enable	R/W	**Copy Cell Enable - Receive User Cell Filter # 0:** This READ/WRITE bit-field permits the user to either configure Receive User Cell Filter # 0 (within the Receive ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the user-defined criteria, per Receive User Cell Filter # 0, or to NOT copy any of these cells. If the user configures Receive User Cell Filter # 0 to copy all cells complying with a certain header-byte pattern, then a copy (or replicate) of this compliant ATM cell will be routed to the Receive Cell Extraction Buffer. If the user configures Receive User Cell Filter # 0 to NOT copy all cells complying with a certain header-byte pattern, then NO copies (or replicates) of these compliant ATM cells will be made nor will any be routed to the Receive Cell Extraction Buffer. 0 - Configures Receive User Cell Filter # 0 to NOT copy any cells that have header byte patterns which are compliant with the user-defined filtering criteria. 1 - Configures Receive User Cell Filter # 0 to copy any cells that have header byte patterns that are compliant with the user-defined filtering criteria, and to route these copies (of cells) to the Receive Cell Extraction Buffer. ***NOTE:*** *This bit-field is only active if Receive User Cell Filter # 0 has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Discard Cell Enable	R/W	**Discard Cell Enable - Receive User Cell Filter # 0:** This READ/WRITE bit-field permits the user to either configure Receive User Cell Filter # 0 (within the Receive ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the user-defined criteria, per Receive User Cell Filter # 0, or NOT discard any of these cells. If the user configures Receive User Cell Filter # 0 to NOT discard any cells that is compliant with a certain header-byte pattern, then the cell will be retained for further processing. 0 - Configures Receive User Cell Filter # 0 to NOT discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. 1 - Configures Receive User Cell Filter # 0 to discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. ***NOTE:*** *This bit-field is only active if Receive User Cell Filter # 0 has been enabled.*
0	Filter if Pattern Match	R/W	**Filter if Pattern Match - Receive User Cell Filter # 0:** This READ/WRITE bit-field permits the user to either configure Receive User Cell Filter # 0 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the user-defined header byte patterns, or to filter ATM cells with header bytes that do NOT match the user-defined header byte patterns. 0 - Configures Receive User Cell Filter # 0 to filter user cells that do NOT match the header byte patterns (as defined in the "? " registers). 1 - Configures Receive User Cell Filter # 0 to filter user cells that do match the header byte patterns (as defined in the "? " registers). ***NOTE:*** *This bit-field is only active if Receive User Cell Filter # 0 has been enabled.*

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 1 (Address = 0x1744)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Pattern Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Pattern Register - Header Byte 1	R/W	**Receive User Cell Filter # 0 - Pattern Register - Header Byte 1:** The User Cell filtering criteria (for Receive User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Header Byte 1 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 2 (Address = 0x1745)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Pattern Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Pattern Register - Header Byte 2	R/W	**Receive User Cell Filter # 0 - Pattern Register - Header Byte 2:** The User Cell filtering criteria (for Receive User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Header Byte 2 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 3 (Address = 0x1746)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Pattern Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Pattern Register - Header Byte 3	R/W	**Receive User Cell Filter # 0 - Pattern Register - Header Byte 3:** The User Cell filtering criteria (for Receive User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Header Byte 3 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 4 (Address = 0x1747)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Pattern Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Pattern Register - Header Byte 4	R/W	**Receive User Cell Filter # 0 - Pattern Register - Header Byte 4:** The User Cell filtering criteria (for Receive User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Header Byte 4 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Byte 1 (Address = 0x1748)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Check Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Check Register - Header Byte 1	R/W	**Receive User Cell Filter # 0 - Check Register - Header Byte 1:** The User Cell filtering criteria (for Receive User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 1 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 1 by the User Cell Filter, when determine whether to filter a given User Cell .Writing a "1" to a particular bit-field in this register, forces the Receive User Cell Filter to check and compare the corresponding bit in Octet # 1 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 1. Writing a "0" to a particular bit-field in this register causes the Receive User Cell Filter to treat the corresponding bit within Octet # 1 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 1 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 1).

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Byte 2 (Address = 0x1749)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Check Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Check Register - Header Byte 2	R/W	**Receive User Cell Filter # 0 - Check Register - Header Byte 2:** The User Cell filtering criteria (for Receive User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 2 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 2 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Receive User Cell Filter to check and compare the corresponding bit in Octet # 2 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 2. Writing a "0" to a particular bit-field in this register causes the Receive User Cell Filter to treat the corresponding bit within Octet # 2 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 2 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 2).

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Byte 3 (Address = 0x174A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Receive User Cell Filter # 0 - Check Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Check Register - Header Byte 3	R/W	**Receive User Cell Filter # 0 - Check Register - Header Byte 3:** The User Cell filtering criteria (for Receive User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 3 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 3 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Receive User Cell Filter to check and compare the corresponding bit in Octet # 3 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 3. Writing a "0" to a particular bit-field in this register causes the Receive User Cell Filter to treat the corresponding bit within Octet # 3 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 3 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 3).

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Register - Byte 4 (Address = 0x174B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Check Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Check Register - Header Byte 4	R/W	**Receive User Cell Filter # 0 - Check Register - Header Byte 4:** The User Cell filtering criteria (for Receive User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 4 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 4 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Receive User Cell Filter to check and compare the corresponding bit in Octet # 4 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 4. Writing a "0" to a particular bit-field in this register causes the Receive User Cell Filter to treat the corresponding bit within Octet # 4 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 4 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Pattern Register - Header Byte 4).

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Filtered Cell Count - Byte 3 (Address = 0x174C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Filtered Cell Count[31:24]	RUR	**Receive User Cell Filter # 0 - Filtered Cell Count[31:24]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Filtered Cell Count - Bytes 2 through 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Receive User Cell Filter # 0 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 0 Register (Address = 0x1743), these register bits will be incremented anytime User Cell Filter # 0 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer. • Both of these actions. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Filtered Cell Count - Byte 2 (Address = 0x174D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Filtered Cell Count[23:16]	RUR	**Receive User Cell Filter # 0 - Filtered Cell Count[23:16]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Filtered Cell Count - Bytes 3, 1 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Receive User Cell Filter # 0 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - Receive User Cell Filter # 0 Register (Address = 0x1743), these register bits will be incremented anytime User Cell Filter # 0 performs any of the following functions. • Discards an incoming User Cell • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Filtered Cell Count - Byte 1 (Address = 0x174E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Filtered Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Filtered Cell Count[15:8]	RUR	**Receive User Cell Filter # 0 - Filtered Cell Count[15:8]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Filtered Cell Count - Bytes 3, 2 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Receive User Cell Filter # 0 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - Receive User Cell Filter # 0 Register (Address = 0x1743), these register bits will be incremented anytime Receive User Cell Filter # 0 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer.· • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Filtered Cell Count - Byte 0 (Address = 0x174F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive User Cell Filter # 0 - Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Receive User Cell Filter # 0 - Filtered Cell Count[7:0]	RUR	**Receive User Cell Filter # 0 - Filtered Cell Count[7:0]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 0 - Filtered Cell Count - Bytes 3 through 1 register contain a 32-bit expression for the number of User Cells that have been filtered by Receive User Cell Filter # 0 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - Receive User Cell Filter # 0 Register (Address = 0x1743), these register bits will be incremented anytime Receive User Cell Filter # 0 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer. • Both of these actions. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter Control - Filter 1 (Address = 0x1753)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				User Cell Filter # 1 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	User Cell Filter # 1 Enable	R/W	**User Cell Filter # 1 - Enable:** This READ/WRITE bit-field permits the user to either enable or disable User Cell Filter # 1. If the user enables User Cell Filter # 1, then User Cell Filter # 0 will function per the configuration settings in Bits 2 through 0, within this register. If the user disables User Cell Filter # 1, then User Cell Filter # 0 then all cells that are applied to the input of User Cell Filter # 1 will pass through to the output of User Cell Filter # 1. 0 - Disables User Cell Filter # 1. 1 - Enables User Cell Filter # 1.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Copy Cell Enable	R/W	**Copy Cell Enable - User Cell Filter # 1:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 1 (within the Receive ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the user-defined criteria, per User Cell Filter # 1, or to NOT copy any of these cells. If the user configures User Cell Filter # 1 to copy all cells complying with a certain header-byte pattern, then a copy (or replicate) of this compliant ATM cell will be routed to the Receive Cell Extraction Buffer .If the user configures User Cell Filter # 1 to NOT copy all cells complying with a certain header-byte pattern, then NO copies (or replicates) of these compliant ATM cells will be made nor will any be routed to the Receive Cell Extraction Buffer. 0 - Configures User Cell Filter # 1 to NOT copy any cells that have header byte patterns which are compliant with the user-defined filtering criteria. 1 - Configures User Cell Filter # 1 to copy any cells that have header byte patterns that are compliant with the user-defined filtering criteria, and to route these copies (of cells) to the Receive Cell Extraction Buffer. ***NOTE:*** *This bit-field is only active if User Cell Filter # 0 has been enabled.*
1	Discard Cell Enable	R/W	**Discard Cell Enable - User Cell Filter # 1:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 1 (within the Receive ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the user-defined criteria, per User Cell Filter # 1, or NOT discard any of these cells. If the user configures User Cell Filter # 1 to NOT discard any cells that is compliant with a certain header-byte pattern, then the cell will be retained for further processing. 0 - Configures User Cell Filter # 1 to NOT discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. 1 - Configures User Cell Filter # 1 to discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. ***NOTE:*** *This bit-field is only active if User Cell Filter # 1 has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Filter if Pattern Match	R/W	**Filter if Pattern Match - User Cell Filter # 1:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 1 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the user-defined header byte patterns, or to filter ATM cells with header bytes that do NOT match the user-defined header byte patterns 0 - Configures User Cell Filter # 1 to filter user cells that do NOT match the header byte patterns (as defined in the "? " registers). 1 - Configures User Cell Filter # 1 to filter user cells that do match the header byte patterns (as defined in the "? " registers). ***NOTE:*** *This bit-field is only active if User Cell Filter # 1 has been enabled.*

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 1 (Address = 0x1754)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Pattern Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Pattern Register - Header Byte 1	R/W	**User Cell Filter # 1 - Pattern Register - Header Byte 1:** The User Cell filtering criteria (for User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Header Byte 1 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 2 (Address = 0x1755)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Pattern Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Pattern Register - Header Byte 2	R/W	**User Cell Filter # 1 - Pattern Register - Header Byte 2:** The User Cell filtering criteria (for User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Header Byte 2 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 3 (Address = 0x1756)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Pattern Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Pattern Register - Header Byte 3	R/W	**User Cell Filter # 1 - Pattern Register - Header Byte 3:** The User Cell filtering criteria (for User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Header Byte 3 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 4 (Address = 0x1757)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Pattern Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Pattern Register - Header Byte 4	R/W	**User Cell Filter # 1 - Pattern Register - Header Byte 4:** The User Cell filtering criteria (for User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Header Byte 4 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Byte 1 (Address = 0x1758)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Check Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Check Register - Header Byte 1	R/W	**User Cell Filter # 1 - Check Register - Header Byte 1:** The User Cell filtering criteria (for User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 1 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 1 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in Octet # 1 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter #1 - Pattern Register - Header Byte 1. Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within Octet # 1 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 1 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 1).

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Byte 2 (Address = 0x1759)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Check Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Check Register - Header Byte 2	R/W	**User Cell Filter # 1 - Check Register - Header Byte 2:** The User Cell filtering criteria (for User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 2 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 2 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in Octet # 2 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 2. Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within Octet # 2 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 2 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 2).

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Byte 3 (Address = 0x175A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Check Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Check Register - Header Byte 3	R/W	**User Cell Filter # 1 - Check Register - Header Byte 3:** The User Cell filtering criteria (for User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 3 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 3 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in Octet # 3 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 3. Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within Octet # 3 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 3 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 3).

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Register - Byte 4 (Address = 0x175B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 Check Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Check Register - Header Byte 4	R/W	**User Cell Filter # 1 - Check Register - Header Byte 4:** The User Cell filtering criteria (for User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 4 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 4 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in Octet # 4 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 4. Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within Octet # 4 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 4 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Pattern Register - Header Byte 4).

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Filtered Cell Count - Byte 3 (Address = 0x175C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Filtered Cell Count[31:24]	RUR	**User Cell Filter # 1 - Filtered Cell Count[31:24]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Filtered Cell Count - Bytes 2 through 0 register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 1 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 1 Register (Address = 0x1753), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer. • Both of these actions. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Filtered Cell Count - Byte 2 (Address = 0x175D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Filtered Cell Count[23:16]	RUR	User Cell Filter # 1 - Filtered Cell Count[23:16]: These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Filtered Cell Count - Bytes 3, 1 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 1 since the last read of this register.Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 1 Register (Address = 0x1753), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Filtered Cell Count - Byte 1 (Address = 0x175E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Filtered Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Filtered Cell Count[15:8]	RUR	**User Cell Filter # 1 - Filtered Cell Count[15:8]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Filtered Cell Count - Bytes 3, 2 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 1 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 1 Register (Address = 0x1753), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Filtered Cell Count - Byte 0 (Address = 0x175F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 1 - Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 1 - Filtered Cell Count[7:0]	RUR	**User Cell Filter # 1 - Filtered Cell Count[7:0]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 1 - Filtered Cell Count - Bytes 3 through 1 register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 1 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 1 Register (Address = 0x1753), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer. • Both of these actions. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter Control - Filter 2 (Address = 0x1763)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				User Cell Filter # 0 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	User Cell Filter # 2 Enable	R/W	**User Cell Filter # 2 - Enable:** This READ/WRITE bit-field permits the user to either enable or disable User Cell Filter # 2. If the user enables User Cell Filter # 0, then User Cell Filter # 2 will function per the configuration settings in Bits 2 through 0, within this register. If the user disables User Cell Filter # 2, then User Cell Filter # 0 then all cells that are applied to the input of User Cell Filter # 2 will pass through to the output of User Cell Filter # 2. 0 - Disables User Cell Filter # 2. 1 - Enables User Cell Filter # 2.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Copy Cell Enable	R/W	**Copy Cell Enable - User Cell Filter # 2:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 2 (within the Receive ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the user-defined criteria, per User Cell Filter # 2, or to NOT copy any of these cells. If the user configures User Cell Filter # 2 to copy all cells complying with a certain header-byte pattern, then a copy (or replicate) of this compliant ATM cell will be routed to the Receive Cell Extraction Buffer. If the user configures User Cell Filter # 2 to NOT copy all cells complying with a certain header-byte pattern, then NO copies (or replicates) of these compliant ATM cells will be made nor will any be routed to the Receive Cell Extraction Buffer. 0 - Configures User Cell Filter # 2 to NOT copy any cells that have header byte patterns which are compliant with the user-defined filtering criteria. 1 - Configures User Cell Filter # 2 to copy any cells that have header byte patterns that are compliant with the user-defined filtering criteria, and to route these copies (of cells) to the Receive Cell Extraction Buffer. ***NOTE:*** *This bit-field is only active if User Cell Filter # 0 has been enabled.*
1	Discard Cell Enable	R/W	**Discard Cell Enable - User Cell Filter # 0:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 2 (within the Receive ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the user-defined criteria, per User Cell Filter # 2, or NOT discard any of these cells. If the user configures User Cell Filter # 2 to NOT discarded any cells that is compliant with a certain header-byte pattern, then the cell will be retained for further processing. 0 - Configures User Cell Filter # 2 to NOT discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. 1 - Configures User Cell Filter # 2 to discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. ***NOTE:*** *This bit-field is only active if User Cell Filter # 0 has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Filter if Pattern Match	R/W	**Filter if Pattern Match - User Cell Filter # 0:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 2 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the user-defined header byte patterns, or to filter ATM cells with header bytes that do NOT match the user-defined header byte patterns. 0 - Configures User Cell Filter # 2 to filter user cells that do NOT match the header byte patterns (as defined in the "? " registers). 1 - Configures User Cell Filter # 2 to filter user cells that do match the header byte patterns (as defined in the "? " registers). ***NOTE:*** *This bit-field is only active if "User Cell Filter # 2" has been enabled.*

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 1 (Address = 0x1764)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Pattern Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Pattern Register - Header Byte 1	R/W	**User Cell Filter # 2 - Pattern Register - Header Byte 1:** The User Cell filtering criteria (for User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Registers", the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Registers" and the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that the user wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Header Byte 1" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 2 (Address = 0x1765)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Pattern Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 0 - Pattern Register - Header Byte 2	R/W	**User Cell Filter # 2 - Pattern Register - Header Byte 2:** The User Cell filtering criteria (for User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Registers", the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Registers" and the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that the user wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 3 (Address = 0x1766)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Pattern Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Pattern Register - Header Byte 3	R/W	**User Cell Filter # 2 - Pattern Register - Header Byte 3:** The User Cell filtering criteria (for User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Registers", the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Registers" and the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that the user wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 4 (Address = 0x1767)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Pattern Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Pattern Register - Header Byte 4	R/W	**User Cell Filter # 2 - Pattern Register - Header Byte 4:** The User Cell filtering criteria (for User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Registers", the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Registers" and the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that the user wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Byte 1 (Address = 0x1768)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Check Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Check Register - Header Byte 1	R/W	**User Cell Filter # 2 - Check Register - Header Byte 1:** The User Cell filtering criteria (for User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Registers", the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Registers" and the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 1" by the User Cell Filter, when determine whether to "filter" a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 1". Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 1").

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Byte 2 (Address = 0x1769)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Check Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Check Register - Header Byte 2	R/W	**User Cell Filter # 2 - Check Register - Header Byte 2:** The User Cell filtering criteria (for User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Registers", the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Registers" and the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 2". Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 2").

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Byte 3 (Address = 0x176A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Check Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Check Register - Header Byte 3	R/W	**User Cell Filter # 2 - Check Register - Header Byte 3:** The User Cell filtering criteria (for User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Registers", the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Registers" and the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 3" by the User Cell Filter, when determine whether to "filter" a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 3". Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 3").

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Register - Byte 4 (Address = 0x176B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Check Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Check Register - Header Byte 4	R/W	User Cell Filter # 2 - Check Register - Header Byte 4: The User Cell filtering criteria (for User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Registers", the four "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Check Registers" and the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 4". Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Pattern Register - Header Byte 4").

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Filtered Cell Count - Byte 3 (Address = 0x176C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Filtered Cell Count[31:24]	RUR	**User Cell Filter # 2 - Filtered Cell Count[31:24]:** These RESET-upon-READ bit-fields, along with that in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Filtered Cell Count - Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 2 since the last read of this register. Depending upon the configuration settings within the "Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 2" Register (Address = 0x1763), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions. • Discards an incoming "User Cell". • Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Receive Cell Extraction Buffer. • Both of these actions. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of "filtered cells" reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Filtered Cell Count - Byte 2 (Address = 0x176D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Filtered Cell Count[23:16]	RUR	**User Cell Filter # 2 - Filtered Cell Count[23:16]:** These RESET-upon-READ bit-fields, along with that in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Filtered Cell Count - Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 2 since the last read of this register. Depending upon the configuration settings within the "Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 2" Register (Address = 0x1763), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions. • Discards an incoming "User Cell". • Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Receive Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of "filtered cells" reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Filtered Cell Count - Byte 1 (Address = 0x176E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Filtered Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Filtered Cell Count[15:8]	RUR	**User Cell Filter # 2 - Filtered Cell Count[15:8]:** These RESET-upon-READ bit-fields, along with that in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Filtered Cell Count - Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 2 since the last read of this register. Depending upon the configuration settings within the "Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 2" Register (Address = 0x1763), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions. • Discards an incoming "User Cell". • Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Receive Cell Extraction Buffer.· • Both of these actions. ***NOTE:*** *If the number of "filtered cells" reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Filtered Cell Count - Byte 0 (Address = 0x176F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 2 - Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 2 - Filtered Cell Count[7:0]	RUR	**User Cell Filter # 2 - Filtered Cell Count[7:0]:** These RESET-upon-READ bit-fields, along with that in the "Receive ATM Cell Processor Block - Receive User Cell Filter # 2 - Filtered Cell Count - Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 2 since the last read of this register. Depending upon the configuration settings within the "Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 2" Register (Address = 0x1763), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions. • Discards an incoming "User Cell". • Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Receive Cell Extraction Buffer. • Both of these actions. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of "filtered cells" reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter Control - Filter 3 (Address = 0x1773)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				User Cell Filter # 3 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	User Cell Filter # 3 Enable	R/W	**User Cell Filter # 3 - Enable:** This READ/WRITE bit-field permits the user to either enable or disable User Cell Filter # 3. If the user enables User Cell Filter # 3, then User Cell Filter # 3 will function per the configuration settings in Bits 2 through 0, within this register. If the user disables User Cell Filter # 3, then User Cell Filter # 3 then all cells that are applied to the input of User Cell Filter # 3 will pass through to the output of User Cell Filter # 3. 0 - Disables User Cell Filter # 3. 1 - Enables User Cell Filter # 3.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Copy Cell Enable	R/W	**Copy Cell Enable - User Cell Filter # 3:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 3 (within the Receive ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per User Cell Filter # 3, or to NOT copy any of these cells. If the user configures User Cell Filter # 3 to copy all cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed to the Receive Cell Extraction Buffer. If the user configures User Cell Filter # 3 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Receive Cell Extraction Buffer. 0 - Configures User Cell Filter # 3 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria. 1 - Configures User Cell Filter # 3 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Receive Cell Extraction Buffer. ***NOTE:*** *This bit-field is only active if "User Cell Filter # 0" has been enabled.*
1	Discard Cell Enable	R/W	**Discard Cell Enable - User Cell Filter # 3:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 3 (within the Receive ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per User Cell Filter # 3, or NOT discard any of these cells. If the user configures User Cell Filter # 3 to NOT discarded any cells that is compliant with a certain "header-byte" pattern, then the cell will be retained for further processing. 0 - Configures User Cell Filter # 3 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria. 1 - Configures User Cell Filter # 3 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria. ***NOTE:*** *This bit-field is only active if "User Cell Filter # 3" has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Filter if Pattern Match	R/W	**Filter if Pattern Match - User Cell Filter # 3:** This READ/WRITE bit-field permits the user to either configure User Cell Filter # 3 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns. 0 - Configures User Cell Filter # 3 to filter user cells that do NOT match the header byte patterns (as defined in the "? " registers). 1 - Configures User Cell Filter # 3 to filter user cells that do match the header byte patterns (as defined in the "? " registers). ***NOTE:*** *This bit-field is only active if User Cell Filter # 3 has been enabled.*

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 1 (Address = 0x1774)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Pattern Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Pattern Register - Header Byte 1	R/W	User Cell Filter # 3 - Pattern Register - Header Byte 1: The User Cell filtering criteria (for User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Header Byte 1 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 2 (Address = 0x1775)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Pattern Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Pattern Register - Header Byte 2	R/W	**User Cell Filter # 3 - Pattern Register - Header Byte 2:** The User Cell filtering criteria (for User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Header Byte 2 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 3 (Address = 0x1776)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Pattern Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Pattern Register - Header Byte 3	R/W	**User Cell Filter # 3 - Pattern Register - Header Byte 3:** The User Cell filtering criteria (for User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Header Byte 3 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 4 (Address = 0x1777)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Pattern Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Pattern Register - Header Byte 4	R/W	**User Cell Filter # 3 - Pattern Register - Header Byte 4:** The User Cell filtering criteria (for User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Header Byte 4 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Byte 1 (Address = 0x1778)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Check Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Check Register - Header Byte 1	R/W	**User Cell Filter # 3 - Check Register - Header Byte 1:** The User Cell filtering criteria (for User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 1 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 1 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in Octet # 1 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 1. Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within Octet # 1 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 1 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 1).

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Byte 2 (Address = 0x1779)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Check Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Check Register - Header Byte 2	R/W	**User Cell Filter # 3 - Check Register - Header Byte 2:** The User Cell filtering criteria (for User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 2 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 2 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in Octet # 2 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 2. Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within Octet # 2 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 2 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 2).

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Byte 3 (Address = 0x177A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Check Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Check Register - Header Byte 3	R/W	**User Cell Filter # 3 - Check Register - Header Byte 3:** The User Cell filtering criteria (for User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 3 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 3 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in Octet # 3 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 3. Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within Octet # 3 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 3 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 3).

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Register - Byte 4 (Address = 0x177B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Check Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Check Register - Header Byte 4	R/W	**User Cell Filter # 3 - Check Register - Header Byte 4:** The User Cell filtering criteria (for User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Registers, the four Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Check Registers and the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 4 of the incoming user cell (in the Receive ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 4 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the User Cell Filter to check and compare the corresponding bit in Octet # 4 (of the incoming user cell) with the corresponding bit in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 4. Writing a "0" to a particular bit-field in this register causes the User Cell Filter to treat the corresponding bit within Octet # 4 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 4 of the incoming user cell with the corresponding bit-field in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Pattern Register - Header Byte 4).

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Filtered Cell Count - Byte 3 (Address = 0x177C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Filtered Cell Count[31:24]	RUR	User Cell Filter # 3 - Filtered Cell Count[31:24]: These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Filtered Cell Count - Bytes 2 through 0 register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 3 Register (Address = 0x1773), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer.· • Both of these actions. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Filtered Cell Count - Byte 2 (Address = 0x177D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Filtered Cell Count[23:16]	RUR	User Cell Filter # 3 - Filtered Cell Count[23:16]: These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Filtered Cell Count - Bytes 3, 1 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 3 since the last read of this register.Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 3 Register (Address = 0x1773), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions.· Discards an incoming User Cell.· Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer.· Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Filtered Cell Count - Byte 1 (Address = 0x177E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Filtered Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Filtered Cell Count[15:8]	RUR	**User Cell Filter # 3 - Filtered Cell Count[15:8]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Filtered Cell Count - Bytes 3, 2 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 3 Register (Address = 0x1773), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Filtered Cell Count - Byte 0 (Address = 0x177F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
User Cell Filter # 3 - Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	User Cell Filter # 3 - Filtered Cell Count[7:0]	RUR	**User Cell Filter # 3 - Filtered Cell Count[7:0]:** These RESET-upon-READ bit-fields, along with that in the Receive ATM Cell Processor Block - Receive User Cell Filter # 3 - Filtered Cell Count - Bytes 3 through 1 register contain a 32-bit expression for the number of User Cells that have been filtered by User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the Receive ATM Cell Processor Block - Receive User Cell Filter Control - User Cell Filter # 3 Register (Address = 0x1773), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming User Cell.· • Copies (or Replicates) an incoming User Cell and routes the copy to the Receive Cell Extraction Buffer.· • Both of these actions. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

RECEIVE PPP PACKET PROCESSOR BLOCK (PPP APPLICATIONS ONLY)

THE RECEIVE PPP PACKET PROCESSOR BLOCK

This section presents the Register Description/Address Map of the control registers associated with the Receive PPP Packet Processor Block.

RECEIVE PPP PACKET PROCESSOR BLOCK REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x1700 - 0x1702	Reserved	R/O	0x00
0x1703	Receive PPP Packet Processor - Control Register	R/W	0x00
0x1704 - 0x170A	Reserved	R/O	0x00
0x170B	Receive PPP Packet Processor - Interrupt Status Register	RUR	0x00
0x170C - 0x170E	Reserved	R/O	0x00
0x170F	Receive PPP Packet Processor - Interrupt Enable Register	R/W	0x00
0x1710	Receive PPP Packet Processor - Good Packet Count Register - Byte 3 (MSB)	RUR	0x00
0x1711	Receive PPP Packet Processor - Good Packet Count Register - Byte 2	RUR	0x00
0x1712	Receive PPP Packet Processor - Good Packet Count Register - Byte 1	RUR	0x00
0x1713	Receive PPP Packet Processor - Good Packet Count Register - Byte 0 (LSB)	RUR	0x00
0x1714	Receive PPP Packet Processor - FCS Error Count Register - Byte 3 (MSB)	RUR	0x00
0x1715	Receive PPP Packet Processor - FCS Error Count Register - Byte 2	RUR	0x00
0x1716	Receive PPP Packet Processor - FCS Error Count Register - Byte 1	RUR	0x00
0x1717	Receive PPP Packet Processor - FCS Error Count Register - Byte 0	RUR	0x00
0x1718	Receive PPP Packet Processor - Aborted Packet Count Register - Byte 3 (MSB)	RUR	0x00
0x1719	Receive PPP Packet Processor - Aborted Packet Count Register - Byte 2	RUR	0x00
0x171A	Receive PPP Packet Processor - Aborted Packet Count Register - Byte 1	RUR	0x00
0x171B	Receive PPP Packet Processor - Aborted Packet Count Register - Byte 0 (LSB)	RUR	0x00
0x171C	Receive PPP Packet Processor - RUNT Packet Count Register - Byte 3 (MSB)	RUR	0x00
0x171D	Receive PPP Packet Processor - RUNT Packet Count Register - Byte 2	RUR	0x00
0x171E	Receive PPP Packet Processor - RUNT Packet Count Register - Byte 1	RUR	0x00
0x171F	Receive PPP Packet Processor - RUNT Packet Count Register - Byte 0 (LSB)	RUR	0x00

Receive PPP Packet Processor Block - Receive PPP Control Register (Address = 0x1703)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Receive CRC-32/ CRC-16*	ABORT Packet upon RxFIFO Overflow Enable	Unused	De-Scram-ble Enable	Delete FCS from Incom-ing Packet	Receive PPP Packet Processor Block Enable
R/O	R/O	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Receive CRC-32/CRC-16*	R/W	**Receive CRC-32/CRC-16* Select:** This READ/WRITE bit-field permits the user to configure the Receive PPP Packet Processor block to either compute and verify a CRC-32 or CRC-16 within the incoming PPP packet-stream. 0 - Configures the Receive PPP Packet Processor block to compute and verify a CRC-16 value within each incoming PPP packet. 1 - Configures the Receive PPP Packet Processor block to compute and verify a CRC-32 value within each incoming PPP packet. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
4	ABORT Packet upon RxFIFO Overflow Enable	R/W	**ABORT Packet upon RxFIFO Overflow Enable:** This READ/WRITE bit-field permits the user to configure the Receive PPP Packet Processor block to automatically abort an incoming PPP packet, anytime an RxFIFO Overflow event occurs. 0 - Disables this Auto-Abort upon RxFIFO Overflow feature. 1 - Enables this Auto-Abort upon RxFIFO Overflow feature. ***NOTE:*** *If the user invokes this feature, then the Receive PPP Packet Processor and Receive POS-PHY Interface blocks will automatically designate each incoming PPP Packet as an erred packet (by pulsing the RxPERR output pin "High" coincident to whenever the very last byte or word of this packet is being placed on the Receive POS-PHY Data Bus) for the duration that this RxFIFO Overflow condition exists.*
3	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Descramble Enable	R/W	**De-Scramble Enable:** This READ/WRITE bit-field permits the user to either enable or disable the De-Scrambler within the Receive PPP Packet Processor block. If the user invokes this features, then the De-Scrambler will use the X^43+1 scrambling polynomial on the payload data within each incoming PPP Packet. 0 - Disables the De-Scrambler within the Receive PPP Packet Processor block. 1 - Enables the De-Scrambler within the Receive PPP Packet Processor block. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
1	Delete FCS from Incoming Packet	R/W	**Delete FCS from the Incoming PPP Packets:** This READ/WRITE bit-field permits the user to configure the Receive PPP Packet Processor block to either retain or remove the FCS byte-fields (from the incoming PPP packet) after it has been verified and prior to it being output via the Receive POS-PHY Interface. 0 - Configures the Receive PPP Packet Processor block to retain the FCS byte-fields within each incoming PPP packet, prior to routing it to the Receive POS-PHY Interface block. 1 - Configures the Receive PPP Packet Processor block to remove the FCS byte-fields from each incoming PPP packet, prior to routing it to the Receive POS-PHY Interface block. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
0	Receive PPP Packet Processor Block Enable	R/W	**Receive PPP Packet Processor Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive PPP Packet Processor block. If the user wishes to operate the XRT79L71 in the PPP Mode, then the user must enable the Receive PPP Packet Processor block. 0 - Disables the Receive PPP Packet Processor block. 1 - Enables the Receive PPP Packet Processor block. ***NOTES:*** 1. *This bit-field is only active if the XRT79L71 has been configured to operate in the PPP Mode.* 2. *The user can invoke a Software RESET to the Receive PPP Packet Processor block by momentarily setting this bit-field to "0".*

Receive PPP Packet Processor - Interrupt Status Register (Address = 0x170B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				RxFIFO Overflow Interrupt Status	Non-Zero FCS Error Count Interrupt Status	Non-Zero Receive ABORT Packet Count Inter-rupt Status	Non-Zero Receive RUNT Packet Count Interrupt Status
R/O	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	RxFIFO Overflow Interrupt Status	RUR	**RxFIFO Overflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the RxFIFO Overflow Interrupt has occurred since the last read of this register, as described below. 0 - Indicates that the RxFIFO Overflow Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the RxFIFO Overflow Interrupt has occurred since the last read of this register.
2	Non-Zero FCS Error Count Interrupt Status	RUR	**Non-Zero FCS Error Count Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Non-Zero FCS Error Count Interrupt has occurred since the last of this register, as described below. 0 - Indicates that the Non-Zero FCS Error Count Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Non-Zero FCS Error Count Interrupt has occurred since the last read of this register. Anytime this particular interrupt occurs, the user is expected to respond to this interrupt by executing the following steps. **a.** To read out the contents of this particular register, and **b.** To read out the contents of the Receive PPP Packet Processor - FCS Error Count Registers (Address = 0x1714 through 0x1717).

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Non-Zero Receive ABORT Packet Count Interrupt Status	RUR	**Non-Zero Receive ABORT Packet Count Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Non-Zero ABORT Error Count Interrupt has occurred since the last read of this register, as described below. 0 - Indicates that the Non-Zero Receive ABORT Packet Count Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Non-Zero Receive ABORT Packet Count Interrupt has occurred since the last read of this register. Anytime this particular interrupt occurs, the user is expected to respond to this interrupt by executing the following steps. **a.** To read out the contents of this particular register, and **b.** To read out the contents of the Receive PPP Packet Processor - Aborted Packet Count Registers (Address = 0x1718 through 0x171B).
0	Non-Zero Receive RUNT Packet Count Interrupt Status	RUR	**Non-Zero Receive RUNT Packet Count Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Non-Zero RUNT Packet Count Interrupt has occurred since the last read of this register, as described below. 0 - Indicates that the Non-Zero Receive RUNT Packet Count Interrupt has NOT occurred since the last reads of this register. 1 - Indicates that the Non-Zero Receive RUNT Packet Count Interrupt has occurred since the last read of this register. Anytime this particular interrupt occurs, the user is expected to respond to this interrupt by executing the following steps. **a.** To read out the contents of this particular register, and **b.** To read out the contents of the Receive PPP Packet Processor - RUNT Packet Count Register (Address = 0x171C through 0x171F).

Receive PPP Packet Processor - Interrupt Enable Register (Address = 0x170F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				RxFIFO Overflow Interrupt Enable	Non-Zero FCS Error Count Interrupt Enable	Non-Zero Receive ABORT Packet Count Interrupt Enable	Non-Zero Receive RUNT Packet Count Interrupt Enable
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	RxFIFO Overflow Interrupt Enable	RUR	**RxFIFO Overflow Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the RxFIFO Overflow Interrupt. If the user enables this interrupt, then the Receive PPP Packet Processor block will generate this interrupt anytime the RxFIFO experiences an Overflow event. 0 - Disables the RxFIFO Overflow Interrupt. 1 - Enables the RxFIFO Overflow Interrupt.
2	Non-Zero FCS Error Count Interrupt Enable	RUR	**Non-Zero FCS Error Count Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Non-Zero FCS Error Count Interrupt. If the user enables this interrupt, then the Receive PPP Packet Processor block will generate an interrupt anytime the Receive PPP Packet Processor - FCS Error Count Registers are incremented from the value "0x00000000" to a "non-zero" value. 0 - Disables the Non-Zero FCS Error Count Interrupt. 1 - Enables the Non-Zero FCS Error Count Interrupt
1	Non-Zero Receive ABORT Packet Count Interrupt Enable	RUR	**Non-Zero Receive ABORT Packet Count Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Non-Zero ABORT Packet Count Interrupt. If the user enables this interrupt, then the Receive PPP Packet Processor block will generate an interrupt anytime the Receive PPP Packet Processor - Aborted Packet Count Registers are incremented from the value "0x00000000" to a "non-zero" value. 0 - Disables the Non-Zero ABORT Packet Count Interrupt 1 - Enables the Non-Zero ABORT Packet Count Interrupt.

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Non-Zero Receive RUNT Packet Count Interrupt Enable	RUR	**Non-Zero RUNT Packet Count Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Non-Zero Receive RUNT Packet Count Interrupt. If the user enables this interrupt, then the Receive PPP Packet Processor block will generate an interrupt anytime the Receive PPP Packet Processor - RUNT Packet Count Registers are incremented from the value "0x00000000" to a "non-zero" value. 0 - Disables the Non-Zero RUNT Packet Count Interrupt. 1 - Enables the Non-Zero RUNT Packet Count Interrupt.

Receive PPP Packet Processor - Good Packet Count Register - Byte 3 (Address = 0x1710)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx_Good_PPP_Packet_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Rx_Good_PPP_Packet_ Count[31:24]	RUR	**Receive Good PPP Packet Count[31:24]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - Good Packet Count Registers - Bytes 2 through 0 contain a 32-bit expression for the number of Good PPP Packets that have been received by the Receive PPP Packet Processor block. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTE:*** *The definition of a Good PPP Packet is any incoming PPP Packet that does not contain any of the following characteristics.* **a.** *Contains FCS Errors* **b.** *Is a RUNT Packet* **c.** *Is an Aborted Packet.*

Receive PPP Packet Processor - Good Packet Count Register - Byte 2 (Address = 0x1711)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx_Good_PPP_Packet_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Rx_Good_PPP_Packet_ Count[23:16]	RUR	**Receive Good PPP Packet Count[23:16]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - Good Packet Count Registers - Bytes 3, 1 and 0 contain a 32-bit expression for the number of Good PPP Packets that have been received by the Receive PPP Packet Processor block. ***NOTE:*** *The definition of a Good PPP Packet is any incoming PPP Packet that does not contain any of the following characteristics.* **a.** *Contains FCS Errors* **b.** *Is a RUNT Packet* **c.** *Is an Aborted Packet.*

Receive PPP Packet Processor - Good Packet Count Register - Byte 1 (Address = 0x1712)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx_Good_PPP_Packet_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Rx_Good_PPP_Packet_ Count[15:8]	RUR	**Receive Good PPP Packet Count[15:8]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - Good Packet Count Registers - Bytes 3, 2 and 0 contain a 32-bit expression for the number of Good PPP Packets that have been received by the Receive PPP Packet Processor block. ***NOTE:*** *The definition of a Good PPP Packet is any incoming PPP Packet that does not contain any of the following characteristics.* **a.** *Contains FCS Errors* **b.** *Is a RUNT Packet* **c.** *Is an Aborted Packet.*

Receive PPP Packet Processor - Good Packet Count Register - Byte 0 (Address = 0x1713)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx_Good_PPP_Packet_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Rx_Good_PPP_Packet_ Count[7:0]	RUR	**Receive Good PPP Packet Count[31:24]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - Good Packet Count Registers - Bytes 3 through 1 contain a 32-bit expression for the number of Good PPP Packets that have been received by the Receive PPP Packet Processor block. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *The definition of a Good PPP Packet is any incoming PPP Packet that does not contain any of the following characteristics.* **a.** *Contains FCS Errors* **b.** *Is a RUNT Packet* **c.** *Is an Aborted Packet.*

Receive PPP Packet Processor - FCS Error Count Register - Byte 3 (Address = 0x1714)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FCS_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	FCS_Error_Count[31:24]	RUR	**FCS Error Count[31:24]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - FCS Error Count Registers - Bytes 2 through 0 contain a 32-bit expression for the number of PPP Packets that have been flagged as containing FCS errors by the Receive PPP Packet Processor block. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.

Receive PPP Packet Processor - FCS Error Count Register - Byte 2 (Address = 0x1715)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FCS_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	FCS_Error_Count[23:16]	RUR	**FCS Error Count[23:16]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - FCS Error Count Registers - Bytes 3, 1 and 0 contain a 32-bit expression for the number of PPP Packets that have been flagged as containing FCS errors by the Receive PPP Packet Processor block.

Receive PPP Packet Processor - FCS Error Count Register - Byte 1 (Address = 0x1716)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FCS_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	FCS_Error_Count[15:8]	RUR	**FCS Error Count[15:8]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - FCS Error Count Registers - Bytes 3, 2 and 0 contain a 32-bit expression for the number of PPP Packets that have been flagged as containing FCS errors by the Receive PPP Packet Processor block.

Receive PPP Packet Processor - FCS Error Count Register - Byte 0 (Address = 0x1717)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FCS_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	FCS_Error_Count[7:0]	RUR	**FCS Error Count[7:0]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - FCS Error Count Registers - Bytes 3 through 1 contain a 32-bit expression for the number of PPP Packets that have been flagged as containing FCS errors by the Receive PPP Packet Processor block.This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.

Receive PPP Packet Processor - Aborted Packet Count Register - Byte 3 (Address = 0x1718)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Aborted_Packet_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Aborted_Packet_Count [31:24]	RUR	**Aborted Packet Count[31:24]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - Aborted Packet Count Registers - Bytes 2 through 0 contain a 32-bit expression for the number of Aborted PPP Packets that have been received by the Receive PPP Packet Processor block. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.

Receive PPP Packet Processor - Aborted Packet Count Register - Byte 2 (Address = 0x1719)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Aborted_Packet_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Aborted_Packet_Count [23:16]	RUR	**Aborted Packet Count[23:16]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - Aborted Packet Count Registers - Bytes 3, 1 and 0 contain a 32-bit expression for the number of Aborted PPP Packets that have been received by the Receive PPP Packet Processor block.

Receive PPP Packet Processor - Aborted Packet Count Register - Byte 1 (Address = 0x171A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Aborted_Packet_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Aborted_Packet_Count [15:8]	RUR	**Aborted Packet Count[15:8]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - Aborted Packet Count Registers - Bytes 3, 2 and 0 contain a 32-bit expression for the number of Aborted PPP Packets that have been received by the Receive PPP Packet Processor block.

Receive PPP Packet Processor - Aborted Packet Count Register - Byte 0 (Address = 0x171B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Aborted_Packet_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Aborted_Packet_Count [7:0]	RUR	**Aborted Packet Count[7:0]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - Aborted Packet Count Registers - Bytes 3 through 1 contain a 32-bit expression for the number of Aborted PPP Packets that have been received by the Receive PPP Packet Processor block. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.

Receive PPP Packet Processor - RUNT Packet Count Register - Byte 3 (Address = 0x171C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RUNT_Packet_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RUNT_Packet_Count [31:24]	RUR	**RUNT Packet Count[31:24]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - RUNT Packet Count Registers - Bytes 2 through 0 contain a 32-bit expression for the number of RUNT PPP Packets that have been received by the Receive PPP Packet Processor block. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.

Receive PPP Packet Processor - RUNT Packet Count Register - Byte 2 (Address = 0x171D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RUNT_Packet_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RUNT_Packet_Count [23:16]	RUR	**RUNT Packet Count[23:16]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - RUNT Packet Count Registers - Bytes 3, 1 and 0 contain a 32-bit expression for the number of RUNT PPP Packets that have been received by the Receive PPP Packet Processor block.

Receive PPP Packet Processor - RUNT Packet Count Register - Byte 1 (Address = 0x171E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RUNT_Packet_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RUNT_Packet_Count [15:8]	RUR	**RUNT Packet Count[15:8]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - RUNT Packet Count Registers - Bytes 3, 2 and 0 contain a 32-bit expression for the number of RUNT PPP Packets that have been received by the Receive PPP Packet Processor block.

Receive PPP Packet Processor - RUNT Packet Count Register - Byte 0 (Address = 0x171F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RUNT_Packet_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RUNT_Packet_Count [7:0]	RUR	**RUNT Packet Count[7:0]:** These RESET-upon-READ bit-fields, along with that of the Receive PPP Packet Processor - RUNT Packet Count Registers - Bytes 3 through 1 contain a 32-bit expression for the number of RUNT PPP Packets that have been received by the Receive PPP Packet Processor block. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.

THE TRANSMIT ATM CELL PROCESSOR BLOCK

This section presents the Register Description/Address Map of the control registers associated with the Transmit ATM Cell Processor block.

TRANSMIT ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
TRANSMIT ATM CELL PROCESSOR/PPP PROCESSOR BLOCK CONTROL REGISTERS			
0x1F00	Transmit ATM Cell Processor Control Register - Byte 3	R/W	0x00
0x1F01	Transmit ATM Cell Processor Control Register - Byte 2	R/W	0x00
0x1F02	Transmit ATM Cell Processor Control Register - Byte 1	R/W	0x00
0x1F03	Transmit ATM Cell/PPP Processor Control Register - Byte 0	R/W	0x00
0x1F04 - 0x1F06	Reserved	R/O	0x00
0x1F07	Transmit ATM Status Register	R/O	0x00
0x1F05 - 0x1F0A	Reserved	R/O	0x00
0x1F0B	Transmit ATM Cell/PPP Processor Interrupt Status Register	RUR	0x00
0x1F0C - 0x1F0E	Reserved	R/O	0x00
0x1F0F	Transmit ATM Cell/PPP Processor Interrupt Enable Register	R/W	0x00
0x1F10 - 0x1F12	Reserved	R/O	0x00
0x1F13	Transmit ATM Cell Insertion/Extraction Memory Control Register	R/O & R/W	0x00
0x1F14	Transmit ATM Cell Insertion/Extraction Memory - Byte 3	R/W	0x00
0x1F15	Transmit ATM Cell Insertion/Extraction Memory - Byte 2	R/W	0x00
0x1F16	Transmit ATM Cell Insertion/Extraction Memory - Byte 1	R/W	0x00
0x1F17	Transmit ATM Cell Insertion/Extraction Memory - Byte 0	R/W	0x00
0x1F18	Transmit ATM Cell - Idle Cell Header Byte # 1 Register	R/W	0x00
0x1F19	Transmit ATM Cell - Idle Cell Header Byte # 2 Register	R/W	0x00
0x1F1A	Transmit ATM Cell - Idle Cell Header Byte # 3 Register	R/W	0x00
0x1F1B	Transmit ATM Cell - Idle Cell Header Byte # 4 Register	R/W	0x00
0x1F1C - 0x1F1E	Reserved	R/O	0x00
0x1F1F	Transmit ATM Cell - Idle Cell Payload Byte Register	R/W	0x00
0x1F20	Transmit ATM Cell - Test Cell Header Byte # 1 Register	R/W	0x00
0x1F21	Transmit ATM Cell - Test Cell Header Byte # 2 Register	R/W	0x00
0x1F22	Transmit ATM Cell - Test Cell Header Byte # 3 Register	R/W	0x00
0x1F23	Transmit ATM Cell - Test Cell Header Byte # 4 Register	R/W	0x00
0x1F24 - 0x1F27	Reserved	R/O	0x00
0x1F28	Transmit ATM Cell - Cell Count Register - Byte 3	RUR	0x00
0x1F29	Transmit ATM Cell - Cell Count Register - Byte 2	RUR	0x00

TRANSMIT ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x1F2A	Transmit ATM Cell - Cell Count Register - Byte 1	RUR	0x00
0x1F2B	Transmit ATM Cell - Cell Count Register - Byte 0	RUR	0x00
0x1F2C	Transmit ATM Cell - Discard Cell Count Register - Byte 3	RUR	0x00
0x1F2D	Transmit ATM Cell - Discard Cell Count Register - Byte 2	RUR	0x00
0x1F2E	Transmit ATM Cell - Discard Cell Count Register - Byte 1	RUR	0x00
0x1F2F	Transmit ATM Cell - Discard Cell Count Register - Byte 0	RUR	0x00
0x1F30	Transmit ATM Cell - HEC Byte Error Count Register - Byte 3	RUR	0x00
0x1F31	Transmit ATM Cell - HEC Byte Error Count Register - Byte 2	RUR	0x00
0x1F32	Transmit ATM Cell - HEC Byte Error Count Register - Byte 1	RUR	0x00
0x1F33	Transmit ATM Cell - HEC Byte Error Count Register - Byte 0	RUR	0x00
0x1F34	Transmit ATM Cell - Parity Error Count Register - Byte 3	RUR	0x00
0x1F35	Transmit ATM Cell - Parity Error Count Register - Byte 2	RUR	0x00
0x1F36	Transmit ATM Cell - Parity Error Count Register - Byte 1	RUR	0x00
0x1F37	Transmit ATM Cell - Parity Error Count Register - Byte 0	RUR	0x00
0x1F38 - 0x1F42	Reserved	R/O	0x00
0x1F43	Transmit ATM Controller - Transmit ATM Filter # 0 Control Register	R/W	0x00
0x1F44	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 1	R/W	0x00
0x1F45	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 2	R/W	0x00
0x1F46	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 3	R/W	0x00
0x1F47	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 4	R/W	0x00
0x1F48	Transmit ATM Controller - Transmit ATM Filter # 0 Check - Header Byte 1	R/W	0x00
0x1F49	Transmit ATM Controller - Transmit ATM Filter # 0 Check - Header Byte 2	R/W	0x00
0x1F4A	Transmit ATM Controller - Transmit ATM Filter # 0 Check - Header Byte 3	R/W	0x00
0x1F4B	Transmit ATM Controller - Transmit ATM Filter # 0 Check - Header Byte 4	R/W	0x00
0x1F4C	Transmit ATM Cell - Cell Count Register - Byte 3	RUR	0x00
0x1F4D	Transmit ATM Cell - Cell Count Register - Byte 2	RUR	0x00
0x1F4E	Transmit ATM Cell - Cell Count Register - Byte 1	RUR	0x00
0x1F4F	Transmit ATM Cell - Cell Count Register - Byte 0	RUR	0x00

TRANSMIT ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x1F50 - 0x1F52	Reserved	R/O	0x00
0x1F53	Transmit ATM Controller - Transmit ATM Filter # 1 Control Register	R/W	0x00
0x1F54	Transmit ATM Controller - Transmit ATM Filter # 1 Pattern - Header Byte 1	R/W	0x00
0x1F55	Transmit ATM Controller - Transmit ATM Filter # 1 Pattern - Header Byte 2	R/W	0x00
0x1F56	Transmit ATM Controller - Transmit ATM Filter # 1 Pattern - Header Byte 3	R/W	0x00
0x1F57	Transmit ATM Controller - Transmit ATM Filter # 1 Pattern - Header Byte 4	R/W	0x00
0x1F58	Transmit ATM Controller - Transmit ATM Filter # 1 Check - Header Byte 1	R/W	0x00
0x1F59	Transmit ATM Controller - Transmit ATM Filter # 1 Check - Header Byte 2	R/W	0x00
0x1F5A	Transmit ATM Controller - Transmit ATM Filter # 1 Check - Header Byte 3	R/W	0x00
0x1F5B	Transmit ATM Controller - Transmit ATM Filter # 1 Check - Header Byte 4	R/W	0x00
0x1F5C	Transmit ATM Cell - Cell Count Register - Byte 3	RUR	0x00
0x1F5D	Transmit ATM Cell - Cell Count Register - Byte 2	RUR	0x00
0x1F5E	Transmit ATM Cell - Cell Count Register - Byte 1	RUR	0x00
0x1F5F	Transmit ATM Cell - Cell Count Register - Byte 0	RUR	0x00
0x1F60 - 0x1F62	Reserved	R/O	0x00
0x1F63	Transmit ATM Controller - Transmit ATM Filter # 2 Control Register	R/W	0x00
0x1F64	Transmit ATM Controller - Transmit ATM Filter # 2 Pattern - Header Byte 1	R/W	0x00
0x1F65	Transmit ATM Controller - Transmit ATM Filter # 2 Pattern - Header Byte 2	R/W	0x00
0x1F66	Transmit ATM Controller - Transmit ATM Filter # 2 Pattern - Header Byte 3	R/W	0x00
0x1F67	Transmit ATM Controller - Transmit ATM Filter # 2 Pattern - Header Byte 4	R/W	0x00
0x1F68	Transmit ATM Controller - Transmit ATM Filter # 2 Check - Header Byte 1	R/W	0x00
0x1F69	Transmit ATM Controller - Transmit ATM Filter # 2 Check - Header Byte 2	R/W	0x00
0x1F6A	Transmit ATM Controller - Transmit ATM Filter # 2 Check - Header Byte 3	R/W	0x00

TRANSMIT ATM CELL PROCESSOR/PPP PACKET PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x1F6B	Transmit ATM Controller - Transmit ATM Filter # 3 Check - Header Byte 4	R/W	0x00
0x1F6C	Transmit ATM Cell - Cell Count Register - Byte 3	RUR	0x00
0x1F6D	Transmit ATM Cell - Cell Count Register - Byte 2	RUR	0x00
0x1F6E	Transmit ATM Cell - Cell Count Register -Byte 1	RUR	0x00
0x1F6F	Transmit ATM Cell - Cell Count Register - Byte 0	RUR	0x00
0x1F70 - 0x1F72	Reserved	R/O	0x00
0x1F73	Transmit ATM Controller - Transmit ATM Filter # 3 Control Register	R/W	0x00
0x1F74	Transmit ATM Controller - Transmit ATM Filter # 3 Pattern - Header Byte 1	R/W	0x00
0x1F75	Transmit ATM Controller - Transmit ATM Filter # 3 Pattern - Header Byte 2	R/W	0x00
0x1F76	Transmit ATM Controller - Transmit ATM Filter # 3 Pattern - Header Byte 3	R/W	0x00
0x1F77	Transmit ATM Controller - Transmit ATM Filter # 3 Pattern - Header Byte 4 - Channe1 N-1	R/W	0x00
0x1F78	Transmit ATM Controller - Transmit ATM Filter # 3 Check - Header Byte 1	R/W	0x00
0x1F79	Transmit ATM Controller - Transmit ATM Filter # 3 Check - Header Byte 2	R/W	0x00
0x1F7A	Transmit ATM Controller - Transmit ATM Filter # 3 Check - Header Byte 3	R/W	0x00
0x1F7B	Transmit ATM Controller - Transmit ATM Filter # 3 Check - Header Byte 4	R/W	0x00
0x1F7C	Transmit ATM Cell - Cell Count Register - Byte 3	RUR	0x00
0x1F7D	Transmit ATM Cell - Cell Count Register - Byte 2	RUR	0x00
0x1F7E	Transmit ATM Cell - Cell Count Register - Byte 1	RUR	0x00
0x1F7F	Transmit ATM Cell - Cell Count Register - Byte 0	RUR	0x00
0x1F80 - 0x2102	Reserved	R/O	0x00

Transmit ATM Cell Processor Block - Transmit ATM Control Register - Byte 2 (Address = 0x1F01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Transmit ATM Cell Processor Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	Transmit ATM Cell Processor Enable	R/W	**Transmit ATM Cell Processor Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit ATM Cell Processor block. If the user wishes to operate a given Channel in the ATM Mode, then the user must enable the Transmit ATM Cell Processor Block. 0 - Disables the Transmit ATM Cell Processor Block 1 - Enables the Transmit ATM Cell Processor Block ***NOTE:*** *The user must set this bit-field to "1" before the user begins to write ATM cell data into the Transmit UTOPIA Interface block.*

Transmit ATM Cell Processor Block - Transmit ATM Control Register - Byte 1 (Address = 0x1F02)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Cell Transmit Mode Enable	ONE SHOT MODE	GFC Insertion Enable - Bit 3 (MSB)	GFC Insertion Enable - Bit 2	GFC Insertion Enable - Bit 1	GFC Insertion Enable - Bit 0 (LSB)	COSET Polynomial Addition	Regenerate HEC Byte Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Test Cell Transmit Mode Enable	R/W	**Test Cell Transmit Mode Enable:** This READ/WRITE bit-field permits the user to enable the Test Cell Transmitter (within the Transmit ATM Cell Processor Block). The user must implement this configuration option in order to perform diagnostic operations with Test Cells. 0 - Disables the Test Cell Transmitter. 1 - Enables the Test Cell Transmitter. ***NOTE:*** *For normal operation, the user should set this bit-field to "1".*
6	One Shot Mode	R/W	**One Shot Mode:** If the user has enabled the Test Cell Transmitter, then this READ/WRITE bit-field permits the user to either configure the Test Cell Transmitter into the One-Shot or in the Continuous Mode. If the user configures the Test Cell Transmitter into the One-Shot Mode, then (whenever the user implements a "0" to "1" transition within Bit 7 [Test Cell Transmit Mode Enable] of this register) then the Test Cell Transmitter will generate and transmit 1024 test cells. Afterwards, the Test Cell Transmitter will halt its transmission of Test Cells until the user implements another "0" to "1" transition within Bit 7 (Test Cell Transmit Mode Enable) within this register. If the user configures the Test Cell Transmitter into the Continuous Mode, then the Test Cell Transmitter will continuously generate and transmit test cells for the duration that Bit 7(Test Cell Transmit Mode Enable) is set to "1". 0 - Configures the Test Cell Transmitter to operate in the Continuous Mode. 1 - Configures the Test Cell Transmitter to operate in the One-Shot Mode.

BIT NUMBER	NAME	TYPE	DESCRIPTION
5	GFC Insertion Enable - Bit 3	R/W	**GFC Insertion Enable - Bit 3 (MSB):** This READ/WRITE bit-field along with GFC Insertion Enable - Bits 2 through 0 permit the user to select the bits (within the GFC nibble of each Outbound ATM cell) that will be modified by the contents that is applied via the Transmit GFC Serial Input port, as described below. 0 - Configures the Transmit GFC Serial Input port to NOT modify the contents of Bit 3 (the most significant bit) within the GFC nibble. 1 - Configures the Transmit GFC Serial Input port to modify the contents of Bit 3 (within the GFC nibble) with the value that is applied via the Transmit GFC Serial Input Port.
4	GFC Insertion Enable - Bit 2	R/W	**GFC Insertion Enable - Bit 2:** This READ/WRITE bit-field along with GFC Insertion Enable - Bits 3, 1 and 0 permit the user to select the bits (within the GFC nibble of each Outbound ATM cell) that will be modified by the contents that is applied via the Transmit GFC Serial Input port, as described below. 0 - Configures the Transmit GFC Serial Input port to NOT modify the contents of Bit 2 within the GFC nibble. 1 - Configures the Transmit GFC Serial Input port to modify the contents of Bit 2 (within the GFC nibble) with the value that is applied via the Transmit GFC Serial Input Port.
3	GFC Insertion Enable - Bit 1	R/W	**GFC Insertion Enable - Bit 1:** This READ/WRITE bit-field along with GFC Insertion Enable - Bits 3, 2 and 0 permit the user to select the bits (within the GFC nibble of each Outbound ATM cell) that will be modified by the contents that is applied via the Transmit GFC Serial Input port, as described below. 0 - Configures the Transmit GFC Serial Input port to NOT modify the contents of Bit 3 (the most significant bit) within the GFC nibble. 1 - Configures the Transmit GFC Serial Input port to modify the contents of Bit 3 (within the GFC nibble) with the value that is applied via the Transmit GFC Serial Input Port.
2	GFC Insertion Enable - Bit 0	R/W	**GFC Insertion Enable - Bit 0 (LSB):** This READ/WRITE bit-field along with GFC Insertion Enable - Bits 2 through 0 permit the user to select the bits (within the GFC nibble of each Outbound ATM cell) that will be modified by the contents that is applied via the Transmit GFC Serial Input port, as described below. 0 - Configures the Transmit GFC Serial Input port to NOT modify the contents of Bit 0 (the least significant bit) within the GFC nibble. 1 - Configures the Transmit GFC Serial Input port to modify the contents of Bit 0 (within the GFC nibble) with the value that is applied via the Transmit GFC Serial Input Port.

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	COSET Polynomial Addition	R/W	**COSET Polynomial Addition:** This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to modulo-add the COSET Polynomial (e.g., x^6 + x^4 + x^2 + 1) to the HEC byte value, within each Outbound ATM cell. 0 - Configures the Transmit ATM Cell Processor block to NOT modulo-add the COSET Polynomial to the HEC byte within each outbound ATM cell. 1 - Configures the Transmit ATM Cell Processor block to modulo-add the COSET Polynomial to the HEC byte within each outbound ATM cell.
0	Regenerate HEC Byte Enable	R/W	**Regenerate HEC Byte Enable:** This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to automatically re-compute and insert a new HEC byte into each ATM cell (that it receives from the Transmit UTOPIA Interface block) that contains an uncorrectable HEC byte. 0 - Does not configure the Transmit ATM Cell Processor block to compute and insert a new HEC byte into ATM cells that contains an uncorrectable HEC Byte error. 1 - Configures the Transmit ATM Cell Processor block to compute and insert a new HEC byte into ATM cells that contains an uncorrectable HEC Byte error.

Transmit ATM Cell Processor Block - Transmit ATM Control - Byte 0 (Address = 0x1F03)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HEC Byte Invert	HEC Byte Check Enable	Transmit UTOPIA Parity Check Enable	Transmit UTOPIA Parity Error - Discard	Transmit UTOPIA - ODD Parity	Reserved		Scrambler Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	HEC Byte Invert	R/W	**HEC Byte Invert:** This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to invert each bit within the newly computed HEC byte of each outbound ATM cell. 0 - Configures the Transmit ATM Cell Processor block to NOT invert the HEC byte values that it inserts into the fifth octet position within each outbound ATM cell. 1 - Configures the Transmit ATM Cell Processor block to invert each bit-field within the newly computed HEC, prior to inserting it into the fifth octet position, within each outbound ATM cell.
6	HEC Byte Check Enable	R/W	**HEC Byte Check Enable:** This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to perform HEC byte checking of all ATM cells that it receives via the Transmit UTOPIA Interface block. 0 - Configures the Transmit ATM Cell Processor block to NOT perform HEC byte checking on all ATM cells that it receives via the Transmit UTOPIA Interface block. 1 - Configures the Transmit ATM Cell Processor block to perform HEC byte checking on all ATM cells that it receives via the Transmit UTOPIA Interface block.
5	Transmit UTOPIA Parity Check Enable	R/W	**Transmit UTOPIA Parity Check Enable:** This READ/WRITE bit-field permits the user to either enable or disable Transmit UTOPIA Interface Parity checking. If the user enables Transmit UTOPIA Interface Parity Checking, then the Transmit ATM Cell Processor block will compute either the EVEN or ODD parity value (depending upon the setting of Bit 3 within this register) of each byte or 16-bit word that is input via the Transmit UTOPIA Data Bus input pins: (TxUData[15:0]). Afterwards, the Transmit ATM Cell Processor block will compare this locally computed parity value with that which the ATM Layer Processor has provided to the TxUPrty input pin. If the Transmit ATM Cell Processor detects any discrepancies between these two parity values (e.g., any parity errors) then it will take action based upon the user's settings for Bit 4 (Transmit UTOPIA Parity Error - Discard). 0 - Disables Transmit UTOPIA Interface Parity Checking. 1 - Enables Transmit UTOPIA Interface Parity Checking.

BIT NUMBER	NAME	TYPE	DESCRIPTION
4	Transmit UTOPIA Parity Error - Discard	R/W	**Transmit UTOPIA Parity Error - Discard Cell:** This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to either discard or retain (for further processing) any ATM cell that contains a Transmit UTOPIA Interface parity error. 0 - Configures the Transmit ATM Cell Processor block to retain (for further processing) all cells that contain Transmit UTOPIA Interface parity errors. 1 - Configures the Transmit ATM Cell Processor block to discard all cells that contain Transmit UTOPIA Interface parity errors. ***NOTE:*** *This bit-field is only valid if Transmit UTOPIA Interface Parity Checking has been enabled.*
3	Transmit UTOPIA - Odd Parity	R/W	**Transmit UTOPIA Parity Value - ODD Parity:** This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to compute either the EVEN or ODD parity value for each byte or 16-bit word within each cell that it processes. Each of these parity values will ultimately be compared with the value that is input via the TxUPrty input pin (on the Transmit UTOPIA Interface block) coincident to when ATM cell data is being applied to the TxUData[15:0] input pins. 0 - Configures the Transmit ATM Cell Processor block to compute and verify the EVEN Parity value of each byte (or 16-bit word) of ATM cell data that it processes. 1 - Configures the Transmit ATM Cell Processor block to compute and verify the ODD Parity value of each byte (or 16-bit word) of ATM cell data that it processes. ***NOTE:*** *This bit-field is only value if Transmit UTOPIA Interface Parity Checking has been enabled.*
2 - 1	Reserved	R/O	
0	Scrambler Enable		**Cell Payload Scrambler Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Cell Payload Scrambler. If the user enables the Cell Payload Scrambler then the Transmit ATM Cell Processor will payload self-synchronous scrambling on all cell payloads bytes (within each outbound ATM cell) with the x^43+1 polynomial. 0 - Disables the Cell Payload Scrambler 1 - Enables the Cell Payload Scrambler

Transmit ATM Cell Processor Block - Transmit ATM Status Register (Address = 0x1F07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							One Shot DONE
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	One Shot DONE	R/O	**One Shot DONE:** This READ-ONLY bit-field indicates whether or not the Test Cell Transmitter has completed its transmission of 1024 test cells, following the instant that the user has commanded the Test Cell to transmit this burst of 1024 cells. 0 - Indicates that the Test Cell Transmitter has NOT completed its transmission of 1024 test cells. 1 - Indicates that the Test Cell Transmitter has completed its transmission of 1024 test cells since the last Transmit Test Cell - One Shot command. ***NOTES:*** *1. This bit-field is only valid if (1) the Test Cell Transmitter is active and (2) if the Test Cell Transmitter has been configured to operate in the One-Shot Mode.* *2. Once this bit-field has been set to "1", it will remain at "1" until the user executes another Transmit Test Cell - One Shot command.*

Transmit ATM Cell Processor Block - Transmit ATM Interrupt Status Register (Address = 0x1F0B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Transmit Cell Extraction Interrupt Status	Transmit Cell Insertion Interrupt Status	Transmit Cell Extraction Memory Overflow Interrupt Status	Transmit Cell Insertion Memory Overflow Interrupt Status	Detection of HEC Byte Error Interrupt Status	Detection of Transmit UTOPIA Parity Error Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Transmit Cell Extraction Interrupt Status	RUR	**Transmit Cell Extraction Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit Cell Extraction interrupt has occurred since the last read of this register. The Transmit ATM Cell Processor block will generate the Transmit Cell Extraction Interrupt anytime it receives an incoming ATM cell (from the TxFIFO) and loads an ATM cell into the Extraction Memory Buffer. 0 - Indicates that the Transmit Cell Extraction Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Transmit Cell Extraction Interrupt has occurred since the last read of this register.
4	Transmit Cell Insertion Interrupt Status	RUR	**Transmit Cell Insertion Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit Cell Insertion interrupt has occurred since the last read of this register. The Transmit ATM Cell Processor block will generate the Transmit Cell Insertion Interrupt anytime a cell (residing in the Transmit Cell Insertion Buffer) is read out of the Transmit Cell Insertion Buffer and is loaded into the outbound ATM cell traffic. 0 - Indicates that the Transmit Cell Insertion Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Transmit Cell Insertion Interrupt has occurred since the last read of this register.

BIT NUMBER	NAME	TYPE	DESCRIPTION
3	Transmit Cell Extraction Memory Overflow Interrupt Status	RUR	**Transmit Cell Extraction Memory Overflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit Cell Extraction Memory Overflow Interrupt has occurred since the last read of this register. The Transmit ATM Cell Processor block will generate this interrupt anytime an overflow event has occurred in the Transmit Cell Extraction Memory Buffer. 0 - Indicates that the Transmit ATM Cell Processor block has NOT declared the Transmit Cell Extraction Memory Overflow Interrupt since the last read of this register. 1 - Indicates that the Transmit ATM Cell Processor block has declared the Transmit Cell Extraction Memory Overflow interrupt since the last read of this register.
2	Transmit Cell Insertion Memory Overflow Interrupt Status	RUR	**Transmit Cell Insertion Memory Overflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit Cell Insertion Memory Overflow Interrupt has occurred since the last read of this register. The Transmit ATM Cell Processor block will generate this interrupt anytime an overflow event has occurred in the Transmit Cell Insertion Memory Buffer. 0 - Indicates that the Transmit ATM Cell Processor block has NOT declared the Transmit Cell Insertion Memory Overflow interrupt since the last read of this register. 1 - Indicates that the Transmit ATM Cell Processor block has declared the Transmit Cell Insertion Memory Overflow interrupt since the last read of this register.
1	Detection of HEC Byte Error Interrupt	RUR	**Detection of HEC Byte Error Interrupt:** This RESET-upon-READ bit-field indicates whether or not the Transmit ATM Cell Processor block has declared the Detection of HEC Byte Error Interrupt since the last read of this register. The Transmit ATM Cell Processor block will generate this interrupt anytime it has received an ATM cell (from the TxFIFO) that contains a HEC byte error. 0 - Indicates that the Transmit ATM Cell Processor block has NOT declared the Detection of HEC Byte Error Interrupt since the last read of this register. 1 - Indicates that the Transmit ATM Cell Processor block has declared the Detection of HEC Byte Error Interrupt since the last read of this register.

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Detection of Transmit UTOPIA Parity Error Interrupt		**Detection of Transmit UTOPIA Parity Error Interrupt:** This RESET-upon-READ bit-field indicates whether or not the Transmit ATM Cell Processor block has declared the Detection of Transmit UTOPIA Parity Error Interrupt since the last read of this register. The Transmit ATM Cell Processor block will generate this interrupt anytime it has received an ATM cell byte or 16-bit word (from the Transmit UTOPIA Interface block) that contains a parity error. 0 - Indicates that the Transmit ATM Cell Processor block has NOT declared the Detection of Transmit UTOPIA Parity Error Interrupt since the last read of this register. 1 - Indicates that the Transmit ATM Cell Processor block has declared the Detection of Transmit UTOPIA Parity Error Interrupt since the last read of this register.

Transmit ATM Cell Processor Block - Transmit ATM Interrupt Enable Register (Address = 0x1F0F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Transmit Cell Extraction Interrupt Enable	Transmit Cell Insertion Interrupt Enable	Transmit Cell Extraction Memory Overflow Interrupt Enable	Transmit Cell Insertion Memory Overflow Interrupt Enable	Detection of HEC Byte Error Interrupt Enable	Detection of Transmit UTOPIA Parity Error Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused		
5	Transmit Cell Extraction Interrupt Enable	R/W	**Transmit Cell Extraction Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit Cell Extraction Interrupt. If the user enables this feature, then the Transmit ATM Cell Processor block will generate the Transmit Cell Extraction Interrupt anytime it receives an incoming ATM cell (from the TxFIFO) and loads this ATM cell into the Transmit Extraction Memory Buffer. 0 - Disables the Transmit Cell Extraction Interrupt. 1 - Enables the Transmit Cell Extraction Interrupt
4	Transmit Cell Insertion Interrupt Enable	R/W	**Transmit Cell Insertion Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit Cell Insertion Interrupt. If the user enables this feature, then the Transmit ATM Cell Processor block will generate the Transmit Cell Insertion Interrupt anytime a cell (residing in the Transmit Cell Insertion Buffer) is read out of the Transmit Cell Insertion Buffer and is loaded into the Outbound ATM cell traffic. 0 - Disables the Transmit Cell Insertion Interrupt. 1 - Enables the Transmit Cell Insertion Interrupt.
3	Transmit Cell Extraction Memory Overflow Interrupt Enable	R/W	**Transmit Cell Extraction Memory Overflow Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit Cell Extraction Memory Overflow Interrupt. If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt any time an overflow event has occurred in the Transmit Cell Extraction Memory buffer. 0 - Disables the Transmit Cell Extraction Memory Overflow Interrupt. 1 - Enables the Transmit Cell Extraction Memory Overflow Interrupt.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Transmit Cell Insertion Memory Overflow Interrupt Enable	R/W	**Transmit Cell Insertion Memory Overflow Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit Cell Insertion Memory Overflow Interrupt. If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt any time an overflow event has occurred in the Transmit Cell Insertion Memory buffer. 0 - Disables the Transmit Cell Insertion Memory Overflow Interrupt. 1 - Enables the Transmit Cell Insertion Memory Overflow Interrupt.
1	Detection of HEC Byte Error Interrupt Enable	R/W	**Detection of HEC Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of HEC Byte Error Interrupt within the Transmit ATM Cell Processor Block. If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt each time it receives an ATM cell (from the TxFIFO) that contains a HEC Byte error. 0 - Disables the Detection of HEC Byte Error Interrupt. 1 - Enables the Detection of HEC Byte Error Interrupt
0	Detection of Transmit UTOPIA Parity Error Interrupt Enable	R/W	**Detection of Transmit UTOPIA Parity Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Detection of Transmit UTOPIA Parity Error Interrupt within the Transmit ATM Cell Processor block. If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt each time it receives an ATM cell byte or 16-bit word (from the TxFIFO) that contains a parity error. 0 - Disables the Detection of Transmit UTOPIA Parity Error Interrupt. 1 - Enables the Detection of Transmit UTOPIA Parity Error Interrupt.

Transmit ATM Cell Processor Block - Transmit ATM Cell Insertion/Extraction Memory Control Register (0x1F13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Transmit Cell Extraction Memory RESET*	Transmit Cell Extraction Memory CLAV	Transmit Cell Insertion Memory RESET*	Transmit Cell Insertion Memory ROOM	Transmit Cell Insertion Memory WSOC
R/O	R/O	R/O	R/W	R/O	R/W	R/O	W/O
0	0	0	1	0	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-5	Unused		
4	Transmit Cell Extraction Memory RESET*	R/W	**Transmit Cell Extraction Memory RESET*:** This READ/WRITE bit-field permits the user to perform a REST operation to the Transmit Cell Extraction Memory. If the user writes a "1" to "0" transition into this bit-field, then the following events will occur. **a.** All of the contents of the Transmit Cell Extraction Memory will be flushed. **b.** All READ and WRITE pointers will be reset to their default positions. ***NOTE:*** *Following this RESET event, the user must write the value "1" into this bit-field in order to enable normal operation within the Transmit Cell Extraction Memory.*
3	Transmit Cell Extraction Memory CLAV	R/O	**Transmit Cell Extraction Memory - Cell Available Indicator:** This READ-ONLY bit-field indicates whether or not there is at least ATM cell of data (residing within the Transmit Cell Extraction Memory) that needs to be read out via the Microprocessor Interface. 0 - Indicates that the Transmit Cell Extraction Memory is empty and contains no ATM cell data. 1 - Indicates that the Transmit Cell Extraction Memory contains at least one ATM cell of data that needs to be read out. ***NOTE:*** *The user should validate each ATM cell that is being read out from the Transmit Cell Extraction memory by checking the state of this bit-field prior to reading out the contents of ATM cell data residing within the Transmit Cell Extraction Memory*

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Transmit Cell Insertion Memory RESET*	R/W	**Transmit Cell Insertion Memory RESET*:** This READ/WRITE bit-field permits the user to perform a RESET operation to the Transmit Cell Insertion Memory.If the user writes a "1" to "0" transition into this bit-field, then the following events will occur. **a.** All of the contents of the Transmit Cell Insertion Memory will be flushed. **b.** All READ and WRITE pointers will be reset to their default positions. ***NOTE:*** *Following this RESET event, the user must write the value "1" into this bit-field in order to enable normal operation of the Transmit Cell Insertion Memory.*
1	Transmit Cell Insertion Memory ROOM	R/O	**Transmit Cell Insertion Memory - ROOM Indicator:** This READ-ONLY bit-field indicates whether or not there is room (e.g., empty space) available for the contents of another ATM cell to be written into the Transmit Cell Insertion Memory. 0 - Indicates that the Transmit Cell Insertion Memory does not contain enough empty space to receive another ATM cell via the Microprocessor Interface. 1 - Indicates that the Transmit Cell Insertion Memory does contain enough empty space to receive another ATM cell via the Microprocessor Interface. ***NOTE:*** *The user should verify that the Transmit Cell Insertion Memory has sufficient empty space to accept another ATM cell of data (via the Microprocessor Interface) by polling the state of this bit-field prior to writing each cell into the Transmit Cell Insertion Memory.*
0	Transmit Cell Insertion Memory WSOC	W/O	**Transmit Cell Insertion Memory - Write SOC (Start of Cell):** Whenever the user is writing the contents of an ATM cell into the Transmit Cell Insertion Memory, then the user is suppose to identify/designate the very first byte of this ATM cell by setting this bit-field to "1". Whenever the user does this, then the Transmit Cell Insertion Memory will know that the next octet that is written into the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data Register - Byte 3 (Address = 0x1F14) is designated as the first byte of the ATM cell currently being written into the Transmit Cell Insertion Memory. This bit-field must be set to "0" during all other WRITE operations to the Transmit ATM Cell Processor - Transmit Cell Insertion/Extraction Memory Data Register

Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data - Byte 3 (Address = 0x1F14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Cell Insertion/Extraction Memory Data[31:24]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Cell Insertion/ Extraction Memory Data[31:24]	R/W	**Transmit Cell Insertion/Extraction Memory Data[31:24]:** These READ/WRITE bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data - Bytes 2 through 0 support the following functions. **a.** They function as the address location for the user to write the contents of an Outbound ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface. **b.** They function as the address location, for which the user to read out the contents of an inbound ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. ***NOTES:*** *1. If the user performs a WRITE operation to this (and the other three address locations), then the user is writing ATM cell data into the Transmit Cell Insertion Memory.* *2. If the user performs a READ operation to this (and the other three address locations), then the user is reading ATM cell data from the Transmit Cell Extraction Memory.* *3. READ and WRITE operations must be performed in a 32-bit (4-byte word) manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, the user must start by writing in or reading out the first byte (of this 4-byte word) of a given ATM cell, into/from this particular address location. Next, the user must perform the READ/WRITE operation (with the second of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 0 register. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.* *4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.* *5. Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.*

Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data - Byte 2 (Address = 0x1F15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Cell Insertion/Extraction Memory Data[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Cell Insertion/ Extraction Memory Data[23:16]	R/W	**Transmit Cell Insertion/Extraction Memory Data[23:16]:** These READ/WRITE bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data - Bytes 3, 1 and 0 support the following functions. **a.** They function as the address location for the user to write the contents of an Outbound ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface. **b.** They function as the address location, for which the user to read out the contents of an inbound ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. ***NOTES:*** *1. If the user performs a WRITE operation to this (and the other three address locations), then the user is writing ATM cell data into the Transmit Cell Insertion Memory.* *2. If the user performs a READ operation to this (and the other three address locations), then the user is reading ATM cell data from the Transmit Cell Extraction Memory.* *3. READ and WRITE operations must be performed in a 32-bit (4-byte word) manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, the user must start by writing in or reading out the first byte (of this 4-byte word) of a given ATM cell, into/from the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 3 register. Next, the user must perform the READ/ WRITE operation (with the second of this 4-byte word) to this particular address location. Afterwards, the user must perform a READ/WRITE operation (with the third of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 1 register. Finally, the user must perform a READ/ WRITE operation (with the fourth of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 0 register. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.* *4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.* *5. W.000henever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.*

Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data - Byte 1 (Address = 0x1F16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Cell Insertion/Extraction Memory Data[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Cell Insertion/ Extraction Memory Data[15:8]	R/W	**Transmit Cell Insertion/Extraction Memory Data[15:8]:** These READ/WRITE bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data - Bytes 3, 2 and 0 support the following functions. **a.** They function as the address location for the user to write the contents of an Outbound ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface. **b.** They function as the address location, for which the user to read out the contents of an inbound ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. ***NOTES:*** *1. If the user performs a WRITE operation to this (and the other three address locations), then the user is writing ATM cell data into the Transmit Cell Insertion Memory.* *2. If the user performs a READ operation to this (and the other three address locations), then the user is reading ATM cell data from the Transmit Cell Extraction Memory.* *3. READ and WRITE operations must be performed in a 32-bit (4-byte word) manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, the user must start by writing in or reading out the first byte (of this 4-byte word) of a given ATM cell, into/from the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 3 register. Next, the user must perform the READ/ WRITE operation (with the second of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this 4-byte word) to this particular register location. Finally, the user must perform a READ/WRITE operation (with the fourth of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 0 register. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.* *4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.* *5. Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.*

Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data - Byte 0 (Address = 0x1F17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Cell Insertion/Extraction Memory Data[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Cell Insertion/ Extraction Memory Data[7:0]	R/W	**Transmit Cell Insertion/Extraction Memory Data[7:0]:** These READ/WRITE bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory Data - Bytes 3, through 1 support the following functions. **a.** They function as the address location for the user to write the contents of an Outbound ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface. **b.** They function as the address location, for which the user to read out the contents of an inbound ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. ***NOTES:***: 1. *If the user performs a WRITE operation to this (and the other three address locations), then the user is writing ATM cell data into the Transmit Cell Insertion Memory.* 2. *If the user performs a READ operation to this (and the other three address locations), then the user is reading ATM cell data from the Transmit Cell Extraction Memory.* 3. *READ and WRITE operations must be performed in a 32-bit (4-byte word) manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, the user must start by writing in or reading out the first byte (of this 4-byte word) of a given ATM cell, into/from the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 3 register. Next, the user must perform the READ/WRITE operation (with the second of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this 4-byte word) to the Transmit ATM Cell Processor Block - Transmit Cell Insertion/Extraction Memory - Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this 4-byte word) to this particular register location. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.* 4. *Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.* 5. *Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.*

Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Header Byte 1 (Address = 0x1F18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Idle Cell Header Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Idle Cell Header Byte - 1 [7:0]	R/W	**Transmit Idle Cell Header Byte - 1[7:0]:** These READ/WRITE register bits, along with that in Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Header Byte 2 through Byte 4 registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 1 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.

Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Header Byte 2 (Address = 0x1F19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Idle Cell Header Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Idle Cell Header Byte - 2 [7:0]	R/W	**Transmit Idle Cell Header Byte - 2[7:0]:** These READ/WRITE register bits, along with that in Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Header Bytes 1, 3 and 4 registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 2 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.

Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Header Byte 3 (Address = 0x1F1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Idle Cell Header Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Idle Cell Header Byte - 3 [7:0]	R/W	**Transmit Idle Cell Header Byte - 3[7:0]:** These READ/WRITE register bits, along with that in Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Header Bytes 1, 2 and 4 registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 3 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.

Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Header Byte 4 (Address = 0x1F1B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Idle Cell Header Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Idle Cell Header Byte - 4 [7:0]	R/W	**Transmit Idle Cell Header Byte - 4[7:0]:** These READ/WRITE register bits, along with that in Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Header Byte 1 through Byte 3 registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 4 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.

Transmit ATM Cell Processor Block - Transmit ATM Idle Cell Payload Register (Address = 0x1F1F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Idle Cell Payload Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Idle Cell Payload Byte[7:0]	R/W	**Transmit Idle Cell Payload Byte [7:0]:** These READ/WRITE register bits permit the user to define the value of the payload bytes of all Idle Cells that are generated and transmitted by the Transmit ATM Cell Processor block. ***NOTE:*** *Each of the 48 payload bytes (within each outbound Idle Cell) will be assigned the value that is written into this register.*

Transmit ATM Cell Processor Block - Transmit Test Cell Header Byte - Byte 1 (Address = 0x1F20)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Test Cell Header Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Test Cell Header Byte 1[7:0]	R/W	**Receive Test Cell Header Byte 1:** These READ/WRITE register bits along with that in the Transmit ATM Cell Processor Block - Transmit Cell Header Byte - Bytes 2 through 4 permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 1. ***NOTE:*** *These register bits are only active if the Transmit Test Cell Generator has been enabled.*

Transmit ATM Cell Processor Block - Transmit Test Cell Header Byte - Byte 2 (Address = 0x1F21)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Test Cell Header Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Test Cell Header Byte 2[7:0]	R/W	**Receive Test Cell Header Byte 2:** These READ/WRITE register bits along with that in the Transmit ATM Cell Processor Block - Transmit Cell Header Byte - Bytes 1, 3 and 4 permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 2. ***NOTE:*** *These register bits are only active if the Transmit Test Cell Generator has been enabled.*

Transmit ATM Cell Processor Block - Transmit Test Cell Header Byte - Byte 3 (Address = 0x1F22)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Test Cell Header Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Test Cell Header Byte 3[7:0]	R/W	**Receive Test Cell Header Byte 3:** These READ/WRITE register bits along with that in the Transmit ATM Cell Processor Block - Transmit Cell Header Byte - Bytes 1, 2 and 4 permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 3. ***NOTE:*** *These register bits are only active if the Transmit Test Cell Generator has been enabled.*

Transmit ATM Cell Processor Block - Transmit Test Cell Header Byte - Byte 4 (Address = 0x1F23)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Test Cell Header Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Test Cell Header Byte 4[7:0]	R/W	**Receive Test Cell Header Byte 4:** These READ/WRITE register bits along with that in the Transmit ATM Cell Processor Block - Transmit Cell Header Byte - Bytes 1 through 3 permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 4. ***NOTE:*** *These register bits are only active if the Transmit Test Cell Generator has been enabled.*

Transmit ATM Cell Processor Block - Transmit ATM Cell Counter - Byte 3 (Address = 0x1F28)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit ATM Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit ATM Cell Count[31:24]	RUR	**Transmit ATM Cell Count - Byte 3[31:24]:** This RESET-upon-READ register, along with the Transmit ATM Cell Count - Bytes 2 through 0 registers, contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTES:*** 1. *The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer.* 2. *The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.* 3. *If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit ATM Cell Counter - Byte 2 (Address = 0x1F29)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit ATM Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit ATM Cell Count[23:16]	RUR	**Transmit ATM Cell Count - Byte 2[23:16]:** This RESET-upon-READ register, along with the Transmit ATM Cell Count - Bytes 3, 1 and 0 registers, contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block. ***NOTES:*** *1. The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer.* *2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.* *3. If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit ATM Cell Counter - Byte 1 (Address = 0x1F2A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit ATM Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit ATM Cell Count[15:8]	RUR	**Transmit ATM Cell Count - Byte 1[15:8]:** This RESET-upon-READ register, along with the Transmit ATM Cell Count - Bytes 3, 2 and 0 registers, contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block. ***NOTES:*** 1. *The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer.* 2. *The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.* 3. *If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit ATM Cell Counter - Byte 0 (Address = 0x1F2B

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit ATM Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit ATM Cell Count[7:0]	RUR	**Transmit ATM Cell Count - Byte 0[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Count - Bytes 3 through 1 registers, contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTES:*** 1. *The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer.* 2. *The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.* 3. *If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit Discarded ATM Cell Count - Byte 3 (Address = 0x1F2C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit - Discard Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit - Discard Cell Count[31:24]	RUR	**Transmit - Discard Cell Count - Byte 3[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit ATM Cell Discard Cell Count - Bytes 2 through 0 registers, contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. This particular register contains the MSB (Most Significant Byte) value of this 32-bit expression. ***NOTES:*** *1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a Transmit UTOPIA Parity error.* *2. If the number of Cells reaches the value "0xFFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit Discarded ATM Cell Count - Byte 2 (Address = 0x1F2D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit - Discard Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit - Discard Cell Count[23:16]	RUR	**Transmit - Discard Cell Count - Byte 2[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit ATM Cell Discard Cell Count - Bytes 3, 1 and 0 registers, contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. ***NOTES:*** *1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a Transmit UTOPIA Parity error.* *2. If the number of Cells reaches the value "0xFFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit Discarded ATM Cell Count - Byte 1 (Address = 0x1F2E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit - Discard Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit - Discard Cell Count[15:8]	RUR	**Transmit - Discard Cell Count - Byte 1[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit ATM Cell Discard Cell Count - Bytes 3, 2 and 0 registers, contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. ***NOTES:*** *1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a Transmit UTOPIA Parity error.* *2. If the number of Cells reaches the value "0xFFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit Discarded ATM Cell Count - Byte 0 (Address = 0x1F2F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit - Discard Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit - Discard Cell Count[7:0]	RUR	**Transmit - Discard Cell Count - Byte 0[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit ATM Cell Discard Cell Count - Bytes 3 through 1 registers, contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. This particular register contains the LSB (Least Significant Byte) value of this 32-bit expression. ***NOTES:*** *1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a Transmit UTOPIA Parity error.* *2. If the number of Cells reaches the value "0xFFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit ATM HEC Byte Error Count Register - Byte 3 (Address = 0x1F30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit - HEC Byte Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit - HEC Byte Error Count[31:24]	RUR	**Transmit - HEC Byte Error Count - Byte 3[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit ATM HEC Byte Error Count Register - Bytes 2 through 0 register, contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the MSB (Most Significant Byte) for this 32-bit expression. ***NOTES:*** *1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the Transmit Cell Insertion Buffer.* *2. If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit ATM HEC Byte Error Count Register - Byte 2 (Address = 0x1F31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit - HEC Byte Error Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit - HEC Byte Error Count[23:16]	RUR	**Transmit - HEC Byte Error Count - Byte 2[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit ATM HEC Byte Error Count Register - Bytes 3, 1 and 0 register, contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). ***NOTES:*** *1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the Transmit Cell Insertion Buffer.* *2. If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit ATM HEC Byte Error Count Register - Byte 1 (Address = 0x1F32)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit - HEC Byte Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit - HEC Byte Error Count[15:8]	RUR	**Transmit - HEC Byte Error Count - Byte 1[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit ATM HEC Byte Error Count Register - Bytes 3, 2 and 0 register, contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). ***NOTES:*** 1. *This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the Transmit Cell Insertion Buffer.* 2. *If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit ATM HEC Byte Error Count Register - Byte 0 (Address = 0x1F33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit - HEC Byte Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit - HEC Byte Error Count[7:0]	RUR	**Transmit - HEC Byte Error Count - Byte 0[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit ATM HEC Byte Error Count Register - Bytes 3 through 1 register, contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the LSB (Least Significant Byte) for this 32-bit expression. ***NOTES:*** 1. *This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the Transmit Cell Insertion Buffer.* 2. *If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register - Byte 3 (Address = 0x1F34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit UTOPIA - Parity Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit UTOPIA - Parity Error Count[31:24]	RUR	**Transmit UTOPIA Parity Error Count - Byte 3[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register - Bytes 2 through 0 registers, contains a 32-bit value for the number of ATM cells that contain Transmit UTOPIA Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the MSB (Most Significant Byte) for this 32-bit expression. ***NOTE:*** *If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register - Byte 2 (Address = 0x1F35)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit UTOPIA - Parity Error Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit UTOPIA - Parity Error Count[23:16]	RUR	**Transmit UTOPIA Parity Error Count - Byte 2[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register - Bytes 3, 1 and 0 registers, contains a 32-bit value for the number of ATM cells that contain Transmit UTOPIA Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). ***NOTE:*** *If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register - Byte 1 (Address = 0x1F36)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit UTOPIA - Parity Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit UTOPIA - Parity Error Count[15:8]	RUR	**Transmit UTOPIA Parity Error Count - Byte 1[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register - Bytes 3, 2 and 0 registers, contains a 32-bit value for the number of ATM cells that contain Transmit UTOPIA Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). ***NOTE:*** *If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register - Byte 0 (Address = 0x1F37)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit UTOPIA - Parity Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit UTOPIA - Parity Error Count[7:0]	RUR	**Transmit UTOPIA Parity Error Count - Byte 0[7:0]:** This RESET-upon-READ register, along with the Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register - Bytes 3 through 1 registers, contains a 32-bit value for the number of ATM cells that contain Transmit UTOPIA Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the LSB (Least Significant Byte) for this 32-bit expression. ***NOTE:*** *If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Filter 0 (Address = 0x1F43)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit User Cell Filter # 0 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 0 Enable	R/W	**Transmit User Cell Filter # 0 - Enable:** This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 0. If the user enables Transmit User Cell Filter # 0, then Transmit User Cell Filter # 0 will function per the configuration settings in Bits 2 through 0, within this register. If the user disables Transmit User Cell Filter # 0, then Transmit User Cell Filter # 0 then all cells that are applied to the input of Transmit User Cell Filter # 0 will pass through to the output of Transmit User Cell Filter # 0. 0 - Disables Transmit User Cell Filter # 0. 1 - Enables Transmit User Cell Filter # 0.
2	Copy Cell Enable	R/W	**Copy Cell Enable - Transmit User Cell Filter # 0:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 0 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the user-defined criteria, per Transmit User Cell Filter # 0, or to NOT copy any of these cells. If the user configures Transmit User Cell Filter # 0 to copy all cells complying with a certain header-byte pattern, then a copy (or replicate) of this compliant ATM cell will be routed to the Transmit Cell Extraction Buffer. If the user configures Transmit User Cell Filter # 0 to NOT copy all cells complying with a certain header-byte pattern, then NO copies (or replicates) of these compliant ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer. 0 - Configures Transmit User Cell Filter # 0 to NOT copy any cells that have header byte patterns which are compliant with the user-defined filtering criteria. 1 - Configures Transmit User Cell Filter # 0 to copy any cells that have header byte patterns that are compliant with the user-defined filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer. ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 0 has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Discard Cell Enable	R/W	**Discard Cell Enable - Transmit User Cell Filter # 0:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 0 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the user-defined criteria, per Transmit User Cell Filter # 0, or NOT discard any of these cells. If the user configures Transmit User Cell Filter # 0 to NOT discarded any cells that is compliant with a certain header-byte pattern, then the cell will be retained for further processing. 0 - Configures Transmit User Cell Filter # 0 to NOT discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. 1 - Configures Transmit User Cell Filter # 0 to discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 0 has been enabled.*
0	Filter if Pattern Match	R/W	**Filter if Pattern Match - Transmit User Cell Filter # 0:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 0 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the user-defined header byte patterns, or to filter ATM cells with header bytes that do NOT match the user-defined header byte patterns. 0 - Configures Transmit User Cell Filter # 0 to filter user cells that do NOT match the header byte patterns (as defined in the "? " registers). 1 - Configures Transmit User Cell Filter # 0 to filter user cells that do match the header byte patterns (as defined in the "? " registers). ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 0 has been enabled.*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 1 (Address = 0x1F44)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Pattern Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Pattern Register - Header Byte 1	R/W	**Transmit User Cell Filter # 0 - Pattern Register - Header Byte 1:** The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 1 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 2 (Address = 0x1F45)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Pattern Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Pattern Register - Header Byte 2	R/W	**Transmit User Cell Filter # 0 - Pattern Register - Header Byte 2:** The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 2 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 3 (Address = 0x1F46)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Pattern Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Pattern Register - Header Byte 3	R/W	**Transmit User Cell Filter # 0 - Pattern Register - Header Byte 3:** The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 3 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 4 (Address = 0x1F47)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Pattern Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Pattern Register - Header Byte 4	R/W	**Transmit User Cell Filter # 0 - Pattern Register - Header Byte 4:** The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 4 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Byte 1 (Address = 0x1F48)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Check Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Check Register - Header Byte 1	R/W	**Transmit User Cell Filter # 0 - Check Register - Header Byte 1:** The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 1 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 1 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 1 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 1. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 1 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 1 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 1).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Byte 2 (Address = 0x1F49)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Check Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Check Register - Header Byte 2	R/W	**Transmit User Cell Filter # 0 - Check Register - Header Byte 2:** The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 2 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 2 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 2 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 2. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 2 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 2 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 2).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Byte 3 (Address = 0x1F4A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Check Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Check Register - Header Byte 3	R/W	Transmit User Cell Filter # 0 - Check Register - Header Byte 3: The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 3 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 3 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 3 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 3. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 3 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 3 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 3).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Byte 4 (Address = 0x1F4B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Check Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Check Register - Header Byte 4	R/W	**Transmit User Cell Filter # 0 - Check Register - Header Byte 4:** The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 4 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 4 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 4 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 4. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 4 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 4 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Register - Header Byte 4).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Filtered Cell Count - Byte 3 (Address = 0x1F4C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Filtered Cell Count[31:24]	RUR	**Transmit User Cell Filter # 0 - Filtered Cell Count[31:24]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Filtered Cell Count - Bytes 2 through 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - User Cell Filter # 0 Register (Address = 0x1F43), these register bits will be incremented anytime User Cell Filter # 0 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Filtered Cell Count - Byte 2 (Address = 0x1F4D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Filtered Cell Count[23:16]	RUR	**Transmit User Cell Filter # 0 - Filtered Cell Count[23:16]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Filtered Cell Count - Bytes 3, 1 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 0 Register (Address = 0x1F43), these register bits will be incremented anytime User Cell Filter # 0 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Filtered Cell Count - Byte 1 (Address = 0x1F4E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Filtered Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Filtered Cell Count[15:8]	RUR	Transmit User Cell Filter # 0 - Filtered Cell Count[15:8]: These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Filtered Cell Count - Bytes 3, 2 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 0 Register (Address = 0x1F43), these register bits will be incremented anytime Transmit User Cell Filter # 0 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Filtered Cell Count - Byte 0 (Address = 0x1F4F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 0 - Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 0 - Filtered Cell Count[7:0]	RUR	**Transmit User Cell Filter # 0 - Filtered Cell Count[7:0]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Filtered Cell Count - Bytes 3 through 1 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 0 Register (Address = 0x1F43), these register bits will be incremented anytime Transmit User Cell Filter # 0 performs any of the following functions. • Discards an incoming User Cell.· • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Filter 1 (Address = 0x1F53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit User Cell Filter # 1 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 1 Enable	R/W	**Transmit User Cell Filter # 1 - Enable:** This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 1. If the user enables Transmit User Cell Filter # 1, then Transmit User Cell Filter # 1 will function per the configuration settings in Bits 2 through 0, within this register. If the user disables Transmit User Cell Filter # 1, then Transmit User Cell Filter # 1 then all cells that are applied to the input of Transmit User Cell Filter # 1 will pass through to the output of Transmit User Cell Filter # 1. 0 - Disables Transmit User Cell Filter # 1. 1 - Enables Transmit User Cell Filter # 1.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Copy Cell Enable	R/W	**Copy Cell Enable - Transmit User Cell Filter # 1:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 1 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the user-defined criteria, per Transmit User Cell Filter # 1, or to NOT copy any of these cells. If the user configures Transmit User Cell Filter # 1 to copy all cells complying with a certain header-byte pattern, then a copy (or replicate) of this compliant ATM cell will be routed to the Transmit Cell Extraction Buffer. If the user configures Transmit User Cell Filter # 1 to NOT copy all cells complying with a certain header-byte pattern, then NO copies (or replicates) of these compliant ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer. 0 - Configures Transmit User Cell Filter # 1 to NOT copy any cells that have header byte patterns which are compliant with the user-defined filtering criteria. 1 - Configures Transmit User Cell Filter # 1 to copy any cells that have header byte patterns that are compliant with the user-defined filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer. ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 1 has been enabled.*
1	Discard Cell Enable	R/W	**Discard Cell Enable - Transmit User Cell Filter # 1:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 1 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the user-defined criteria, per Transmit User Cell Filter # 1, or NOT discard any of these cells. If the user configures Transmit User Cell Filter # 1 to NOT discarded any cells that is compliant with a certain header-byte pattern, then the cell will be retained for further processing. 0 - Configures Transmit User Cell Filter # 1 to NOT discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. 1 - Configures Transmit User Cell Filter # 1 to discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 1 has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Filter if Pattern Match	R/W	**Filter if Pattern Match - Transmit User Cell Filter # 1:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 1 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the user-defined header byte patterns, or to filter ATM cells with header bytes that do NOT match the user-defined header byte patterns. 0 - Configures Transmit User Cell Filter # 1 to filter user cells that do NOT match the header byte patterns (as defined in the "? " registers). 1 - Configures Transmit User Cell Filter # 1 to filter user cells that do match the header byte patterns (as defined in the "? " registers). ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 1 has been enabled.*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 1 (Address = 0x1F54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Pattern Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Pattern Register - Header Byte 1	R/W	**Transmit User Cell Filter # 1 - Pattern Register - Header Byte 1:** The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 1 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 2 (Address = 0x1F55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Pattern Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Pattern Register - Header Byte 2	R/W	**Transmit User Cell Filter # 1 - Pattern Register - Header Byte 2:** The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 2 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 3 (Address = 0x1F56)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Pattern Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Pattern Register - Header Byte 3	R/W	**Transmit User Cell Filter # 1 - Pattern Register - Header Byte 3:** The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 3 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 4 (Address = 0x1F57)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Pattern Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Pattern Register - Header Byte 4	R/W	**Transmit User Cell Filter # 1 - Pattern Register - Header Byte 4:** The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 4 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Byte 1 (Address = 0x1F58)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Check Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Check Register - Header Byte 1	R/W	**Transmit User Cell Filter # 1 - Check Register - Header Byte 1:** The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 1 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 1 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 1 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 1. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 1 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 1 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 1).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Byte 2 (Address = 0x1F59)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Check Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Check Register - Header Byte 2	R/W	**Transmit User Cell Filter # 1 - Check Register - Header Byte 2:** The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 2 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 2 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 2 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 2. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 2 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 2 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 2).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Byte 3 (Address = 0x1F5A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Check Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Check Register - Header Byte 3	R/W	**Transmit User Cell Filter # 1 - Check Register - Header Byte 3:** The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 3 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 3 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 3 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 3. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 3 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 3 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 3).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Byte 4 (Address = 0x1F5B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Check Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Check Register - Header Byte 4	R/W	**Transmit User Cell Filter # 1 - Check Register - Header Byte 4:** The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 4 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 4 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 4 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 4. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 4 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 4 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Register - Header Byte 4).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Filtered Cell Count - Byte 3 (Address = 0x1F5C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Filtered Cell Count[31:24]	RUR	**Transmit User Cell Filter # 1 - Filtered Cell Count[31:24]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Filtered Cell Count - Bytes 2 through 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - User Cell Filter # 1 Register (Address = 0x1F53), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Filtered Cell Count - Byte 2 (Address = 0x1F5D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Filtered Cell Count[23:16]	RUR	**Transmit User Cell Filter # 1 - Filtered Cell Count[23:16]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Filtered Cell Count - Bytes 3, 1 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 1 Register (Address = 0x1F53), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Filtered Cell Count - Byte 1 (Address = 0x1F5E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Filtered Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Filtered Cell Count[15:8]	RUR	**Transmit User Cell Filter # 1 - Filtered Cell Count[15:8]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Filtered Cell Count - Bytes 3, 2 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 1 Register (Address = 0x1F53), these register bits will be incremented anytime Transmit User Cell Filter # 1 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer.· • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Filtered Cell Count - Byte 0 (Address = 0x1F5F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 1 - Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 1 - Filtered Cell Count[7:0]	RUR	**Transmit User Cell Filter # 1 - Filtered Cell Count[7:0]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Filtered Cell Count - Bytes 3 through 1 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 1 Register (Address = 0x1F53), these register bits will be incremented anytime Transmit User Cell Filter # 1 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Filter 2 (Address = 0x1F63)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit User Cell Filter # 2 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 2 Enable	R/W	**Transmit User Cell Filter # 2 - Enable:** This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 2. If the user enables Transmit User Cell Filter # 2, then Transmit User Cell Filter # 2 will function per the configuration settings in Bits 2 through 0, within this register. If the user disables Transmit User Cell Filter # 2, then Transmit User Cell Filter # 2 then all cells that are applied to the input of Transmit User Cell Filter # 2 will pass through to the output of Transmit User Cell Filter # 2. 0 - Disables Transmit User Cell Filter # 2. 1 - Enables Transmit User Cell Filter # 2.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Copy Cell Enable	R/W	**Copy Cell Enable - Transmit User Cell Filter # 2:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 2 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the user-defined criteria, per Transmit User Cell Filter # 2, or to NOT copy any of these cells. If the user configures Transmit User Cell Filter # 2 to copy all cells complying with a certain header-byte pattern, then a copy (or replicate) of this compliant ATM cell will be routed to the Transmit Cell Extraction Buffer. If the user configures Transmit User Cell Filter # 2 to NOT copy all cells complying with a certain header-byte pattern, then NO copies (or replicates) of these compliant ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer. 0 - Configures Transmit User Cell Filter # 2 to NOT copy any cells that have header byte patterns which are compliant with the user-defined filtering criteria. 1 - Configures Transmit User Cell Filter # 2 to copy any cells that have header byte patterns that are compliant with the user-defined filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer. ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 2 has been enabled.*
1	Discard Cell Enable	R/W	**Discard Cell Enable - Transmit User Cell Filter # 2:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 2 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the user-defined criteria, per Transmit User Cell Filter # 2, or NOT discard any of these cells. If the user configures Transmit User Cell Filter # 2 to NOT discarded any cells that is compliant with a certain header-byte pattern, then the cell will be retained for further processing. 0 - Configures Transmit User Cell Filter # 2 to NOT discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. 1 - Configures Transmit User Cell Filter # 2 to discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 2 has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Filter if Pattern Match	R/W	**Filter if Pattern Match - Transmit User Cell Filter # 2:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 2 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the user-defined header byte patterns, or to filter ATM cells with header bytes that do NOT match the user-defined header byte patterns. 0 - Configures Transmit User Cell Filter # 2 to filter user cells that do NOT match the header byte patterns (as defined in the "? " registers). 1 - Configures Transmit User Cell Filter # 2 to filter user cells that do match the header byte patterns (as defined in the "? " registers). ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 2 has been enabled.*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 1 (Address = 0x1F64)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Pattern Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Pattern Register - Header Byte 1	R/W	**Transmit User Cell Filter # 2 - Pattern Register - Header Byte 1:** The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 1 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 2 (Address = 0x1F65)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Pattern Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Pattern Register - Header Byte 2	R/W	**Transmit User Cell Filter # 2 - Pattern Register - Header Byte 2:** The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 2 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 3 (Address = 0x1F66)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Pattern Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Pattern Register - Header Byte 3	R/W	**Transmit User Cell Filter # 2 - Pattern Register - Header Byte 3:** The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 3 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 4 (Address = 0x1F67)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Pattern Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Pattern Register - Header Byte 4	R/W	**Transmit User Cell Filter # 2 - Pattern Register - Header Byte 4:** The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 4 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Byte 1 (Address = 0x1F68)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Check Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Check Register - Header Byte 1	R/W	**Transmit User Cell Filter # 2 - Check Register - Header Byte 1:** The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 1 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 1 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 1 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 1. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 1 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 1 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 1).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Byte 2 (Address = 0x1F69)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Check Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Check Register - Header Byte 2	R/W	Transmit User Cell Filter # 2 - Check Register - Header Byte 2: The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 2 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 2 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 2 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 2. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 2 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 2 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 2).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Byte 3 (Address = 0x1F6A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Check Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Check Register - Header Byte 3	R/W	**Transmit User Cell Filter # 2 - Check Register - Header Byte 3:** The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 3 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 3 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 3 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 3. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 3 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 3 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 3).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Byte 4 (Address = 0x1F6B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Check Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Check Register - Header Byte 4	R/W	**Transmit User Cell Filter # 2 - Check Register - Header Byte 4:** The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 4 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 4 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 4 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 4. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 4 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 4 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Register - Header Byte 4).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Filtered Cell Count - Byte 3 (Address = 0x1F6C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Filtered Cell Count[31:24]	RUR	**Transmit User Cell Filter # 2 - Filtered Cell Count[31:24]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Filtered Cell Count - Bytes 2 through 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - User Cell Filter # 2 Register (Address = 0x1F63), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Filtered Cell Count - Byte 2 (Address = 0x1F6D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Filtered Cell Count[23:16]	RUR	Transmit User Cell Filter # 2 - Filtered Cell Count[23:16]: These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Filtered Cell Count - Bytes 3, 1 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 2 Register (Address = 0x1F63), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Filtered Cell Count - Byte 1 (Address = 0x1F6E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Filtered Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Filtered Cell Count[15:8]	RUR	**Transmit User Cell Filter # 2 - Filtered Cell Count[15:8]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Filtered Cell Count - Bytes 3, 2 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 2 Register (Address = 0x1F63), these register bits will be incremented anytime Transmit User Cell Filter # 2 performs any of the following functions. • Discards an incoming User Cell.· • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Filtered Cell Count - Byte 0 (Address = 0x1F6F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 2 - Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 2 - Filtered Cell Count[7:0]	RUR	Transmit User Cell Filter # 2 - Filtered Cell Count[7:0]: These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Filtered Cell Count - Bytes 3 through 1 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 2 Register (Address = 0x1F63), these register bits will be incremented anytime Transmit User Cell Filter # 2 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Filter 3 (Address = 0x1F63)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit User Cell Filter # 3 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 3 Enable	R/W	**Transmit User Cell Filter # 3 - Enable:** This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 3. If the user enables Transmit User Cell Filter # 3, then Transmit User Cell Filter # 3 will function per the configuration settings in Bits 2 through 0, within this register. If the user disables Transmit User Cell Filter # 3, then Transmit User Cell Filter # 3 then all cells that are applied to the input of Transmit User Cell Filter # 3 will pass through to the output of Transmit User Cell Filter # 3. 0 - Disables Transmit User Cell Filter # 3. 1 - Enables Transmit User Cell Filter # 3.

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	Copy Cell Enable	R/W	**Copy Cell Enable - Transmit User Cell Filter # 3:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 3 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the user-defined criteria, per Transmit User Cell Filter # 3, or to NOT copy any of these cells. If the user configures Transmit User Cell Filter # 3 to copy all cells complying with a certain header-byte pattern, then a copy (or replicate) of this compliant ATM cell will be routed to the Transmit Cell Extraction Buffer. If the user configures Transmit User Cell Filter # 3 to NOT copy all cells complying with a certain header-byte pattern, then NO copies (or replicates) of these compliant ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer. 0 - Configures Transmit User Cell Filter # 3 to NOT copy any cells that have header byte patterns which are compliant with the user-defined filtering criteria. 1 - Configures Transmit User Cell Filter # 3 to copy any cells that have header byte patterns that are compliant with the user-defined filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer. ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 3 has been enabled.*
1	Discard Cell Enable	R/W	**Discard Cell Enable - Transmit User Cell Filter # 3:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 3 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the user-defined criteria, per Transmit User Cell Filter # 3, or NOT discard any of these cells. If the user configures Transmit User Cell Filter # 3 to NOT discarded any cells that is compliant with a certain header-byte pattern, then the cell will be retained for further processing. 0 - Configures Transmit User Cell Filter # 3 to NOT discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. 1 - Configures Transmit User Cell Filter # 3 to discard any cells that have header byte patterns that are compliant with the user-defined filtering criteria. ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 3 has been enabled.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
0	Filter if Pattern Match	R/W	**Filter if Pattern Match - Transmit User Cell Filter # 3:** This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 3 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the user-defined header byte patterns, or to filter ATM cells with header bytes that do NOT match the user-defined header byte patterns. 0 - Configures Transmit User Cell Filter # 3 to filter user cells that do NOT match the header byte patterns (as defined in the "? " registers). 1 - Configures Transmit User Cell Filter # 3 to filter user cells that do match the header byte patterns (as defined in the "? " registers). ***NOTE:*** *This bit-field is only active if Transmit User Cell Filter # 3 has been enabled.*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 1 (Address = 0x1F64)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Pattern Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Pattern Register - Header Byte 1	R/W	**Transmit User Cell Filter # 3 - Pattern Register - Header Byte 1:** The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 1 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 2 (Address = 0x1F65)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Pattern Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Pattern Register - Header Byte 2	R/W	**Transmit User Cell Filter # 3 - Pattern Register - Header Byte 2:** The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 2 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 3 (Address = 0x1F66)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Pattern Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Pattern Register - Header Byte 3	R/W	**Transmit User Cell Filter # 3 - Pattern Register - Header Byte 3:** The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 3 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 4 (Address = 0x1F67)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Pattern Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Pattern Register - Header Byte 4	R/W	**Transmit User Cell Filter # 3 - Pattern Register - Header Byte 4:** The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that the user wishes to use as part of the User Cell Filtering criteria, into this register. The user will also write in a value into the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 4 that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Byte 1 (Address = 0x1F68)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Check Register - Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Check Register - Header Byte 1	R/W	**Transmit User Cell Filter # 3 - Check Register - Header Byte 1:** The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 1 permits the user to define the User Cell Filtering criteria for Octet # 1 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 1 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 1 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 1 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 1. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 1 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 1 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 1).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Byte 2 (Address = 0x1F69)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Check Register - Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Check Register - Header Byte 2	R/W	**Transmit User Cell Filter # 3 - Check Register - Header Byte 2:** The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 2 permits the user to define the User Cell Filtering criteria for Octet # 2 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 2 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 2 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 2 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 2. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 2 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 2 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 2).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Byte 3 (Address = 0x1F6A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Check Register - Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Check Register - Header Byte 3	R/W	**Transmit User Cell Filter # 3 - Check Register - Header Byte 3:** The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 3 permits the user to define the User Cell Filtering criteria for Octet # 3 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 3 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 3 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 3 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 3. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 3 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 3 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 3).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Byte 4 (Address = 0x1F6B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Check Register - Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Check Register - Header Byte 4	R/W	**Transmit User Cell Filter # 3 - Check Register - Header Byte 4:** The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers, the four Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers and the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 4 permits the user to define the User Cell Filtering criteria for Octet # 4 within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in Octet 4 of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 4 by the User Cell Filter, when determine whether to filter a given User Cell. Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in Octet # 4 (of the incoming user cell) with the corresponding bit in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 4. Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within Octet # 4 (in the incoming user cell) as a don't care (e.g., to forgo the comparison between the corresponding bit in Octet # 4 of the incoming user cell with the corresponding bit-field in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Register - Header Byte 4).

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Filtered Cell Count - Byte 3 (Address = 0x1F6C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Filtered Cell Count[31:24]	RUR	**Transmit User Cell Filter # 3 - Filtered Cell Count[31:24]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Filtered Cell Count - Bytes 2 through 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - User Cell Filter # 3 Register (Address = 0x1F63), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.N ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Filtered Cell Count - Byte 2 (Address = 0x1F6D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Filtered Cell Count[23:16]	RUR	**Transmit User Cell Filter # 3 - Filtered Cell Count[23:16]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Filtered Cell Count - Bytes 3, 1 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 3 Register (Address = 0x1F63), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Filtered Cell Count - Byte 1 (Address = 0x1F6E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Filtered Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Filtered Cell Count[15:8]	RUR	**Transmit User Cell Filter # 3 - Filtered Cell Count[15:8]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Filtered Cell Count - Bytes 3, 2 and 0 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 3 Register (Address = 0x1F63), these register bits will be incremented anytime Transmit User Cell Filter # 3 performs any of the following functions. • Discards an incoming User Cell. • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer.· • Both of these actions. If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Filtered Cell Count - Byte 0 (Address = 0x1F6F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit User Cell Filter # 3 - Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit User Cell Filter # 3 - Filtered Cell Count[7:0]	RUR	**Transmit User Cell Filter # 3 - Filtered Cell Count[7:0]:** These RESET-upon-READ bit-fields, along with that in the Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Filtered Cell Count - Bytes 3 through 1 register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the Transmit ATM Cell Processor Block - Transmit User Cell Filter Control - Transmit User Cell Filter # 3 Register (Address = 0x1F63), these register bits will be incremented anytime Transmit User Cell Filter # 3 performs any of the following functions. • Discards an incoming User Cell.· • Copies (or Replicates) an incoming User Cell and routes the copy to the Transmit Cell Extraction Buffer. • Both of these actions. This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression. ***NOTE:*** *If the number of filtered cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").*

TRANSMIT PPP PACKET PROCESSOR BLOCK REGISTERS

THE TRANSMIT PPP PACKET PROCESSOR BLOCK

This section presents the Register Description/Address Map of the control registers associated with the Transmit PPP Packet Processor block.

TABLE 5: TRANSMIT PPP PACKET PROCESSOR BLOCK - REGISTER/ADDRESS MAP

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x1F00 - 0x1F02	**RESERVED**	**R/O**	**0x00**
0x1F03	Transmit PPP Packet Processor - Transmit PPP Control Register - Byte 2	R/W	0x00
0x1F04 - 0x1F0A	Reserved	R/O	0x00
0x1F0B	Transmit PPP Packet Processor - Transmit PPP Interrupt Status Register	RUR	0x00
0x1F0C - 0x1F0E	Reserved	R/O	0x00
0x1F0F	Transmit PPP Packet Processor - Transmit PPP Interrupt Enable Register	R/W	0x00

Transmit PPP Packet Processor - Transmit PPP Control Register (Address = 0x1F03)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Transmit CRC-32/ CRC-16*	Scramble Enable	Transmit PPP Packet Processor Block Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 3	Unused	R/O	
2	Transmit CRC-32/CRC-16* Select:	R/W	**Transmit CRC-32/CRC-16* Select:** This READ/WRITE bit-field permits the user to configure the Transmit PPP Packet Processor block to either compute and append a CRC-32 (4 bytes) or a CRC-16 (two bytes) to the back-end of each Outbound PPP Packet. 0 - Configures the Transmit PPP Packet Processor block to compute and append a CRC-16 value to the back-end of each Outbound PPP Packet. 1 - Configures the Transmit PPP Packet Processor block to compute and append a CRC-32 value to the back-end of each Outbound PPP Packet. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the PPP Mode.*

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Scramble Enable	R/W	**Scramble Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Scrambler within the Transmit PPP Packet Processor block. If the user invokes this feature, then the Scrambler will subject the contents of each outbound PPP Packet to the X^43+1 scrambling polynomial. 0 - Disables the Scrambler within the Transmit PPP Packet Processor block. 1 - Enables the Scrambler within the Transmit Packet Processor block. ***NOTE:*** *This bit-field is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
0	Transmit PPP Packet Processor Block Enable	R/W	**Transmit PPP Packet Processor Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit PPP Packet Processor block. If the user wishes to operate the XRT79L71 in the PPP Mode, then the user must enable the Transmit PPP Packet Processor block .0 - Disables the Transmit PPP Packet Processor block. 1 - Enables the Transmit PPP Packet Processor block. ***NOTES:*** 1. *This bit-field is only active if the XRT79L71 has been configured to operate in the PPP Mode.* 2. *The user can invoke a Software RESET to the Transmit PPP Packet Processor block by momentarily setting this bit-field to "0".*

Transmit PPP Packet Processor - Interrupt Status Register (Address = 0x1F0B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						TxFIFO Underflow Interrupt Status	Transmit POS-PHY Parity Error Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-2	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	TxFIFO Underflow Interrupt Status	RUR	**TxFIFO Underflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the TxFIFO Underflow Interrupt has occurred since the last read of this register, as described below. 0 - Indicates that the TxFIFO Underflow Interrupt has not occurred since the last read of this register. 1 - Indicates that the TxFIFO Underflow Interrupt has occurred since the last read of this register. ***NOTE:*** *The Transmit PPP Packet Processor block will generate the TxFIFO Underflow Interrupt, if it is allowed to deplete the TxFIFO while the Link Layer Processor is in the midst of transmitting a PPP Packet to the Transmit POS-PHY Interface. If the TxFIFO becomes depleted before the Link Layer Processor was able to complete its transmission of a given packet, then all of the following events will occur.* **a.** The Transmit PPP Packet Processor block will generate the TxFIFO Underflow Interrupt. **b.** That portion of the PPP Packet, that was written into the Transmit POS-PHY Interface (and in-turn the TxFIFO) prior to the TxFIFO Underflow event, will be transmitted as an Aborted packet. **c.** That portion of the PPP Packet, that is to be written after the TxFIFO Underflow event will be discarded.
0	Transmit POS-PHY Parity Error Interrupt Status	RUR	**Transmit POS-PHY Parity Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Transmit POS-PHY Parity Error Interrupt has occurred since the last read of this register, as described below. 0 - Indicates that the Transmit POS-PHY Parity Error Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Transmit POS-PHY Parity Error Interrupt has occurred since the last reads of this register.

Transmit PPP Packet Processor - Interrupt Enable Register (Address = 0x1F0F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						TxFIFO Underflow Interrupt Enable	Transmit POS-PHY Parity Error Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	TxFIFO Underflow Interrupt Enable	R/W	TxFIFO Underflow Interrupt Status: This READ/WRITE bit-field permits the user to either enable or disable the TxFIFO Underflow Interrupt. If the user enables this interrupt, then the Transmit PPP Packet Processor block will generate an interrupt anytime the TxFIFO is depleted while the Link Layer Processor is in the midst of writing a packet to the Transmit POS-PHY Interface. The purpose of this interrupt is to warn the user that all of the following events will be occurring, in conjunction with this interrupt. **a.** That portion of the PPP Packet, that was written into the Transmit POS-PHY Interface (and in-turn the TxFIFO) prior to the TxFIFO Underflow event, will be transmitted as an Aborted Packet. **b.** That portion of the PPP Packet that is to be written after the TxFIFO Underflow event will be discarded. ***NOTE:*** *The TxFIFO Underflow Interrupt will NOT occur if the TxFIFO becomes depleted while the Link Layer Processor is NOT currently writing any packet data to the Transmit POS-PHY Interface.0 - Disables the TxFIFO Underflow Interrupt.1 - Enables the TxFIFO Underflow Interrupt.*
0	Transmit POS-PHY Parity Error Interrupt Enable	R/W	**Transmit POS-PHY Parity Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit POS-PHY Parity Error Interrupt. If the user enables this interrupt, then the Transmit PPP Packet Processor block will generate an interrupt anytime the Transmit POS-PHY Interface detects a Parity Error with a given byte of word of PPP data that is being presented to the Transmit POS-PHY Data Bus pins (TxPData[15:0]). 0 - Disables the Transmit POS-PHY Parity Error Interrupt. 1 - Enables the Transmit POS-PHY Parity Error Interrupt. ***NOTE:*** *This bit-field is only active if Parity Checking has been enabled on the Transmit POS-PHY Interface block. Parity Checking is enabled if and only if Bit 6 (Parity Check Enable) within the Transmit POS-PHY Interface - Transmit Control Register - Byte 0 (Address = 0x0582) has been set to "1".*

4.0 PIN DESCRIPTIONS (SEE 79L71-HARDWARE-MANUAL.PDF)

5.0 ELECTRICAL CHARACTERISTICS (SEE 79L71-HARDWARE-MANUAL.PDF)

6.0 MICROPROCESSOR INTERFACE (SEE 79L71-HARDWARE-MANUAL.PDF)

7.0 ARCHITECTURAL/FUNCTIONAL DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC - CLEAR CHANNEL FRAMER AND HIGH-SPEED HDLC CONTROLLER MODE APPLICATIONS (SEE 79L71-CC-ARC-DESC.PDF)

8.0 ARCHITECTURAL DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC - ATM UNI APPLICATIONS (SEE 79L71-ATM-ARC-DESC.PDF)

9.0 ARCHITECTURAL DESCRIPTION OF THE XRT79L71 1-CHANNEL DS3/E3 ATM UNI/PPP/CLEAR-CHANNEL FRAMER WITH LIU IC - POS-PHY/PPP APPLICATIONS (SEE 79L71-PPP-ARC-DESC.PDF)

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	07/18/02	1st release of the XRT99L00 mkII.0 preliminary data sheet.
P1.0.1	02/12/03	Added package outline and pin-out diagram.
P1.0.2	05/03	Added Pin Descriptions
P1.0.3	06/03	Added Electrical Specifications and Register Information.
P1.0.4	07/03	Default Value added to Address Locations 104 and 105 in register map. Add pin TxSer (C9) to pin list. I/O Control Register (Direct Address = 0x1101, edit Bit 4 AMI/Zero Sup*.
P1.0.5	12/03	Created a Register Manual document.
P1.0.6	03/04	Major revisions and additions to registers
P1.0.7	04/04	Various edits
P1.0.8	10/04	More edits and corrections
P1.0.9	10/05	Edits and corrections.
1.0.0	06/07	Release to production - no changes

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