

## 2200 MHz / 200 MHz Twin PLL

### Description

U2784B is a low power twin PLL manufactured with TEMIC's advanced UHF process. The maximum operating frequency is 2200 MHz and 200 MHz respectively.

It features a wide supply voltage range from 2.7 to 5.5 V. Prescaler and power down function for both PLL's is integrated. Applications are DECT, DCS 1800 and WLAN.

### Features

- Very low current consumption (typical 3 V/12 mA)
- Supply voltage range 2.7 to 5.5 V
- Maximum input frequency PLL1: 2200 MHz, PLL2: 200 MHz
- 2 pins for separate power down functions
- Output for PLL lock status
- Prescaler 64/65 for PLL1 and 8/9 for PLL2
- SSO-20 package
- ESD protected according to MIL-STD 883C method 3015 cl. 2

### Benefits

- Low current consumption leads to extended talk time
- Twin PLL saves costs and space
- One foot print for all TEMIC twin PLL's saves design-in time

### Block Diagram

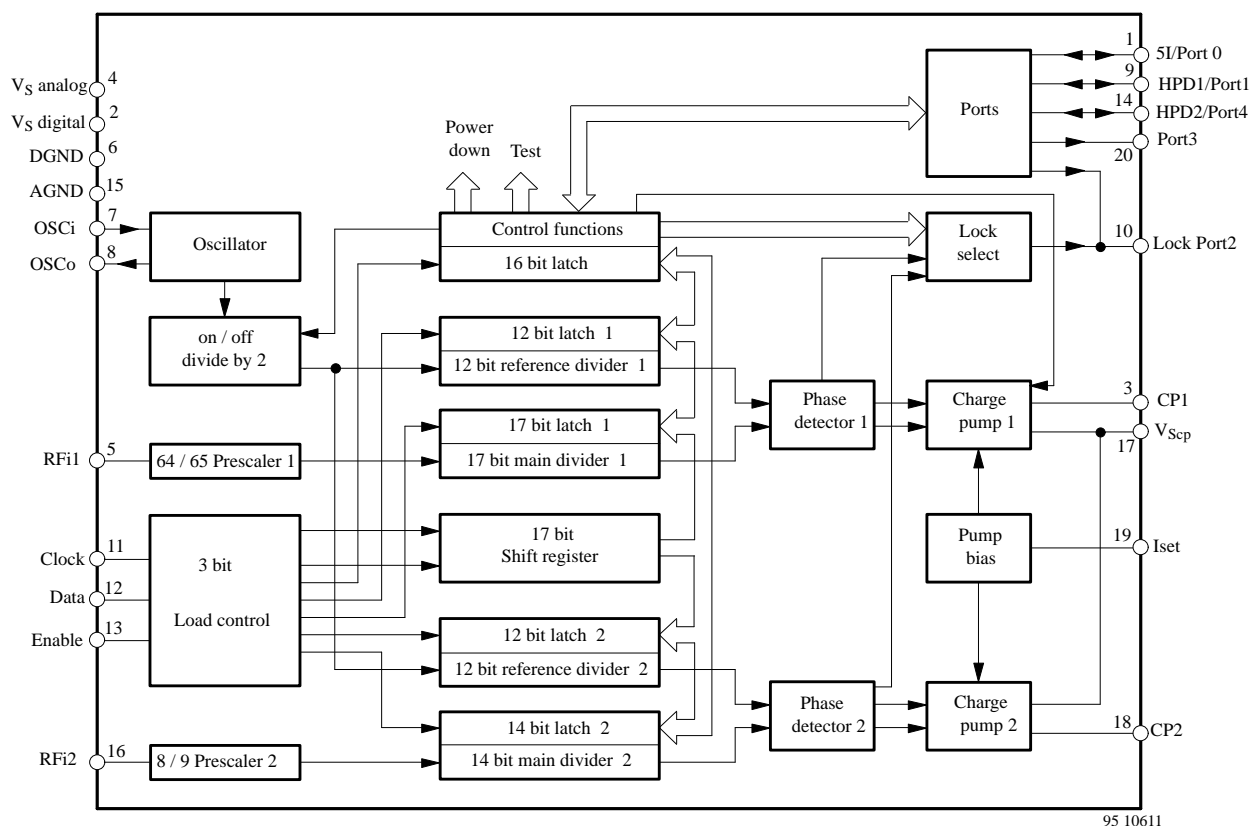
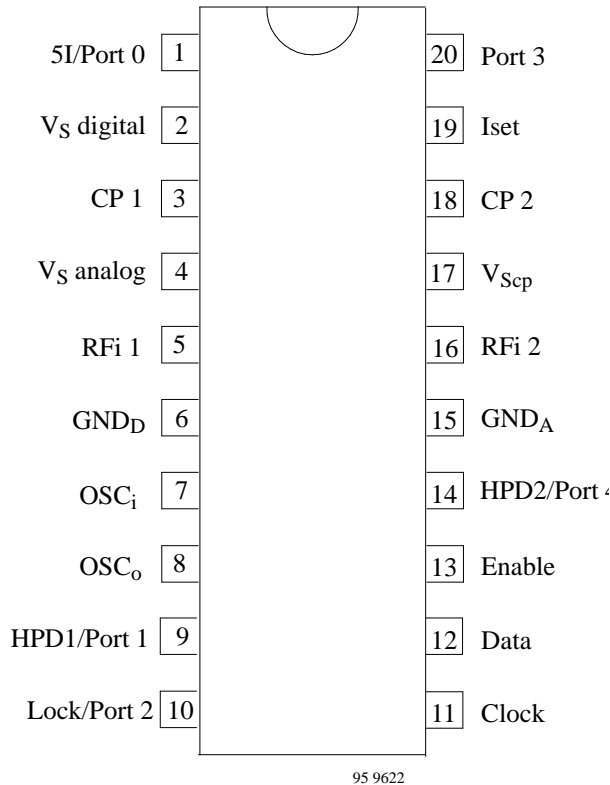


Figure 6.

## Ordering Information

Extended Type Number	Package	Remarks
U2784B-BFS	SSO20	Rail, MOQ 830 pcs
U2784B-BFSG3	SSO20	Tape and reel, MOQ 4000 pcs

## Pin Description



Pin	Symbol	Function
1	5I/Port 0	5I – Control input / o.c.output
2	VS digital	Power supply digital section
3	CP 1	Charge pump output of synthesizer 1
4	VS analog	Power supply analog section
5	RFi 1	RF divider input synthesizer
6	GND <sub>D</sub>	Ground for digital section
7	OSC <sub>i</sub>	Reference oscillator input
8	OSC <sub>o</sub>	Reference oscillator output
9	HPD 1/ Port 1	Hardware power down input of synthesizer 1 / o.c.output
10	Lock/ Port 2	Lock output / o.c.output / testmode output
11	Clock	3-wire-bus: serial clock input
12	Data	3-wire-bus: serial data input
13	Enable	3-wire-bus: serial enable input
14	HPD 2/ Port 4	Hardware power down input of synthesizer 2 / o.c.output
15	GND <sub>A</sub>	Ground for analog section
16	RFi 2	RF divider input synthesizer 2
17	V <sub>Scp</sub>	Charge pump supply voltage
18	CP 2	Charge pump output of synthesizer 2
19	Iset	Reference pin for charge pump currents
20	Port 3	o.c.output

## Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage Pins 2, 4 and 17	V <sub>S</sub> , V <sub>Scp</sub>	6	V
Input voltage Pins 1, 3, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18 and 20	V <sub>i</sub>	0 to V <sub>S</sub>	V
Junction temperature	T <sub>j</sub>	125	°C
Storage temperature range	T <sub>stg</sub>	-40 to +125	°C

## Operating Range

Parameters	Symbol	Value	Unit
Supply voltage Pins 2, 4 and 17	V <sub>S</sub> , V <sub>Scp</sub>	2.7 to 5.5	V
Ambient temperature range	T <sub>amb</sub>	-40 to +85	°C

## Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO20	$R_{thja}$	140	K/W

## Electrical Characteristics

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_S = 2.7$  to  $5.5$  V,  $V_{Scp} = 5$  V, unless otherwise specified

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
<b>DC Supply</b>						
Supply current	$V_S = 3$ V	$I_S$		12		mA
Supply current CP	$V_{CP} = 5$ V, PLL in lock condition	$I_{CP}$		1		$\mu\text{A}$
<b>PLL 1</b>						
Input voltage	$f_{RFi1} = 400 - 2200$ MHz	$V_{RFi1}$	20		200	mV <sub>RMS</sub>
Scaling factor prescaler		$S_{PSC}$	64/65			
Scaling factor main counter		$S_M$	5		2047	
Scaling factor swallow counter		$S_S$	0		63	
Reference counter		$S_R$	5		4095	
<b>PLL 2</b>						
Input voltage	$f_{RFi2} = 50$ MHz $f_{RFi2} = 100 - 200$ MHz	$V_{RFi2}$	40 20		200 200	mV <sub>RMS</sub>
Scaling factor prescaler		$S_{PSC}$	8/9			
Scaling factor main counter		$S_M$	5		2047	
Scaling factor swallow		$S_S$	0		7	
Reference counter		$S_R$	5		4095	
<b>Reference oscillator</b>						
Recommended crystal series resistance			10		200	$\Omega$
External reference input frequency	AC coupled sinewave $RF/2 = 0$ $RF/2 = 1$	$OSC_i$	1 1		20 40	MHz
External reference input amplitude	AC coupled sinewave <sup>2)</sup>	$OSC_i$		100		mV <sub>RMS</sub>
<b>Logic input levels (Clock, Data, Enable, HPD1, HPD2, 5I)</b>						
High input level		$V_{IH}$	1.5			V
Low input level		$V_{iL}$	0		0.4	V
High input current		$I_{iH}$	-5		5	$\mu\text{A}$
Low input current		$I_{iL}$	-5		5	$\mu\text{A}$
<b>Logic output levels (Port 0, 1, 2, 3, 4, Lock)</b>						
Leakage current	$V_{OH} = 5.5$ V	$I_L$			10	$\mu\text{A}$
Saturation voltage	$I_{OL} = 0.5$ mA	$V_{SL}$			0.4	V
<b>Charge pump output (<math>R_{set} = \text{tbd.}</math>)</b>						
Source current	$V_{CP} \leq V_{Scp}/2$ $5I = L$ $5I = H$	PLL2 PLL1 PLL1 $I_{source}$		-1 -0.2 -1		mA
Sink current	$V_{CP} \leq V_{Scp}/2$ $5I = L$ $5I = H$	PLL2 PLL1 PLL1 $I_{sink}$		1 0.2 1		mA
Leakage current	$V_{CP} \leq V_{Scp}/2$	$I_L$		$\pm 5$		nA

<sup>1)</sup> RMS voltage at 50  $\Omega$ ; <sup>2)</sup>  $OSC_o$  is open if an external reference frequency is applied

## Serial Programming Bus

Reference and programmable counters can be programmed by the 3-wire-bus (Clock, Data and Enable). After setting enable signal to high condition, the data status is transferred bit by bit on the rising edge of the clock signal into the shift register, starting with the MSB-bit. After the Enable signal returns to low condition the programmed information is loaded according to the addressbits (last three bits) into the addressed latch. Additional leading bits are ignored and there is no check made the 3-wire-bus remains active and the IC can be programmed.

Data is entered with the most significant bit first. The leading bits deliver the divider or control information. The trailing three bits are the address field. There are six different addresses used. The trailing address bits are decoded upon the falling edge of the Enable signal. the internal Loadpulse is beginning with the falling edge of the Enable signal and ending with the falling edge of the Clock signal. Therefore a minimum holdtime clock-enable  $t_{HCE}$  is required.

## Bit Allocation

MSB																LSB				
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15	Bit 16	Bit 17	Bit 18	Bit 19	Bit 20	
data bits																address bits				
D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A2	A1	A0	
PLL1 M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	S5	S4	S3	S2	S1	PLL1 S0	0	0	1	
					PLL1 R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	PLL1 R0	0	1	0	
			PLL2 M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	S2	S1	PLL2 S0	0	1	1	
					PLL2 R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	PLL2 R0	1	0	0	
	RF/2	Test	SIP	TRI 2	TRI 1	PS2	PS1	H2P	H1P	LP B	LPA	P4	P3	P2	P1	P0	1	0	1	
															SP D 5I	SP D 2	SP D 1	1	1	0

## Scaling Factors

### PGD of PLL1:

S0 ... S5: These bits are setting the swallow counter  $S_S$ .  
 $S_S = S0*2^0 + S1*2^1 + \dots + S4*2^4 + S5*2^5$   
 allowed scalling factors for  $S_S$ : 0 ... 63,  $S_S < S_M$

M0 ... M10: These bits are setting the main counter  $S_M$ .  
 $S_M = M0*2^0 + M1*2^1 + \dots + M9*2^9 + M10*2^{10}$   
 allowed scalling factors for  $S_M$ : 5 ... 2047

$S_{PGD}$ : Total scalling factor of the programmable counter:  
 $S_{PGD} = (64*S_M) + S_S$  Condition:  $S_S < S_M$

### PGD of PLL2:

S0 ... S4: These bits are setting the swallow counter  $S_S$ .  
 $S_S = S0*2^0 + S1*2^1 + S2*2^2$   
 allowed scalling factors for  $S_S$ : 0 ... 7,  $S_S < S_M$

M0 ... M9: These bits are setting the main counter  $S_M$ .  
 $S_M = M0*2^0 + M1*2^1 + \dots + M9*2^9 + M10*2^{10}$   
 allowed scalling factors for  $S_M$ : 5 ... 2047

$S_{PGD}$ : Total scalling factor of the programmable counter:  
 $S_{PGD} = (8*S_M) + S_S$  Condition:  $S_S < S_M$

### RFD of PLL1 and PLL2:

R0 ... R11: These bits are setting the reference counter  $S_R$ .  
 $S_R = R0*2^0 + \dots + R10*2^{10} + R11*2^{11}$   
 allowed scalling factors for  $S_R$ : 5 ... 4095

RF/2 = 1:  $S_{RFD} = 2 * S_R$

RF/2 = 0:  $S_{RFD} = S_R$

## Serial Programming Bus

### Control Bits:

P0 ... P4: o.c. output ports (1 = high impedance)

LPA, LPB: selection of P2 output or locksignal      LPA    LPB    function of pin 10

0	0	o.c. output P2
0	1	locksignal of synthesizer 2
1	0	locksignal of synthesizer 1
1	1	wiredor locksignal of both synthesizer

H1P, H2P: selection of P1/4 output or hardware power down input of synthesizer 1/2 (0 = Port / 1 = HPD)

5IP: selection of P0 output or high current switching input for the charge pump current of synthesizer 1  
(0 = Port / 1 = charge pump 1 current switch input)

PS1, PS2: phase selection of synthesizer 1 and synthesizer 2 (1 = normal / 0 = invers)

	PS-PLL1/2 = 1	PS-PLL1/2 = 0
	CP1/2	CP1/2
$f_R > f_P$	$I_{sink}$	$I_{source}$
$f_R < f_P$	$I_{source}$	$I_{sink}$
$f_R = f_P$	0	0

RF/2: divide by 2 prescaler for reference divider (0 = off / 1 = on)

SPD1, SPD2: software power down bit of synthesizer 1/2 (0 = powerdown / 1 = powerup)

5I: software switch for the charge pump current of synthesizer 1 (0 = low current / 1 = high current)

TRI1, TRI2: enables tristate for the charge pump of synthesizer 1/2 (0 = normal / 1 = tristate)

TEST: enables counter testmode (0 = disabled / 1 = enabled)

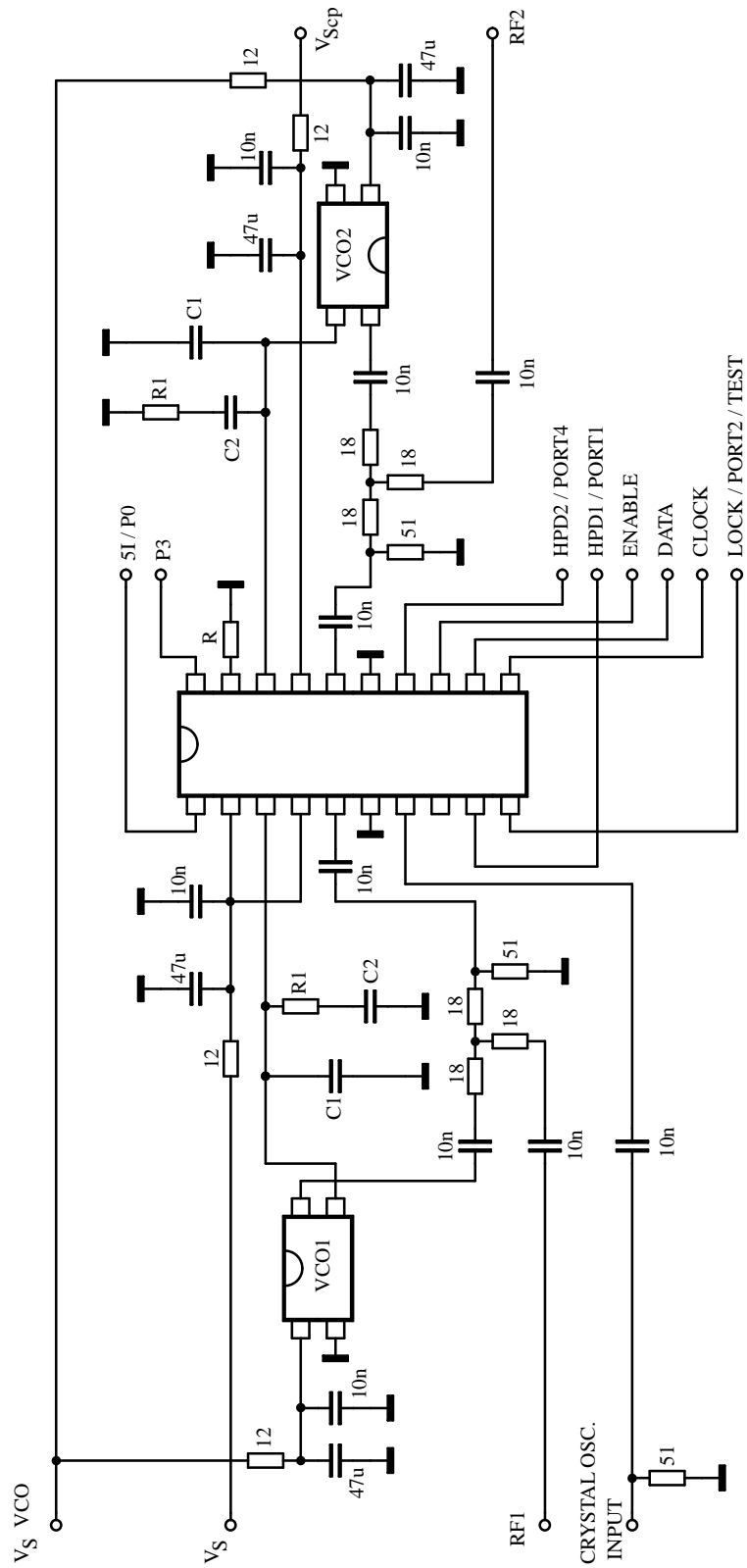
TEST	LPA	LPB	PS1	PS2	Testsignal at pin 10
1	1	0	1	x	RFD1
1	1	0	0	x	PGD1
1	0	1	x	1	RFD2
1	0	1	x	0	PGD2

To operate the software power down mode the following condition must be set: HXP = 0; power up and power down will be set by SPD<sub>X</sub> = 1 (on) and SPD<sub>X</sub> = 0 (off).

To operate the hardware power down mode the following condition must be set: HXP = 1; SPD<sub>X</sub> = 1; power up and power down will be set by high and low state at the hardware power down pins 9/14.

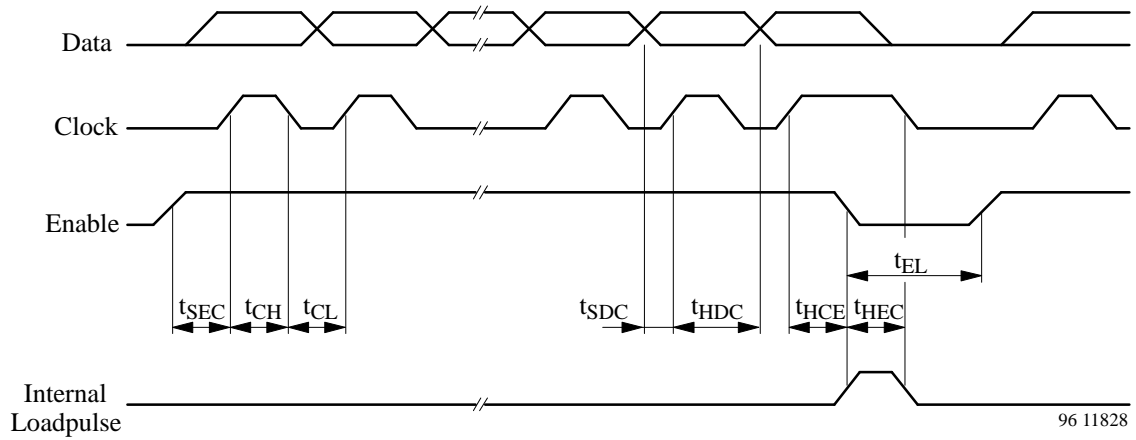
High current of charge pump synthesizer 1 is active when 5I = 1 and if 5IP = 1 the charge pump current control input pin 1 is in high state.

## Application Circuit

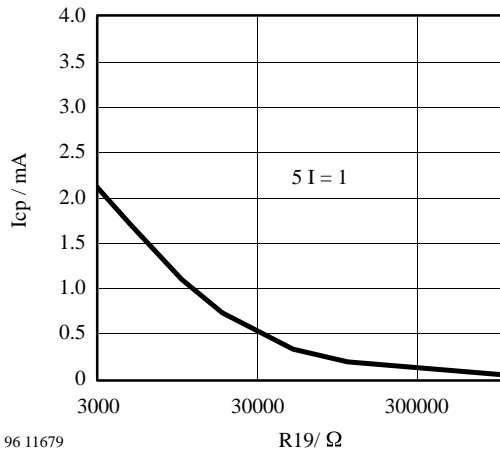


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## Timing Diagram Serial Bus

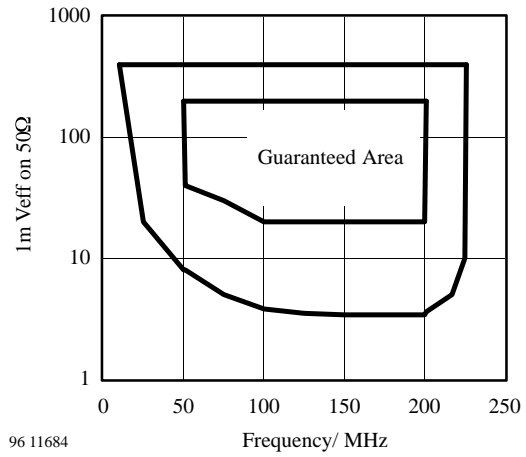


Clock High Time	$t_{CH}$	> 750	ns
Clock Low Time	$t_{CL}$	> 350	ns
Clock Period	$t_{PER}$	> 1100	ns
Set up Time Data to Clock	$t_{SDC}$	> 100	ns
Hold Time Data to Clock	$t_{HDC}$	> 400	ns
Hold Time Clock to Enable	$t_{HCE}$	> 400	ns
Hold Time Enable to Clock	$t_{HEC}$	> 400	ns
Enable Low Time	$t_{EL}$	> 200	ns
Set up Time Enable to Clock	$t_{SEC}$	> 4000	ns



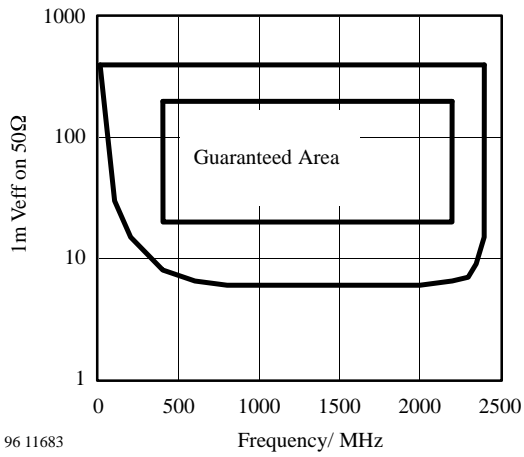
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Figure 7. Charge pump characteristics



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Figure 9. Input sensitivity of PLL2

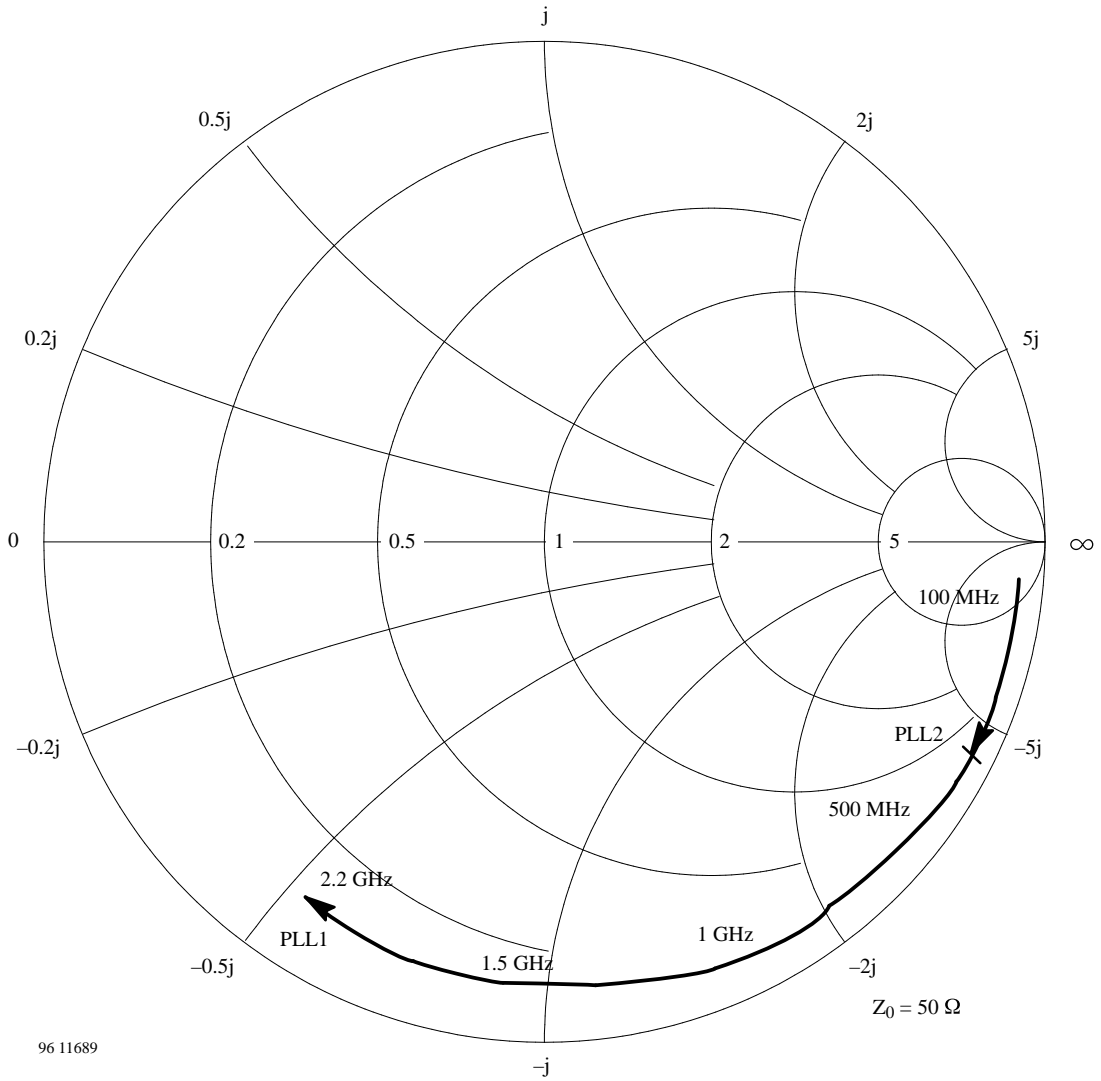


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Figure 8. Input sensitivity of PLL1



**Input Impedance of PLL1 and PLL2**



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1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**TEMIC TELEFUNKEN microelectronic GmbH** semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**TEMIC** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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