

TITE LAMP

# SM14LV1.7C TVSarray™

#### **FEATURES**

- ULTRA LOW CLAMP FOR SENSITIVE I/O PORTS
- Clamps voltage to 1.7V max above signal level
- Operates over range from 3V through 30V
- Protects 10 lines uni and bi-directional to voltage bus
- UL 94V-O Flammability Classification

#### **APPLICATIONS**

- RS-232-B
- RS-422-A
- RS-423-A
- RS-485

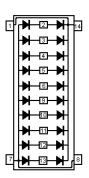
#### **MAXIMUM RATINGS**

- Operating Temperature: -55°C to +50°C
- Storage Temperature: -55°C to +125°C
- Forward Surge Current: 8A (6/70μs)
- Minimum Reverse Breakdown Voltage (VBR): 35V
- Working Peak Reverse Voltage V<sub>RWM</sub> to 30V
- Continuous forward current, I<sub>F</sub>: 400mA
- Power dissipation, (P<sub>D</sub>): 500mW
- Derating factor: 4.0 mW/°C

### TITEClamp™ TVS SERIES



SO-14 Package



**Device Pin Out Configuration** 

#### **PACKAGING**

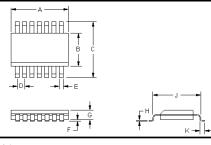
- Tape & Reel per EIA Standard 481
- 2,500 pieces per 13 inch reel (STANDARD)
- Carrier tube 50 pcs (OPTIONAL)

#### MECHANICAL

- Molded SOIC 14 PIN Surface Mount
- Weight 2.5 grams (approximate)
- Marking: Logo, Date Code
- Pin 1 defined by dot

#### ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless otherwise specified $V_F$ V<sub>F</sub>(surge) CAP CAP CAP ĺκ $l_R$ @ I<sub>F</sub> @ $I_{PP} = 8 A$ $V_{RR}$ $V_{RWM}$ @10V @ 3V @15V +25°c +50°c DEVICE @100µA 100mA 6/70 µs PART NUMBER MARKING **VOLTS VOLTS** pF pF рF **VOLTS VOLTS** MIN MAX MAX $@V_R$ MAX **TYP** TYP TYP MAX MAX $@V_R$ LV1.7C 35 45 30 SM14LCV1.7C 30 200\* 30 500\* 20 27 0.5 1.70

#### OUTLINE



DIM         MIN         MAX         MIN         MAX           A         0.336         0.344         8.53         8.74           B         0.150         0.158         3.81         4.01           C         0.228         0.244         5.79         6.19           E         0.011         0.021         0.28         0.53           F         0.004         0.010         0.10         0.20           G         0.053         0.069         1.35         1.75           H         0.006         0.010         0.15         0.25           J         0.189         0.206         4.80         5.23           K         0.016         0.050         0.41         1.27					
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INCHES

MILLIMETERS

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Microsemi

<sup>\*</sup> These values of leakage current I<sub>R</sub> represent multiple diodes as a result of their common anode or cathode connections.





## SM14LV1.7C TVSarray™

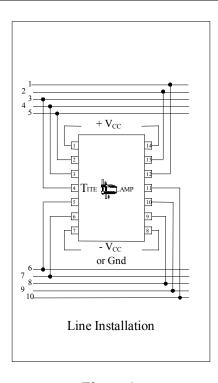
# Application Notes For Using The SM14LV1.7C TITEClamp<sup>™</sup> TVSarray<sup>™</sup>

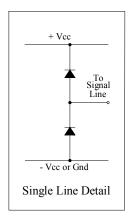
The SM14LV1.7C TITEClamp TVSarray is a 10 wire protector designed for clamping voltage spikes to lowest possible levels between the signal line and the Vcc supply or ground. This device incorporates Microsemi's proprietary "Self Programmable" feature that provides exceedingly tight clamping of only 1.7V maximum above signal line voltages ranging from 3.0V up through 30V. Destructive over-current is diverted through the plus and minus Vcc rails or ground for negative transients.

One size fits all

**Downsizing** of on chip components **to sub-micron** dimensions has improved performance, reduced component size and cost **at the expense of lower failure voltage thresholds**. The demand has surfaced for improved protection across data lines in highly automated manufacturing, monitoring and control systems. These environments are usually harsh and subject to conducted and induced transient voltages originating from sources including motors, solenoids and welders.

The connection points are shown in figure 1. Pins 1 and 14 are connected to +Vcc, with pins 7 & 8 being either -Vcc or ground. The lines are spread out for purposes of illustrating the connections; however, the traces between signal lines and the TVS should be at an absolute minimum to reduce parasitic reluctance which causes overshoot per Faraday's laws of induction, V=L(di/dt). In figure 2, the segment for a single wire is detailed for improved illustration. A scaled illustration of clamping on a 12V signal line example is shown in figure 3. This depicts a small but acceptable rise in voltage above the signal during worse case transient conditions.







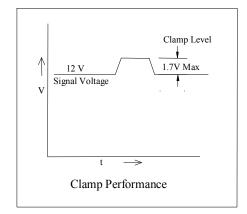


Figure 3.

Figure 1.

Precautions in component placement and board layout:

- 1. Place the SM14LV1.7C directly at the board/signal line interface.
- 2. Keep all traces short for both signal lines and Vcc (and ground if applicable).
- 3. Eliminate ground loops.

If the reader has further technical questions, please contact Microsemi-Scottsdale applications engineering at 480-941-6433 or 480-941-6524.