

Fundamental Quartz Crystal Oscillator

■GENERAL DESCRIPTION

The NJU6363 series is a C-MOS fundamental quartz crystal oscillator that consists of an oscillation amplifier, 3-stage divider and 3-state output buffer.

The 3-stage divider generates only one frequency selected of $f_0, f_0/2, f_0/4, f_0/8, f_0/16$ and $f_0/32$ by internal circuits is output.

The oscillation amplifier is realized very low stand-by current using NAND circuit.

The 3-state output buffer is C-MOS compatible.

■PACKAGE OUTLINE

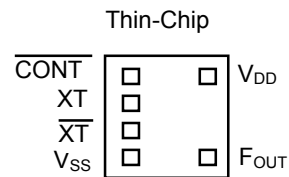


NJU6369XC-D

■FEATURES

- Low Operating Current 1mA @1.8V
- Operating Voltage 1.5 to 3.6V
- Maximum Oscillation Frequency 40MHz(T.B.D) @1.5V
- High Fan-out $I_{OH}/I_{OL} = T.B.D @1.8V$
- 3-Stage Divider Maximum Divider $f_0/32$
- Oscillation Stop and Output Stand-by Function
- 3-State Output Buffer
- Oscillation Capacitors C_g and C_d on-chip
- Package Outline Thin-Chip
- C-MOS Technology

■PAD LOCATION



■LINE-UP TABLE

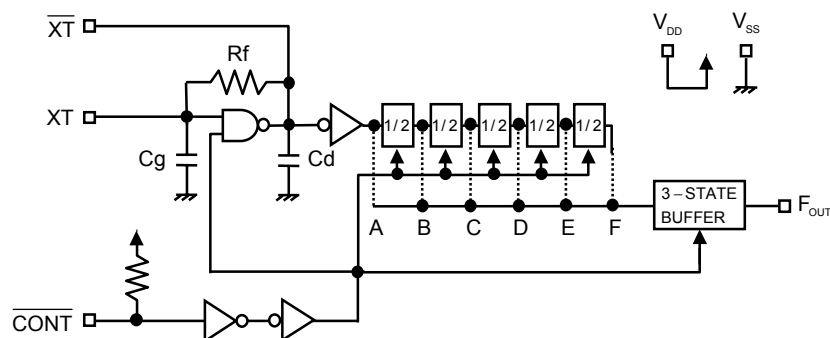
Type No.	F _{OUT}	Internal Connect	C _g /C _d	
NJU6363	A	f_0	Connected A Line	23/23pF
	B	$f_0/2$	Connected B Line	23/23pF
	C	$f_0/4$	Connected C Line	23/23pF
	D	$f_0/8$	Connected D Line	23/23pF
	E	$f_0/16$	Connected E Line	23/23pF
	F	$f_0/32$	Connected F Line	23/23pF

■COORDINATES

No	Pad Name	X	Y
1	$\overline{\text{CONT}}$	-178	231
2	XT	-178	77
3	$\overline{\text{XT}}$	-178	-77
4	V _{SS}	-178	-231
5	F _{OUT}	206	-231
6	V _{DD}	206	231

Starting Point: Chip Center Unit[um]
 Chip Size: 0.7x0.75mm
 Thin-Chip Thickness(-D): 200±20um
 Pad Size: 90x90um

■BLOCK DIAGRAM



■TERMINAL DESCRIPTION

SYMBOL	FUNCTION
	Oscillation and 3-state Output Buffer Control
$\overline{\text{CONT}}$	$\overline{\text{CONT}}$ F_{OUT}
	H or OPEN Output either one frequency selected of f_0 , $f_0/2, f_0/4, f_0/8, f_0/16$ and $f_0/32$ Note1)
	L Oscillation Stop and High impedance Output
$\overline{\text{XT}}$	Quartz Crystal Connecting Terminals
$\overline{\text{XT}}$	
V_{SS}	$V_{\text{SS}}=0\text{V}$
F_{OUT}	Frequency Output
V_{DD}	$V_{\text{DD}}=1.8/2.5\text{V}/3.3\text{V}$

Note1) Refer to the line-up table.

■ABSOLUTE MAXIMUM RATINGS

($T_a=25^\circ\text{C}$)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	$V_{\text{SS}}-0.5$ to $V_{\text{DD}}+0.5$	V
Output Voltage	V_{O}	-0.5 to $V_{\text{DD}}+0.5$	V
Input Current	I_{IN}	± 10	mA
Output Current	I_{O}	± 25	mA
Operating Temperature Range	T_{opr}	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$

Note2) If the supply voltage(V_{DD}) is less than 7.0V, the input voltage must not over the V_{DD} level though 7.0V is limit specified.

Note3) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V _{DD}		1.5		3.6	V

(V_{DD}=1.8V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I _{DD}	A version, fosc=16MHz, C _L =5pF			1	mA
		B version, fosc=16MHz, C _L =5pF			1	
		C version, fosc=16MHz, C _L =5pF			1	
		D version, fosc=16MHz, C _L =5pF			1	
		E version, fosc=16MHz, C _L =5pF			1	
		F version, fosc=16MHz, C _L =5pF			1	
Oscillation Stopping Current	I _{STB}	$\overline{\text{CONT}} = V_{SS}$, No load		1	3	uA
Stand-by Current	I _{st}	$\overline{\text{CONT}} = \text{XT} = V_{SS}$, No load Note4)			1	uA
Input Voltage	V _{IH}		1.26		1.8	V
	V _{IL}		0		0.54	V
Output Current	I _{OH}	VOH=1.62V	T.B.D			mA
	I _{OL}	VOL=0.18V	T.B.D			mA
Input Current	I _{IN}	$\overline{\text{CONT}} = 0.8V_{DD}$		3.0	4.5	uA
		$\overline{\text{CONT}} = 0.2V_{DD}$		0.5	0.7	uA
3-state Off Leakage Current	I _{OZ}	$\overline{\text{CONT}} = V_{SS}$, F _{OUT} = V _{DD} or V _{SS}			±0.1	uA
Feedback Resistance	R _f			T.B.D		KΩ
Internal Capacitor	C _g /C _d	fosc=16MHz		T.B.D		pF
Maximum Oscillation Frequency	F _{MAX}		40			MHz
Output Signal Symmetry	SYM	C _L =5pF, @V _{DD} /2	45	50	55	%
Output Signal Rise Time	t _r	C _L =5pF, 10% to 90%		T.B.D	T.B.D	ns
Output Signal Fall Time	t _f	C _L =5pF, 90% to 10%		T.B.D	T.B.D	ns
Output Disable time	T _{PLZ}	C _L =5pF, R _{UP} =10kΩ			250	ns
Output Enable Time	T _{PZL}	C _L =5pF, R _{UP} =10kΩ			250	ns

Note4) Excluding input current on $\overline{\text{CONT}}$ Terminal.

($V_{DD}=2.5V, T_a=25^{\circ}C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	A version, $f_{osc}=16MHz, C_L=5pF$			2	mA
		B version, $f_{osc}=16MHz, C_L=5pF$			1.5	
		C version, $f_{osc}=16MHz, C_L=5pF$			1	
		D version, $f_{osc}=16MHz, C_L=5pF$			1	
		E version, $f_{osc}=16MHz, C_L=5pF$			1	
		F version, $f_{osc}=16MHz, C_L=5pF$			1	
Oscillation Stopping Current	I_{STB}	$\overline{CONT} = V_{SS}$, No load		2	5	μA
Stand-by Current	I_{st}	$\overline{CONT} = XT = V_{SS}$, No load Note4)			1	μA
Input Voltage	V_{IH}		1.75		2.5	V
	V_{IL}		0		0.75	V
Output Current	I_{OH}	$V_{OH}=2.25V$	T.B.D			mA
	I_{OL}	$V_{OL}=0.25V$	T.B.D			mA
Input Current	I_{IN}	$\overline{CONT} = 0.8V_{DD}$		7.5	12.0	μA
		$\overline{CONT} = 0.2V_{DD}$		1.2	2.0	μA
3-state Off Leakage Current	I_{OZ}	$\overline{CONT} = V_{SS}$, $F_{OUT} = V_{DD}$ or V_{SS}			± 0.1	μA
Feedback Resistance	R_f			T.B.D		$K\Omega$
Internal Capacitor	C_g/C_d	$f_{osc}=16MHz$		T.B.D		pF
Maximum Oscillation Frequency	F_{MAX}		40			MHz
Output Signal Symmetry	SYM	$C_L=5pF, @V_{DD}/2$	45	50	55	%
Output Signal Rise Time	t_r	$C_L=5pF, 10\%$ to 90%		T.B.D	T.B.D	ns
Output Signal Fall Time	t_f	$C_L=5pF, 90\%$ to 10%		T.B.D	T.B.D	ns
Output Disable time	T_{PLZ}	$C_L=5pF, R_{UP}=10k\Omega$			200	ns
Output Enable Time	T_{PZL}	$C_L=5pF, R_{UP}=10k\Omega$			200	ns

Note4) Excluding input current on \overline{CONT} Terminal.

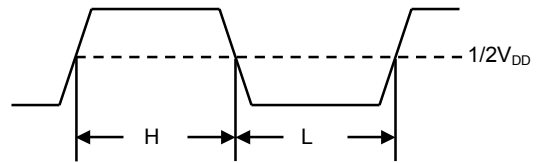
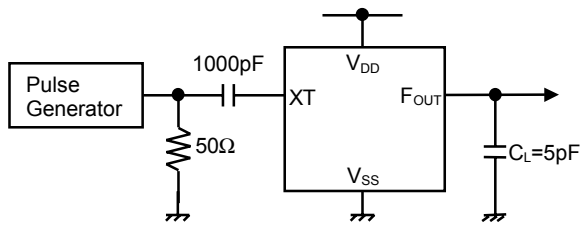
($V_{DD}=3.3V, T_a=25^{\circ}C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	A version, fosc=16MHz, $C_L=5pF$			2.5	mA
		B version, fosc=16MHz, $C_L=5pF$			2	
		C version, fosc=16MHz, $C_L=5pF$			1.5	
		D version, fosc=16MHz, $C_L=5pF$			1.5	
		E version, fosc=16MHz, $C_L=5pF$			1.5	
		F version, fosc=16MHz, $C_L=5pF$			1.5	
Oscillation Stopping Current	I_{STB}	$\overline{CONT} = V_{SS}$, No load		2	5	uA
Stand-by Current	I_{st}	$\overline{CONT} = XT = V_{SS}$, No load Note4)			1	uA
Input Voltage	V_{IH}		2.31		3.3	V
	V_{IL}		0		0.99	V
Output Current	I_{OH}	$V_{OH}=2.97V$	T.B.D			mA
	I_{OL}	$V_{OL}=0.33V$	T.B.D			mA
Input Current	I_{IN}	$\overline{CONT} = 0.8V_{DD}$		10.0	15.0	uA
		$\overline{CONT} = 0.2V_{DD}$		1.8	3.0	uA
3-state Off Leakage Current	I_{OZ}	$\overline{CONT} = V_{SS}$, $F_{OUT} = V_{DD}$ or V_{SS}			± 0.1	uA
Feedback Resistance	R_f			T.B.D		K Ω
Internal Capacitor	C_g/C_d	fosc=16MHz		T.B.D		pF
Maximum Oscillation Frequency	F_{MAX}		60			MHz
Output Signal Symmetry	SYM	$C_L=5pF$, @ $V_{DD}/2$	45	50	55	%
Output Signal Rise Time	t_r	$C_L=5pF$, 10% to 90%		T.B.D	T.B.D	ns
Output Signal Fall Time	t_f	$C_L=5pF$, 90% to 10%		T.B.D	T.B.D	ns
Output Disable time	T_{PLZ}	$C_L=5pF, R_{UP}=10k\Omega$			150	ns
Output Enable Time	T_{PZL}	$C_L=5pF, R_{UP}=10k\Omega$			150	ns

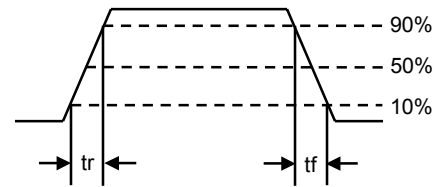
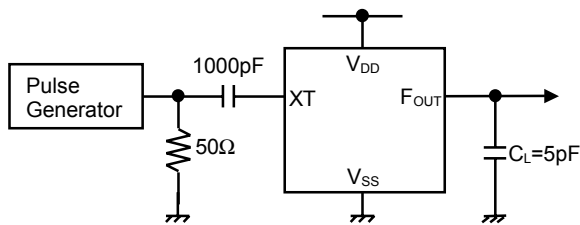
Note4) Excluding input current on \overline{CONT} Terminal.

MEASUREMENT CIRCUITS

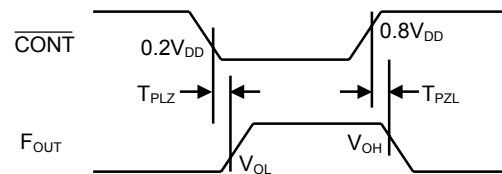
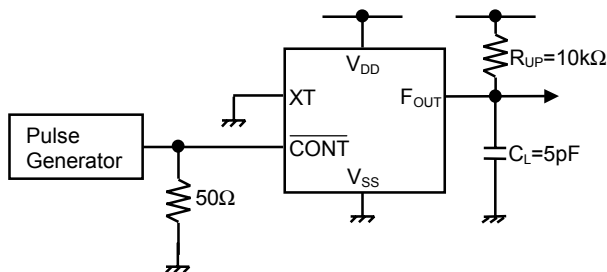
(1) Output Signal Symmetry ($C_L=5pF$)



(2) Output Signal Rise/Fall Time ($C_L=5pF$)



(3) Output Disable/Enable Time ($C_L=5pF, R_{UP}=10k\Omega$)



[CAUTION]
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