

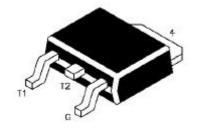


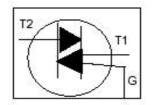


An ISO/TS 16949, ISO 9001 and ISO 14001 Certified Company

TRIAC

**CJD136** 





DPAK (TO-252) Plastic Package

For use in high bidirectional transient and blocking voltage applications, and for high thermal cycling performance. Typical Applications include Motor Control, Industrial and Domestic Lighting, Heating and Static Switching.

#### **ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITION	VALUE	UNIT
Repetitive Peak Off State Voltage	*V <sub>DRM</sub>		600	V
RMS on State Current	I <sub>T (RMS)</sub>	full sine wave, T <sub>mb</sub> ≤107ºC	4.0	Α
Non Repetitive Peak on State Current	I <sub>TSM</sub>	full sine wave, T <sub>J</sub> =25°C prior to		
		t=20ms	25	Α
		t=16.7ms	27	Α
I <sup>2</sup> t for Fusing	l <sup>2</sup> t	t=10ms	3.1	A <sup>2</sup> s
Repetitive Rate of Rise of on State Current After Triggering	dl <sub>⊤</sub> /dt	$I_{TM}$ =6A, $I_{G}$ =0.2A, $dI_{G}$ / $dt$ =0.2A/ $\mu$ s		
- Carron 7 mor 111 ggoring		T2+ G+	50	A/μs
		T2+ G-	50	A/μs
		T2- G-	50	A/μs
		T2- G+	10	A/μs
Peak Gate Current	$I_{GM}$		2.0	Α
Peak Gate Voltage	$V_{GM}$		5.0	V
Peak Gate Power	$P_{GM}$		5.0	W
Average Gate Power	P <sub>G (AV)</sub>	Over any 20ms period	0.5	W
Storage Temperature	$T_{stg}$		- 40 to +150	۰C
Operating Junction Temperature	T <sub>j</sub>		125	۰C

<sup>\*</sup>The rate of rise of current should not excees 3A/ms

#### THERMAL RESISTANCE

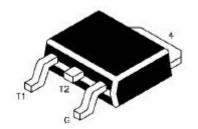
Junction to Mounting Base	R <sub>th (j-mb)</sub>	full cycle	3.0 max	K/W
		half cycle	3.7 max	K/W
Junction to Ambient (typical)	R <sub>th (j-a)</sub>	in free air	60 typ	K/W

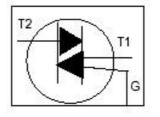
#### ELECTRICAL CHARACTERISTICS (T<sub>1</sub>=25°C unless specified otherwise)

		,			
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Gate Trigger Current	I <sub>GT</sub>	$V_{D}=12V, I_{T}=0.1A$			
		T2+ G+		35	mΑ
		T2+ G-		35	mΑ
		T2- G-		35	mΑ
		T2- G+		70	mΑ

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	MX XY
XY= Date Code	

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C unless specified otherwise)

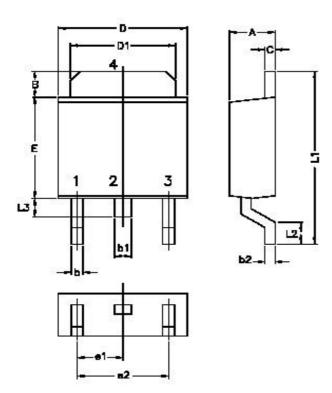
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Latching Current	Ι <sub>L</sub>	V <sub>D</sub> =12V, I <sub>GT</sub> =0.1A			
		T2+ G+		20	mA
		T2+ G-		30	mΑ
		T2- G-		20	mΑ
		T2- G+		30	mA
Holding Current	I <sub>H</sub>	$V_D=12V$ , $I_{GT}=0.1A$		15	mA
On State Voltage	V <sub>T</sub>	I <sub>T</sub> =5A		1.7	V
Gate Trigger Voltage	$V_{GT}$	$V_{D}=12V, I_{T}=0.1A$		1.5	V
		$V_D = 400V, I_T = 0.1A, T_J = 125$ °C	0.25		V
Off State Leakage Current	I <sub>D</sub>	$V_D = max$ , $V_{DRM} = max$ , $T_J = 125$ °C		0.5	mA

#### **DYNAMIC CHARACTERISTICS**

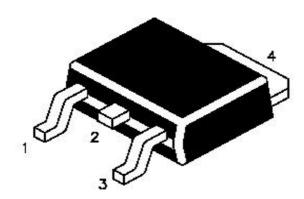
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Critical Rate of Rise of off State Voltage	d <sub>VD</sub> /dt	V <sub>DM</sub> =67% V <sub>DRM</sub> =max, T <sub>J</sub> =125°C, exponential waveform, gate open circuit	100			V/μs
Critical Rate of Change of Commutating Voltage	dV <sub>com</sub> /dt	V <sub>DM</sub> =400V, T <sub>J</sub> =95°C, I <sub>T(RMS)</sub> =4A, d/ <sub>com</sub> /dt=1.8A/ms, gate open circuit		50		V/μs
Gate Controlled turn on time	t <sub>gt</sub>	$I_{TM}$ =6A, $V_D$ = $V_{DRM}$ max, $I_G$ =0.1A, $dI_G$ / $dt$ =5A/ $\mu$ s		2.0		μs

CJD136Rev171104E

# DPAK (TO-252) Plastic Package

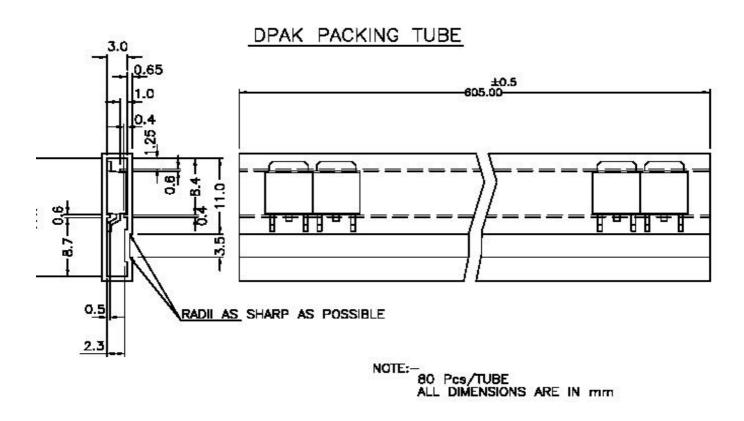


DIM	MIN.	MAX.
Α	2.20	2.40
В	1.30	1.50
b	0.55	0.65
b1	0.75	0.85
b2	0.46	0.58
С	0.46	0.58
D	6.40	6.60
D1	5.20	5.40
Е	5.40	5.60
e1	2.25	2.35
e2	4.50	4.70
L1	9.25	9.75
L2	0.5	-
L3	0.90	1.10



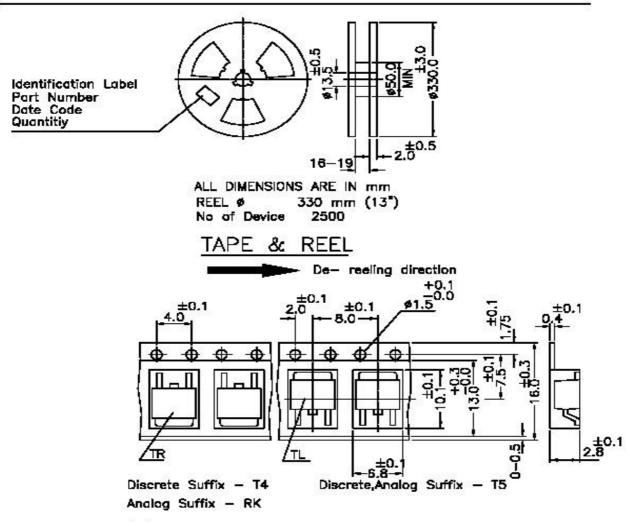
## PIN CONFIGURATION

- 1. T1 MAIN TERMINAL 1
- 2. T2 MAIN TERMINAL 2
- 3. G GATE
- 4. FIN (T2)

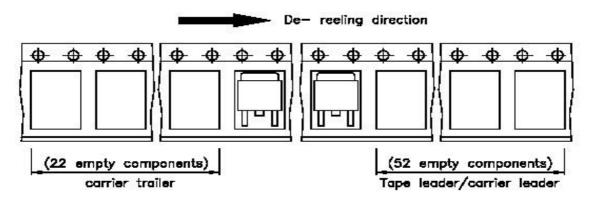


CJD136Rev171104E

# DPAK TAPE & REEL SPECIFICATION



Notes:
A maximum of three consecutive components may be missing. Provided this gap is followed by six consecutive components.



CJD136Rev171104E

Customer Notes CJD136

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#### **Disclaimer**

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