Synchronous Buck PWM Controller

Features

- Single 12V Power Supply Required
- 0.8V Reference with 1% Accuracy
- Shutdown and Soft-start Function
- 300KHz Fixed Switching Frequency
- Voltage Mode PWM Control Design
- Up to 100% Duty Cycle
- Under-Voltage Protection
- Over-Current Protection
- SOP-14 Package
- Lead Free Available (RoHS Compliant)

Applications

- Graphic Cards

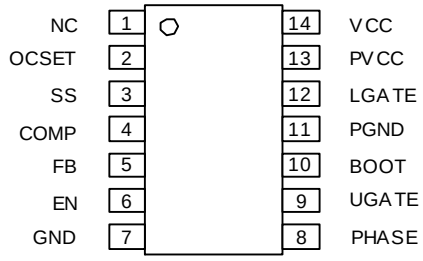
General Description

The APW7074 uses fixed 300KHz switching frequency, voltage mode, synchronous PWM controller which drives dual N-channel MOSFETs. The device integrates all of the control, monitoring and protecting functions into a single package, provides one controlled power output with under-voltage and over-current protections.

The APW7074 provides excellent regulation for output load variation. The internal 0.8V temperature-compensated reference voltage is designed to meet the requirement of low output voltage applications.

The APW7074 with excellent protection functions: POR, OCP and UVP. The Power-On-Reset (POR) circuit can monitor the VCC, EN, and OCSET voltage to make sure the supply voltage exceeds their threshold voltage while the controller is running. The Over-Current Protection (OCP) monitors the output current by using the voltage drop across the upper and lower MOSFET's $R_{DS(ON)}$. When the output current reaches the trip point, the controller will run the soft-start function until the fault events are removed. The Under-Voltage Protection (UVP) monitors the voltage at FB pin (V_{FB}) for short-circuit protection, when the V_{FB} is less 50% V_{REF}, the controller will shutdown the IC directly.

Pin Outs



SOP-14
TOP VIEW

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

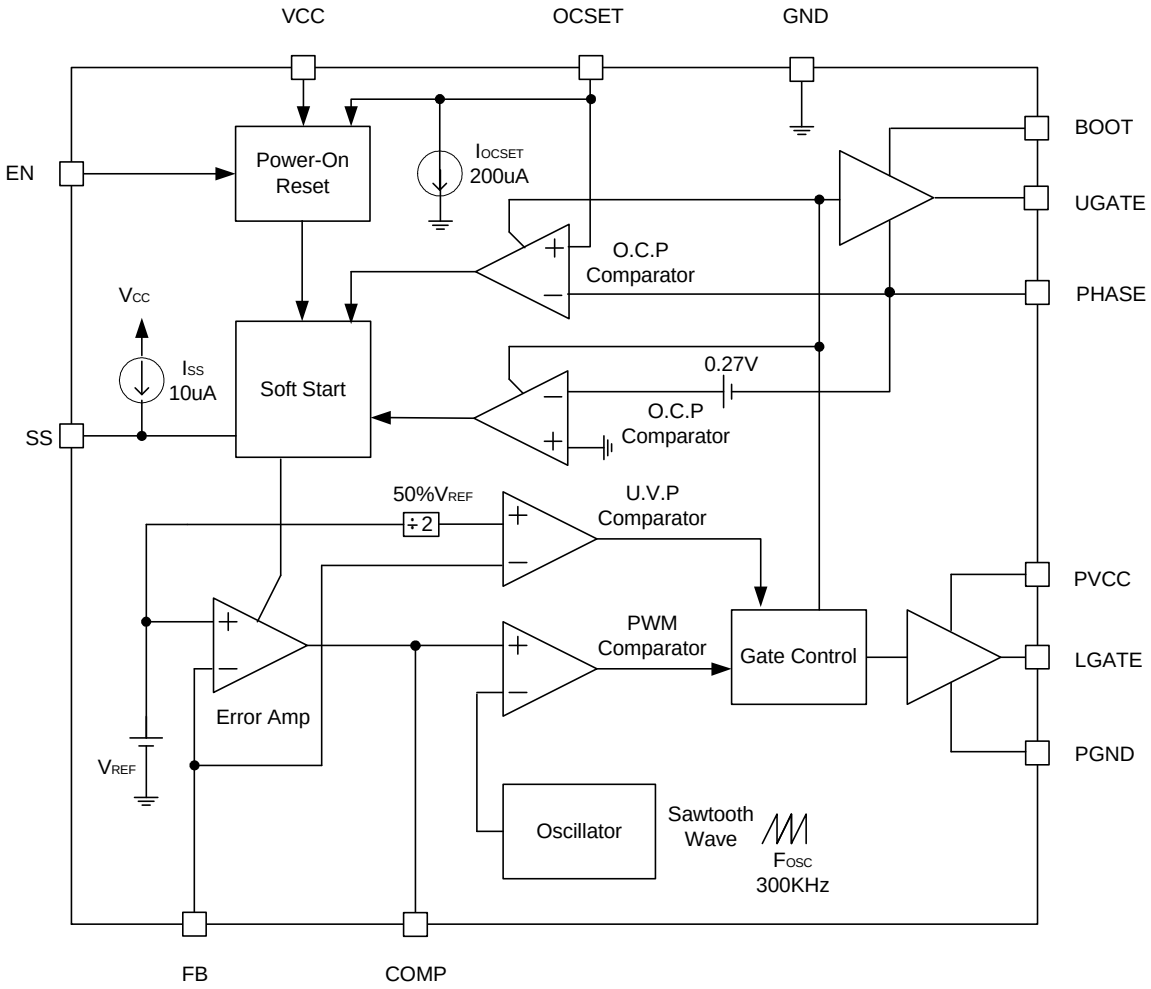
Rev. A.2 - Feb., 2006

Ordering and Marking Information

APW7074 □□-□□□ LeadFreeCode HandlingCode Temp.Range PackageCode	PackageCode K : SOP - 14 Temp.Range E : -20 to 70°C HandlingCode TU : Tube TR : Tape & Reel LeadFreeCode L : Lead Free Device Blank : Original Device
APW7074 K : APW7074 XXXXX	XXXXX- Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCC, PVCC	VCC, PVCC to GND	-0.3 to +16	V
BOOT	BOOT to PHASE	-0.3 to +16	V
UGATE	UGATE to PHASE <400ns pulse width >400ns pulse width	-5 to BOOT+5 -0.3 to BOOT +0.3	V
LGATE	LGATE to PGND <400ns pulse width >400ns pulse width	-5 to PVCC+5 -0.3 to BOOT +0.3	V
PHASE	PHASE to GND <400ns pulse width >400ns pulse width	-5 to +21 -0.3 to 16	V
OCSET	OCSET to GND	VCC+0.3	V
FB, COMP	FB, COMP to GND	-0.3 to 7	V
PGND	PGND to GND	-0.3 to +0.3	V
T_J	Junction Temperature Range	-20 to +150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Soldering Temperature (10 Seconds)	300	°C
V_{ESD}	Minimum ESD Rating	±2	KV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
VCC, PVCC	IC Supply Voltage	10.8 to 13.2	V
V_{IN}	Converter Input Voltage	2.2 to 13.2	V
V_{OUT}	Converter Output Voltage	0.8 to 5	V
I_{OUT}	Converter Output Current	0 to 25	A
T_A	Ambient Temperature Range	-20 to 70	°C
T_J	Junction Temperature Range	-20 to 125	°C

Electrical Characteristics

Unless otherwise specified, these specifications apply over VCC=12V, and T_A =-20~70°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7074			Unit
			Min	Typ	Max	
INPUT SUPPLY CURRENT						
I_{CC}	VCC Supply Current (Shutdown mode)	UGATE, LGATE and EN = GND		0.5	1	mA
	VCC Supply Current	UGATE and LGATE Open		5	10	mA

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VCC=12V, and T_A =-20~70°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7074			Unit
			Min	Typ	Max	
POWER-ON RESET						
	Rising VCC Threshold		9	9.5	10.0	V
	Falling VCC Threshold		7.5	8	8.5	V
	Rising V_{OCSET} Threshold			1.3		V
	V_{OCSET} Hysteresis Voltage			0.1		V
	Rising EN threshold Voltage			1.3		V
	EN Hysteresis Voltage			0.1		V
OSCILLATOR						
F_{OSC}	Oscillator Frequency		255	300	345	kHz
V_{OSC}	Ramp Amplitude	(nominal 1.35V to 2.95V)		1.6		V
Duty	Duty Cycle Range		0		100	%
REFERENCE						
V_{REF}	Reference Voltage			0.80		V
	Reference Voltage Tolerance		-1		+1	%
PWM ERROR AMPLIFIER						
Gain	Open Loop Gain	R_L = 10k, C_L = 10pF (Note3)		88		dB
GBWP	Open Loop Bandwidth	R_L = 10k, C_L = 10pF (Note3)		15		MHz
SR	Slew Rate	R_L = 10k, C_L = 10pF (Note3)		6		V/us
	FB Input Current	V_{FB} = 0.8V		0.1	1	uA
V_{COPM}	COMP High Voltage			5.5		V
V_{COPM}	COMP Low Voltage			0		V
I_{COMP}	COMP Source Current	V_{COMP} = 2V		5		mA
I_{COMP}	COMP Sink Current	V_{COMP} = 2V		5		mA
GATE DRIVERS						
I_{UGATE}	Upper Gate Source Current	BOOT = 12V, V_{UGATE} -V_{PHASE} = 2V		2.6		A
I_{UGATE}	Upper Gate Sink Current	BOOT = 12V, V_{UGATE} -V_{PHASE} = 2V		1.05		A
I_{LGATE}	Lower Gate Source Current	PVCC = 12V, V_{LGATE} = 2V		4.9		A
I_{LGATE}	Lower Gate Sink Current	PVCC = 12V, V_{LGATE} = 2V		1.4		A
R_{UGATE}	Upper Gate Source Impedance	BOOT = 12V, I_{UGATE} = 0.1A		2	3	Ω
R_{UGATE}	Upper Gate Sink Impedance	BOOT = 12V, I_{UGATE} = 0.1A		1.6	2.4	Ω

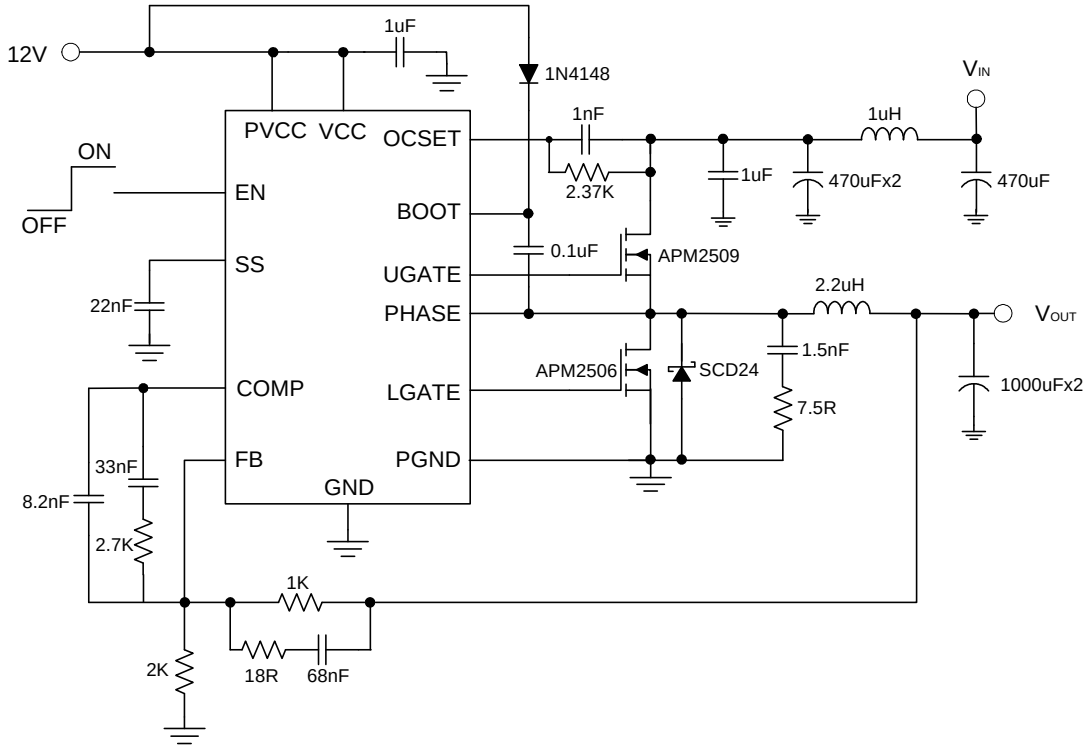
Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VCC=12V, and T_A =-20~70°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7074			Unit
			Min	Typ	Max	
GATE DRIVERS (Cont.)						
R_{LGATE}	Lower Gate Source Impedance	PVCC = 12V, I_{LGATE} = 0.1A		1.3	1.95	Ω
R_{LGATE}	Lower Gate Sink Impedance	PVCC = 12V, I_{LGATE} = 0.1A		1.25	1.88	Ω
T_D	Dead Time			20		nS
PROTECTION						
UV_{FB}	FB Under Voltage Level	Percent of V_{REF}	45	50	55	%
I_{OCSET}	OCSET Source Current (Hi-Side)	V_{OCSET} = 11.5V	150	200	250	uA
V_{OCP}	OCP Voltage (Low-Side)		230	270	310	mV
SOFT START						
I_{SS}	Soft-Start Charge Current		8	10	12	uA

Note 3:Guaranteed by design.

Typical Application Circuit



Function Pin Descriptions

VCC (Pin14)

Power supply input pin. Connect a nominal 12V power supply to this pin. The power-on reset function monitors the input voltage by this pin. It is recommended that a decoupling capacitor (1 to 10uF) be connected to GND for noise decoupling.

PVCC (Pin13)

This pin provides a supply voltage for the lower gate drive, connect this pin to VCC pin in normal use.

BOOT (Pin10)

This pin provides the bootstrap voltage to the upper gate driver for driving the N-channel MOSFET.

PHASE (Pin8)

This pin is the return path for the upper gate driver. Connect this pin to the upper MOSFET source. This pin is also used to monitor the voltage drop across the MOSFET for over-current protection.

GND (Pin7)

This pin is the signal ground pin. Connect the GND pin to a good ground plane.

PGND (Pin11)

This pin is the power ground pin for the lower gate driver. It should be tied to GND pin on the board.

COMP (Pin4)

This pin is the output of PWM error amplifier. It is used to set the compensation components.

FB (Pin5)

This pin is the inverting input of the PWM error amplifier. It is used to set the output voltage and the compensation components. This pin is also monitored for under-voltage protection; if the FB voltage is under 50% of reference voltage, the device will be shut down.

UGATE (Pin9)

This pin is the gate driver for the upper MOSFET of PWM output.

LGATE (Pin12)

This pin is the gate driver for the lower MOSFET of PWM output.

SS (Pin3)

Connect a capacitor to GND and a 10uA current source charges this capacitor to set the soft-start time.

OCSET (Pin2)

This pin serves two functions: a shutdown control and the setting of over current limit threshold. Pulling this pin below 1.3V will shutdown the controller, forcing the UGATE and LGATE signals to be low.

A resistor (Rocset) connected between this pin and the drain of the high side MOSFET will determine the over current limit. An internal 200uA current source will flow through this resistor, creating a voltage drop, which will be compared with the voltage across the high side MOSFET. The threshold of the over current limit is therefore given by:

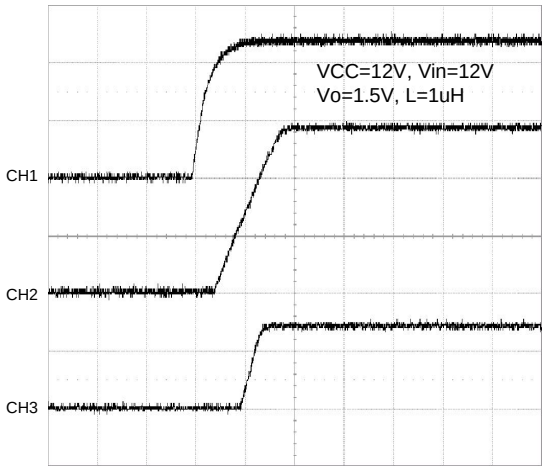
$$I_{PEAK} = \frac{I_{OCSET}(200uA) \times R_{OCSET}}{R_{DS(ON)}}$$

EN (Pin6)

Pull this pin above 1.3V to enable the device and pull this pin below 1.2V to disable the device. In shutdown, the SS is discharged and the UGATE and LGATE pins are held low. Note that don't leave this pin open.

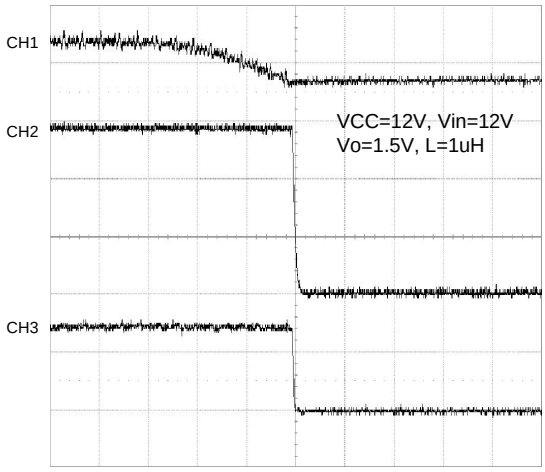
Typical Characteristics

Power On



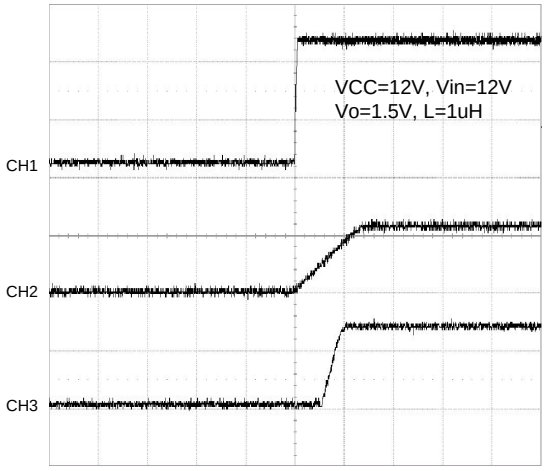
CH1: Vcc (5V/div)
CH2: SS (2V/div)
CH3: Vo (1V/div)
Time: 10ms/div

Power Off



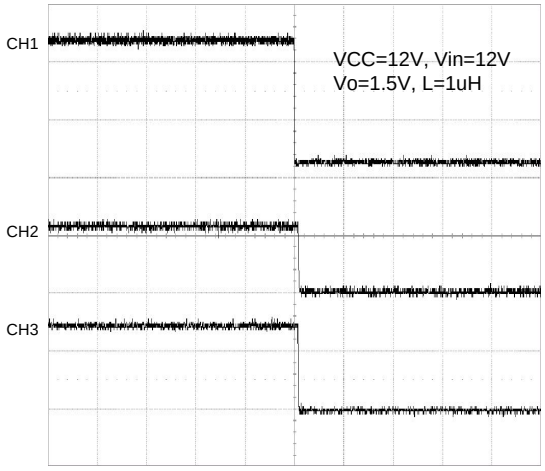
CH1: Vcc (5V/div)
CH2: SS (2V/div)
CH3: Vo (1V/div)
Time: 2ms/div

EN (EN=Vcc)



CH1: EN (5V/div)
CH2: SS (5V/div)
CH3: Vo (1V/div)
Time: 10ms/div

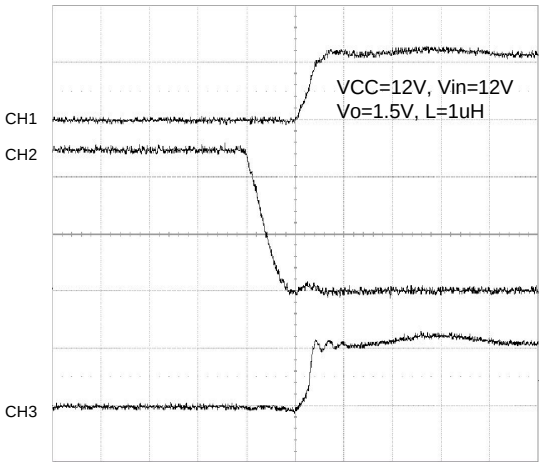
Shutdown (EN=GND)



CH1: EN (5V/div)
CH2: SS (5V/div)
CH3: Vo (1V/div)
Time: 10ms/div

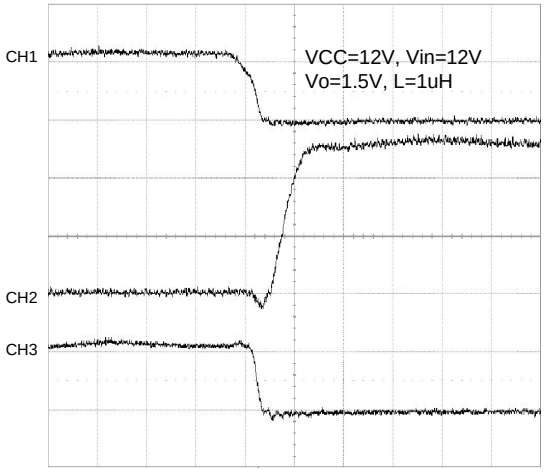
Typical Characteristics

UGATE Rising



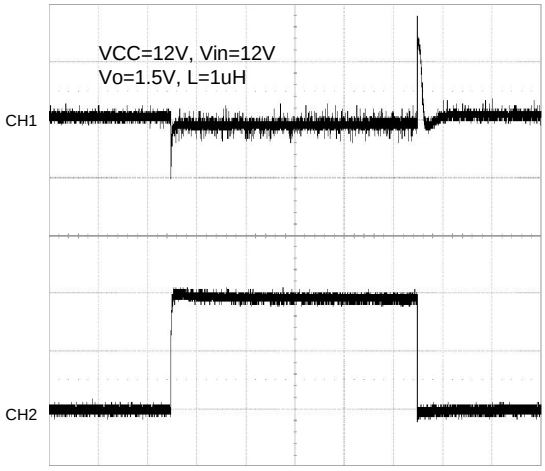
CH1: Ug (20V/div)
CH2: Lg (5V/div)
CH3: Phase (10V/div)
Time: 50ns/div

UGATE Falling



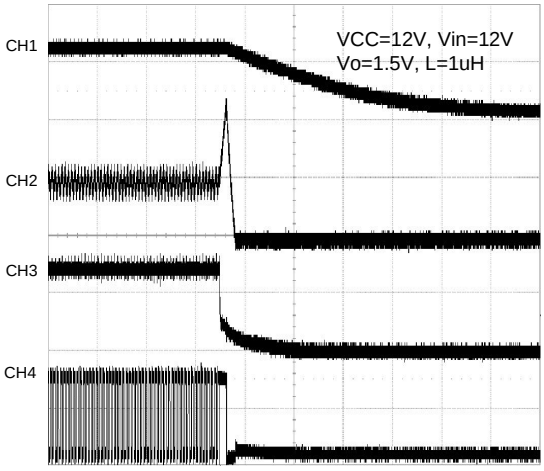
CH1: Ug (20V/div)
CH2: Lg (5V/div)
CH3: Phase (10V/div)
Time: 50ms/div

Load Transient Response



CH1: Vo (500mV/div)
CH2:Io (5A/div)
Time: 200us/div

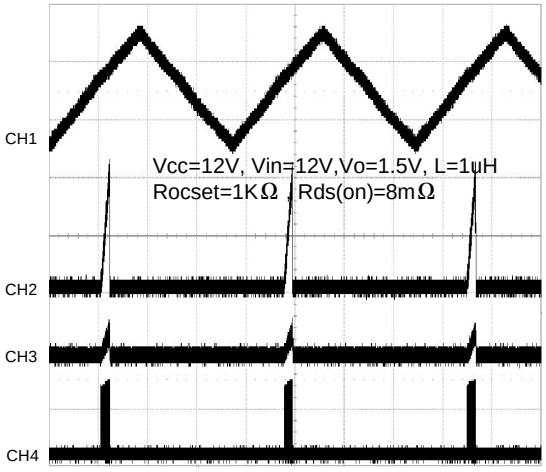
Under Voltage Protection



CH1: SS (5V/div)
CH2: Io (5A/div)
CH3: Vo (1V/div)
CH4: Ug (10V/div)
Time: 50ms/div

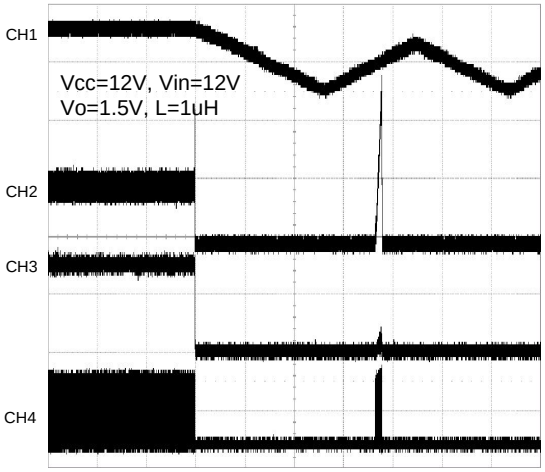
Typical Characteristics

Over Current Protection



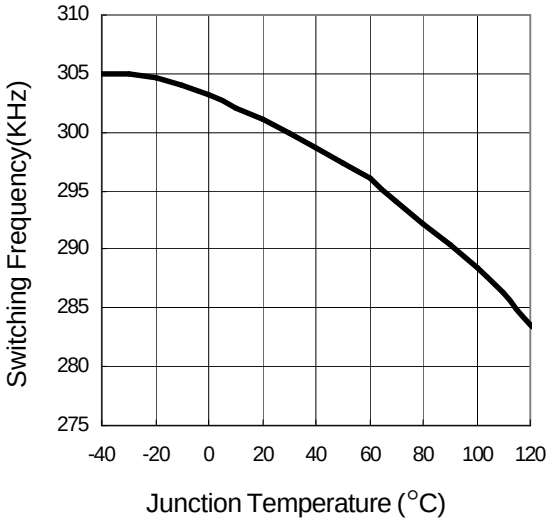
CH1: SS (5V/div)
CH2: IL (10A/div)
CH3: Vo (1V/div)
CH4:Ug (20V/div)
Time: 10ms/div

Short Test

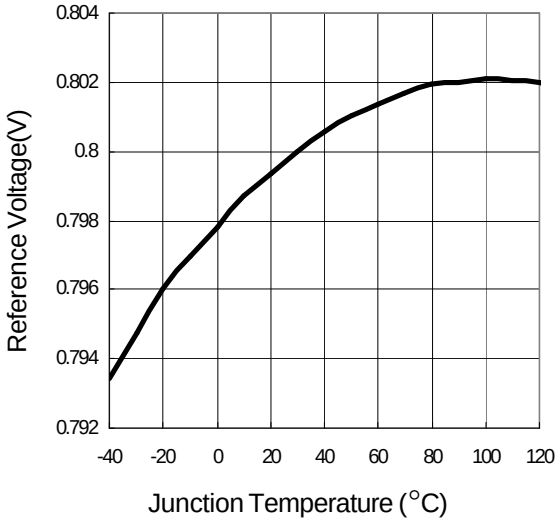


CH1: SS (5V/div)
CH2: IL (10A/div)
CH3: Vo (1V/div)
CH4:Ug (20V/div)
Time: 10ms/div

Switching Frequency vs. Junction Temperature

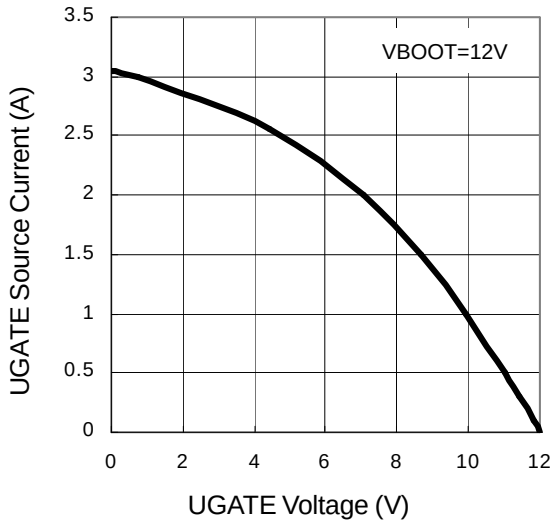


Reference Voltage vs. Junction Temperature

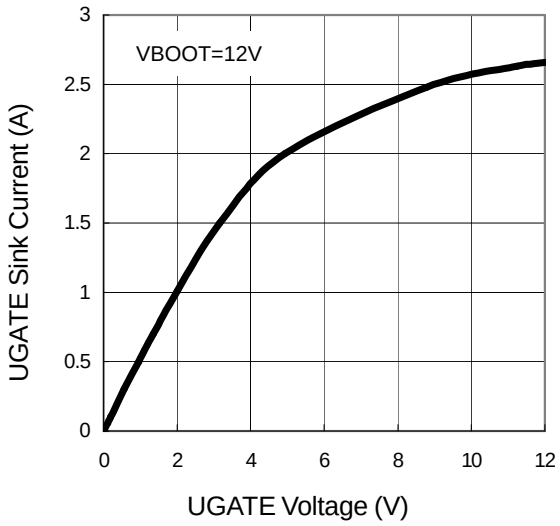


Typical Characteristics

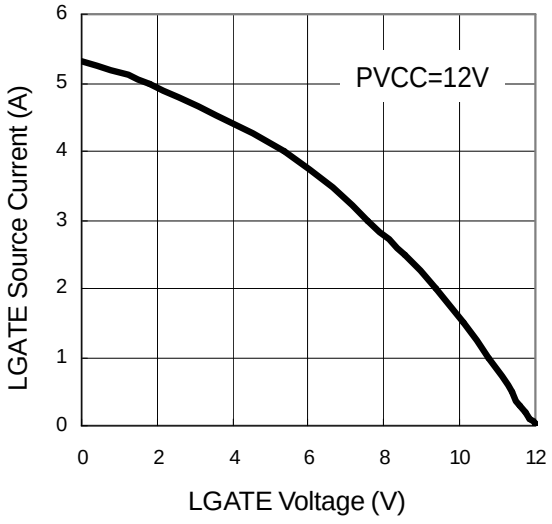
UGATE Source current vs. UGATE Voltage



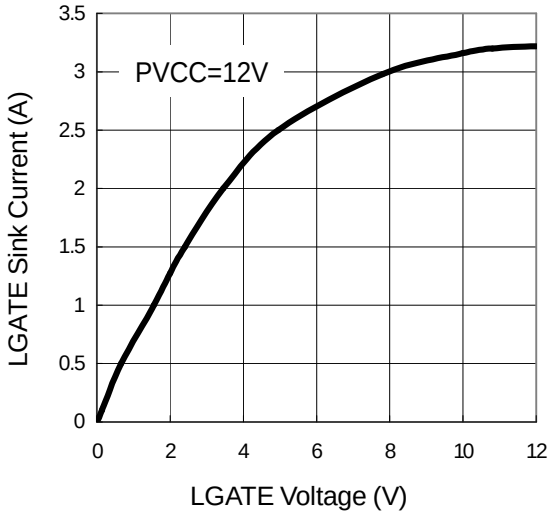
UGATE Sink current vs. UGATE Voltage



LGATE Source current vs. LGATE Voltage



LGATE Sink current vs. LGATE Voltage



Function Descriptions

Power On Reset (POR)

The Power-On Reset (POR) function of APW7074 continually monitors the input supply voltage (VCC), the enable (EN) pin and OCSET pin. The supply voltage (VCC) must exceed its rising POR threshold voltage. The voltage at OCSET pin is equal to V_{IN} less a fixed voltage drop (Vocset = V_{IN} - V_{ROCSET}). EN pin can be pulled high with connecting a resistor to VCC. The POR function initiates soft-start operation after V_{CC}, EN and OCSET voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and VCC are equivalent and the +12V power source must exceed the rising VCC threshold. The POR function inhibits operation at disabled status (EN pin low). With both input supplies above their POR thresholds, the device initiates a soft-start interval.

Soft-Start/EN

The SS/EN pins control the soft-start and enable or disable the controller. Connect a soft-start capacitor from SS pin to GND to set the soft-start interval. Figure1. shows the soft-start interval. When VCC reaches its Power-On-Reset threshold (9.5V), internal 10uA current source starts to charge the capacitor. When the SS reaches the enabled threshold about 1.8V, the internal 0.8V reference starts to rise and follows the SS; the error amplifier output (COMP) suddenly raises to 1.35V, which is the valley of the triangle wave of the oscillator, leads the V_{OUT} to start up. Until the SS reaches about 4.2V, the internal reference completes the soft-start interval and reaches to 0.8V; then V_{OUT} is in regulation. The SS still rises to 5.5V and then stops.

$$T_{Soft-Start} = t_2 - t_1 = \frac{C_{SS}}{I_{SS}} \cdot 2.4V$$

Where:

C_{SS} = external Soft-Start capacitor

I_{SS} = Soft-Start current=10uA

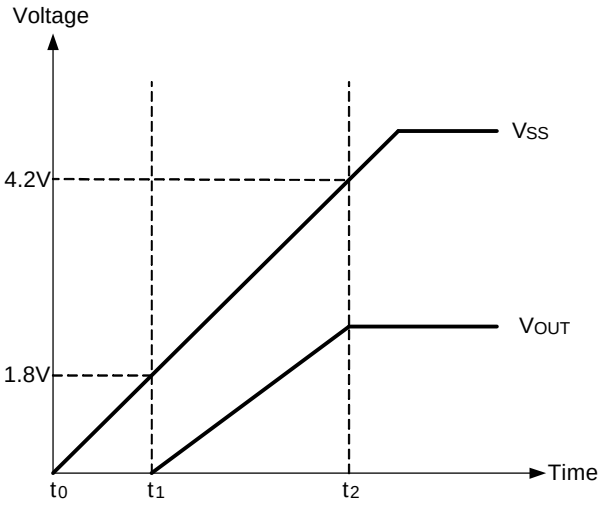


Figure 1. Soft-Start Internal

Over-Current Protection (monitor upper MOSFET)

The APW7074 provides two manners to protect the converter from abnormal output load; one monitors the voltage across the upper MOSFET and use the OCSET pin to set the over-current trip point, the other monitors the voltage across the lower MOSFET by comparing with an internal reference voltage (0.27V).

A resistor (R_{OCSET}) connected between OCSET pin and the drain of the upper MOSFET will determine the over current limit. An internal 200uA current source will flow through this resistor, creating a voltage drop, which will be compared with the voltage across the upper MOSFET. When the voltage across the upper MOSFET exceeds the voltage drop across the R_{OCSET}, an over-current will be detected. The threshold of the over current limit is therefore given by:

$$I_{LIMIT} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be determined.

Function Descriptions (Cont.)

Over-Current Protection (Cont.)

- The MOSFET' $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacturer's datasheet.
- The minimum I_{OCSET} (170uA) and minimum R_{OCSET} should be used in the above equation.
- Note that the I_{LIMIT} is the current flow through the upper MOSFET; I_{LIMIT} must be greater than maximum output current add the half of inductor ripple current.

An over current condition will shut down the device and discharge the C_{SS} with a 10uA sink current and then initiate the soft-start sequence. If the over current condition is not removed during the soft-start interval, the device will be shut down while the over current is detected and the SS still rises to 4V to complete its cycle. The soft start function will be cycled until the over current condition is removed. Both over-current protections have the same behavior while an over current condition is detected.

Over-Current Protection (monitor lower MOSFET)

The other over-current protection monitors the output current by using the voltage drop across the lower MOSFET's $R_{DS(ON)}$ and this voltage drop will be compared with the internal 0.27V reference voltage. If the voltage drop across the lower MOSFET's $R_{DS(ON)}$ is larger than 0.27V, an over-current condition is detected. The threshold of the over current limit is given by:

$$I_{LIMIT} = \frac{0.27V}{R_{DS(ON)}}$$

For the over-current is never occurred in the normal operating load range; the parameters $R_{DS(ON)}$ and I_{LIMIT} in the above equation also have the same notices as the previous section.

Under Voltage Protection

The FB pin is monitored during converter operation by their own Under Voltage (UV) comparator. If the FB voltage drops below 50% of the reference voltage (50% of 0.8V = 0.4V), a fault signal is internally generated, and the device turns off both high-side and low-side MOSFET and the converter's output is latched to be floating.

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.8V. The output voltage is determined by:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

Where R_{OUT} is the resistor connected from V_{OUT} to FB and R_{GND} is the resistor connected from FB to GND.

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

Application Information (Cont.)

Output Inductor Selection (Cont.)

where Fs is the switching frequency of the regulator.

Although increase of the inductor value and frequency reduces the ripple current and voltage, a tradeoff will exist between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_S) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFET and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be parallel to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1uF can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement. There are two components of loss in the MOSFETs: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following:

$$P_{UPPER} = I_{OUT}\,(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_S$$

$$P_{LOWER} = I_{OUT}\,(1+TC)(R_{DS(ON)})(1-D)$$

Where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction loss while the upper MOSFET include an additional transition loss. The switching internal, t_{SW}, is a function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Application Information (Cont.)

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB and V_{OUT} should be added. The compensation network is shown in Fig. 5. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

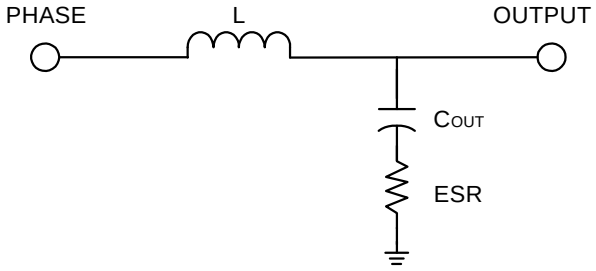


Figure 2. The Output LC Filter

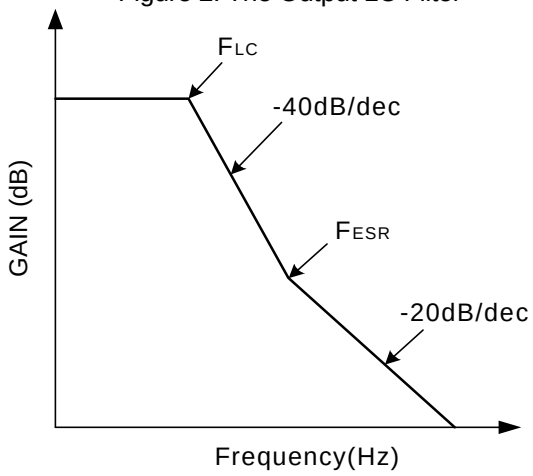


Figure 3. The LC Filter GAIN and Frequency

The PWM modulator is shown in Figure 4. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

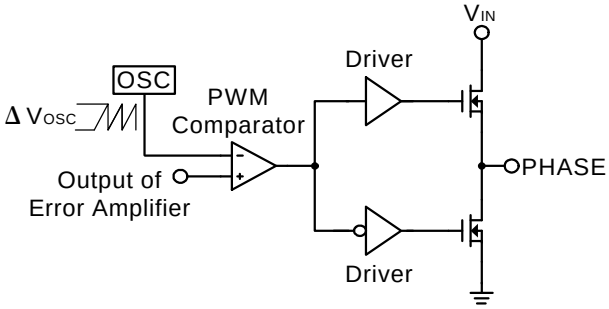


Figure 4. The PWM Modulator

The compensation network is shown in Figure 5. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1} // \left(R2 + \frac{1}{sC2}\right)}{R1 // \left(R3 + \frac{1}{sC3}\right)}$$

$$= \frac{R1 + R3}{R1 \times R3 \times C1} \times \frac{\left(s + \frac{1}{R2 \times C2}\right) \times \left(s + \frac{1}{(R1 + R3) \times C3}\right)}{s\left(s + \frac{C1 + C2}{R2 \times C1 \times C2}\right) \times \left(s + \frac{1}{R3 \times C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2 \times \pi \times R2 \times C2}$$

$$F_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C3}$$

$$F_{P1} = \frac{1}{2 \times \pi \times R2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

$$F_{P2} = \frac{1}{2 \times \pi \times R3 \times C3}$$

Application Information (Cont.)

PWM Compensation (Cont.)

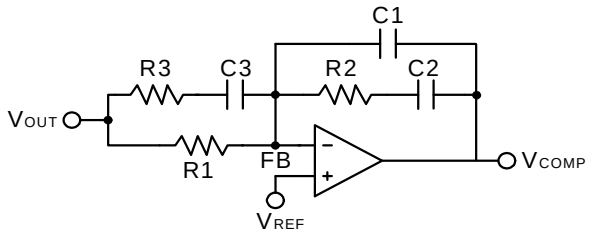


Figure 5. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} X GAIN_{PWM} X GAIN_{AMP}$$

Figure 6. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1.Choose a value for R1, usually between 1K and 5K.

2.Select the desired zero crossover frequency F_O:

$(1/5 \sim 1/10) X F_S > F_O > F_{ESR}$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3.Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

$$F_{Z1} = 0.75 X F_{LC}$$

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4.Set the pole at the ESR zero frequency F_{ESR}:

$$F_{P1} = F_{ESR}$$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5.Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

$$F_{P2} = 0.5 X F_S$$

$$F_{Z2} = F_{LC}$$

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_S}$$

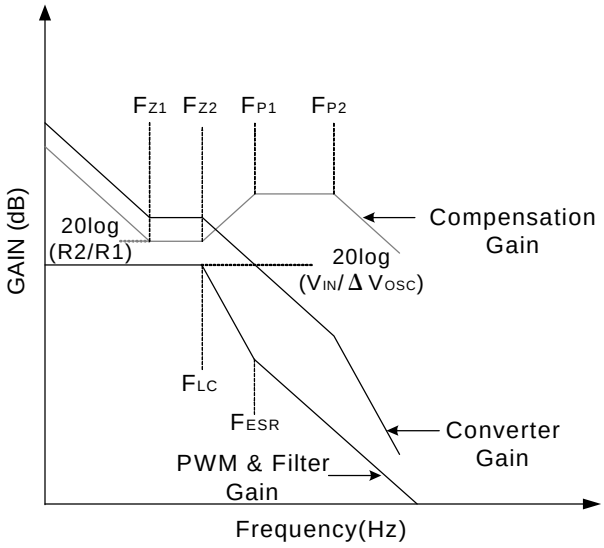


Figure 6. Converter Gain and Frequency

Layout Considerations

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 300KHz, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic

Application Information (Cont.)

Layout Considerations (Cont.)

circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short, wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separate till combined using ground plane construction or single point grounding. Figure 7. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.

- The traces from the gate drivers to the MOSFETs (UG, LG) should be short and wide.

- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.

- Decoupling capacitor, compensation component, the resistor dividers, boot capacitors, and SS capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).

- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.

- The drain of the MOSFETs (V_{IN} and Phase nodes) should be a large plane for heat sinking.

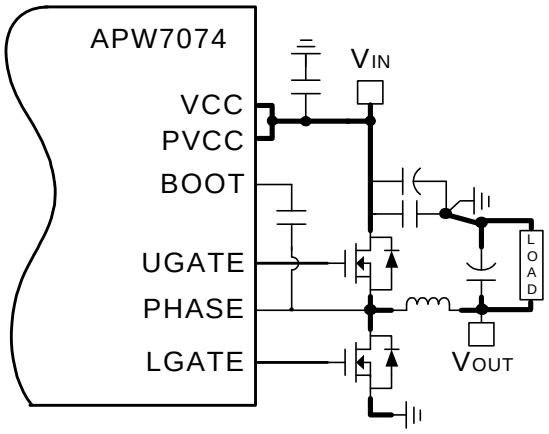
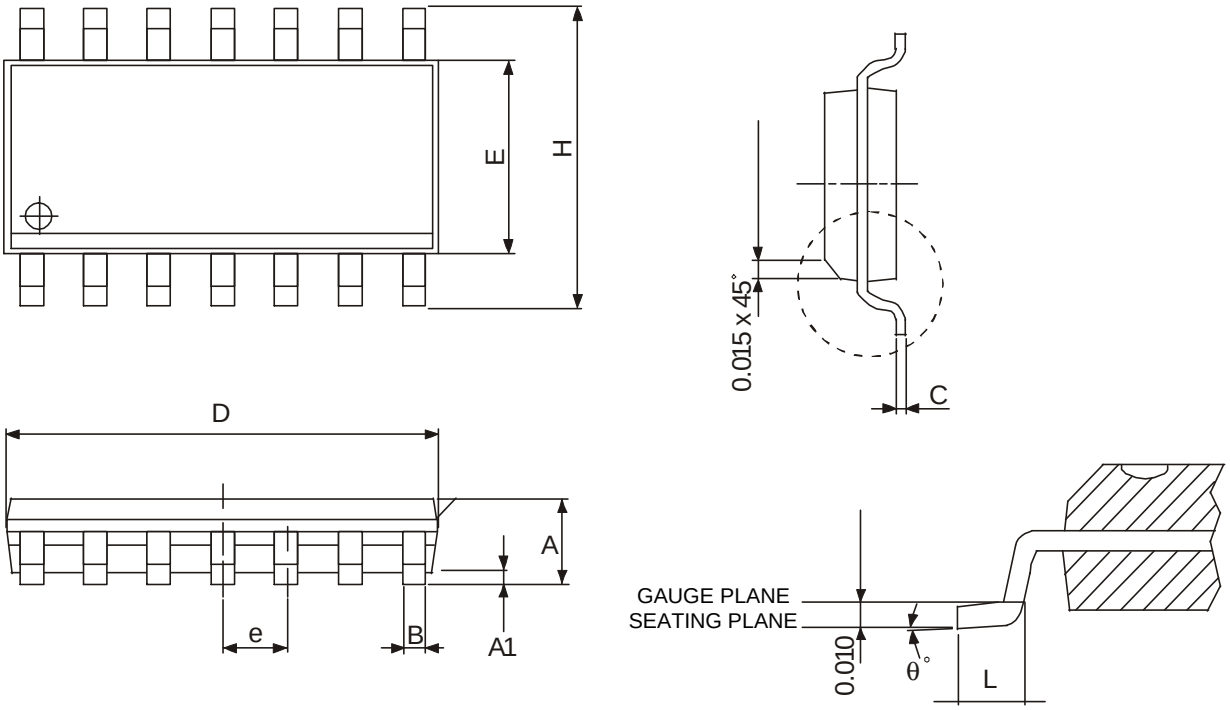


Figure 7.Layout Guidelines

Package Information

SOP – 14 (150mil)

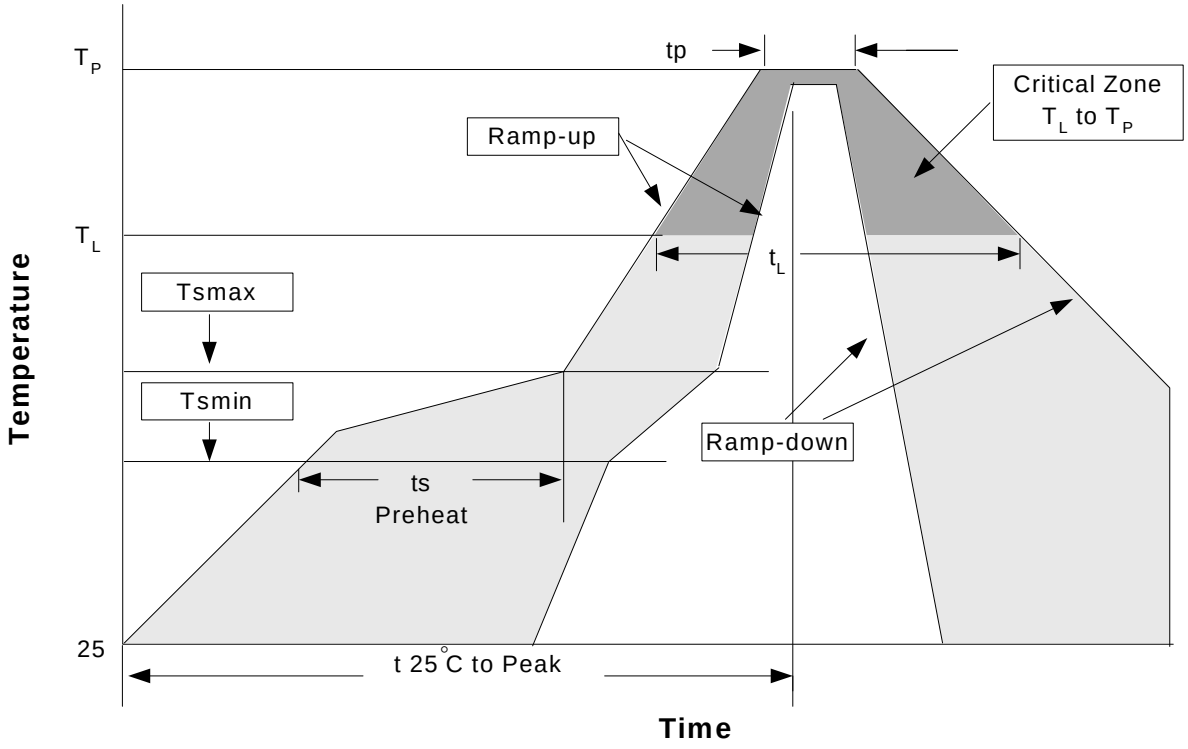


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.477	1.732	0.058	0.068
A1	0.102	0.255	0.004	0.010
B	0.331	0.509	0.013	0.020
C	0.191	0.2496	0.0075	0.0098
D	8.558	8.762	0.336	0.344
E	3.82	3.999	0.150	0.157
e	1.274		0.050	
H	5.808	6.215	0.228	0.244
L	0.382	1.274	0.015	0.050
θ°	0°	8°	0°	8°

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

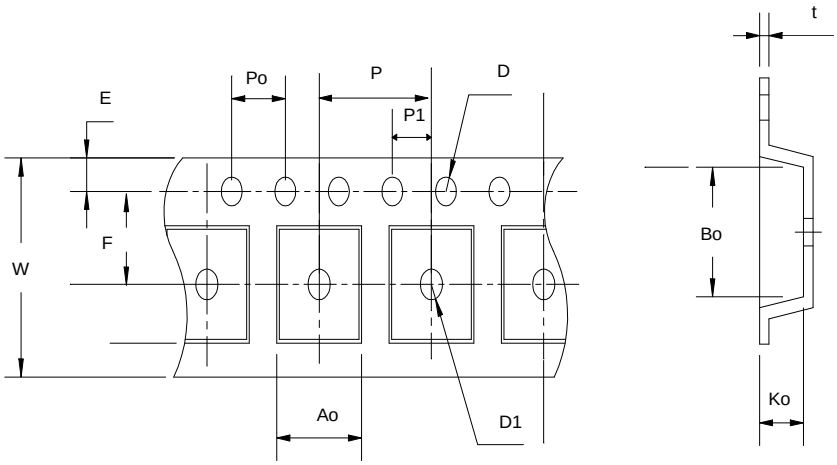
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

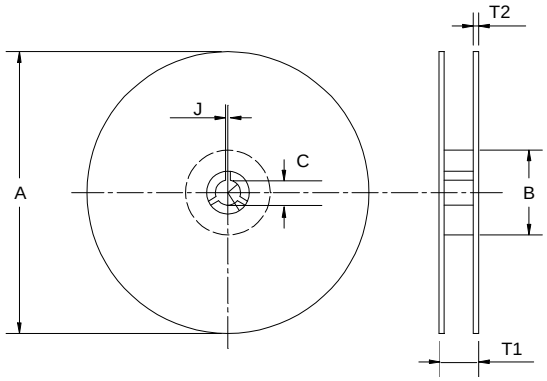
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP-14 (150mil)	330REF	100REF	13.0 + 0.5 - 0.2	2 ± 0.5	16.5REF	2.5 ± 025	16.0 ± 0.3	8	1.75
	F	D	D1	Po	P1	Ao	Ko	t	
	7.5	ϕ0.50 + 0.1	ϕ1.50 (MIN)	4.0	2.0	6.5	2.10	0.3±0.05	

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 14	24	21.3	2500

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