

LINEAR SYSTEMS

Linear Integrated Systems

3N165, 3N166

MONOLITHIC DUAL P-CHANNEL
ENHANCEMENT MODE MOSFET

FEATURES

VERY HIGH INPUT IMPEDANCE

HIGH GATE BREAKDOWN

ULTRA LOW LEAKAGE

LOW CAPACITANCE

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source or Drain-Gate Voltage (NOTE 2)

3N165 40 V

3N166 30 V

Transient G-S Voltage (NOTE 3) ± 125 V

Gate-Gate Voltage ± 80 V

Drain Current (NOTE 2) 50 mA

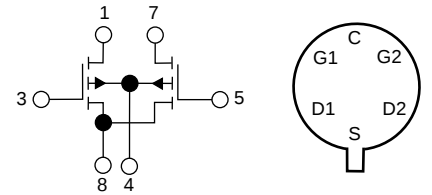
Storage Temperature -65°C to $+200^\circ\text{C}$

Operating Temperature -55°C to $+150^\circ\text{C}$

Lead Temperature (Soldering, 10 sec.) $+300^\circ\text{C}$

Power Dissipation (One Side) 300 mW

Total Derating above 25°C 4.2 mW/ $^\circ\text{C}$



Device Schematic

TO-99
Bottom View

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

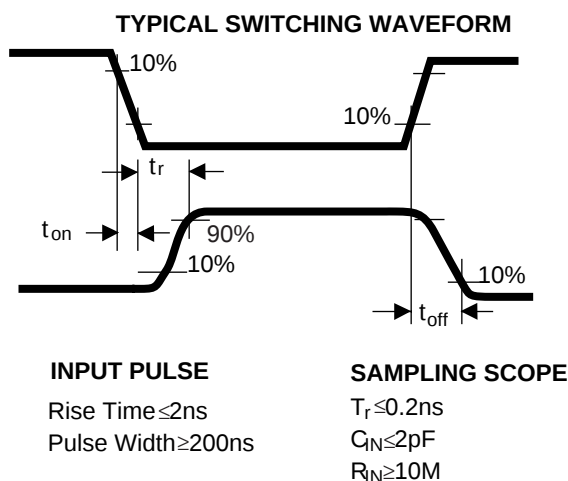
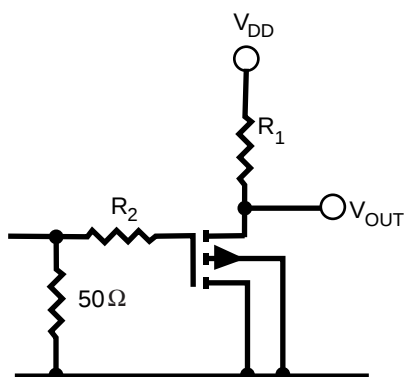
SYMBOL	CHARACTERISTICS	LIMITS		UNITS	CONDITIONS
		MIN.	MAX.		
I_{GSSR}	Gate Reverse Leakage Current	--	10	pA	$V_{GS} = 40$ V
I_{GSSF}	Gate Forward Leakage Current	--	-10		$V_{GS} = -40$ V
		--	-25		$T_A = +125^\circ\text{C}$
I_{DSS}	Drain to Source Leakage Current	--	-200		$V_{DS} = -20$ V
I_{SDS}	Source to Drain Leakage Current	--	-400		$V_{SD} = -20$ V $V_{DB} = 0$
$I_{D(on)}$	On Drain Current	-5	-30	mA	$V_{DS} = -15$ V $V_{GS} = -10$ V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	V	$V_{DS} = -15$ V $I_D = -10$ μA
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	V	$V_{DS} = V_{GS}$ $I_D = -10$ μA
$r_{DS(on)}$	Drain Source ON Resistance	--	300	ohms	$V_{GS} = -20$ V $I_D = -100$ μA
g_{fs}	Forward Transconductance	1500	3000	μS	$V_{DS} = -15$ V $I_D = -10$ mA $f = 1$ kHz
g_{os}	Output Admittance	--	300	μS	
C_{iss}	Input Capacitance	--	3.0	pF	$V_{DS} = -15$ V $I_D = -10$ mA $f = 1$ MHz
C_{rss}	Reverse Transfer Capacitance	--	0.7		
C_{oss}	Output Capacitance	--	3.0		
$R_E(Y_{fs})$	Common Source Forward Transconductance	1200	--	μS	$V_{DS} = -15$ V $I_D = -10$ mA $f = 100$ MHz (NOTE 4)

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MATCHING CHARACTERISTICS 3N165

SYMBOL	CHARACTERISTICS	LIMITS		UNITS	CONDITIONS
		MIN.	MAX.		
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		$V_{DS} = -15\text{ V}$ $I_D = -500\text{ }\mu\text{A}$ $f=1\text{kHz}$
V_{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	$V_{DS} = -15\text{ V}$ $I_D = -500\text{ }\mu\text{A}$
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature	--	100	$\mu\text{V}/^\circ\text{C}$	$V_{DS} = -15\text{ V}$ $I_A = -500\text{ }\mu\text{A}$ $T_A = -55^\circ\text{C to } +25^\circ\text{C}$



Switching Times Test Circuit

NOTES:

1. MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures:
To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanent damage to the devices.
2. Per transistor.
3. Devices must not be tested at $\pm 125\text{V}$ more than once, nor for longer than 300ms.
4. For design reference only, not 100% tested.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.