

384-OUTPUT TFT-LCD SOURCE DRIVER
(COMPATIBLE WITH 256-GRAY SCALES)
DESCRIPTION

The μ PD160040 is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ -corrected by an internal D/A converter and 8-by-2 external power modules.

Because the output dynamic range is as large as $V_{SS2} + 0.2$ V to $V_{DD2} - 0.2$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity.

FEATURES

- CMOS level input
- 384 outputs
- Input of 8 bits (gray scale data) by 6 dots
- Capable of outputting 256 values by means of 8-by-2 external power modules (16 units) and a D/A converter
- Logic power supply voltage (V_{DD1}): 2.5 to 3.6 V
- Driver power supply voltage (V_{DD2}): 12.5 to 15.5 V (switchable, V_{SEL})
- Output dynamic range: $V_{SS2} + 0.2$ V to $V_{DD2} - 0.2$ V
- High-speed data transfer: $f_{CLK.} = 55$ MHz MAX. (internal data transfer speed when operating at 3.0 V $\leq V_{DD1} \leq 3.6$ V)
 $f_{CLK.} = 40$ MHz MAX. (internal data transfer speed when operating at 2.5 V $\leq V_{DD1} < 3.0$ V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Output inversion function (POL21, POL 22)
- Output reset control is possible (MODE)
- Through-rate control is possible (SRC)
- Output resistance control is possible (ORC)
- Single bank arrangement is possible (loaded with slim TCP)

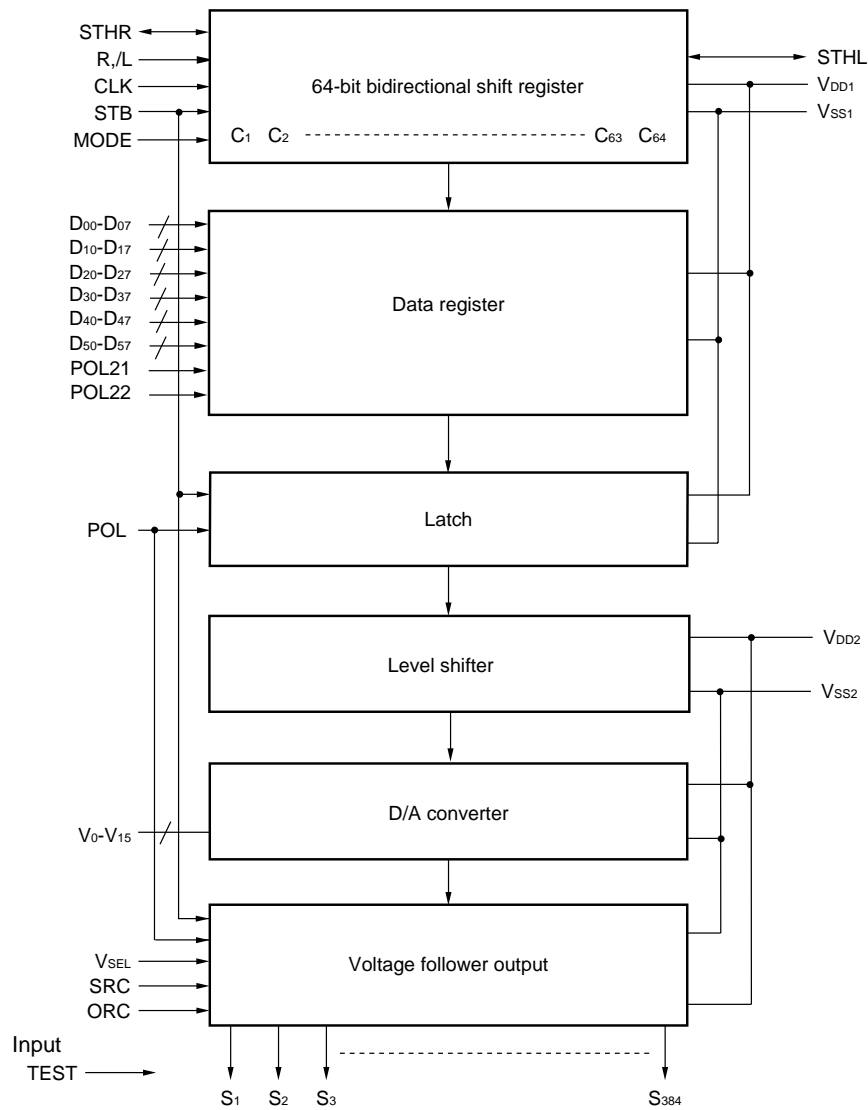
ORDERING INFORMATION

Part Number	Package
μ PD160040N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

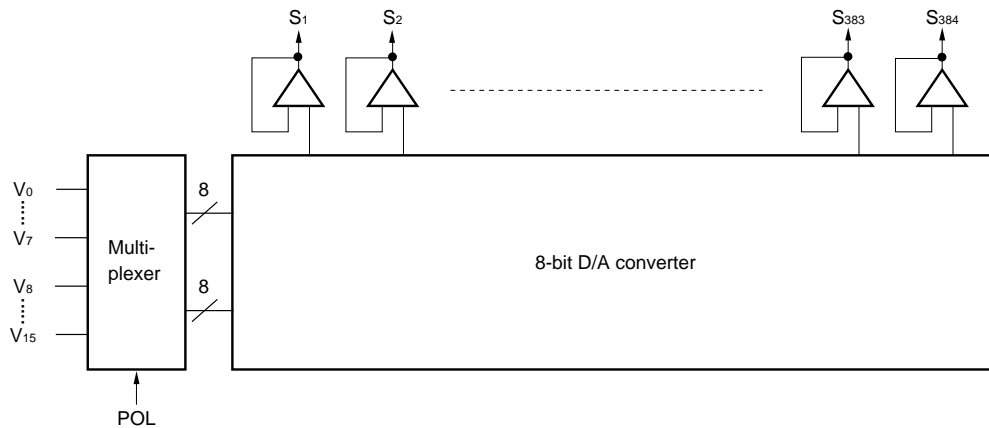
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1. BLOCK DIAGRAM

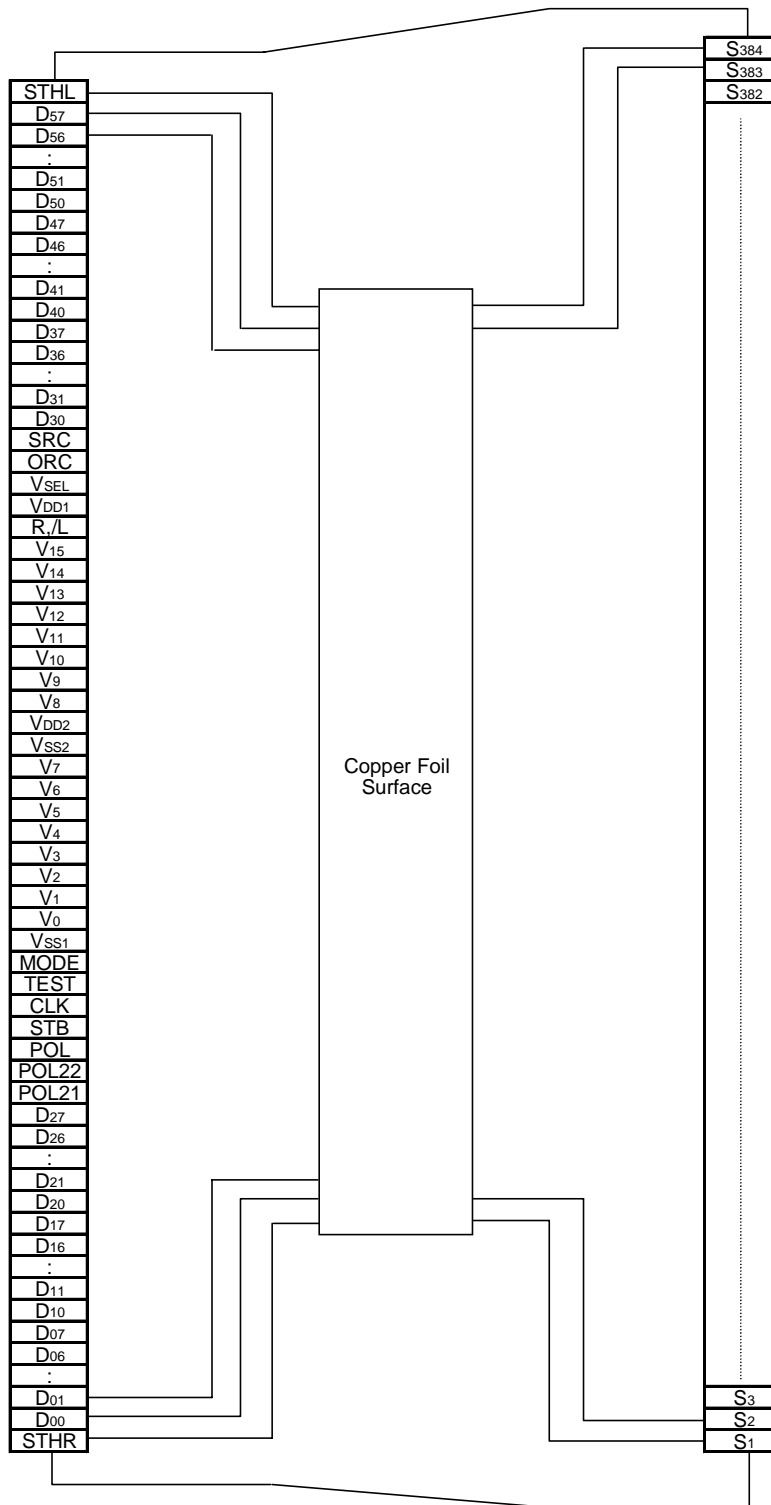


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD160040N-xxx) (Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S ₁ to S ₃₈₄	Driver	Output	The D/A converted 256-gray-scale analog voltage is output.
D ₀₀ to D ₀₇	Port 1 display data	Input	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). D _{x0} : LSB, D _{x7} : MSB
D ₁₀ to D ₁₇			
D ₂₀ to D ₂₇			
D ₃₀ to D ₃₇	Port 2 display data	Input	
D ₄₀ to D ₄₇			
D ₅₀ to D ₅₇			
R,/L	Shift direction control	Input	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR input, S ₁ →S ₃₈₄ , STHL output R,/L = L (left shift): STHL input, S ₃₈₄ →S ₁ , STHR output
★ STHR	Right shift start pulse	I/O	These are the start pulse input/output pins when connected in cascade. Loading of display data starts when a H level is read at the rising edge of CLK. A H level should be input at the pulse of one cycle of the clock signal. If the start pulse input is more than 2 CLK, the first 1 CLK of the H-level input is valid. For right shift, STHR is input and STHL is output. For left shift, STHL is input and STHR is output.
★ STHL	Left shift start pulse	I/O	
CLK	Shift clock	Input	The shift clock input pin of shift register. The display data is loaded into the data register at the rising edge. When 66-clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. In addition, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
SRC	Through rate control	Input	SRC = H: High-through-rate period (large current consumption) SRC = L: Low-through-rate period (small current consumption) SRC is pulled up to the V _{DD1} in the IC.
ORC	Output resistance control	Input	ORC = H: Low output resistance period ORC = L: High output resistance period ORC is pulled up to the V _{DD1} in the IC.
POL	Polarity input	Input	POL = L: The S _{2n-1} output uses V ₀ -V ₇ as the reference supply. The S _{2n} output uses V ₈ -V ₁₅ as the reference supply. POL = H: The S _{2n-1} output uses V ₈ -V ₁₅ as the reference supply. The S _{2n} output uses V ₀ -V ₇ as the reference supply. S _{2n-1} indicates the odd output and S _{2n} indicates the even output. Input of the POL signal is allowed the setup time (t _{POL-STB}) with respect to STB's rising edge. When it switches such as POL = H→L or L→H, all output pins are output reset during STB = H. When it does not switch, all output pins become Hi-Z (high impedance) during STB = H. Refer to 7. RELATIONSHIP BETWEEN MODE, STB, SRC, ORC, POL, AND OUTPUT WAVEFORM for details.

(2/2)

Pin Symbol	Pin Name	I/O	Description
MODE	Output reset control	Input	MODE = H or open: Output reset MODE = L: No output reset MODE is pulled up to the V _{DD1} in the IC.
POL21, POL22	Data inversion	Input	Select of inversion or no inversion for input data. POL21: Data inversion or no inversion of Port1. POL22: Data inversion or no inversion of Port2 POL21, POL22 = H: Data are inverted in the IC. POL21, POL22 = L: Data are not inverted in the IC.
V _{SEL}	Driver voltage select	Input	The driver voltage can be switched by controlling the stationary bias current of the output amplifier via V _{SEL} . V _{SEL} = H: V _{DD2} = 12.5 to (14.0 V) (large bias current) V _{SEL} = L or open: V _{DD2} = (14.0 V) to 15.0 V (small bias current) LPC is pulled down to the V _{SS1} in the IC.
TEST	Test	Input	Normally, set the TEST pin to H or leave open. This pin is pulled up to V _{DD1} in the IC.
V ₀ -V ₁₅	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. Make sure to maintain the following relationships. V _{DD2} – 0.2 V ≥ V ₀ > V ₁ > V ₂ > V ₁ > V ₂ >... ... > V ₆ > V ₇ ≥ 0.5 V _{DD2} + 0.5 V 0.5 V _{DD2} – 0.5 V ≥ V ₈ > V ₉ > V ₁₀ > > V ₁₄ > V ₁₅ ≥ V _{SS2} + 0.2 V
V _{DD1}	Logic power supply	–	2.5 to 3.6 V
V _{DD2}	Driver power supply	–	12.5 to 15.5 V
V _{SS1}	Logic ground	–	Grounding
V _{SS2}	Driver ground	–	Grounding

- Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V₀-V₁₅ in that order. Reverse this sequence to shut down.**
- 2. To stabilize the supply voltage, please be sure to insert a 0.47 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.1 μF is also advised between the γ-corrected power supply terminals (V₀, V₁, V₂,... ..., V₁₅) and V_{SS2}.**

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD160040 incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r₀ to r₂₅₃) are designed so that the ratio of LCD panel (γ-compensated voltages to V₀'-V₂₅₅' and V₀''-V₂₅₅'' is almost equivalent as shown in Figure 5-2. For the 2 sets of eight γ-compensated power supplies, V₀-V₇ and V₈-V₁₅, respectively, input gray scale voltages of the same polarity with respect to the 0.5 V_{DD2}.

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2}, V_{SS2} and 0.5 V_{DD2}, and γ-corrected voltages V₀ to V₁₅ and the input data. Be sure to maintain the voltage relationships below.

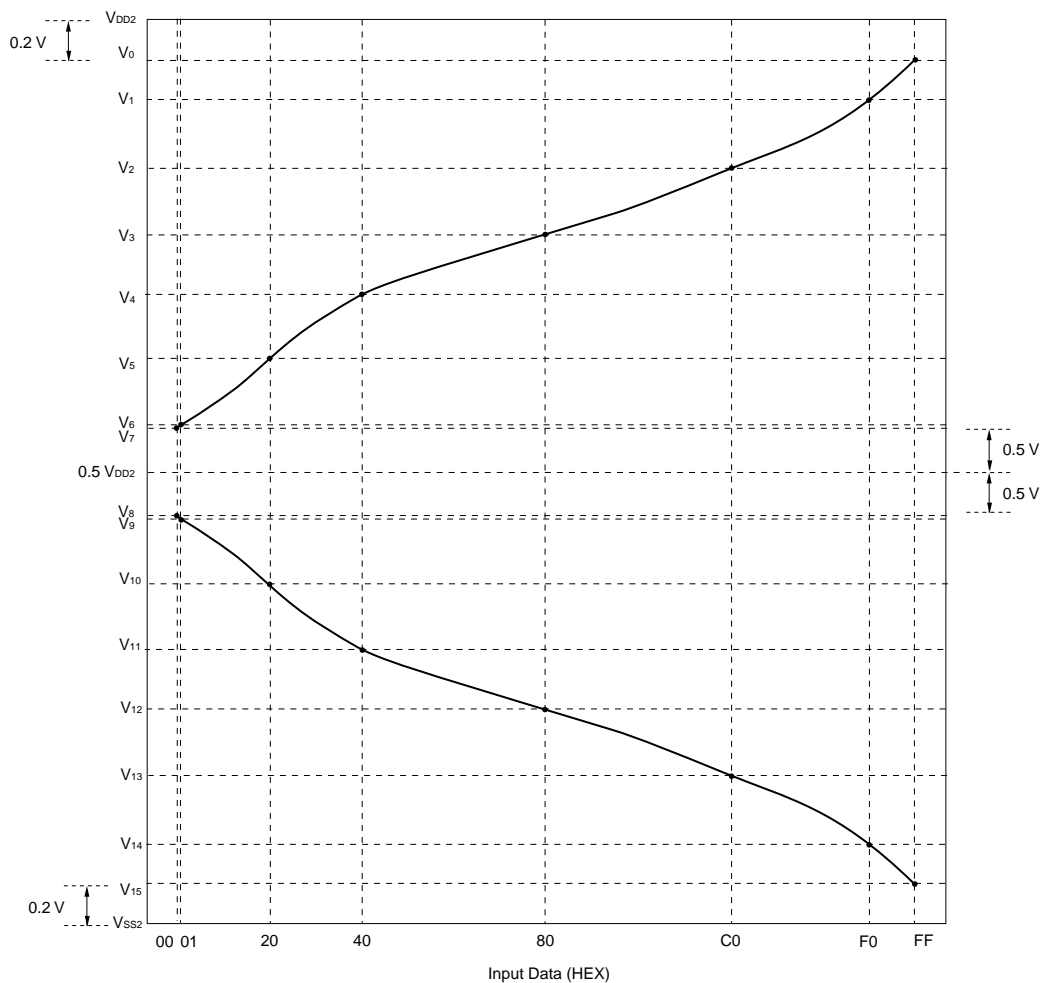
$$V_{DD2} - 0.2 V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5 V_{DD2} + 0.5 V$$

$$0.5 V_{DD2} - 0.5 V \geq V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} \geq V_{SS2} + 0.2 V$$

Also, V₆-V₇ and V₈-V₉ are left open in the IC. Be sure to input the gray scale level power supply at a constant level to the all pins, as V₀-V₁₅.

Figures 5-3 shows the relationship between the input data and the output voltage.

Figure 5-1. Relationship between Input Data and γ-corrected Power Supplies



6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 8 bits x 2 RGBs (6 dots)

Input width: 48 bits (2-pixel data)

(1) R,/L = H (right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

(2) R,/L = L (left shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

POL	S _{2n-1} ^{Note}	S _{2n} ^{Note}
L	V ₀ -V ₇	V ₈ -V ₁₅
H	V ₈ -V ₁₅	V ₀ -V ₇

Note S_{2n-1} (odd output), S_{2n} (even output), n = 1, 2, ..., 192.

7. RELATIONSHIP BETWEEN MODE, STB, SRC, ORC, POL, AND OUTPUT WAVEFORM

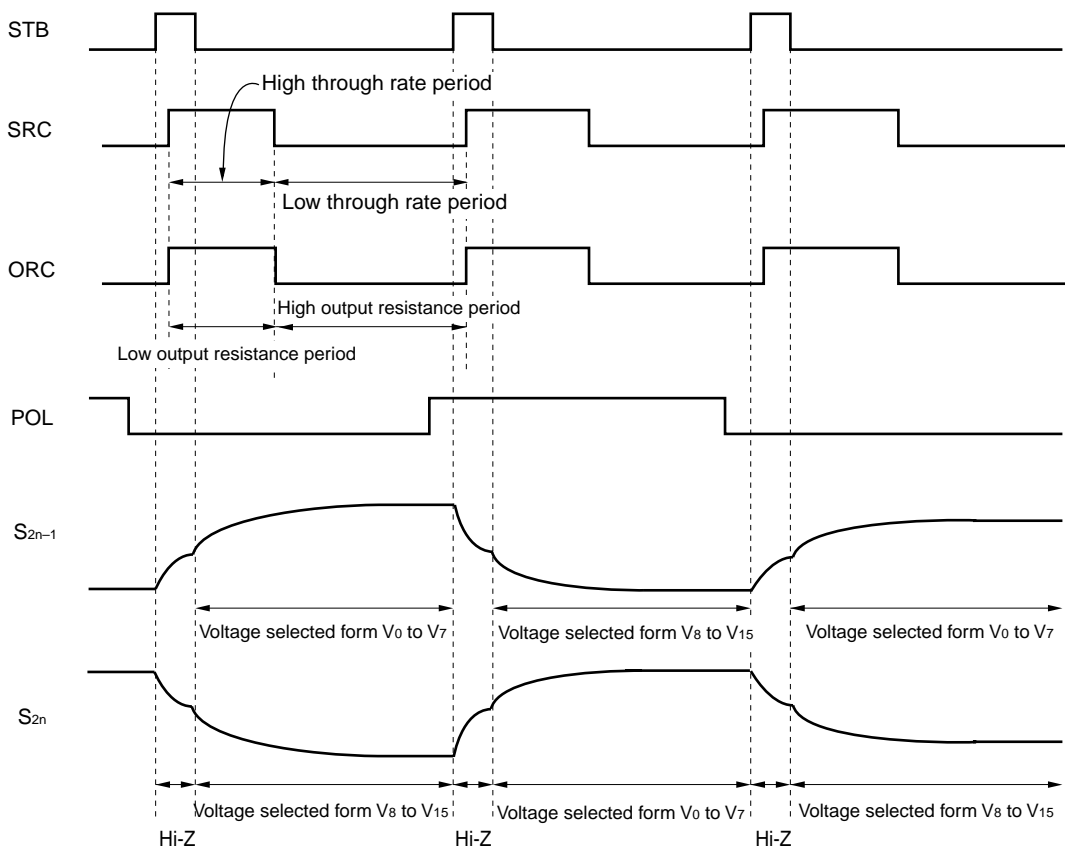
When MODE = H or open and STB = H, all outputs are reset (short) and the gray-scale voltage is output to LCD in synchronization with the falling edge of STB.

When MODE = L and STB = H, all outputs became Hi-Z and the gray-scale voltage is output to the LCD in synchronization with the falling edge of STB.

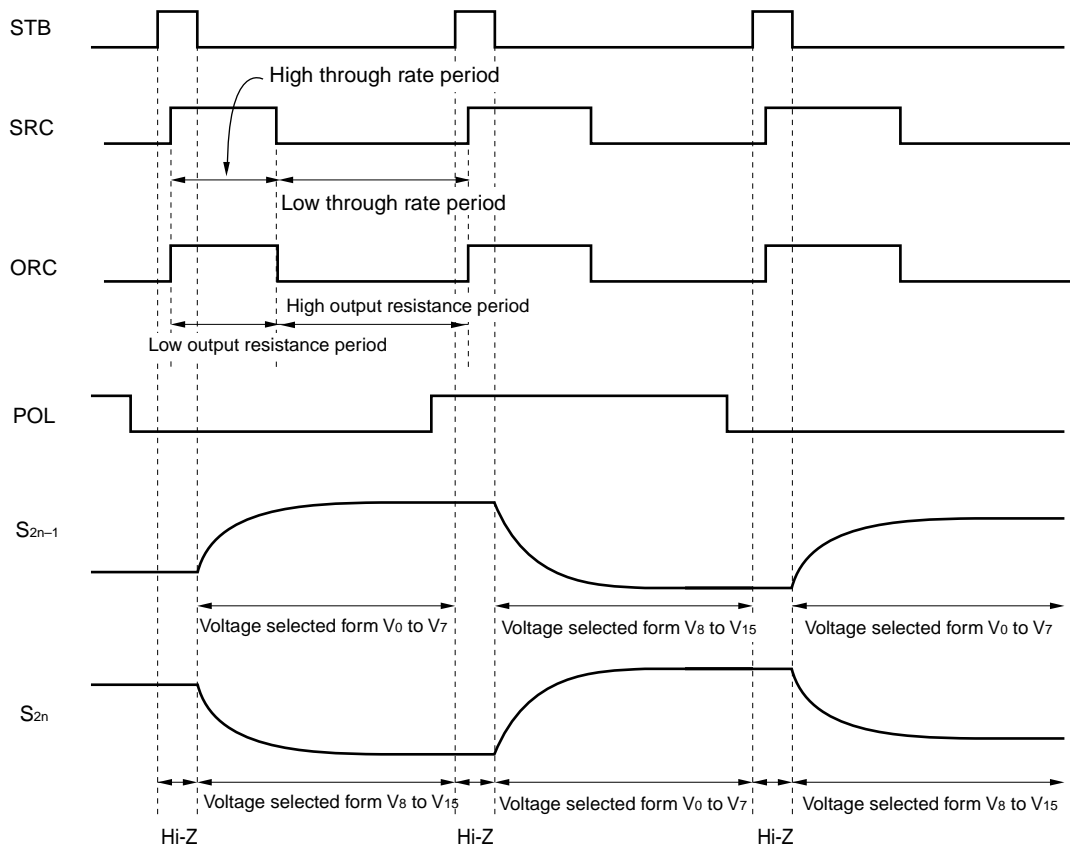
Also, setting the SRC pin to H level allows the bias current value of the output amplifier to rise temporarily, and setting the ORC pin to H level allows the output resistance value of the amplifier to lower temporarily.

For the timing and the processing of STB, SRC, or ORC during a high-level period, We recommend a thorough evaluation of the LCD panel specifications in advance.

(1) MODE = H or open



(2) MODE = L



8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic part supply voltage	V _{DD1}	-0.5 to +4.0	V
Driver part supply voltage	V _{DD2}	-0.5 to +17.0	V
Logic part input voltage	V _{I1}	-0.5 to V _{DD1} + 0.5	V
Driver part input voltage	V _{I2}	-0.5 to V _{DD2} + 0.5	V
Logic part output voltage	V _{O1}	-0.5 to V _{DD1} + 0.5	V
Driver part output voltage	V _{O2}	-0.5 to V _{DD2} + 0.5	V
Operating ambient temperature	T _A	-10 to +75	°C
Storage temperature	T _{stg}	-55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = -10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Logic part supply voltage	V _{DD1}		2.5		3.6	V
Driver part supply voltage	V _{DD2}	V _{SEL} = H	12.5	13.0	(14.0)	V
		V _{SEL} = L or open	(14.0)	15.0	15.5	
High-level input voltage	V _{IH}		0.7 V _{DD1}		V _{DD1}	V
Low-level input voltage	V _{IL}		0		0.3 V _{DD1}	V
γ-corrected voltage	V ₀ -V ₇		0.5 V _{DD2} + 0.5		V _{DD2} - 0.2	V
	V ₈ -V ₁₅		0.2		0.5 V _{DD2} - 0.5	V
Driver part output voltage	V _O		0.2		V _{DD2} - 0.2	V
Clock frequency	f _{CLK}	3.0 V ≤ V _{DD1} ≤ 3.6 V			55	MHz
		2.5 V ≤ V _{DD1} < 3.0 V			40	MHz

Remark The value enclosed in parentheses is a reference value.

Electrical Characteristics (T_A = -10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 12.5 to 15.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I _{IL}				±1.0	μA
High-level output voltage	V _{OH}	STHR (STHL), I _{OH} = 0 mA	V _{DD1} - 0.1			V
Low-level output voltage	V _{OL}	STHR (STHL), I _{OL} = 0 mA			0.1	V
★ γ-corrected resistance	R _γ	V _{DD2} = 15.0 V, V ₀ -V ₇ = V ₈ -V ₁₅ = 7.0 V	5.14	10.3	15.4	kΩ
★ Driver output current	I _{VOH}	V _X = 12.0 V, V _{OUT} = 11.0 V ^{Note1}			-0.40	mA
	I _{VOL}	V _X = 1.0 V, V _{OUT} = 2.0 V ^{Note1}	0.65			mA
★ Output voltage deviation	ΔV _O	T _A = 25°C, V _{SS2} + 1.0 V to V _{DD2} - 1.0 V		±10	±20	mV
★ Output swing voltage difference deviation	ΔV _{P-P1}	V _{DD1} = 3.3 V, V _{OUT} = 7.0 to 8.0 V ^{Note1}		±5	±10	mV
	ΔV _{P-P2}	V _{DD2} = 15.0 V, V _{OUT} = 4.0 to 11.0 V ^{Note1}		±7	±15	mV
	ΔV _{P-P3}	T _A = 25°C, V _{OUT} = 1.0 to 14.0 V ^{Note1}		±10	±20	mV
★ Logic part dynamic current consumption	I _{DD1}	V _{DD1} ^{Notes2,3}		1.3	12	mA
★ Driver part dynamic current consumption	I _{DD2}	V _{DD2} , with no load ^{Notes3,4}		12	30	mA

Notes 1. V_X refers to the output voltage of analog output pins S₁ to S₃₈₄.

V_{OUT} refers to the voltage applied to analog output pins S₁ to S₃₈₄

2. f_{STB} = 64 kHz, f_{CLK} = 54 MHz

3. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

4. Refers to the current consumption per driver when cascades are connected under the assumption of SXGA single-sided mounting (10 units).

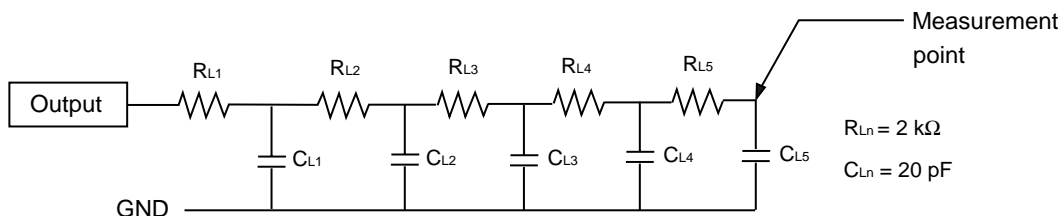
Switching Characteristics (T_A = -10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 12.5 to 15.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t _{PLH1}	C _L = 15 pF, 3.0 V ≤ V _{DD} ≤ 3.6 V			17	ns
		C _L = 15 pF, 2.5 V ≤ V _{DD} < 3.0 V			24	ns
★ Driver output delay time	t _{PLH2} ^{Note}	C _L = 100 pF, R _L = 10 kΩ			5	μs
	t _{PLH3} ^{Note}				10	μs
	t _{PHL2} ^{Note}				5	μs
	t _{PHL3} ^{Note}				10	μs
Input capacitance	C _{I1}	logic input, except STHR (STHL), T _A = 25°C		5	10	pF
	C _{I2}	STHR (STHL), T _A = 25°C		10	15	pF

Note t_{PLH2}, t_{PHL2} refer to the arrival time from falling edge of STB to target voltage ±10%

t_{PLH3}, t_{PHL3} refer to the arrival time from falling edge of STB to target voltage ±0.02 V (condition: V_O = 3.0 V ↔ 12.0 V)

★ <Test Condition>



Timing Requirements (T_A = -10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{SS1} = 0 V, t_r = t_f = 5.0 ns)

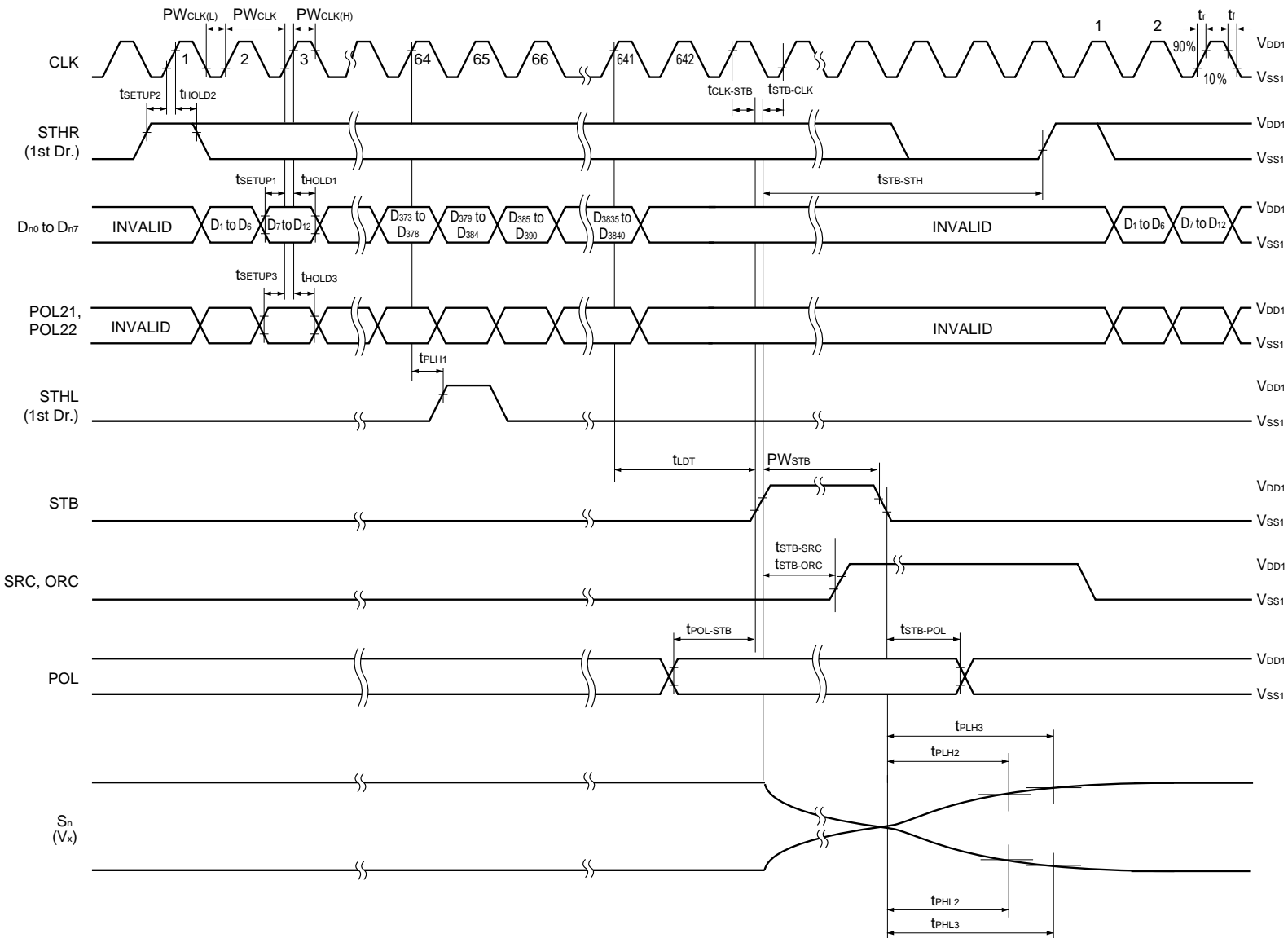
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW _{CLK}	3.0 V ≤ V _{DD1} ≤ 3.6 V	18			ns
		2.5 V ≤ V _{DD1} < 3.0 V	25			ns
Clock pulse high period	PW _{CLK (H)}	3.0 V ≤ V _{DD1} ≤ 3.6 V	4			ns
		2.5 V ≤ V _{DD1} < 3.0 V	6			ns
Clock pulse low period	PW _{CLK (L)}		4			ns
Data setup time	t _{SETUP1}		0			ns
Data hold time	t _{HOLD1}		4			ns
Start pulse setup time	t _{SETUP2}		0			ns
Start pulse hold time	t _{HOLD2}		4			ns
POL21, POL22 setup time	t _{SETUP3}		0			ns
POL21, POL22 hold time	t _{HOLD3}		4			ns
STB pulse width	PW _{STB}		1.0			μs
Last data timing	t _{LDT}		2			CLK
CLK-STB time	t _{CLK-STB}	CLK ↑ → STB ↑	4			ns
STB-CLK time	t _{STB-CLK}	STB ↑ → CLK ↑	4			ns
Time between STB and start pulse	t _{STB-STH}	STB ↑ → STHR (STHL) ↑	2			CLK
POL-STB time	t _{POL-STB}	POL ↑ or ↓ → STB ↑	4			ns
STB-POL time	t _{STB-POL}	STB ↓ → POL ↓ or ↑	4			ns
STB-SRC time	t _{STB-SRC}	STB ↑ → SRC ↑	0			ns
STB-ORC time	t _{STB-ORC}	STB ↓ → ORC ↑	0			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

Switching Characteristic Waveform

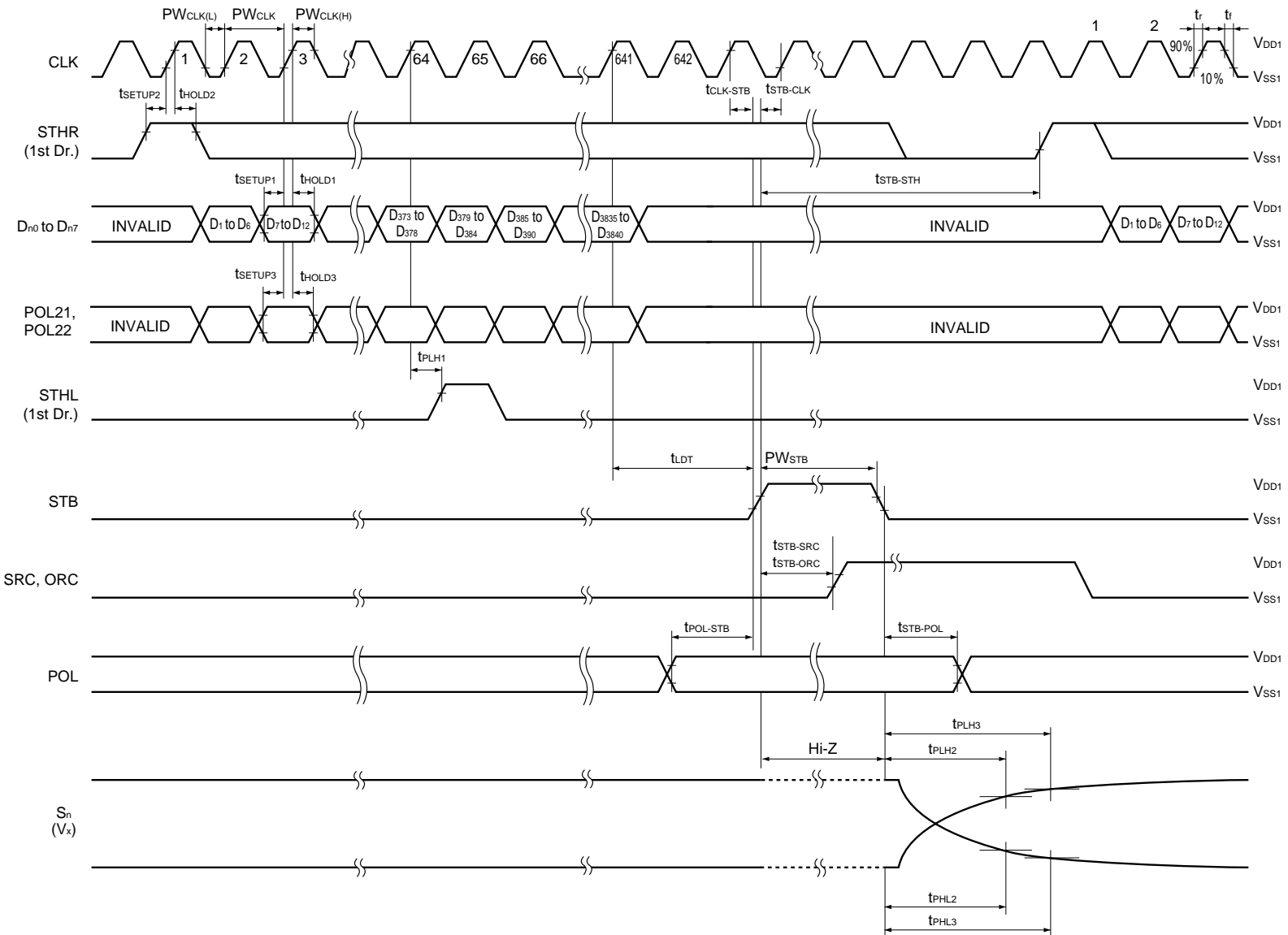
(1) R/L=H, MODE = H or open

Unless otherwise specified, V_{IH} , V_{IL} are defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$ (numbers clock and display data are example when in SXGA).



(2) R/L = H, MODE = L

Unless otherwise specified, V_{IH} , V_{IL} are defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$ (Numbers clock and display data are example when in SXGA).



9. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD160040.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD160040N-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100g (per solder).
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C, pressure 3 to 8 kg/cm ² , time 3 to 5 sec. Real bonding 165 to 180°C, pressure 25 to 45 kg/cm ² , time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.