

# PESDxV4UW series

Very low capacitance quadruple ESD protection diode arrays in SOT665 package

Rev. 01 — 22 April 2005

Product data sheet

## 1. Product profile

### 1.1 General description

Very low capacitance quadruple ElectroStatic Discharge (ESD) protection diode arrays in ultra small SOT665 plastic package designed to protect up to four signal lines from the damage caused by ESD and other transients.

### 1.2 Features

- ESD protection of up to four lines
- Very low diode capacitance
- Low clamping voltage
- Ultra low leakage current:  $I_{RM} = 3 \text{ nA}$
- ESD protection up to 12 kV
- IEC 61000-4-2; level 4 (ESD)

### 1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- Portable electronics
- Subscriber Identity Module (SIM) card protection

### 1.4 Quick reference data

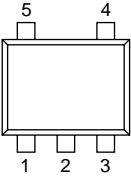
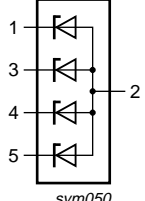
Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RWM}$	reverse stand-off voltage					
	PESD3V3V4UW		-	-	3.3	V
	PESD5V0V4UW		-	-	5.0	V
$C_d$	diode capacitance	$f = 1 \text{ MHz};$ see <a href="#">Figure 5</a> ; $V_R = 0 \text{ V}$				
	PESD3V3V4UW		-	15	18	pF
	PESD5V0V4UW		-	12	15	pF

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## 2. Pinning information

**Table 2: Pinning**

Pin	Description	Simplified outline	Symbol
1	cathode 1		 <p style="text-align: right; font-size: small;">sym050</p>
2	common anode		
3	cathode 2		
4	cathode 3		
5	cathode 4		

## 3. Ordering information

**Table 3: Ordering information**

Type number	Package		
	Name	Description	Version
PESD3V3V4UW	-	plastic surface mounted package; 5 leads	SOT665
PESD5V0V4UW			

## 4. Marking

**Table 4: Marking codes**

Type number	Marking code
PESD3V3V4UW	W1
PESD5V0V4UW	W2

## 5. Limiting values

**Table 5: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$P_{PP}$	peak pulse power	8/20 $\mu$ s	<a href="#">[1]</a> <a href="#">[2]</a>		
	PESD3V3V4UW		-	16	W
	PESD5V0V4UW		-	16	W
$I_{PP}$	peak pulse current	8/20 $\mu$ s	<a href="#">[1]</a> <a href="#">[2]</a>		
	PESD3V3V4UW		-	1.5	A
	PESD5V0V4UW		-	1.5	A

**Table 5: Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-65	+150	°C
$T_{stg}$	storage temperature		-65	+150	°C

[1] Non-repetitive current pulse 8/20  $\mu$ s exponential decay waveform according to IEC 61000-4-5; see [Figure 1](#).

[2] Measured from pin 1, 3, 4 or 5 to 2.

**Table 6: ESD maximum ratings**

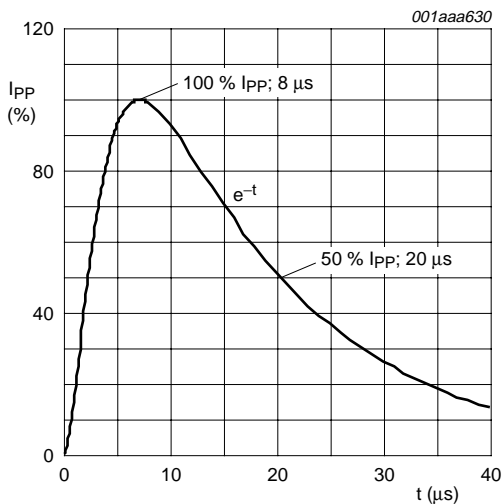
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1] [2]		
	PESD3V3V4UW		-	12	kV
	PESD5V0V4UW		-	12	kV
	PESDxV4UW series	HBM MIL-STD 883	-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses; see [Figure 2](#).

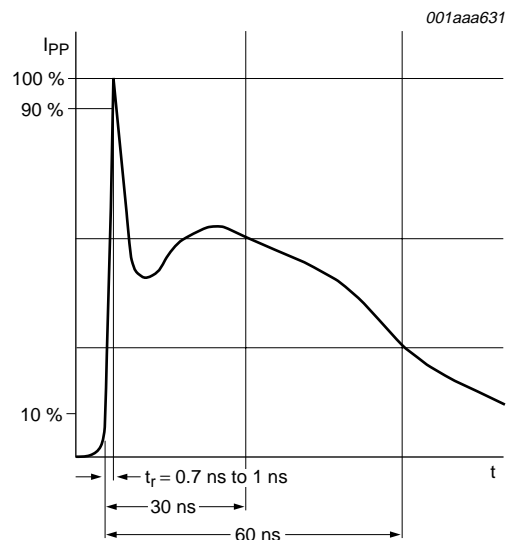
[2] Measured from pin 1, 3, 4 or 5 to 2.

**Table 7: ESD standards compliance**

Standard	Conditions
IEC 61000-4-2; level 4 (ESD); see <a href="#">Figure 2</a>	> 8 kV (contact)
HBM MIL-STD 883; class 3	> 4 kV



**Fig 1. 8/20  $\mu$ s pulse waveform according to IEC 61000-4-5**



**Fig 2. ESD pulse waveform according to IEC 61000-4-2**

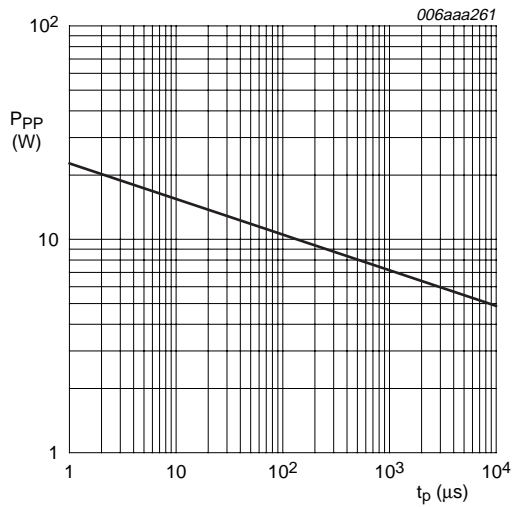
## 6. Characteristics

**Table 8: Characteristics**
 $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per diode</b>						
$V_{RWM}$	reverse stand-off voltage					
	PESD3V3V4UW		-	-	3.3	V
	PESD5V0V4UW		-	-	5.0	V
$I_{RM}$	reverse leakage current	see <a href="#">Figure 6</a> ;				
	PESD3V3V4UW	$V_{RWM} = 3.3\text{ V}$	-	40	300	nA
	PESD5V0V4UW	$V_{RWM} = 5.0\text{ V}$	-	3	25	nA
$V_{BR}$	breakdown voltage	$I_R = 1\text{ mA}$				
	PESD3V3V4UW		5.3	5.6	5.9	V
	PESD5V0V4UW		6.4	6.8	7.2	V
$C_d$	diode capacitance	$f = 1\text{ MHz}$ ; see <a href="#">Figure 5</a> ;				
	PESD3V3V4UW	$V_R = 0\text{ V}$	-	15	18	pF
		$V_R = 3.3\text{ V}$	-	9	12	pF
	PESD5V0V4UW	$V_R = 0\text{ V}$	-	12	15	pF
		$V_R = 5\text{ V}$	-	6	9	pF
$V_{CL}$	clamping voltage		<a href="#">[1]</a> <a href="#">[2]</a>			
	PESD3V3V4UW	$I_{PP} = 1\text{ A}$	-	-	9	V
		$I_{PP} = 2\text{ A}$	-	-	11	V
	PESD5V0V4UW	$I_{PP} = 1\text{ A}$	-	-	11	V
		$I_{PP} = 1.7\text{ A}$	-	-	13	V
$r_{dif}$	differential resistance	$I_R = 1\text{ mA}$				
	PESD3V3V4UW		-	-	200	$\Omega$
	PESD5V0V4UW		-	-	100	$\Omega$

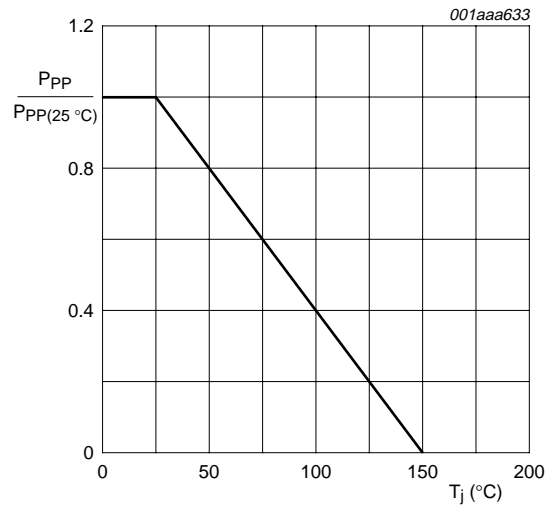
[1] Non-repetitive current pulse 8/20  $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5; see [Figure 1](#).

[2] Measured from pin 1, 3, 4 or 5 to 2.



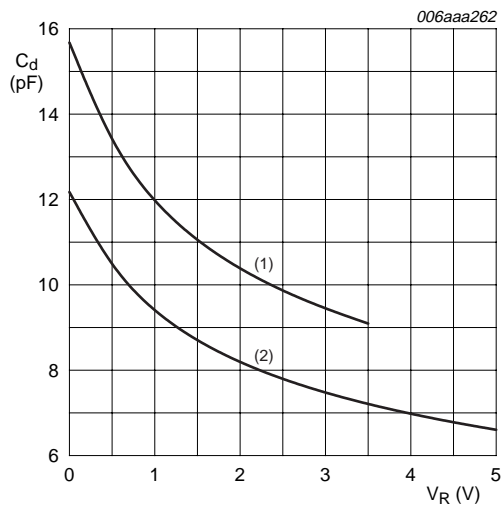
$T_{amb} = 25\text{ °C}$

**Fig 3. Peak pulse power dissipation as a function of exponential pulse duration  $t_p$ ; typical values**



$T_{amb} = 25\text{ °C}$

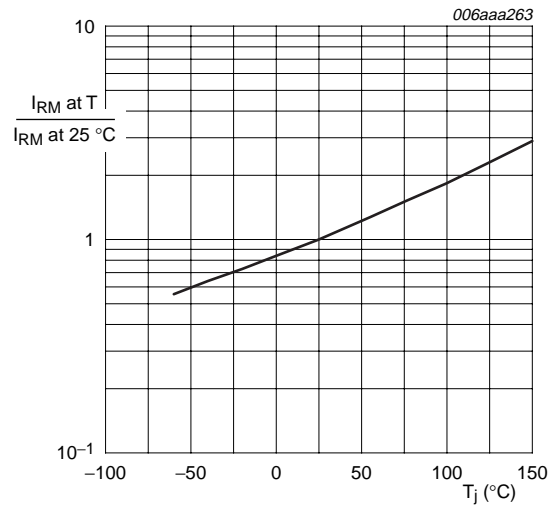
**Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values**



$f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$

- (1) PESD3V3V4UW
- (2) PESD5V0V4UW

**Fig 5. Diode capacitance as a function of reverse voltage; typical values**



PESD3V3V4UW  
PESD5V0V4UW

**Fig 6. Relative variation of reverse leakage current as a function of junction temperature; typical values**

## 7. Application information

The PESDxV4UW series is designed for protection of up to four unidirectional data lines from the damage caused by ESD and surge pulses. The PESDxV4UW series may be used on lines where the signal polarities are above or below ground. The PESDxV4UW series provides a surge capability of 16 W per line for an 8/20  $\mu$ s waveform.

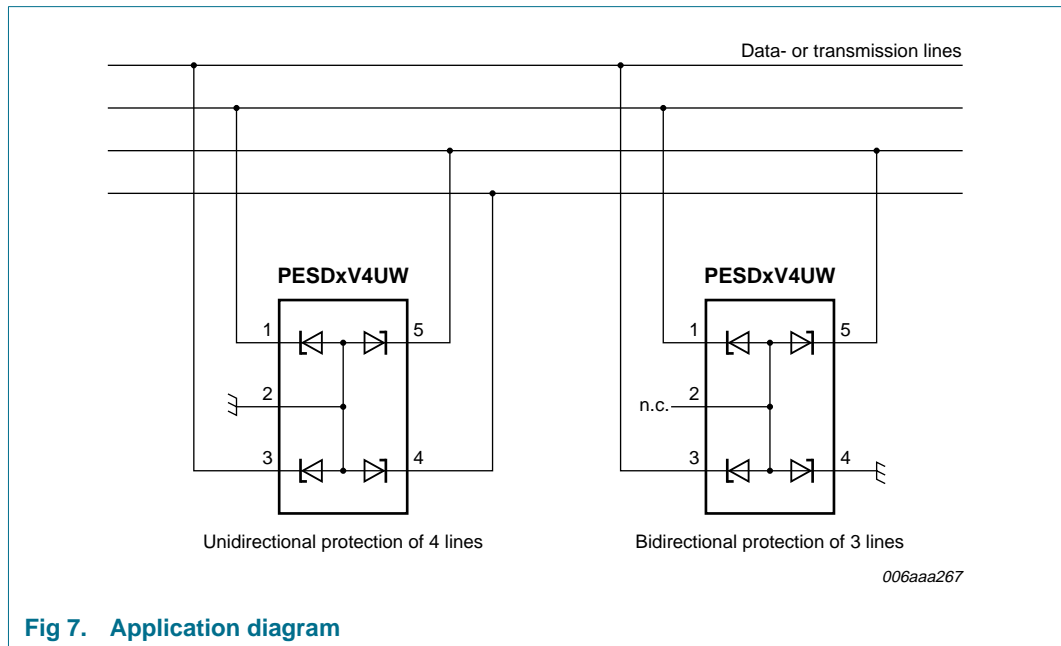


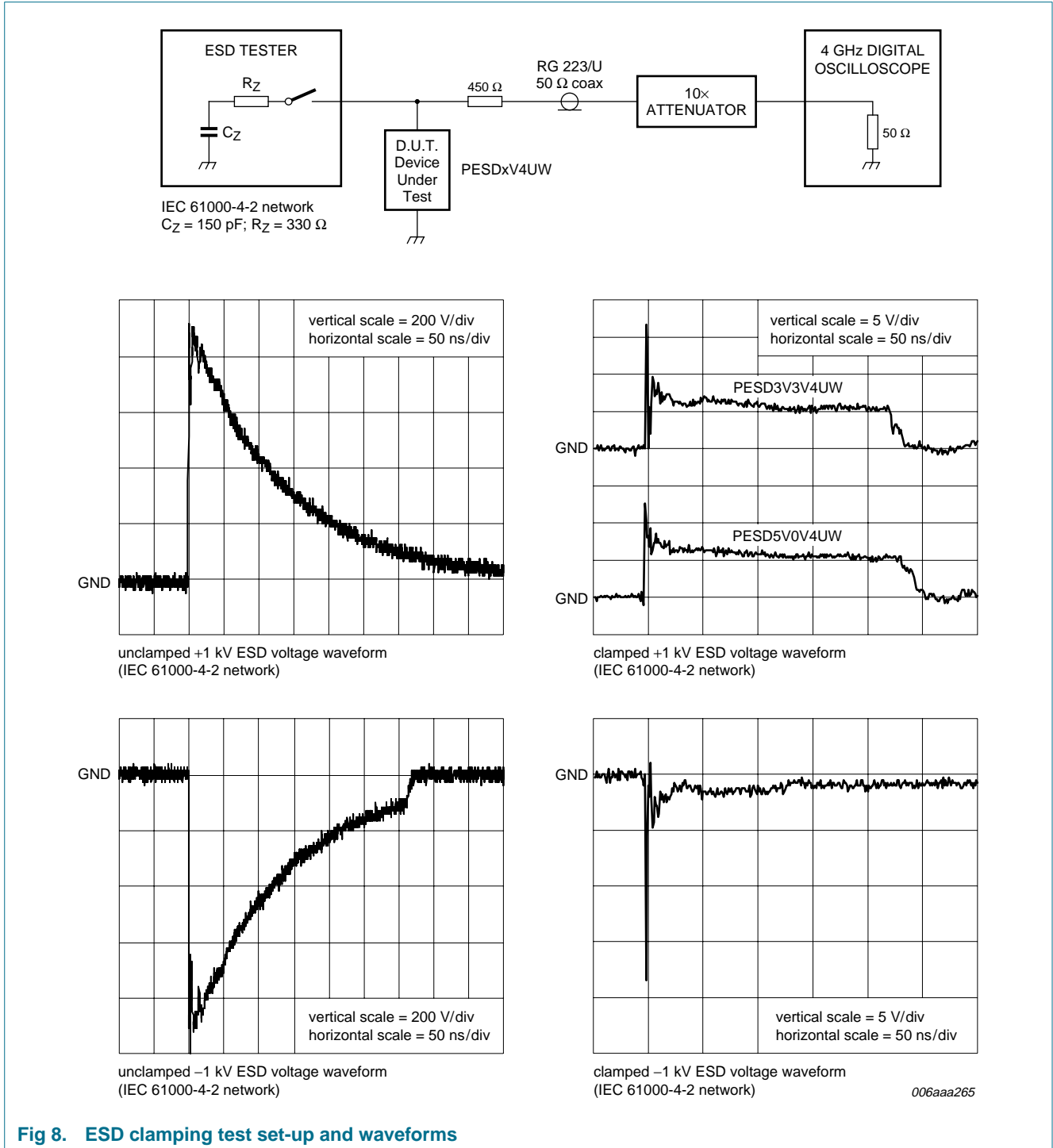
Fig 7. Application diagram

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

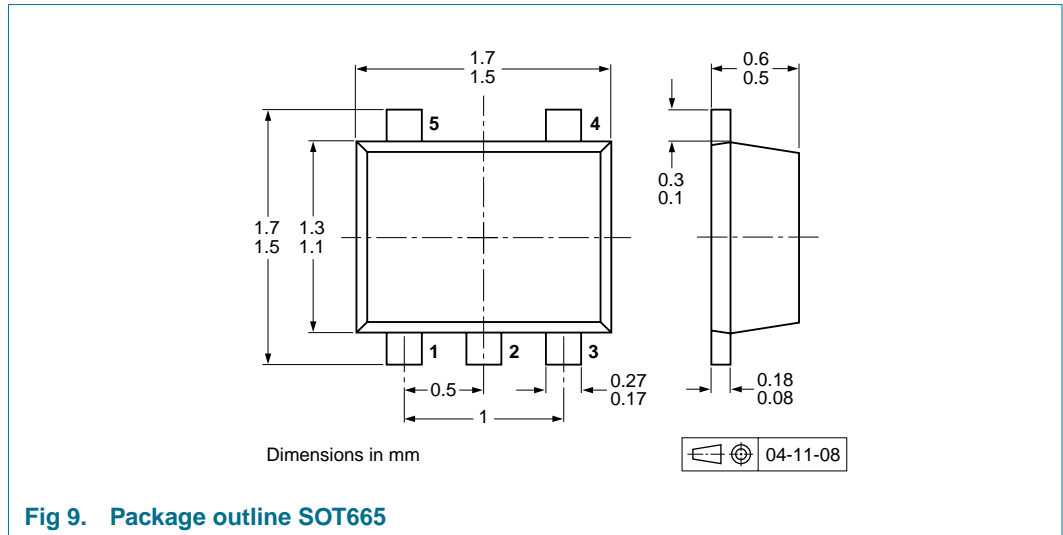
1. Place the PESDxV4UW as close to the input terminal or connector as possible.
2. The path length between the PESDxV4UW and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all printed-circuit board conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer printed-circuit boards, use ground vias.

**8. Test information**



**Fig 8. ESD clamping test set-up and waveforms**

## 9. Package outline



## 10. Packing information

**Table 9: Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	Description	Packing quantity
			4000
PESD3V3V4UW	SOT665	4 mm pitch, 8 mm tape and reel	-115
PESD5V0V4UW			

[1] For further information and the availability of packing methods, see [Section 15](#).



## 11. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PESDXV4UW_SER_1	20050422	Product data sheet	-	9397 750 14481	-

## 12. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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