

# HAT1043M

Silicon P Channel Power MOS FET  
Power Switching

# HITACHI

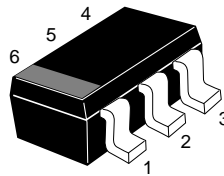
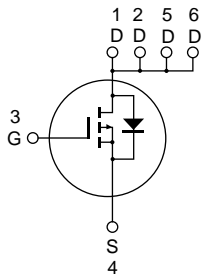
ADE-208-754D (Z)  
5th Edition  
February 1999

## Features

- Low on-resistance
- Low drive current
- High density mounting
- 2.5 V gate drive device can be driven from 3 V source

## Outline

TSOP-6



4 Source  
3 Gate  
1, 2, 5, 6 Drain

## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-20	V
Gate to source voltage	$V_{GSS}$	±12	V
Drain current	$I_D$	-4.4	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	-17.6	A
Body-drain diode reverse drain current	$I_{DR}$ <sup>Note 2</sup>	-4.4	A
Channel dissipation	$Pch_{(pulse)}$ <sup>Note 2</sup>	2.0	W
	$Pch_{(continuous)}$ <sup>Note 3</sup>	1.05	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

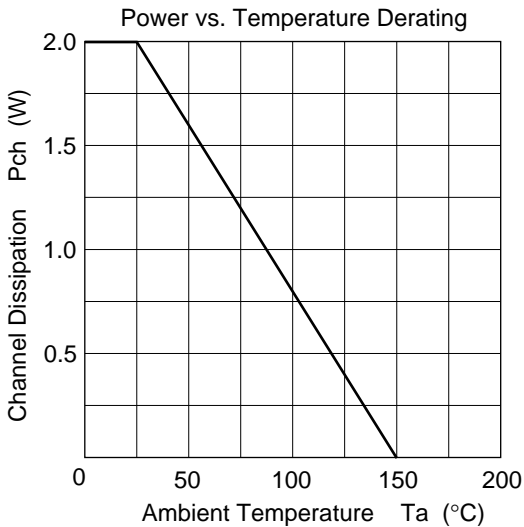
- Note: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$   
 2. When using the alumina ceramic board (50 x 50 x 0.7 mm),  $PW \leq 5 s$ ,  $T_a = 25^\circ C$   
 3. When using the alumina ceramic board (50 x 50 x 0.7 mm),  $T_a = 25^\circ C$

## Electrical Characteristics (Ta = 25°C)

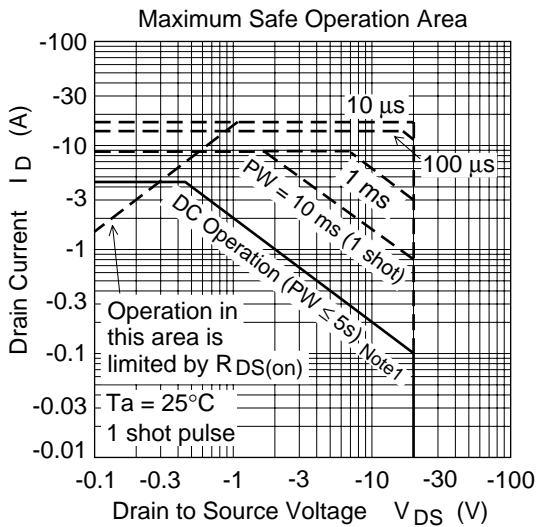
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±0.1	μA	$V_{GS} = \pm 12 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	μA	$V_{DS} = -20 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$I_D = -1 \text{ mA}$ , $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	55	65	mΩ	$I_D = -3 \text{ A}$ , $V_{GS} = -4.5 \text{ V}$ <sup>Note 1</sup>
		—	85	110	mΩ	$I_D = -3 \text{ A}$ , $V_{GS} = -2.5 \text{ V}$ <sup>Note 1</sup>
Forward transfer admittance	$ y_{fs} $	4	7	—	S	$I_D = -3 \text{ A}$ , $V_{DS} = -10 \text{ V}$ <sup>Note 1</sup>
Input capacitance	$C_{iss}$	—	750	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	$C_{oss}$	—	310	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	220	—	pF	$f = 1 \text{ MHz}$
Total Gate charge	$Q_g$	—	11	—	nc	$V_{DD} = -10 \text{ V}$
Gate to Source charge	$Q_{gs}$	—	2	—	nc	$V_{GS} = -4.5 \text{ V}$
Gate to Drain charge	$Q_{gd}$	—	3.5	—	nc	$I_D = -4.4 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = -4.5 \text{ V}$ , $I_D = -3 \text{ A}$
Rise time	$t_r$	—	100	—	ns	$R_L = 3.3 \Omega$
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	$t_f$	—	100	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-0.95	-1.23	V	$I_F = -4.4 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	50	—	ns	$I_F = -4.4 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = -20 \text{ A}/\mu s$

- Note: 1. Pulse test

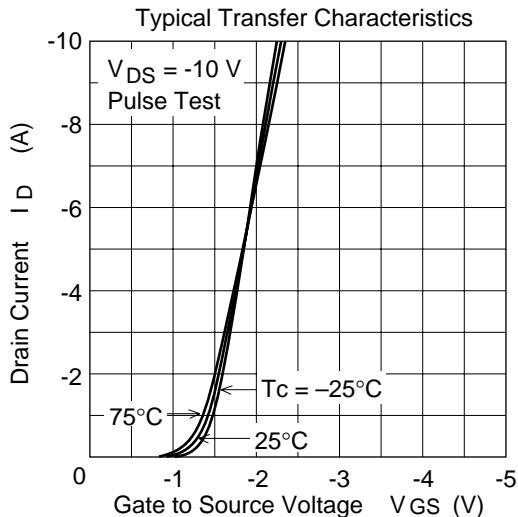
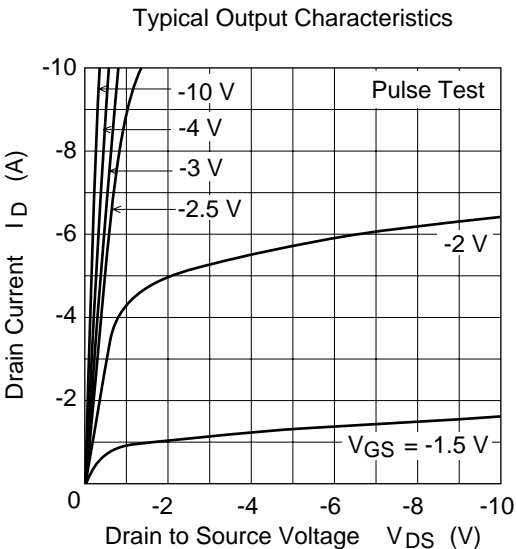
Main Characteristics



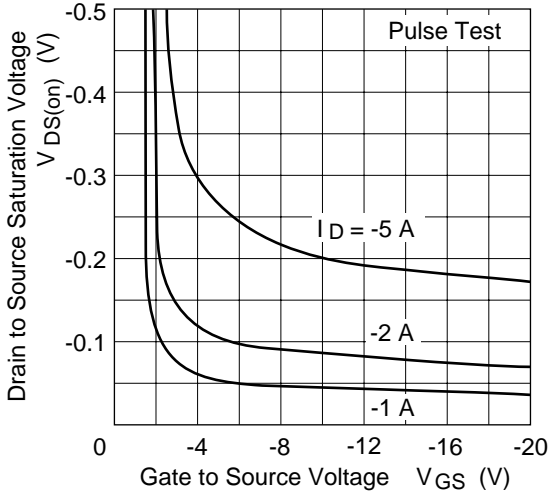
Test Condition  
When using the alumina ceramic board  
(50x50x0.7mm), (PW ≤ 5s)



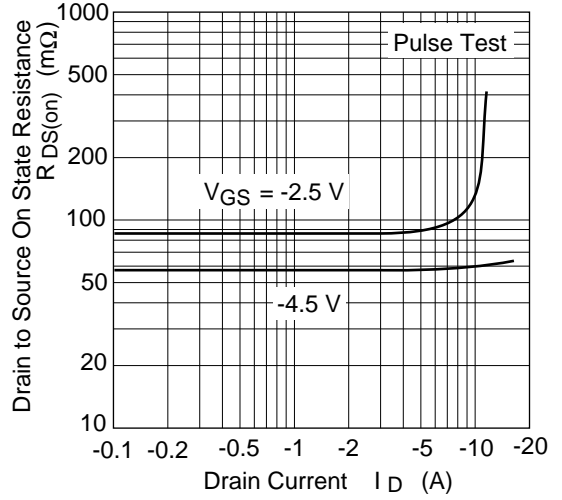
Note 1 When using the alumina ceramic board  
(50x50x0.7mm)



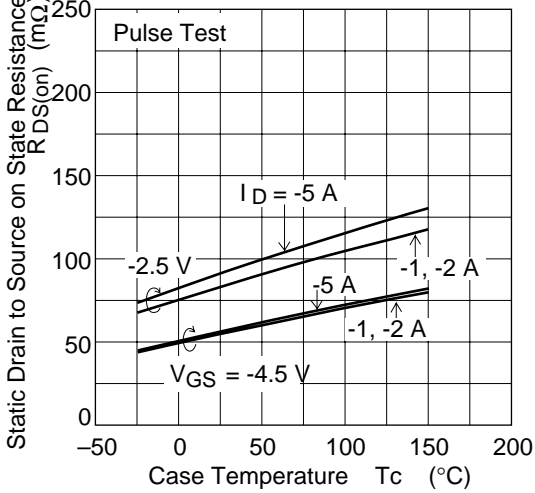
Drain to Source Saturation Voltage vs. Gate to Source Voltage



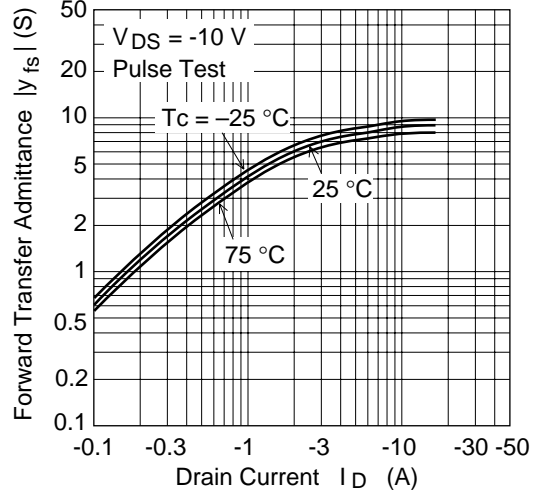
Static Drain to Source on State Resistance vs. Drain Current

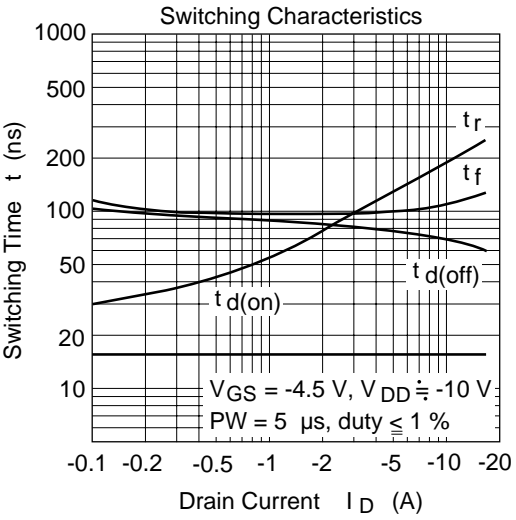
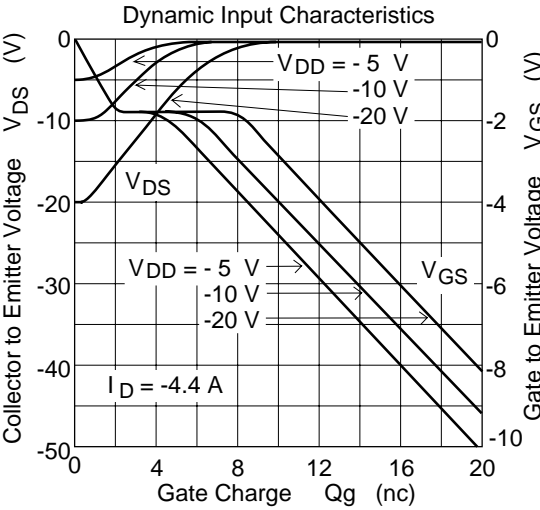
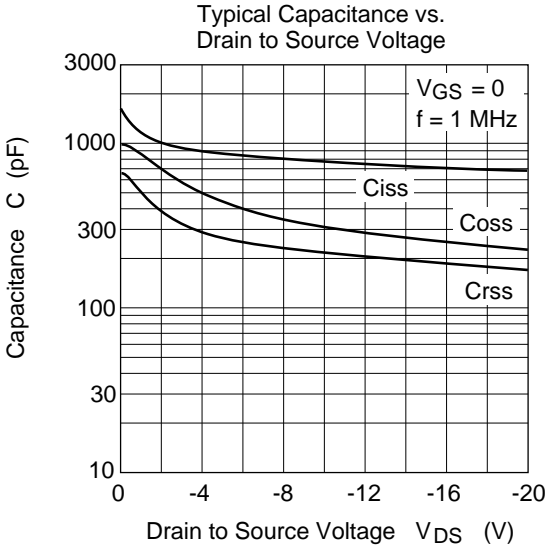
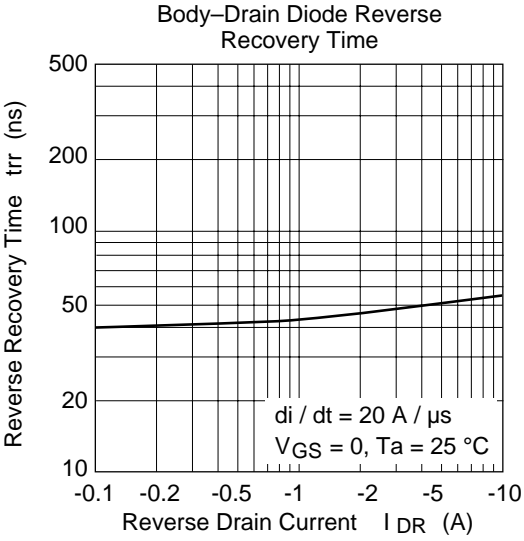


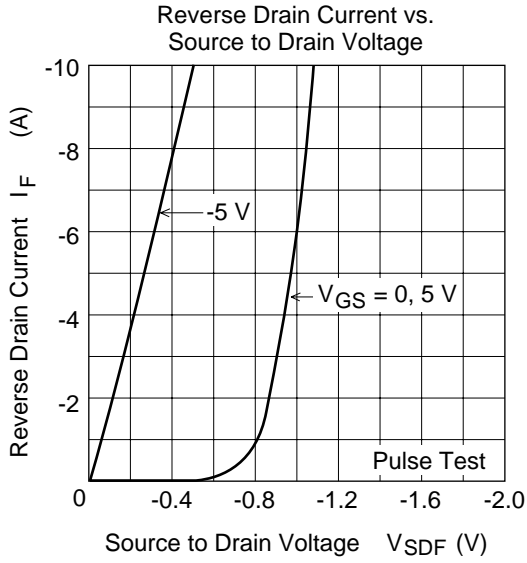
Static Drain to Source on State Resistance vs. Temperature



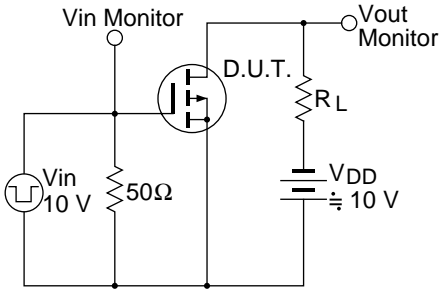
Forward Transfer Admittance vs. Drain Current



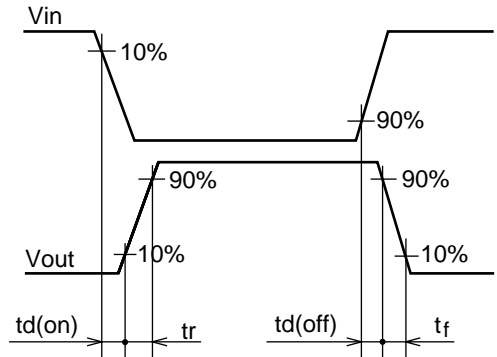




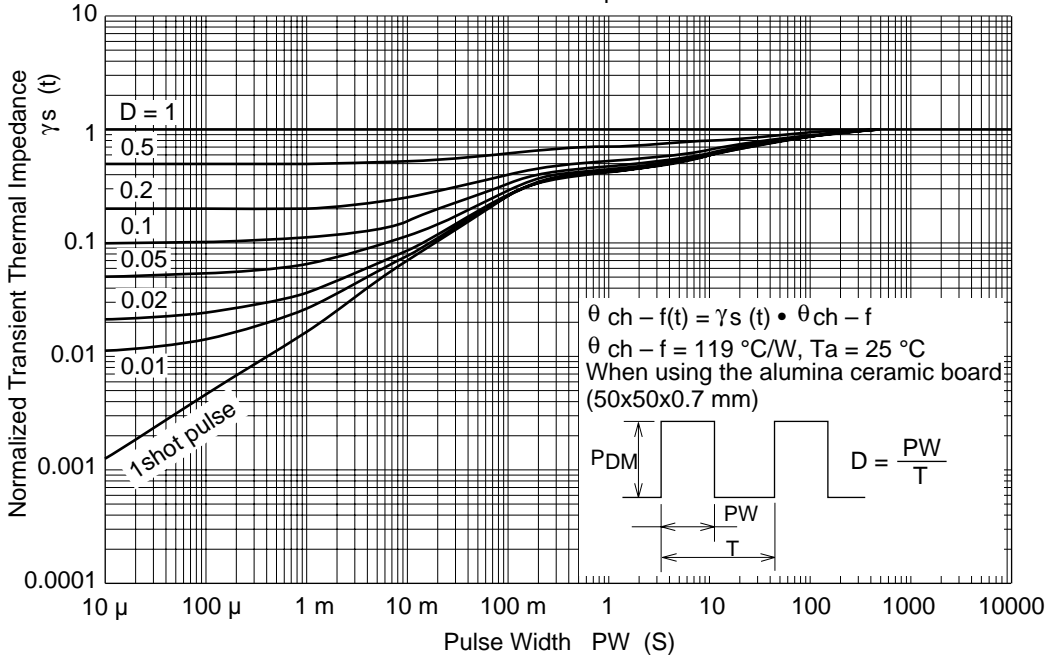
Switching Time Test Circuit



Switching Time Waveform

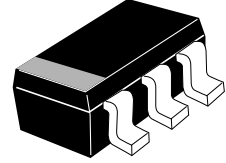
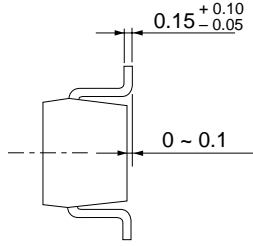
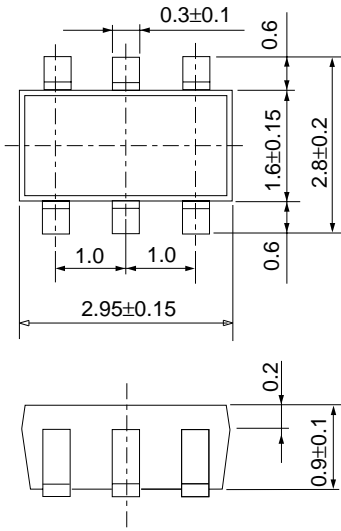


Normalized Transient Thermal Impedance vs. Pulse Width



## Package Dimensions

Unit: mm



Hitachi Code	TSOP-6
EIAJ	-
JEDEC	-



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