Receiver for Point-to-Point Multiplex Systems

Description

Local, low speed multiplex systems reduce the amount of wires and connectors, save costs and weight and increase the safety in automotive and industrial applications. The U6057B is an ideal receiver for an 8-bit data word with simple protocol of a fixed length. It checks the correct data transmission and provides the data word in an 8-bit shift register for a microcontroller.

Features

- Only a single data line is necessary
- Quadruple comparison of the data signal for high transmission safety
- Minimum of peripherals
- Master/slave operation
- Wide supply-voltage range
- According to VDE 0839
- Load-dump protected

Ordering Information

Extended Type Number	Package	Remarks
U6057B–FL	SO20	

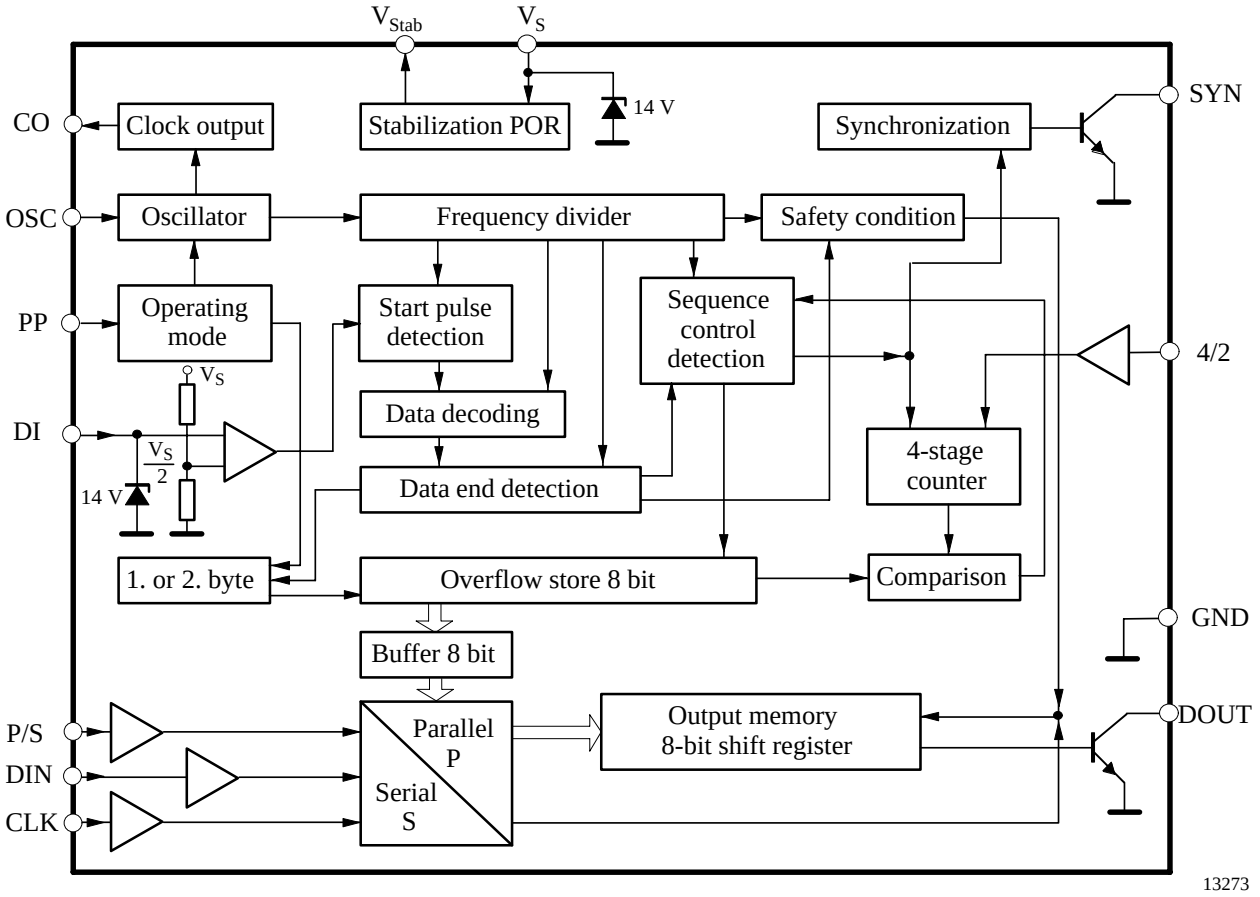


Figure 1. Block diagram

Pin Configuration

Table 1. Pin description

Pin	Symbol	Function
1	GND	Ground
2	DIN	Serial data input
3	nc	
4	P/S	Parallel/serial switch-over
5	CLK	Clock input for shift register
6	nc	
7	DOUT	Serial data output for the µC
8	nc	
9	2/4	2/4-fold comparison
10	SYN	Synchronization
11	CO	Clock output for cascading
12	PP	Program pin
13	DT	Data input of data line
14	nc	
15	nc	
16	nc	
17	nc	
18	OCS	RC-oscillator input
19	V_{stab}	Stabilized voltage
20	V_S	Supply voltage

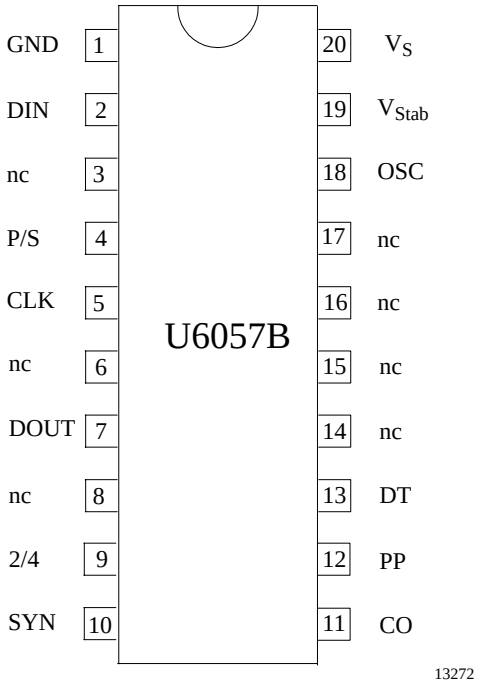


Figure 2. Pinning of U6057B

Functional Description

Power Supply

For protection against interference and surges, the U6057B must be equipped with an RC-circuit for current limitation in the event of overvoltages and for buffering in the event of voltage dips at V_S.

Suggested dimensions: Rv = 510 Ω, C_V = 100 µF (see figure 3)

An integrated 14-V Z-diode is located between V_S and GND.

Oscillator

All timing in the circuit is derived from an RC-oscillator. The oscillator's charging time t_1 is determined by an external resistor, R_{OSC}, and its discharge time t_2 by an integrated 2-kΩ resistor. Since the tolerance and temperature sensitivity of the integrated resistor are considerable greater than those of the external resistor, $t_1/t_2 \geq 20$ must be selected for stability reasons. The minimum value of R_{OSC} should not be less than 68 kΩ.

Recommended frequencies and dimensioning:

$f_{OSC} = 1 / C_{OSC} (0.79 \times R_{OSC} + 2260\ \Omega)$

f_{OSC} = 25.6 kHz, C_{OSC} = 220 pF, R_{OSC} = 200 kΩ

Table 2. Times derived from the transmitted frequency (6.4 kHz)

Description	Time
Start pulse	312 µs
One bit	156 µs
Information bit	156 µs
Zero bit	156 µs
Information unit	625 µs
Data word	5 ms + 312 µs start bit
Data pause	9.688 ms
Transmission cycle	15 ms
Minimum reaction time	60 ms
Data word master – slave	10 ms + 312 µs start bit
Data pause master – slave	4.688 ms

Supply Voltage 5 V

The receivers can be supplied from one stabilized, noise-free voltage source. In this case, the series resistor and the filter capacitor are not required. Pin V_{Stab} is also supplied by the 5-V supply (see figure 4).

Structure of the Data Word

A switch information unit consists of four parts:

1. One bit for receiver synchronization

2. Information bit with "High" = switch open
   "Low" = switch closed

3. Zero bit

4. Zero bit

The data word consists of two start bits and eight information units. For a transmitter frequency of 6.4 kHz, the data word length is 5 ms plus the start pulse followed by a 10-ms-long data interval. The data interval has high potential. When the supply voltage is applied, data transmission is constantly repeated in accordance with this pattern.

Data Decoding

If a negative edge appears at the data input, the receiver checks whether a start pulse or a fault is present by measuring the duration of the pulse (a minimum time must be observed). If there is a fault, the receiver waits for the next negative edge.

If it recognizes a start pulse, it checks whether an information unit with 8 bits is following and stores this in an 8-bit overflow store. The arriving data are ignored if there is no 8-bit string owing to a fault or a synchronism. The receiver is synchronized by each one bit. Scanning of the information takes place in the middle of the information bit. In order to make scanning sufficiently precise, the oscillator frequency of the receiver was selected to be four times as large as that of the transmitter. The deviation of the receiver frequency to the four-fold transmitter frequency may be up to $\pm 15\%$ while still guaranteeing reliable data cognition.

Data Check

The data read into the 8-bit overflow store is compared with the content of the buffer. If this is identical, a 4-stage counter is incremented by one stage. If this is not identical, the counter is reset. The new data combination is transferred to the buffer after each comparison irrespective of the result.

After double or quadruple coincidence has been established, the content of the buffer is always transferred to the output memory.

Since the period of data transmission is 15 ms this results in a minimum delay time of 60 ms or 30 ms for detection of a change of the data word. Faults on the data line and switch bouncing may lead to an extension of the delay time.

Precondition to transfer the data word into the output memory: Input P/S must be in high potential.

Synchronization

Proper data transfer requires a synchronization between the internal data processing and the microcontroller's read-out frequency.
The U6057B provides a synchronization pulse (Pin SYN) of $t = 16 \times 1/f_{OSC}$ which triggers the microcontroller to read-out data in the following time window of typically 2×15 ms or 4×15 ms. The synchronization is derived from the positive edge of the internal transfer pulse. This pulse causes the data transfer to the output shift register after double/quadruple data word comparison.

The microcontroller reads the output shift register after each synchronization pulse. In practise, the time delay for data recognition varies depending on the event of data signal change on the data line and the status of the internal 4-stage (or 2-stage) counter. This counter is 0 after each synchronization pulse. With a programmed quadruple comparison the data recognition time ranges from 4×15 ms to 7×15 ms whereas it may range from 2×15 ms to 3×15 ms in the case of the programmed double comparison.

If the system is operated with multiple change of the data-word during the comparison time (4×15 ms or 2×15 ms), the data recognition time may last longer than mentioned above.

Note: In master – slave operation, each IC produces its own synchronization pulse.

Cascading (Master – Slave Operation)

Determination of master or slave is defined by the connecting of the Pin PP:

Master/ alone:	PP open or PP to V_S
Slave:	PP to GND

In master mode, the oscillator is connected with R_{OSC} and $C_{OSC,}$ and the clock output is active. In slave mode, the oscillator is blocked and must be activated by the clock output of the master. The master recognizes the start-bit and decodes the first eight information bits. The slave also

recognizes the start-bit but decodes the second eight information bits.

There are several possibilities of cascading

- CLK and DOUT are always connected in parallel. Each shift register can be read-out individually by a separate P/S line (see figure 5).
- CLK and P/S are always connected in parallel. $DOUT_{MASTER}$ and $DOUT_{SLAVE}$ are connected with each other. The 16-bit data word can be read-out serially via $DOUT_{SLAVE}$ in one operation (see figure 6)
- Combinations with U6052B and U6057B (see figure 7)

Loading and Reading-out the Shift Register

Loading and reading-out of data from the shift register is controlled by the three inputs DIN, CLK and P/S.

Input P/S = high parallel operation
No data can be read-out from the shift register. Data which arrive via the data line are stored in the shift register. Output DOUT is disabled (high resistance).

Input P/S = low serial operation
The information available at DIN is transferred to the shift register by the positive edge of CLK and advanced by one position by each further positive edge. The data word appears at DOUT.

The maximum clock frequency is 40 kHz.

The eighth flip-flop is a master – slave flip-flop. The information of the eighth flip-flop is transferred to the slave with each negative edge from CLK and is available at the output DOUT.

DIN, CLK and EN are high-resistance inputs and process a switching threshold of approximate 1.8 V. DOUT is an open-collector output.

Input 4/2

The number of comparisons can be defined by the wiring configuration of input 4/2.

4-fold comparison: Input 4/2 open
2-fold comparison: Input 4/2 connected to V_S

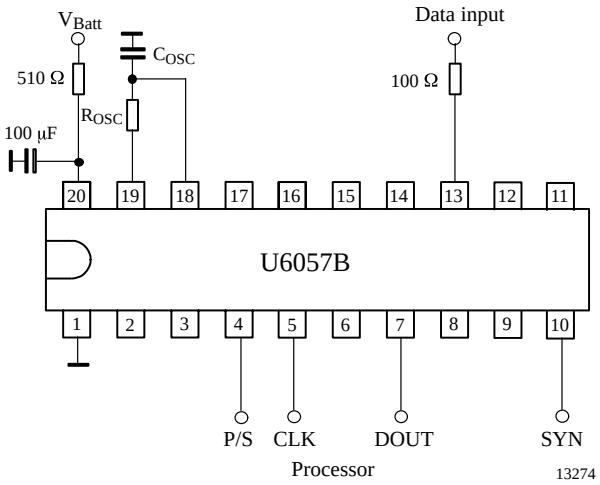


Figure 3. Supplied with battery voltage

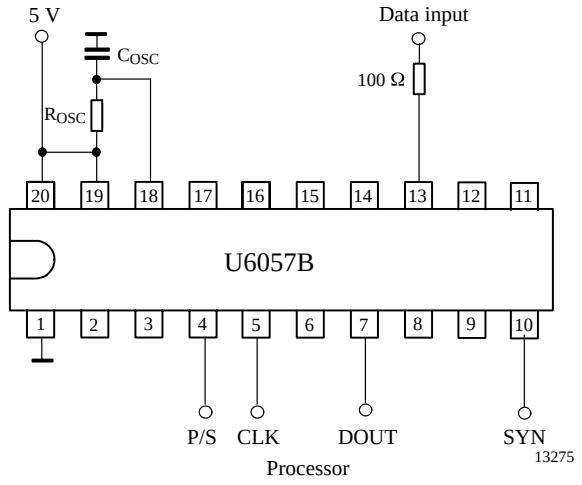


Figure 4. Supplied with a stabilized 5-V voltage

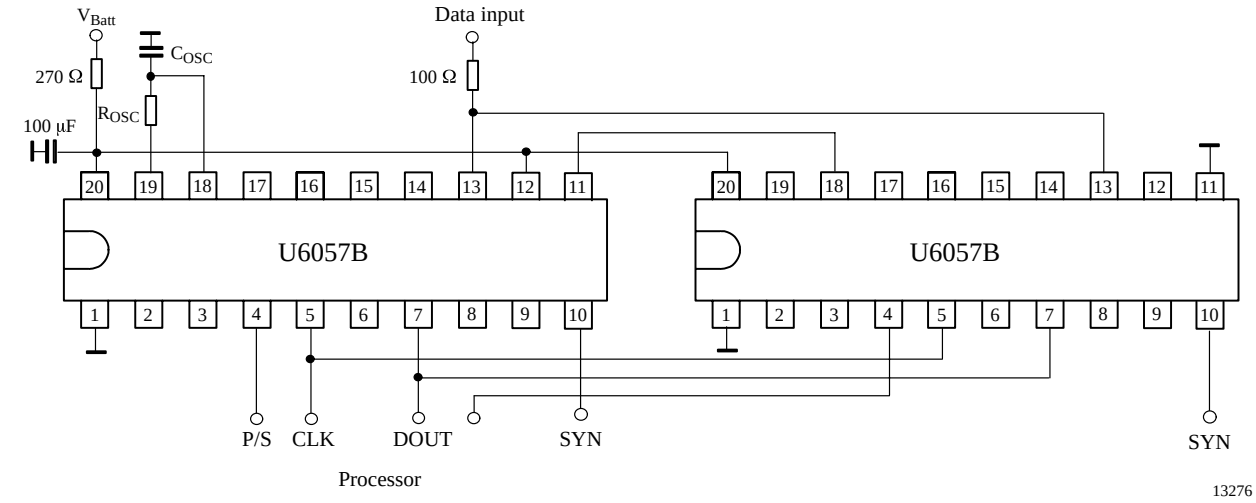


Figure 5. Master – slave operation, read-out: 2 × 8 bit, supplied with 12-V battery

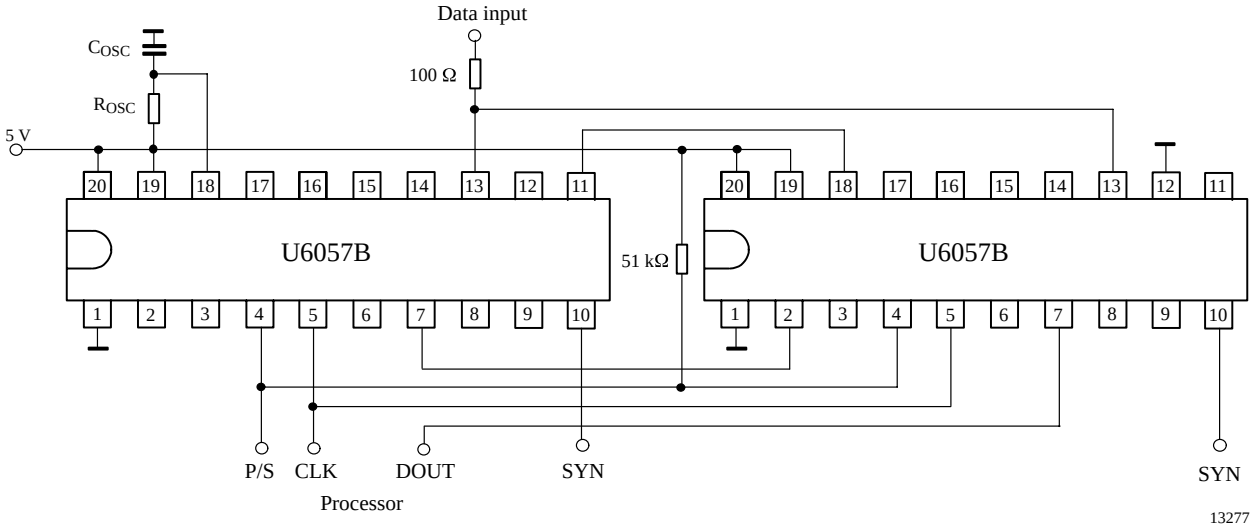


Figure 6. Master – slave operation, read-out: 1 × 16 bit, supplied with stabilized 5 V

Absolute Maximum Ratings

Receiver with recommended circuitry

Parameters	Symbol	Value	Unit
Supply voltage (static)	V_S	25	V
Power dissipation T_{amb} = 85°C	P_{tot}	920	mW
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	–55 to +125	°C
Ambient temperature range	T_{amb}	–40 to +85	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SO20	R_{thJA}	90	K/W

Electrical Characteristics

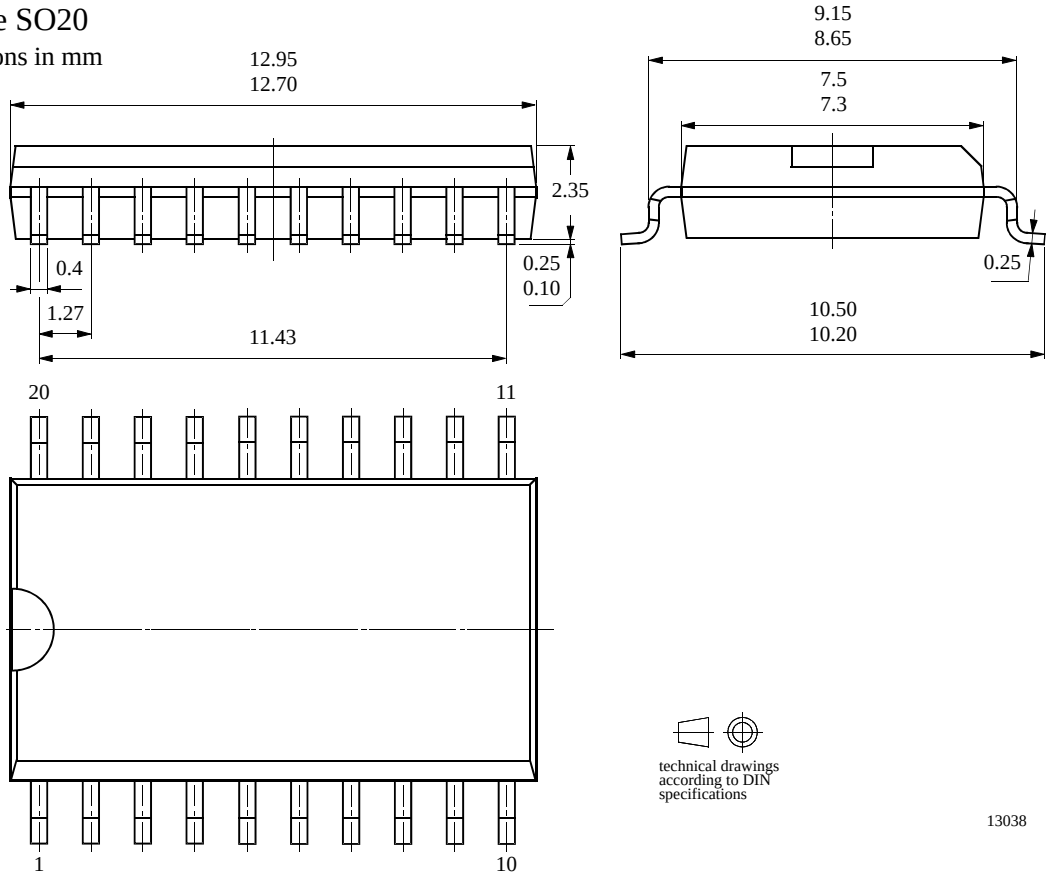
V_{Batt} = 13.5 V, T_{amb} = 25°C, reference point = GND
Receiver with recommended circuitry

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{Batt}	6		16	V
5-V supply (without R_V and C_V)		V_S	4.75		5.0	V
Stabilized voltage		V_{Stab}		5.2		V
Supply current		I_S		1.5	3.0	mA
Internal clamping		V_Z		14.3		V
POR threshold		V_{POR}	2.5	3.4	4.0	V
Protection resistor		R_V	510			Ω
Protection capacitor		C_V		100		µF
Input data DIN						
Threshold voltage		$V_{DIN–TH}$	1.6	1.8	2.3	V
Input current	V_{DIN} = 0 V	$–I_{DIN–IN}$			2.0	µA
Internal pull-down resistor		$R_{DIN–IN}$		100		kΩ
Input clock CLK						
Threshold voltage		$V_{CLK–TH}$	1.6	1.8	2.3	V
Input current	V_{CLK} = 0 V	$–I_{CLK–IN}$			2.0	µA
Internal pull-down resistor		$R_{CLK–IN}$		100		kΩ
Clock frequency		f_{CLK}	1.0	24.8	40	kHz
Delay time CLK – DOUT		t_{DEL}		10		µs
Clock pulse length		t_{CPL}	12			µs
Waiting time P/S – CLK		t_{WT}	1			µs
Input parallel/serial P/S						
Threshold voltage		$V_{P/S–TH}$	1.6	1.8	2.3	V
Input current	$V_{P/S}$ = 0 V	$–I_{P/S–IN}$			2.0	µA
Internal pull-down resistor		$R_{P/S–IN}$		100		kΩ
Input data 2/4						
Threshold voltage		$V_{2/4–TH}$	1.6	1.8	2.3	V
Input current	$V_{2/4}$ = 0 V	$–I_{2/4–IN}$			2.0	µA
Internal pull-down resistor		$R_{2/4–IN}$		100		kΩ

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Serial data output DOUT (open collector)						
Saturation voltage	1 mA	V_{DOUT}			0.2	V
Current capability		I_{DOUT}			1.0	mA
Leakage current		I_{LDOUT}			5.0	µA
Rise time	R_{DOUT} = 51 kΩ to V_{stab}	t_{rOUT}		2		µs
Fall time	R_{DOUT} = 51 kΩ to V_{stab}	t_{fOUT}		200		ns
Oscillator input OSC						
Internal discharge resistor		R_{DIS}	1.6	2.0	2.4	kΩ
Lower threshold	$V_{stab} \times 0.214$	$V_{OSC-THL}$		1.1		V
Upper threshold	$V_{stab} \times 0.615$	$V_{OSC-THH}$		3.3		V
Input current	V_{OSC} = 0 V	$-I_{OSC}$			1.0	µA
Frequency		f_{OSC}	1.0	24.8	40.0	kHz
Data input DI						
Threshold voltage		V_{DI}		$V_S \times 0.5$		V
Input current		$-I_{DI}$			1.0	µA
Internal pull-down resistor		R_{DI}		100		kΩ
Internal clamping		V_{ZDI}		14.3		V
External protection		R_{DI-EXT}	0.1		70	kΩ
Program Pin PP						
Lower threshold		V_{PPtl}		$V_S \times 0.24$		V
Upper threshold		V_{PPth}		$V_S \times 0.50$		V
Pin PP open		V_{PPO}		$V_S \times 0.37$		V
Input current	V_{PP} = 0 V V_{PP} = V_S	$-I_{PP}$ I_{PP}		50 50		µA µA
Clock output CO						
Output current	V_{CO} = 0 V	$-I_{CO}$	110		300	µA
Output open		$V_{CO-open}$		$V_{stab} \times 0.8$		V
Output current	VCO = 1 V	I_{CO}			1.0	mA
Saturation voltage low	VCO = 1 V	V_{CO}			1.2	V
Internal pull-down resistor		R_{CO}		200		kΩ
Synchronization output SYN (open collector)						
Saturation voltage	1 mA	V_{SYN}			0.2	V
Current capability		I_{SYN}			1.0	mA
Leakage current		I_{LSYN}			5.0	µA
Rise time	R_{SYN} = 51 kΩ to V_{stab}	t_{rSYN}		2		µs
Fall time	R_{SYN} = 51 kΩ to V_{stab}	t_{fSYN}		200		ns

Package Information

Package SO20
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423