ICs for Communications

ATM Buffer Manager
ABM

PXB 4330 Version 1.1

Data Sheet 09.99

DS 1

PXB 4330 Data Sheet		
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Preface

The ATM Buffer Manager (ABM) is part of Infineon's ATM Layer chipset consisting of four devices that provide a complete solution of ATM Layer functionality on ATM Line Cards for Enterprise- and Central Office Switches, DSLAMs and Access Multiplexers. The chipset has a featureset for processing ATM Layer functionality for STM-4/OC-12 requirements in a very cost effective way. The ABM is a very powerful and feature-rich solution for an effective ATM Traffic Management and includes buffer capacity for up to 128 K cells with a bi-directional throughput of 687 MBit/sec. The device supports CBR, VBR-rt, VBR-nrt, ABR, UBR and UBR+ traffic.

The document provides a complete reference information on functional -, operational -, interface - and register description as well as electrical characteristics and package information. For application specific questions different application notes can be provided upon request.

Organization of this Document

This Data Sheet is divided into 10 chapters and is organized as follows:

- Chapter 1, Overview
  Gives a general description of the product and its family, lists the key features, includes a Logic Symbol, and presents some typical applications.
- Chapter 2, Pin Descriptions
  Provides detailed pin desciptions and a pin out diagram for the PXB 4330.
- Chapter 3, Functional Description
  Provides detailed descriptions of all major functional blocks of the device.
- Chapter 4, Operational Description
  Describes initialization and test, configuration and connection setup, queues and classes, and connection types.
- Chapter 5, Interface Descriptions
  Begins with information about the UTOPIA Interfaces, RAM Interfaces, Microprocessor Interface, and JTAG Test Interface, and concludes with the Clocking concept.
- Chapter 6, Register Descriptions
  Provides both an overview of the ABM Register Set and detailed descriptions of the registers.
- Chapter 7,Electrical Characteristics
  Gives Absolute Maximum Ratings, Operating Ranges, DC and AC Characteristics, Timing information and diagrams for the various interfaces, Capacitances, and Package Characteristics.
- Chapter 8, Package Outlines
  Includes detailed package information.
- Chapter 9, References
  Provides detailed bibliographic information for references cited in the document.

- Chapter 10, Acronyms
  Includes abbreviations frequently used in this document and their meanings.

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Please provide in the subject of your e-mail:
device name (ABM), device number (PXB 4330), device version (Version 1.1),

and in the body of your e-mail:
document type (Data Sheet), issue date (09.99) and document revision number (DS 2).

1 Overview

The PXB 4330 ATM Buffer Manager (ABM) is a member of the Infineon ATM layer chip set. The chip set consists of:

- PXB 4330 E ATM Buffer Manager ABM
- PXB 4340 E ATM OAM Processor AOP
- PXB 4350 E ATM Layer Processor ALP
- PXB 4360 F Content Addressable Memory Element CAME

These chips comprise a complete chip set with which to build an ATM switch. A generic ATM switch consists of a switching fabric and switch ports as shown in **Figure 1-1**.

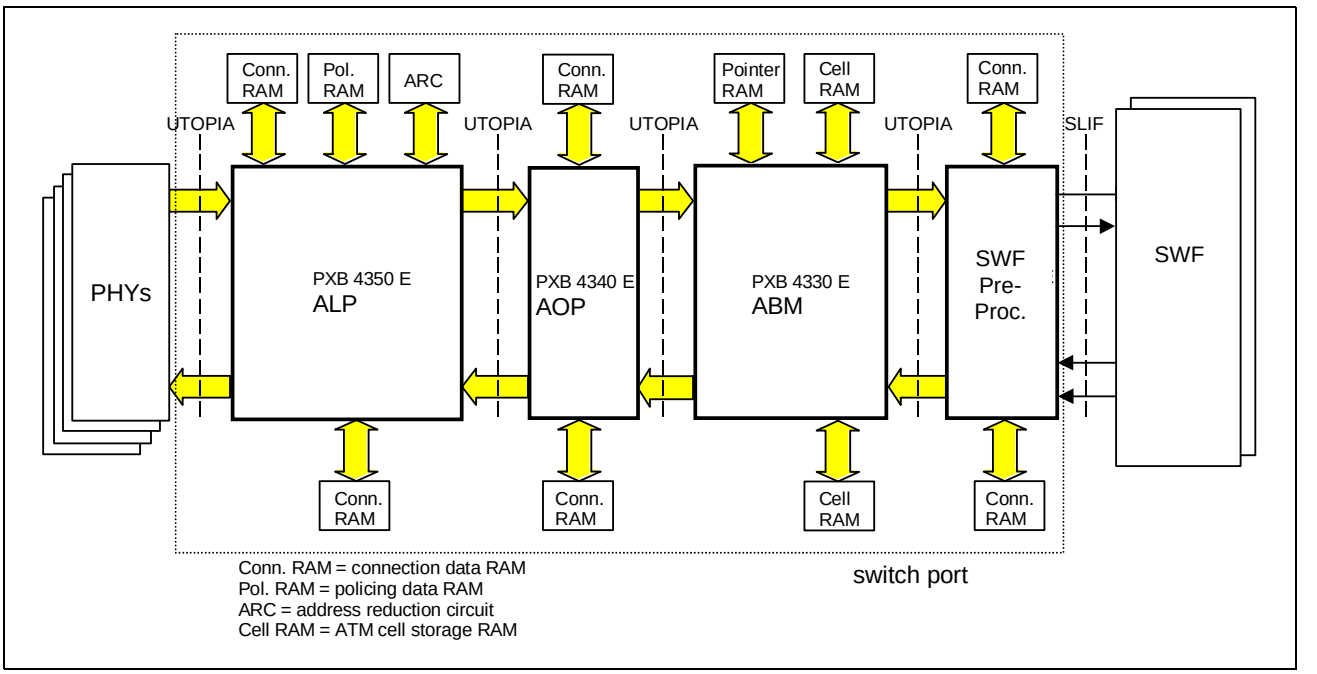
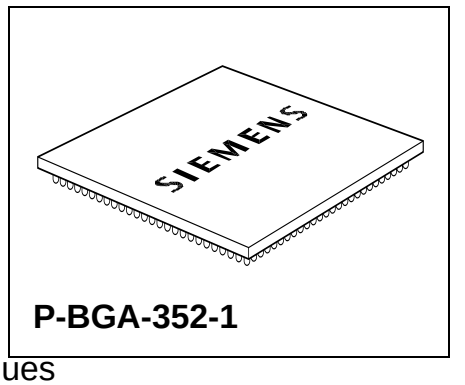


Figure 1-1 ATM Switch Basic Configuration

In the Infineon ATM layer chip set, the traffic management function is performed by the PXB 4330 E ABM. Policing, header translation, and cell counting is performed by the PXB 4350 E ALP; OAM functions by the PXB 4340 E AOP. The PXB 4360 F CAME can be used optionally as an external Address Reduction Circuit (ARC) for the PXB 4350 E ALP.

Version 1.1 **CMOS**

1.1 Features



P-BGA-352-1

Performance

- ATM layer processing up to STM-4/OC-12 equivalent
- Throughput up to 687 Mbit/s, bi-directional
- Uni-directional mode with resources of both directions usable (optional)
- Up to 8192 connections, individually assignable to queues
- Up to 1024 queues per direction, individually assignable to schedulers and to service classes
- FIFO queuing within each queue
- Up to 48 schedulers per direction with programmable service rates, individually assignable to PHYs (up to 96 schedulers per direction by cascading two ABM chips, see Application Note [7])
- Up to 16 traffic classes with individually selectable thresholds for service classes
- Up to 24 PHYs

Queuing Functions

- Common high-priority real-time bypass for both directions
- High-priority real-time bypass for each scheduler
- Queueing per-VC for up to 1024 connections per direction
- Weighted fair queuing with 15,360 weight factors programmable for each queue
- Optional shaping selectable for each queue (peak rate limiting) with minimum rate 100 cells/s (63,488 programmable rates)

Traffic Class Support

- Common and per scheduler high-priority real-time bypass for CBR and VBR-rt
- Guaranteed buffer space for CBR and VBR-rt
- Optional cell spacing for CBR (using per-VC queuing)

Type	Package
PXB 4330	P-BGA-352-1

- Per-VC queuing for VBR-nrt, ABR, UBR+, GFR
- Guaranteed rates, programmable per queue, via weight factors for VBR-nrt, ABR, UBR+
- PCR limitation programmable for VBR-nrt, ABR, UBR
- EFCI marking and CI/NI update in backward RM cells for ABR
- Per connection optional EPD/PPD support for ABR, UBR and UBR+
- Selective low-priority packet discard for GFR
- Queue sharing for UBR
- Up to 16 traffic classes with individual thresholds

Thresholds

- Cell acceptance based on thresholds
- Thresholds for individual queues, traffic classes, schedulers and whole buffer
- PPD/maximum discard thresholds
- EPD discard thresholds
- CLP discard thresholds
- EFCI and CI/NI thresholds

Interfaces

- Two external SDRAM Interfaces for cell storage, one for upstream and one for downstream direction, each 2 x 16 Mbit for 64K cells
- One common cell pointer SSRAM Interface with 128K x 16bit or 64K x 16bit
- Multiport UTOPIA Level 2 Interface in up- and downstream direction according to The ATM Forum, UTOPIA Level 1 and 2 specifications [**1, 2**]
- 4-cell FIFO buffer at UTOPIA upstream interfaces and downstream receive interface
- 64-cell shared buffer for up to 24 PHYs at UTOPIA downstream transmit interface
- 16-bit Microprocessor Interface, configurable as Intel or Motorola type
- Boundary Scan Interface according to JTAG [**4**]

Supervision Functions

- Internal pointer supervision
- Cell header protection function

Technology

- 0.35 µ CMOS
- Ball Grid Array BGA-352 package (Power BGA)
- Temperature range from -40°C to 85°C
- Power dissipation 1.3 W (typical)

Operating Modes

Mode	Throughput	Resources
Bi-directional	2 x 622 Mbps	2 x 1024 Queues 2 x 48 Schedulers
Uni-directional	622 Mbps	2048 Queues 96 Schedulers
Uni-directional with one Core disabled*	622 Mbps	1024 Queues 48 Schedulers

* This mode is used for power reduction and for elimination of one of the two external SDRAMs (only 1M SSRAM is required in this case)

1.2 Logic Symbol

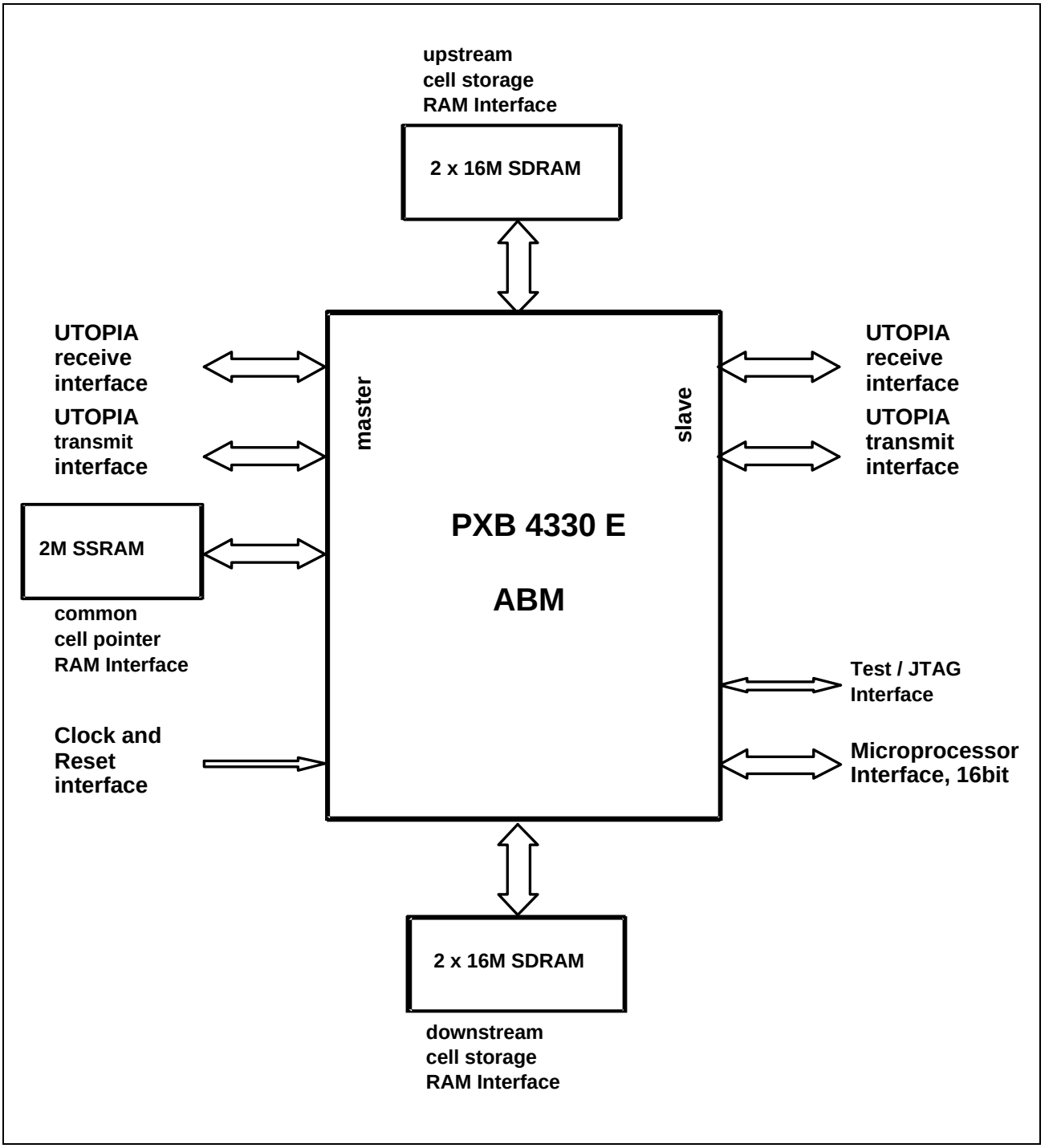


Figure 1-2 Logic Symbol

1.3 ABM Overview

The ATM Buffer Manager (ABM) has four UTOPIA Level 2 interfaces with selectable bus width of 8- or 16-bits running up to 52 MHz. This enables up to 622 Mbit/s equivalent throughput. Internal processing speed is limited to 687 Mbit/s. One receive/transmit UTOPIA Interface operates in Master Mode, the other in Slave Mode. The UTOPIA interfaces are connected internally to two identical ABM Cores as shown in **Figure 1-3** below.

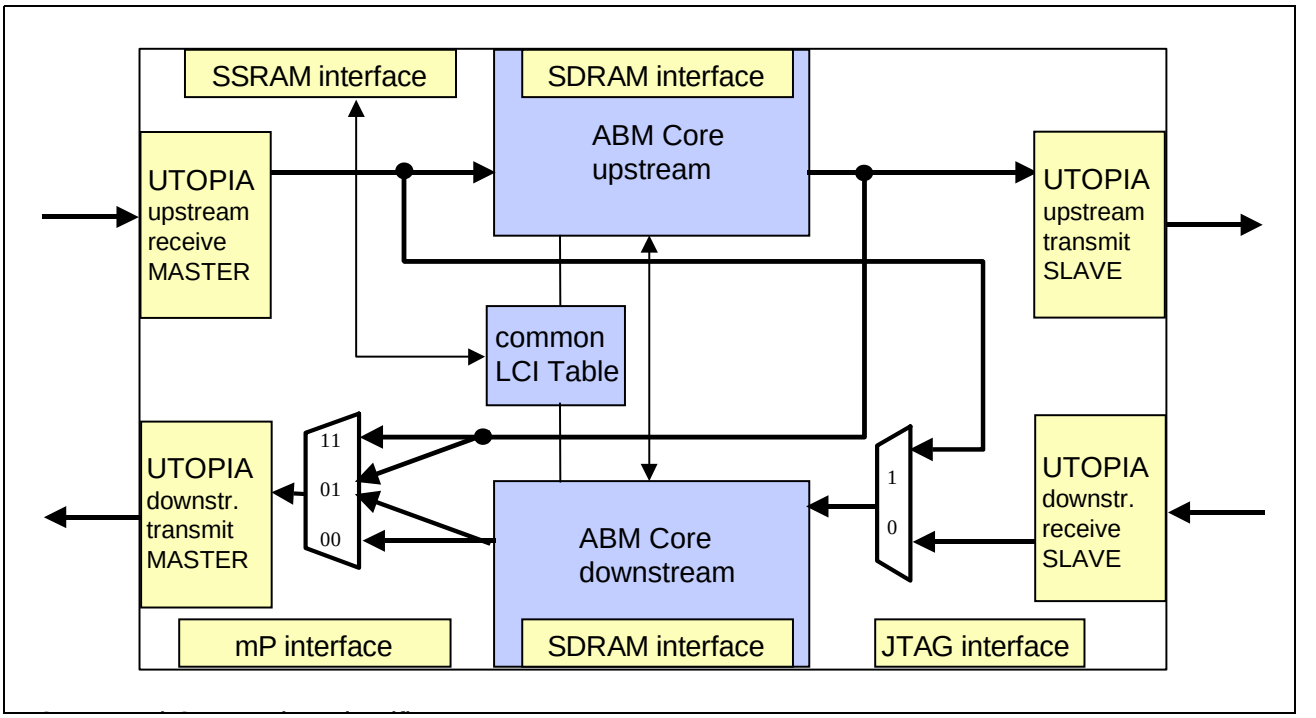


Figure 1-3 ABM Block Diagram

Multiplexers in the downstream data stream are provided for selection of uni-directional or bi-directional operating modes. In Uni-directional Mode, one of the ABM Cores can be inactivated to save power consumption and reduce external RAM requirements. Both ABM Cores contain these high-level queuing functions:

- Per-VC queuing for up to 1024 connections
- 48 Schedulers with weighted fair queuing
- Real-time bypass
- Peak rate limiter

The queueing functions are described in more detail in **"Functional Description" on page 3-37**. The ABM Cores also control the external SDRAM for storage of up to 64K cells. They share the common Local Connection Identifier (LCI) table and the external SSRAM in which the cell pointers are stored.

1.4 ATM Layer Chip Set Overview

The PXB 4330 E ABM is a member of the Infineon ATM Layer chip set. The chip set includes:

- PXB 4330 E ATM Buffer Manager ABM
- PXB 4340 E ATM OAM Processor AOP
- PXB 4350 E ATM Layer Processor ALP
- PXB 4360 F Content Addressable Memory Element CAME.

These chips form a complete chip set with which to build an ATM switch. A generic ATM switch consists of a switching fabric and switch ports as shown in **Figure 1-4**.

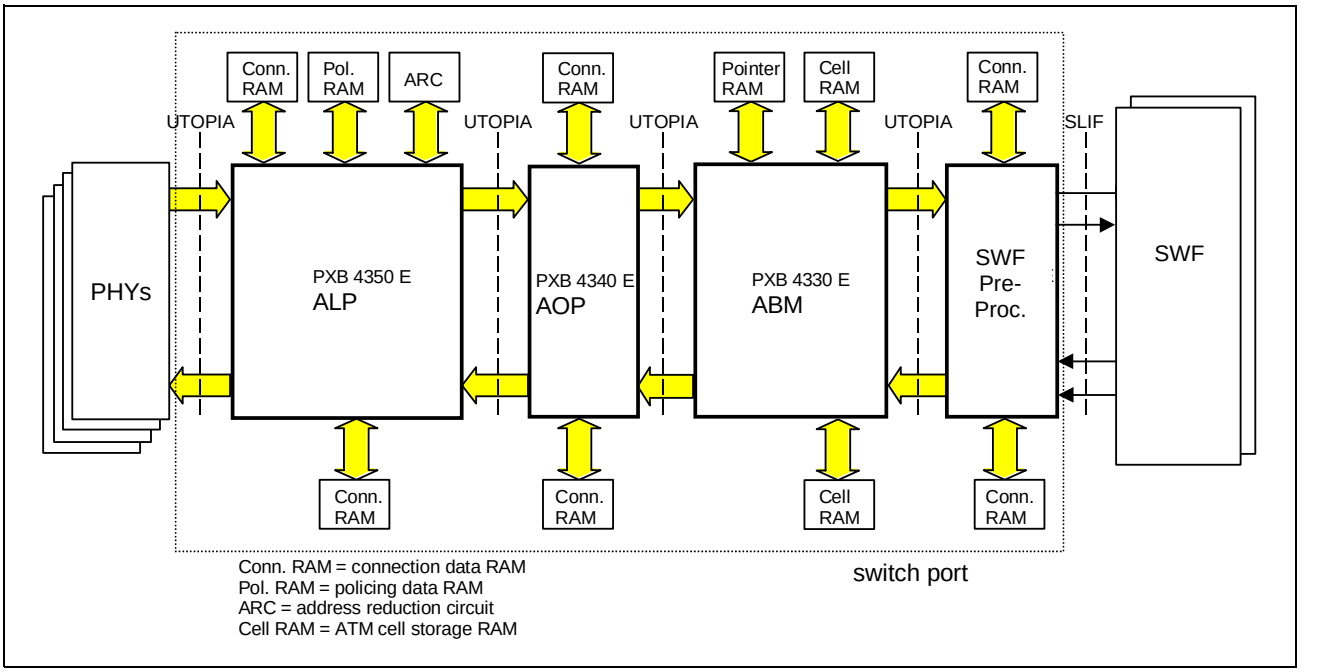


Figure 1-4 ATM Switch Basic Configuration

In the Infineon ATM Layer chip set, the switching fabric is expected to perform cell routing only. All other ATM layer functions are performed on the switch ports: policing, header translation, and cell counting by the PXB 4350 E ALP; OAM functions by the PXB 4340 E AOP; and traffic management by the PXB 4330 E ABM. The PXB 4360 F CAME can be used optionally as an external Address Reduction Circuit (ARC) for the PXB 4350 E ALP.

Only two interfaces are used for data transfer: the industry standard UTOPIA [**1, 2**] Level 2 multi-PHY interfaces and the proprietary Switch Link InterFace (SLIF). SLIF is a serial, differential, high-speed link using LVDS [**3**] levels.

For low-throughput applications, a single-board switch with 622 Mbit/s throughput can be built with only one PXB 4350 E ALP, one PXB 4340 E AOP, and one PXB 4330 E ABM. Such a mini-switch (**Figure 1-5**) is basically a stand alone single port switch, without the switching network access which would be provided by the PXB 4325 E ASP.

Alternatively, the single-board solution could be used as a multiplexer connecting many subscriber lines to one access line.

If full OAM functionality is not needed, the PXB 4340 E AOP chip could be omitted. Minimum OAM and multicast functionality are also built into the PXB 4350 E ALP. The Address Reduction Circuit (ARC) could be omitted if the built-in address reduction is sufficient.

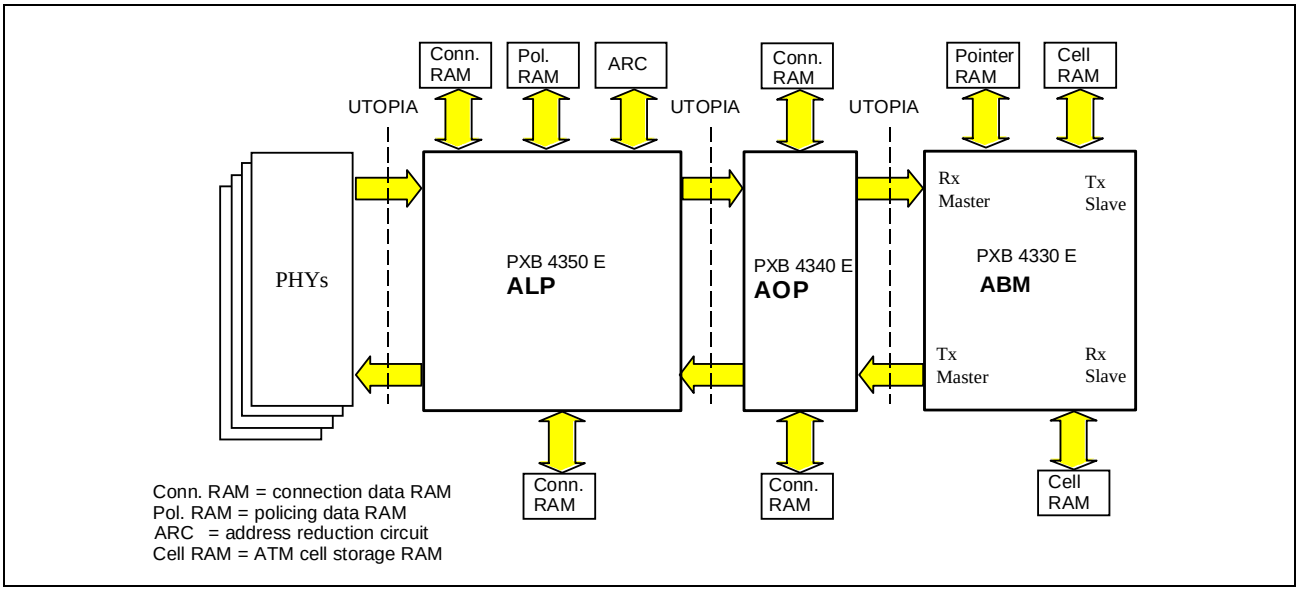


Figure 1-5 Mini Switch with 622 Mbit/s Throughput

In addition to the two applications illustrated in **Figure 1-4** and **Figure 1-5**, many other combinations of the chip set are possible in the design of ATM switches. Various combinations of functionality are possible because of the modular design of the chip set. Address reduction, multicast, policing, redundant switching network, and other functions can be implemented by appropriate chip combinations. The number of supported connections scales with the amount of external connection RAM. Policing data RAM can be omitted if the function is not required. Thus, the functionality and size of an ATM switch can be tailored exactly to the requirements of the specific application, without carrying the overhead burden of unnecessary functions.

1.5 Nomenclature

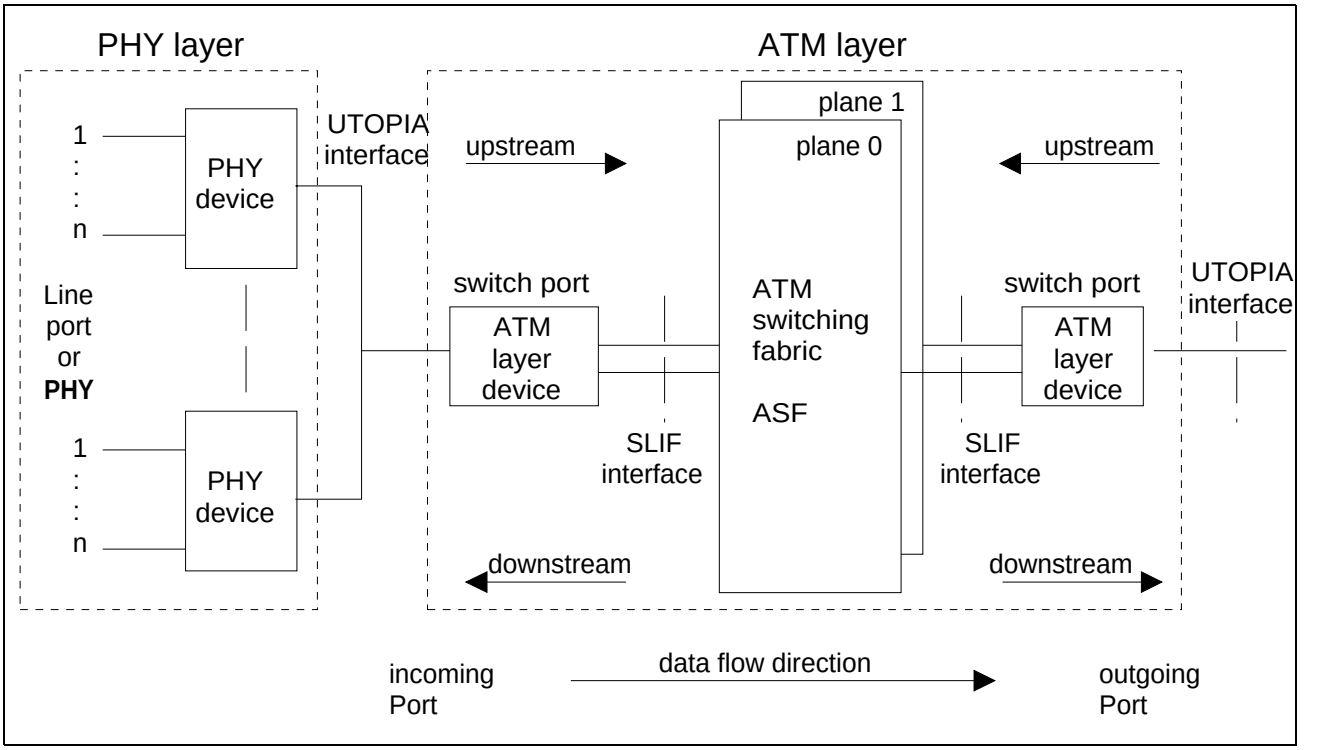


Figure 1-6 Nomenclature

Figure 1-6 shows a typical ATM Switch with the following elements:

- PHY = Line port.
- PHY device = A component (chip) containing the Physical Media Dependent (PMD) and Transmission Convergence (TC) sublayers of one or several line ports. The PMD and TC together form the Physical or PHY Layer. The UTOPIA Interface is used for the interface between the PHY and ATM layers.
- UTOPIA = Universal Test and OPerations Interface for ATM, defined by The ATM Forum in [**1**] and [**2**].
- Switch port = In the Infineon ATM switching strategy, performs all ATM Layer functions except routing.
- ATM layer device = Combinations of the chips PXB 4350 E ALP, PXB 4340 E AOP, PXB 4330 E ABM, and PXB 4325 E ASP as shown for example in **Figure 1-1**. They perform the ATM Layer functions such as header translation, policing, OAM, traffic management, etc. and are interconnected with the UTOPIA Interface.
- ATM Switching Fabric (ASF) = An array of PXB 4310 E ASM chips; provides space switching of ATM cells (routing), including buffering of cells for cell level congestion.
- Planes 0 and 1 = Two redundant switching fabrics, which are identical.
- Incoming/outgoing port = Refers to a connection with the data flow direction as shown in **Figure 1-6**.
- Upstream/downstream = Refers to the ATM switching network; the direction towards the ASF is upstream, the direction coming from the ASF is downstream.

1.6 System Integration

The ABM has two operational modes: Bi-directional Mode and Uni-directional Mode. The directional terminology for the modes refers to the usage of the ABM cores, not to the connections. The connections are bi-directional in all cases. In Bi-directional Mode, one ABM core is used exclusively for the cells of a connection in the upstream direction and the other core exclusively handles cells of the same connection in the downstream direction. In Uni-directional Mode, only one core always will be used to handle the cells of a connection both in up- and downstream direction. The two basic applications for these modes are the switch port (**Figure 1-4**) and the mini-switch (**Figure 1-5**), respectively.

On a switch port, both the upstream and downstream cell flow pass through the same ABM device. One ABM Core is used for each direction as shown in **Figure 1-7**.

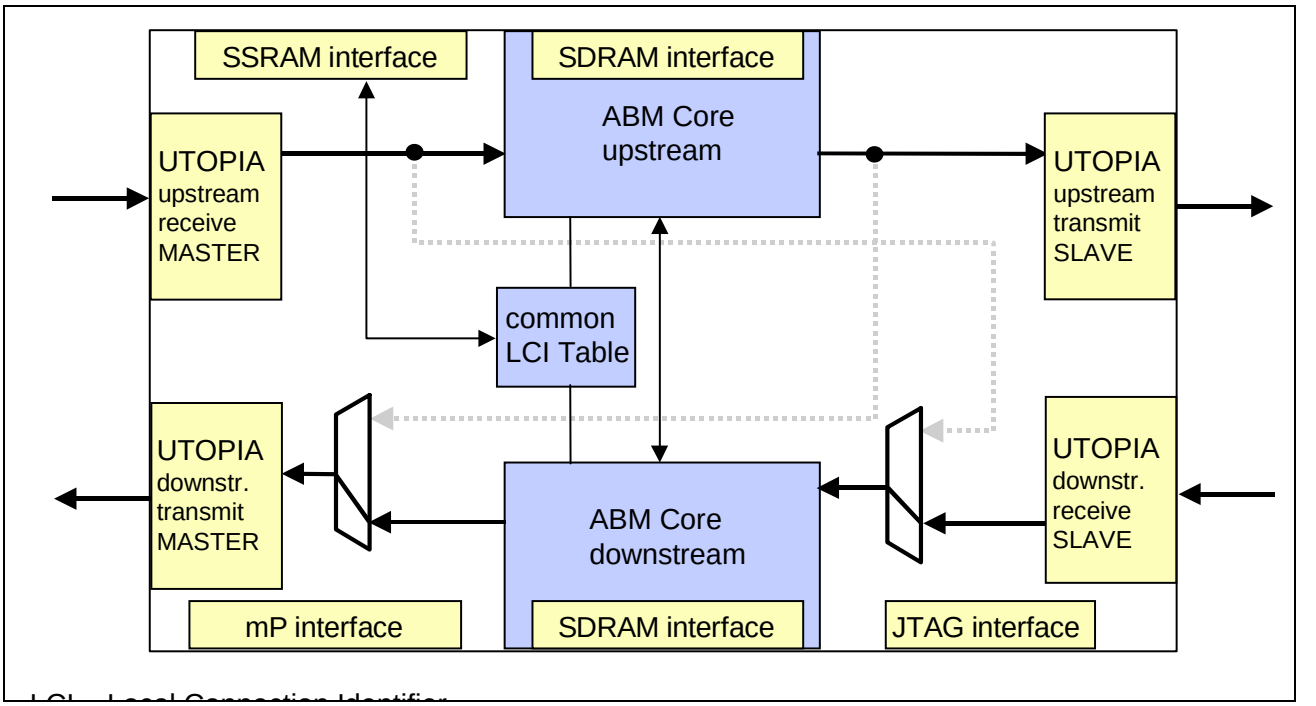


Figure 1-7 ABM in Bi-directional Mode

The ABM assumes that all connections are setup bi-directionally with the same Local Connection Identifier (LCI) in both directions. In the Infineon ATM chip set environment (**see Figure 1-4, Figure 1-5 and Figure 1-3**), the LCI is provided by the PXB 4350 E ALP and contains VPI, VCI, and PHY information. If the ABM is not used with the ALP, it can operate on VPI or VCI identifiers only. In these cases, queuing is done for VCCs and VPCs, respectively. Also, the AOP could work with full functionality with a header translation device to provide a connection identifier in the VPI field. In this case, the number of connections is reduced to 4096 per direction.

In a mini-switch, the throughput is only one times 622 Mbit/s. Only the UTOPIA Rx and Tx master interfaces are active. Both ABM Cores are selected from the multiplexer

options shown in **Figure 1-8**. Each cell is forwarded to both ABM Cores; but, the LCI table entry for the connection determines which of the two Cores accepts the cell. The other Core ignores it. Thus, each cell is stored and queued in one of the two Cores. The cell streams of both Cores are multiplexed together at the output. The schedulers must be programmed such that the sum of all output rates does not exceed the maximum rate supported by the UTOPIA transmit interface.

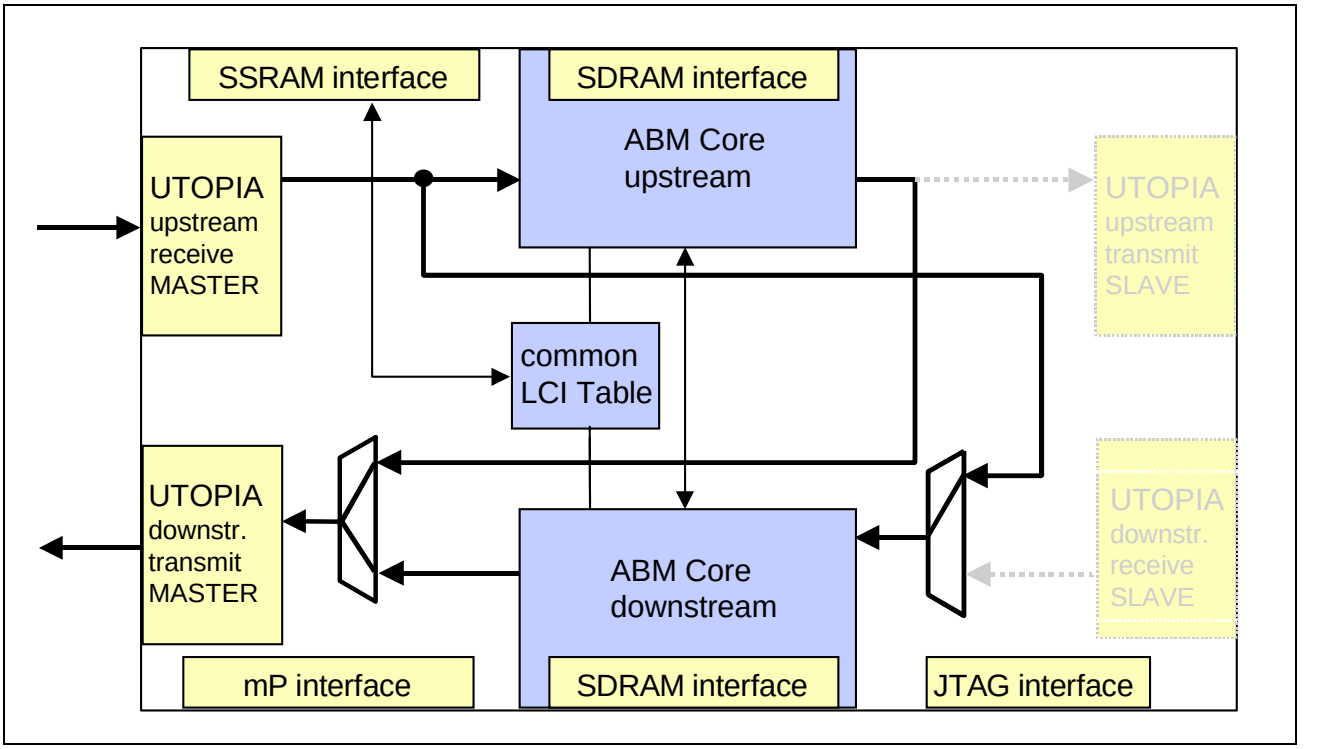


Figure 1-8 ABM in Uni-directional Mode Using both Cores

If the resources of one Core are sufficient, the downstream Core can be deactivated (see **Figure 1-9**). This reduces the power consumption and allows omission of the external downstream SDRAM. It also permits the SSRAM to be smaller (see below).

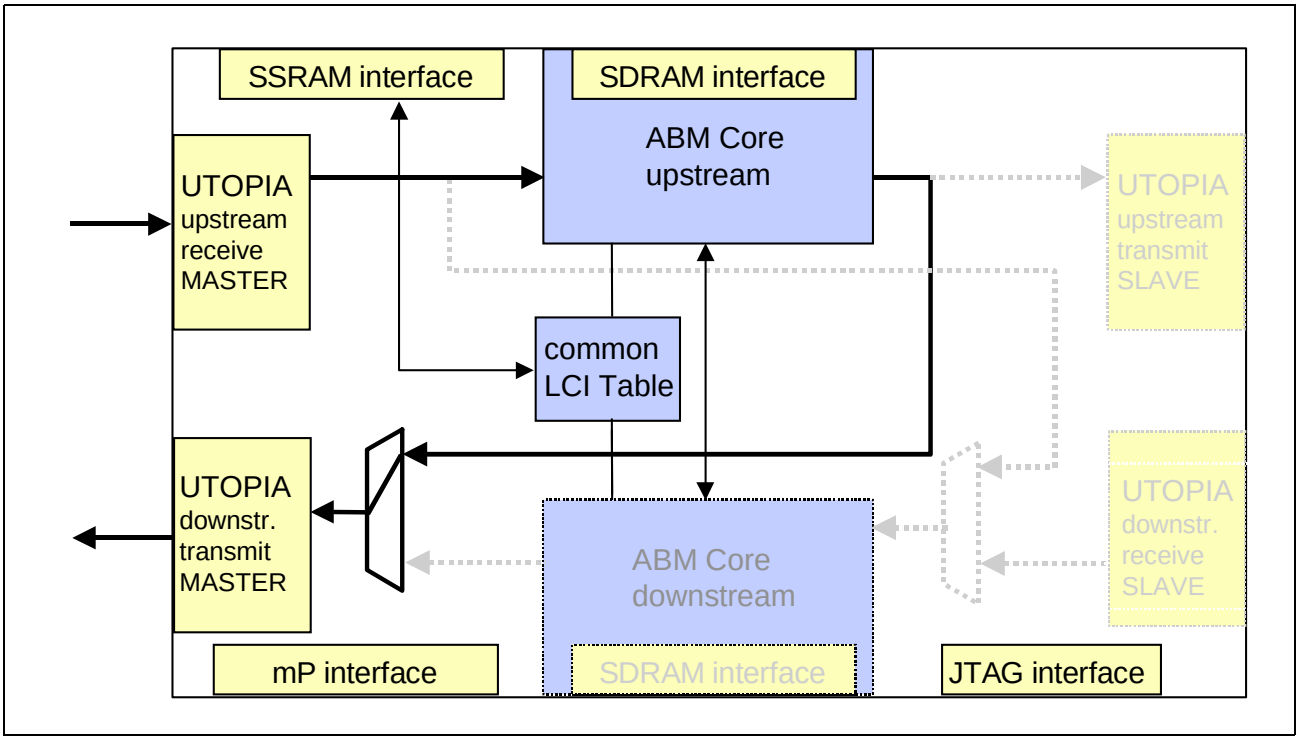


Figure 1-9 ABM in Uni-directional Mode Using one Core

1.6.1 LCI Translation in Mini-Switch Configurations

In Uni-directional applications, the ABM can be programmed to make a minimum header translation. This is necessary in a Mini-Switch configuration as both the forward and backward direction of a connection traverse the devices in the same direction. The OAM functions in the ALP or AOP device need the same LCI for forward and backward direction of a connection.

This is clarified by the example shown in **Figure 1-10** in which a connection is setup from PHY_1 to PHY_2. VPI/VCI_1 is the identifier on the transmission line where PHY_1 is connected. The terminal sends ATM cells with this identifier and expects cells in the backward direction from PHY_2 with the same identifier. The ALP in the upstream direction translates VPI/VCI_1 into LCI1, the unique local identifier for this connection in the upstream direction. Similarly, for the backward connection from PHY_2 to PHY_1, the ALP receives ATM cells from PHY_2 with the identifier VPI/VCI_2 and translates them into LCI_2.

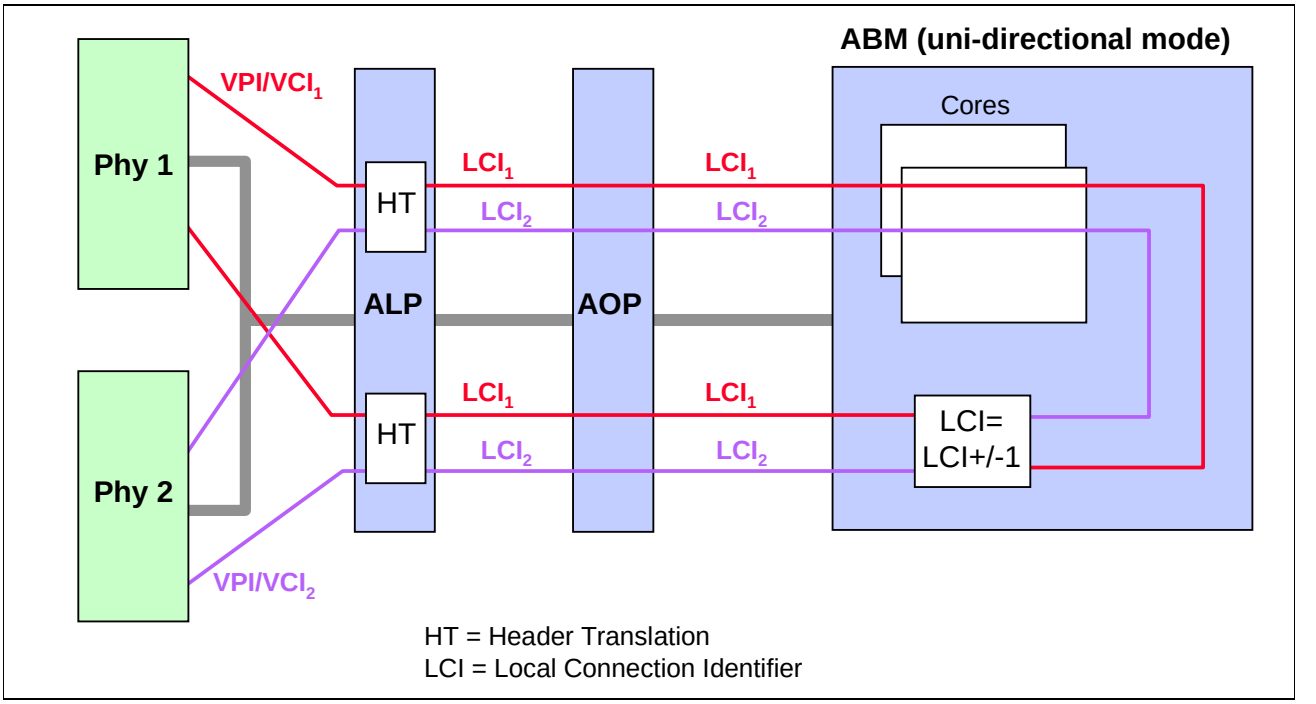


Figure 1-10 Connection Identifiers in Mini-Switch Configuration

For minimum complexity, the header translation of the ABM is done by inverting the Least Significant Bit (LSB) of the LCI. This measure divides the available LCI range into two parts: *odd* LCI values for forward connections and *even* LCI values for backward connection (i.e. it reduces the available number of connection identifiers to 4096, because two LCI values are used per connection).
This is not a restriction in the case of arbitrary address reduction modes as, for example, the ALP with the CAME chip, as ATM connections are always setup bi-directionally with the same VPI/VCI in both directions of a link.

Note: In case of fixed address reduction, as, for example, the ALP with the built-in Address Reduction Circuit (ARC), the usable LCI range may be seriously restricted, depending on the PHY configuration.

2 Pin Descriptions

2.1 Pin Diagram

(top view)

P-BGA-352-1

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF
1	VSS	VSS	CPADR 3	$\overline{CP}$ $\overline{ADSC}$	UTATM CLK	TXCLA VU0	TXDAT U13	TXDAT U9	TXDAT U6	TXDAT U2	TXPRT YU	TXADR U2	VSS	VSS	$\overline{TXENB}$ $\overline{U0}$	RXCLA VD1	RXDAT D14	RXDAT D10	RXDAT D7	RXDAT D3	RXDAT D0	RXADR D2	$\overline{RXENB}$ $\overline{D2}$	$\overline{MPCS}$	VSS	VSS
2	VSS	VDD	VSS	CPADR 2	$\overline{CPGW}$	TXCLA VU3	TXDAT U15	TXDAT U12	TXDAT U8	TXDAT U4	TXDAT U1	TXADR U3	TXADR U0	$\overline{TXENB}$ $\overline{U3}$	RXCLA VD3	RXDAT D15	RXDAT D12	RXDAT D8	RXDAT D4	RXDAT D1	RXADR D3	$\overline{RXENB}$ $\overline{D3}$	MP MOD	VSS	VDD	VSS
3	CPADR 8	VSS	VDD	CPADR 5	CPADR 1	TST OUT2	TXCLA VU2	TXDAT U14	TXDAT U11	TXDAT U7	TXDAT U3	TXSOC U	TXADR U1	$\overline{TXENB}$ $\overline{U2}$	RXCLA VD2	RXDAT D13	RXDAT D9	RXDAT D5	RXDAT D2	RXSOC D	RXADR D0	$\overline{RXENB}$ $\overline{D0}$	MPRDY	VDD	VSS	MPDAT 15
4	CPADR 12	CPADR 9	CPADR 6	VDD	CPADR 4	CPADR 0	$\overline{CPOE}$	TXCLA VU1	VDD	TXDAT U10	TXDAT U5	TXDAT U0	VDD	$\overline{TXENB}$ $\overline{U1}$	RXCLA VD0	RXDAT D11	RXDAT D6	VDD	RXPRT YD	RXADR D1	$\overline{RXENB}$ $\overline{D1}$	$\overline{MPINT}$	VDD	$\overline{MPWR}$	MPDAT 14	MPDAT 11
5	CPADR 16	CPADR 13	CPADR 10	CPADR 7																			$\overline{MPRD}$	MPDAT 13	MPDAT 10	MPDAT 7
6	CPDAT 3	CPDAT 0	CPADR 14	CPADR 11																			MPDAT 12	MPDAT 9	MPDAT 6	MPDAT 3
7	CPDAT 6	CPDAT 4	CPDAT 1	CPADR 15																			MPDAT 8	MPDAT 5	MPDAT 2	MPDAT 0
8	CPDAT 10	CPDAT 7	CPDAT 5	CPDAT 2																			MPDAT 4	MPDAT 1	MPADR 7	MPADR 4
9	CPDAT 13	CPDAT 11	CPDAT 8	VDD																			VDD	MPADR 6	MPADR 3	MPADR 1
10	$\overline{RCASU}$	CPDAT 15	CPDAT 12	CPDAT 9																			MPADR 5	MPADR 2	RDATD 31	RDATD 29
11	RADRU 0	$\overline{RRASU}$	$\overline{RWEU}$	CPDAT 14																			MPADR 0	RDATD 30	RDATD 28	RDATD 26
12	RADRU 3	RADRU 2	RADRU 1	$\overline{RCSU}$																			RDATD 27	RDATD 25	RDATD 24	RDATD 23
13	VSS	RADRU 6	RADRU 5	RADRU 4																			VDD	RDATD 22	RDATD 21	VSS
14	VSS	RADRU 7	RADRU 8	VDD																			RDATD 18	RDATD 19	RDATD 20	VSS
15	RADRU 9	RADRU 10	RADRU 11	RDATU 1																			RDATD 13	RDATD 15	RDATD 16	RDATD 17
16	RDATU 0	RDATU 2	RDATU 4	RDATU 6																			RDATD 8	RDATD 10	RDATD 12	RDATD 14
17	RDATU 3	RDATU 5	RDATU 8	RDATU 11																			RDATD 3	RDATD 6	RDATD 9	RDATD 11
18	RDATU 7	RDATU 9	RDATU 12	VDD																			VDD	RDATD 2	RDATD 5	RDATD 7
19	RDATU 10	RDATU 13	RDATU 15	RDATU 18																			RADRD 8	RADRD 11	RDATD 1	RDATD 4
20	RDATU 14	RDATU 16	RDATU 19	RDATU 22																			RADRD 4	RADRD 7	RADRD 10	RDATD 0
21	RDATU 17	RDATU 20	RDATU 23	RDATU 26																			RADRD 0	RADRD 3	RADRD 6	RADRD 9
22	RDATU 21	RDATU 24	RDATU 27	RDATU 30																			$\overline{RWED}$	$\overline{RCSD}$	RADRD 2	RADRD 5
23	RDATU 25	RDATU 28	RDATU 31	VDD	TST MOD1	$\overline{OUT}$ $\overline{TRI}$	SYS CLK	$\overline{RXENB}$ $\overline{U3}$	VDD	RXDAT U0	RXDAT U5	RXDAT U10	RXDAT U15	VDD	TXADR D0	TXPRT YD	TXDAT D4	VDD	TXDAT D11	TXDAT D15	TXCLA VD3	TCK	VDD	$\overline{TRST}$	$\overline{RRASD}$	RADRD 1
24	RDATU 29	VSS	VDD	TST OUT1	TSCAN M	$\overline{RESET}$	$\overline{RXENB}$ $\overline{U2}$	RXADR U2	RXPRT YU	RXDAT U3	RXDAT U7	RXDAT U12	RXCLA VU0	RXCLA VU3	$\overline{TXENB}$ $\overline{D2}$	TXADR D3	TXDAT D1	TXDAT D5	TXDAT D8	TXDAT D12	TXCLA VD0	UTPHY CLK	TDI	VDD	VSS	$\overline{RCASD}$
25	VSS	VDD	VSS	TSCAN EN	$\overline{UTTRI}$	$\overline{RXENB}$ $\overline{U1}$	RXADR U1	RXSOC U	RXDAT U2	RXDAT U6	RXDAT U9	RXDAT U13	RXCLA VU1	RXCLA VU2	$\overline{TXENB}$ $\overline{D1}$	TXADR D1	TXSOC D	TXDAT D2	TXDAT D6	TXDAT D9	TXDAT D13	TXCLA VD1	TDO	VSS	VDD	VSS
26	VSS	VSS	TST CLK	EXT FREEZ	$\overline{RXENB}$ $\overline{U0}$	RXADR U0	RXADR U3	RXDAT U1	RXDAT U4	RXDAT U8	RXDAT U11	RXDAT U14	VSS	VSS	$\overline{TXENB}$ $\overline{D0}$	$\overline{TXENB}$ $\overline{D3}$	TXADR D2	TXDAT D0	TXDAT D3	TXDAT D7	TXDAT D10	TXDAT D14	TXCLA VD2	TMS	VSS	VSS

Bottom View

Figure 2-1 Pin Configuration

Some pins are connected to an internal pull up resistor or to an internal pull down resistor. Such pins are indicated as follows in Table 2-1:

- Pins shown with a [1)] are connected with an internal pull up resistor.
- Pins shown with a [2)] are connected with an internal pull down resistor.

Note: The ABM signal pins are not 5V I/O tolerant. For further details refer to "Electrical Characteristics" on page 7-174.

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Clock and Reset (4 pins)			
F24	$\overline{\text{RESET}}$	I	Chip Reset
G23	SYSCLK	I	Main Chip Clock
AB24	UTPHYCLK	I	UTOPIA Clock at PHY side (Master).
E1	UTATMCLK	I	UTOPIA Clock at ATM side (Slave).
Utopia Interface Receive Upstream Master (30 pins)			
N23, M26, M25, M24, L26, M23, L25, K26, L24, K25, L23, J26, K24, J25, H26, K23 [2)]	RXDATU (15:0)	I	Receive Data Bus from PHY side.
G26, H24, G25, F26	RXADRU (3:0)	O	Address Outputs to PHY side.
J24 [2)]	RXPRTYU	I	Odd Parity of RXDATU(15:0) from PHY side.
H23, G24, F25, E26	$\overline{\text{RXENBU}}$ (3:0)	O	Enable signal to PHY side.
P24, P25, N25, N24 [2)]	RXCLAVU (3:0)	I	Cell Available signal from PHY side.
H25 [2)]	RXSOCU	I	Start of Cell signal from PHY side.

Table 2-1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Utopia Interface Transmit Downstream Master (30 pins)			
Y23, AB26, AA25, Y24, W23, AA26, Y25, W24, Y26, W25, V24, U23, W26, V25, U24, V26	TXDATD (15:0)	O	Transmit Data Bus to PHY side.
T24, U26, T25, R23	TXADRD (3:0)	O	Address Bus to PHY side.
T23	TXPRTYD	O	Odd Parity to PHY side.
T26, R24, R25, R26	$\overline{\text{TXENBD}}$ (3:0)	O	Enable signal to PHY side.
AA23, AC26, AB25, AA24 [2)]	TXCLAVD (3:0)	I	Cell Available signal from PHY side.
U25	TXSOCD	O	Start of Cell signal to PHY side.
Utopia Interface Receive Downstream Slave (30 pins)			
T2, U1, T3, U2, T4, V1, U3, V2, W1, U4, V3, W2, Y1, W3, Y2, AA1 [2)]	RXDATD (15:0)	I	Receive Data Bus from ATM side.
AA2, AB1, Y4, AA3 [2)]	RXADRD (3:0)	I	Address Bus from ATM side.
W4 [2)]	RXPRTYD	I	Odd Parity of RXDATD(15:0) from ATM side.
AB2, AC1, AA4, AB3 [1)]	$\overline{\text{RXENBD}}$ (3:0)	I	Enable signals from ATM side.
R2, R3, T1, R4	RXCLAVD (3:0)	O	Cell Available signal to ATM side.
Y3 [2)]	RXSOCD	I	Start of Cell signal from ATM side.

Table 2-1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Utopia Interface Transmit Upstream Slave (30 pins)			
G2, H3, G1, H2, J3, K4, H1, J2, K3, J1, L4, K2, L3, K1, L2, M4	TXDATU (15:0)	O	Transmit Data Bus to ATM side.
M2, M1, N3, N2 [2)]	TXADRU (3:0)	I	Address Bus from ATM side.
L1	TXPRTYU	O	Odd Parity of RXDATU(15:0) to ATM side.
P2, P3, P4, R1 [1)]	$\overline{\text{TXENBU}}$ (3:0)	I	Enable signal from ATM side.
F2, G3, H4, F1	TXCLAVU (3:0)	O	Cell Available signal to ATM side.
M3	TXSOCU	O	Start of Cell signal to ATM side.
Microprocessor Interface (30 pins)			
AF3, AE4, AD5, AC6, AF4, AE5, AD6, AC7, AF5, AE6, AD7, AC8, AF6, AE7, AD8, AF7	MPDAT (15:0)	I/O	Microprocessor Data Bus
AE8, AD9, AC10, AF8, AE9, AD10, AF9, AC11	MPADR (7:0)	I	Address Bus from Microprocessor
AD4	$\overline{\text{MPWR}}$	I	$\overline{\text{WR}}$ when MPMOD=0 (Intel Mode) R/$\overline{\text{W}}$ when MPMOD=1 (Motorola Mode).
AC5	$\overline{\text{MPRD}}$	I	$\overline{\text{RD}}$ when MPMOD=0 (Intel Mode) $\overline{\text{DS}}$ when MPMOD=1 (Motorola Mode).
AD1	$\overline{\text{MPCS}}$	I	Chip Select from Microprocessor.

Table 2-1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
AB4	$\overline{\text{MPINT}}$	O	Interrupt Request to Microprocessor. Open drain, needs external pull-up resistor. Interrupt pins of several devices can be wired-or together.
AC3	MPRDY	O	Ready Output to Microprocessor for read and write accesses.
AC2 [2)]	MPMOD	I	Select Intel type processor when connected to logical 0 or select Motorola type processor when connected to logical 1.
Cell Storage RAM Upstream (48 pins)			
C23, D22, A24, B23, C22, D21, A23, B22, C21, D20, A22, B21, C20, D19, A21, B20, C19, A20, B19, C18, D17, A19, B18, C17, A18, D16, B17, C16, A17, B16, D15, A16	RDATU (31:0)	I/O	Data Bus of Upstream Cell Storage RAM
C15, B15, A15, C14, B14, B13, C13, D13, A12, B12, C12, A11	RADRU (11:0)	O	Address Bus of Upstream Cell Storage RAM
D12	$\overline{\text{RCSU}}$	O	RAM Chip Select
B11	$\overline{\text{RRASU}}$	O	RAM Row Address Strobe
A10	$\overline{\text{RCASU}}$	O	RAM Column Address Strobe

Table 2-1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
C11	$\overline{\text{RWEU}}$	O	RAM Write Enable
Cell Storage RAM Downstream (48 pins)			
AE10, AD11, AF10, AE11, AC12, AF11, AD12, AE12, AF12, AD13, AE13, AE14, AD14, AC14, AF15, AE15, AD15, AF16, AC15, AE16, AF17, AD16, AE17, AC16, AF18, AD17, AE18, AF19, AC17, AD18, AE19, AF20	RDATD (31:0)	I/O	Data Bus of Downstream Cell Storage RAM
AD19, AE20, AF21, AC19, AD20, AE21, AF22, AC20, AD21, AE22, AF23, AC21	RADRD (11:0)	O	Address Bus of Downstream Cell Storage RAM
AD22	$\overline{\text{RCSD}}$	O	RAM Chip Select
AE23	$\overline{\text{RRASD}}$	O	RAM Row Address Strobe
AF24	$\overline{\text{RCASD}}$	O	RAM Column Address Strobe
AC22	$\overline{\text{RWED}}$	O	RAM Write Enable

Table 2-1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Common Up- and Downstream Cell Pointer RAM (36 pins)			
B10, D11, A9, C10, B9, A8, D10, C9, B8, A7, C8, B7, A6, D8, C7, B6	CPDAT (15:0)	I/O	Data Bus of Cell Pointer RAM
A5, D7, C6, B5, A4, D6, C5, B4, A3, D5, C4, D3, E4, C1, D2, E3, F4	CPADR (16:0)	O	Address Bus of Cell Pointer RAM
D1	$\overline{\text{CPADSC}}$	O	RAM Synchronous Address Status Processor
E2	$\overline{\text{CPGW}}$	O	RAM Global Write
G4	$\overline{\text{CPOE}}$	O	RAM Output Enable
JTAG Boundary Scan (5 pins)			
AC24 [1)]	TDI	I	Test Data Input. This pin has an internal pull-up resistor. In normal operation, it must not be connected.
AB23 [1)]	TCK	I	Test Clock. This pin has an internal pull-up resistor. In normal operation, it must not be connected.
AD26 [1)]	TMS	I	Test Mode Select. This pin has an internal pull-up resistor. In normal operation, it must not be connected.
AD23 [2)]	$\overline{\text{TRST}}$	I	Test Data Reset This pin has an internal pull-down resistor. In normal operation, it must not be connected.
AC25	TDO	O	Test Data Output In normal operation, must not be connected.

Table 2-1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Test (2 pins)			
F23	$\overline{\text{OUTTRI}}$	I	Outputs in Tristate mode. All internal pull-up and pull-down resistors are disconnected. This pin has no internal pull-up resistor and needs an external pull-up resistor.
E25 [1)]	$\overline{\text{UTTRI}}$	I	UTOPIA Outputs in Tristate mode. This pin has an internal pull-up resistor.
Production Test (7 pins)			
D25	TSCANEN	I	Test Scan Enable. Active high, internal pull-down resistor. Must not be connected in normal operation.
E24 [2)]	TSCANM	I	Test Scan Mode. Active high, internal pull-down resistor. Must not be connected in normal operation.
D26 [1)]	EXTFREEZ	I	For device test only, do not connect. These pins have internal pull-up resistors. Must not be connected in normal operation.
E23 [1)]	TSTMOD1	I	
D24	TSTOUT1	O	For device test only, do not connect.
F3	TSTOUT2	O	
C26	TSTCLK	O	For device test only, do not connect.
Supply (28 V_{SS} and 24 V_{DD} pins)			
A1, A2, A13, A14, A25, A26, B1, B3, B24, B26, C2, C25, N1, N26, P1, P26, AD2, AD25, AE1, AE24, AE3, AE26, AF1, AF2, AF13, AF14, AF25, AF26			V_{SS}, Chip Ground (All pins should be connected to the same level)
AC4, AC9, AC13, AC18, AC23, AD3, AD24, AE2, AE25, B2, B25, C3, C24, D4, D9, D14, D18, D23, J23, J4, N4, P23, V4, V23			V_{DD}, Chip 3.3 V Supply (All pins should be connected to the same level)

Total signal pins: 300; total power pins: 52.

3 Functional Description

3.1 The ABM Core

Figure 3-1 shows the block diagram of an ATM Buffer Manager (ABM) Core. Cells with up to 687 Mbit/s (with 52 MHz SYSCLK) are assigned to Schedulers and queues within the Cell Acceptance block. As it enters, each cell is checked to verify that it would not exceed the respective thresholds which are provided for queues, schedulers, QoS classes (traffic classes), as well as the total buffer capacity. Once accepted, a cell cannot be lost, but will appear at the output after some time (exception: queue has been disabled while cells are stored).

The optional Peak Rate Limiter is provided for the shaping of individual queues.

The demultiplexer forwards the cells to the respective Scheduler. The Scheduler sorts them into queues and schedules them for retransmission according to the programmed configuration. The Scheduler is the key queuing element of the ABM. The behavior of the Scheduler is described below. The output multiplexer combines the cell streams for all Schedulers. Their output rates must be programmed such that the sum rate does not exceed the total output bandwidth.

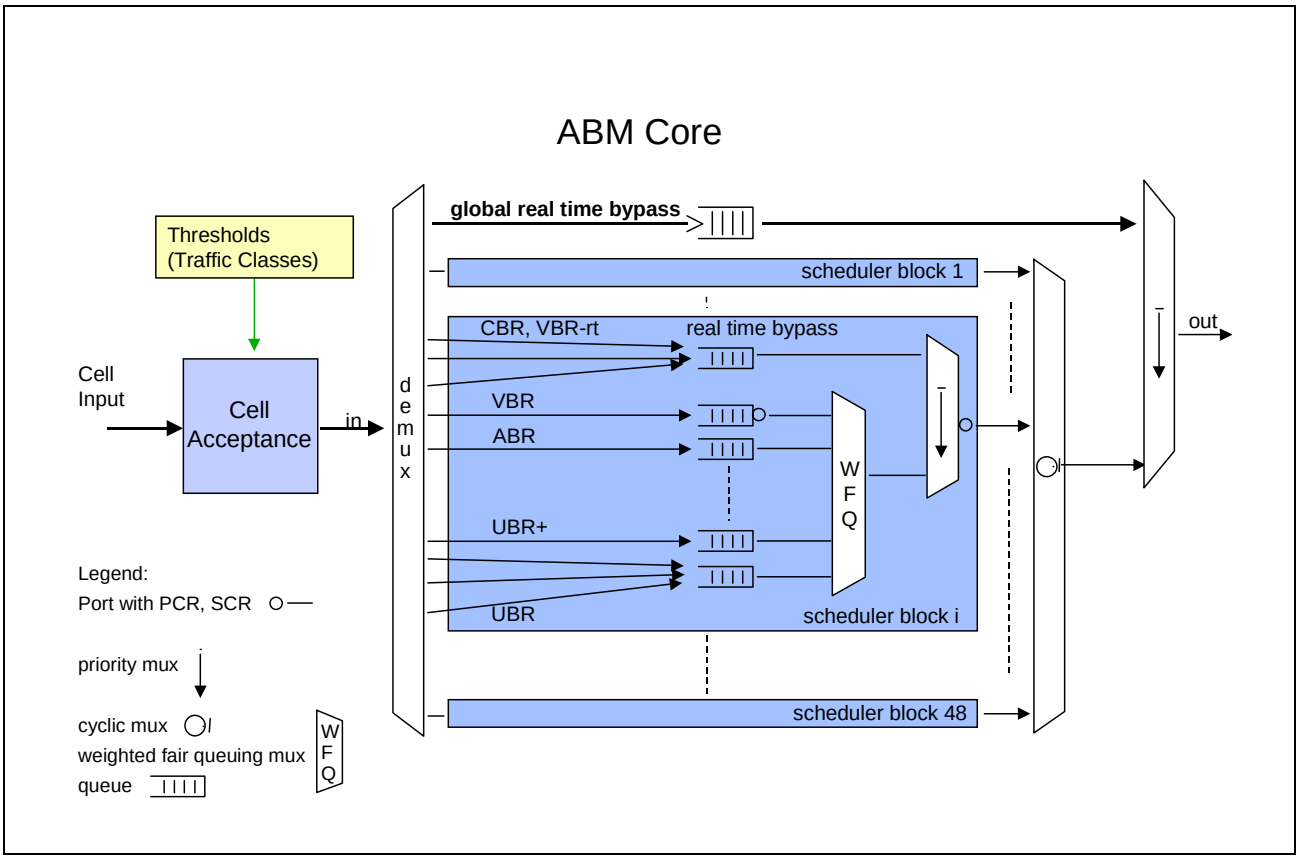


Figure 3-1 Block Diagram of one ABM Core

3.1.1 ABM Configuration

The ABM uses tables and pointer mechanisms for configuration flexibility, as shown in **Figure 3-2**. The free assignment of connections (LCIs) to queues allows queuing on a per-VC basis as well as permitting the sharing of a queue by several connections. Each queue can be assigned to any Scheduler. Independent of the Schedulers, each queue is also assigned to a traffic class with individual thresholds for up to 16 service classes.

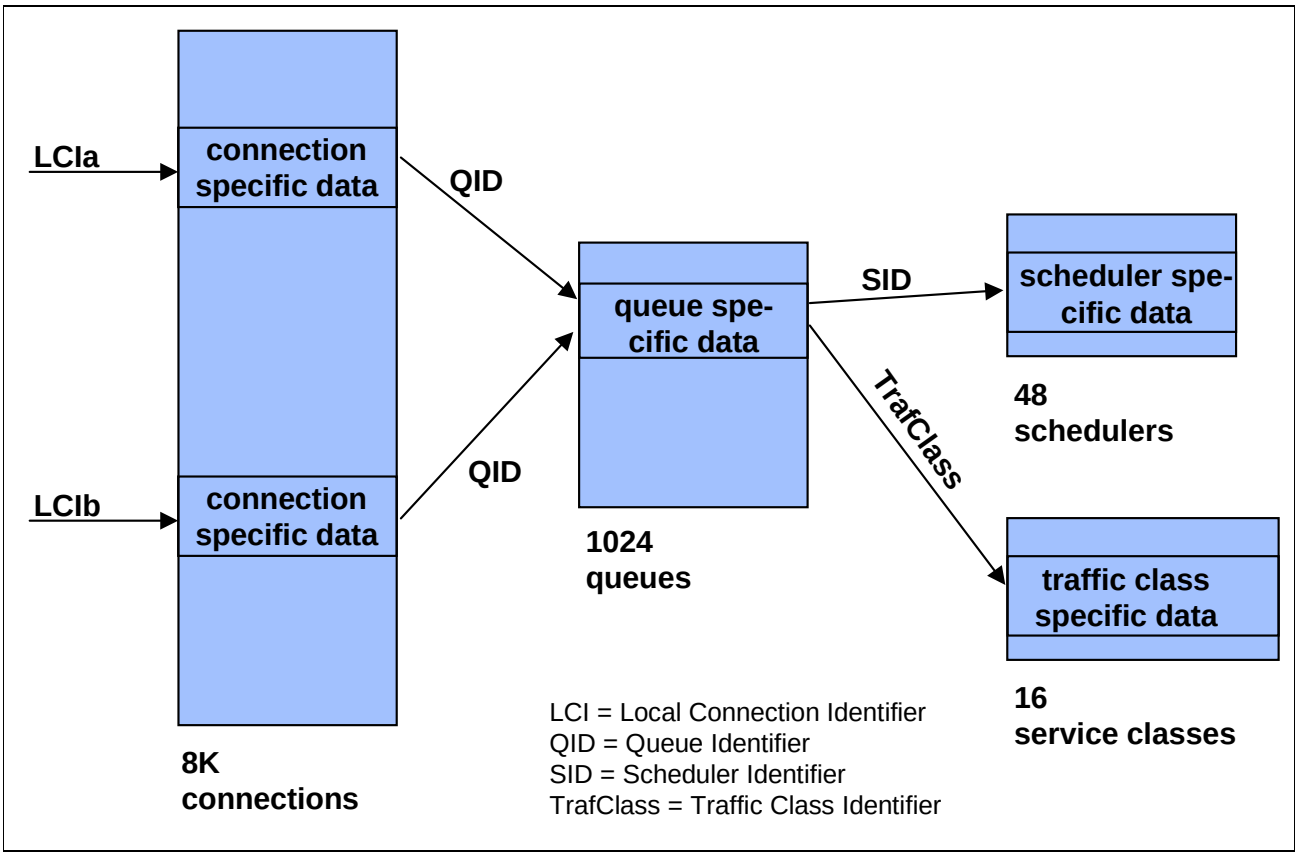


Figure 3-2 ABM Configuration

3.1.2 The Scheduler

The basic building block of the ABM is the Scheduler. A Scheduler is a cascade of two multiplexers: a Weighted Fair Queuing (WFQ) Multiplexer, and a Priority Multiplexer, as shown in **Figure 3-3**. The inputs of the multiplexers are connected to a programmable number of queues.

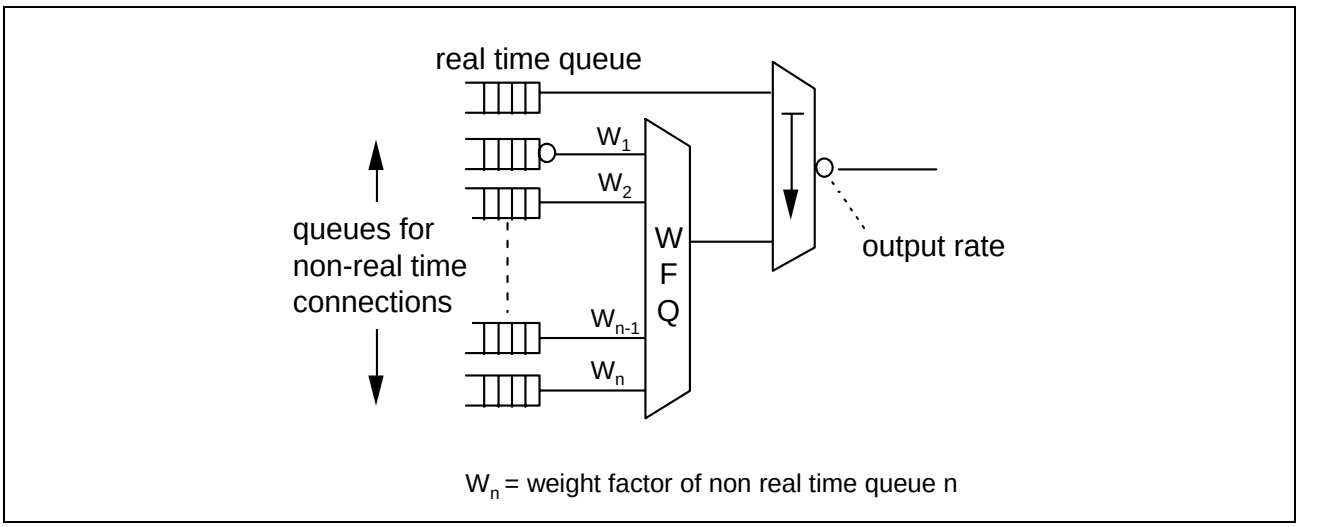


Figure 3-3 Scheduler Structure

One single queue is provided for all real-time connections. It is connected directly to the high-priority input of the Priority Multiplexer (marked with the arrow symbol). The 2-input Priority Multiplexer first takes a cell from the high-priority input; and, only if there is no cell here, then looks at the low-priority input where the WFQ Multiplexer is connected. Thus, real-time traffic is always prioritized. As the output rate of the Scheduler is limited - as denoted in **Figure 3-3** with the bubble symbol at the Priority Multiplexer output - the non-real-time connections share the remaining bandwidth. This behavior is shown in **Figure 3-4**.

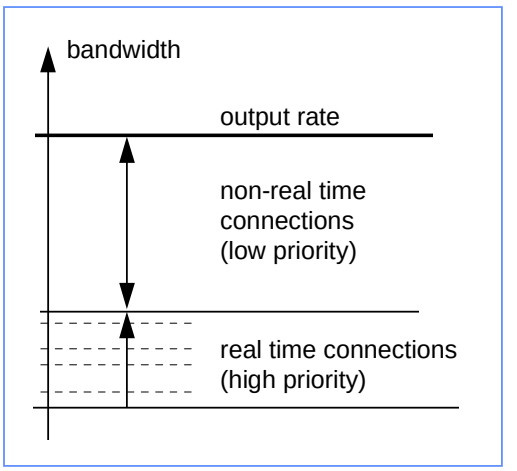


Figure 3-4 Scheduler Behavior

The WFQ Multiplexer permits sharing of the remaining bandwidth by the non-real-time connections. The WFQ Multiplexer has a maximum of 1023 inputs with a weight factor assigned to each input. It distributes the remaining bandwidth among active or occupied queues according to the weight factors.

The WFQ Multiplexer has the following properties:

- Fair distribution of bandwidth
- Guaranteed Quality of Service (QoS) for each connection (minimum service rate, bounded delay)
- Load conserving, that is, the output is always 100%
- Protection against misbehaving users (exceeding their bandwidth budget).

These are important, for example, in data connections having start-stop behavior. An example is shown in **Figure 3-5**. The duration of the data bursts and the idle periods vary over a wide range.

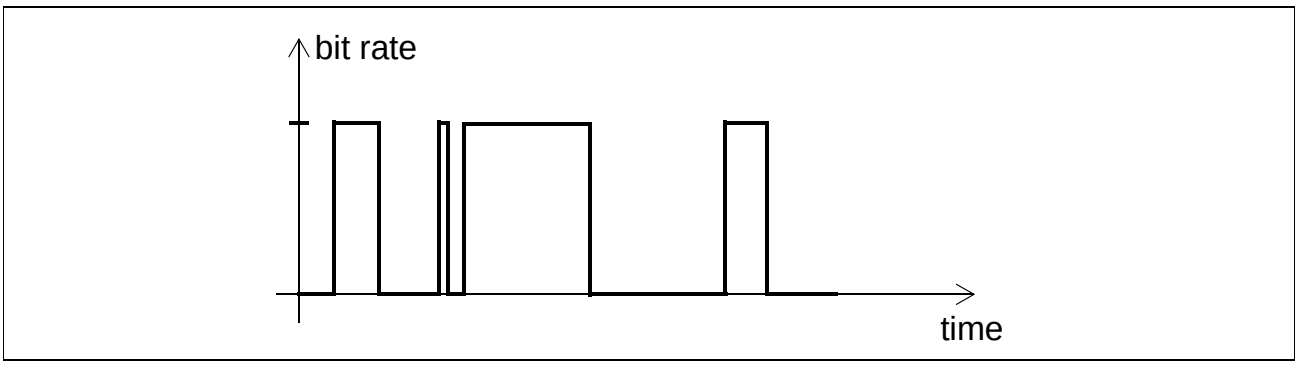


Figure 3-5 Data Traffic Example

For non-real-time connections, normally one queue is assigned to each connection, that is, per-VC queuing. During idle periods, the queues will run empty, and, when a data burst is sent, they fill up again. The WFQ Multiplexer automatically deals with the varying load situations and always distributes the bandwidth according to the weight factors. An example of a Scheduler with one real-time queue (Queue 1) and nine non-real-time queues (Queue 2 through Queue 10) is shown in **Figure 3-6**. Queue 1 is shared by a number of connections with different bit rates.

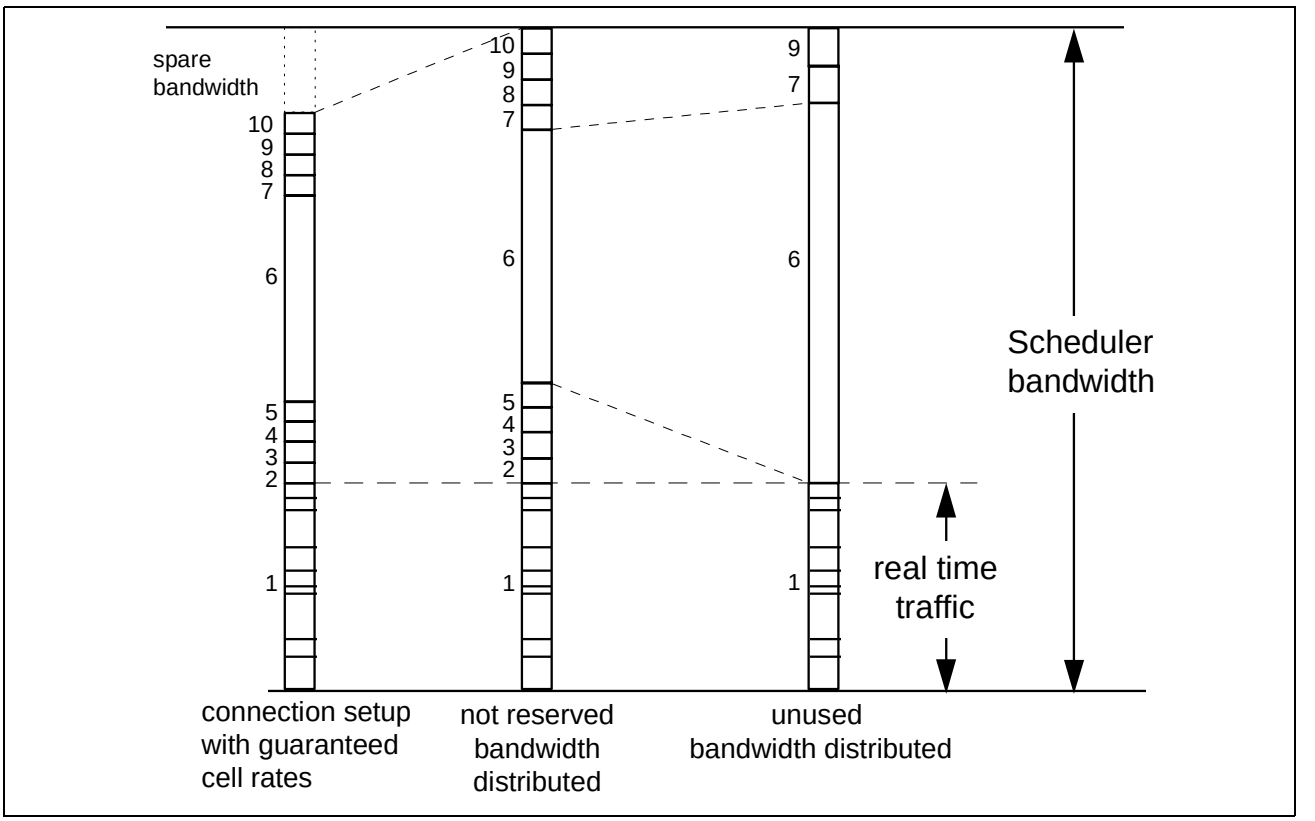


Figure 3-6 Scheduler Behavior Example

The left column in **Figure 3-6** shows the Scheduler load as seen from Connection Acceptance Control (CAC). New connections are accepted as long as their guaranteed rates fit the spare bandwidth of the Scheduler. "Guaranteed rate" is defined below.

The center column shows the case in which all Queues 2..10 are filled; that is, all non-real time connections are sending data. The total non-real-time bandwidth, including the spare bandwidth, is then distributed to the 9 queues according to their weight. In this case, two weight factors are defined, 1 and 10.

The right column shows the case of only three queues (6, 7 and 9) filled; all other connections are not sending data at this time. Again, the available bandwidth is fairly distributed among the queues, still conserving the 1:10 ratio defined by their weights.

Notice that bandwidth of the real-time connections is not affected by bandwidth re-adjustments; but, remains constant over time under the assumption that real-time connections are constantly sending data. If, however, a real-time connection should not use its bandwidth, the bandwidth would be used immediately by the non-real-time connections. The behavior shown in **Figure 3-6** of the WFQ Multiplexer for non-real-time connections has advantages for both the network operator and for the end user:

- The available bandwidth is always used completely, resulting in optimum usage of transmission resources
- A user paying for a higher guaranteed rate also obtains higher throughput under all load conditions.

Guaranteed Rate

The guaranteed rate is the rate which the network must guarantee the user at any time.

Table 3-1 Guaranteed Rates for each Traffic Class

Traffic Class	Guaranteed Rate	Comment
CBR	PCR	
VBR-rt	SCR...PCR	Guaranteed rate can be chosen below PCR for statistical multiplexing gain
VBR-nrt	SCR	
ABR	MCR	
UBR+	MCR	
UBR	none	Guaranteed rate always > 0 with WFQ Multiplexer

3.1.3 Scheduler Usage

The ABM chip allows arbitrary assignment of connections to queues and of queues to Schedulers. A Scheduler can be assigned to any UTOPIA PHY. Usage of a Scheduler differs in switch input (ingress) or output (egress). For the Mini-Switch application (see **Figure 1-5**) the ingress case does not exist.

At a switch output, the Schedulers provide constant cell streams to fill the payloads of the PHYs. Either the entire cell stream of a PHY is provided or it is disassembled into several VPCs as shown in **Figure 3-7**. A VPC may contain both real-time and data connections. This is the case for a VPC which connects two corporate networks (virtual private networks), for example. The Scheduler concept has the advantage that data traffic is automatically adjusted after setup or teardown of a real-time connection. The output rate of a Scheduler in both applications is usually constant.

The Schedulers always react to UTOPIA backpressure or can be controlled completely by backpressure instead of shaping. All Schedulers whose physical outputs are asserting backpressure are hold on serving. Scheduler serving time slots which are lost due to temporary backpressure are maintained and served later, if possible. Therefore, the rate with some CDV will be maintained. The maximum number of stored time slots which can be configured is equal to the maximum burst possible for that port or path.

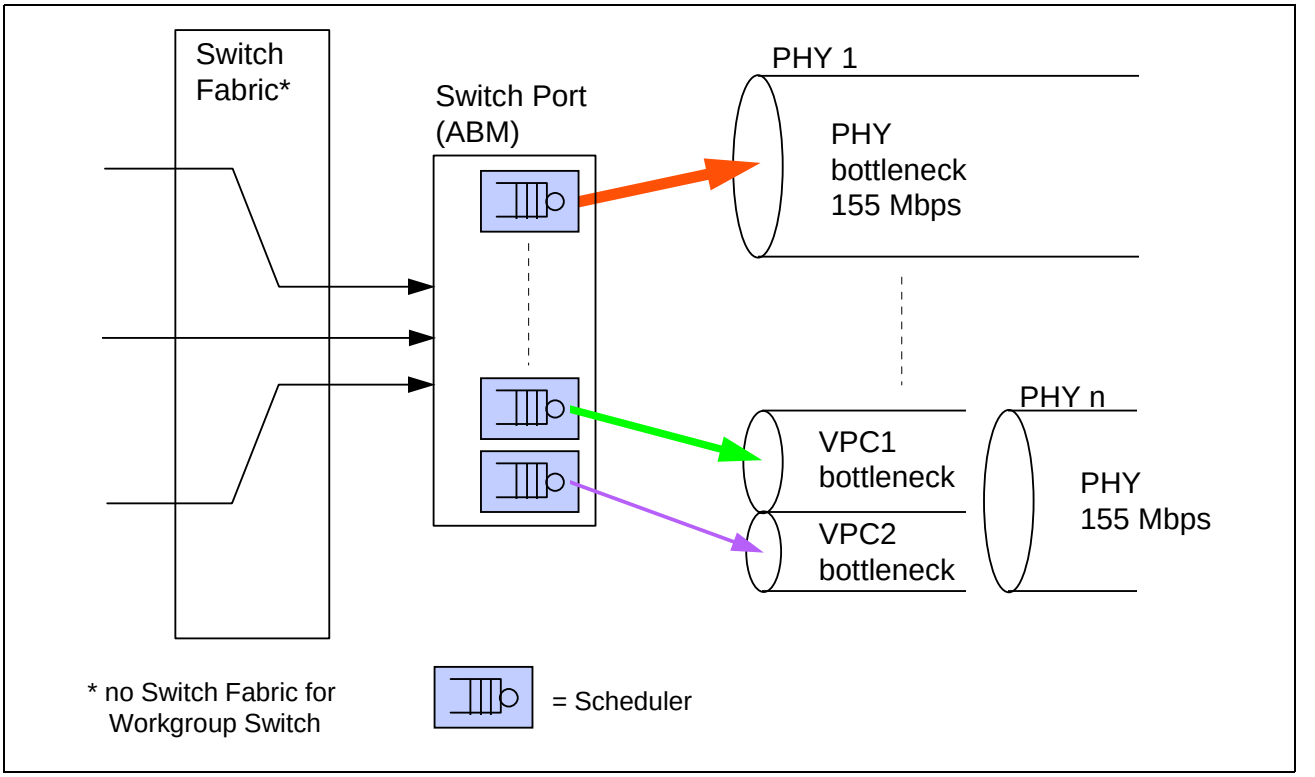


Figure 3-7 Scheduler Usage at Switch Output

At a switch input, each Scheduler is assigned to a switch output (**Figure 3-8**). A switch with **n** ports needs $\mathbf{n^2}$ Schedulers. The output rate of each Scheduler is re-adjusted continuously to obtain maximum switch throughput without overloading the switch port output rate. This principle is called Preemptive Congestion Control, that is, congestion due to overload is avoided.

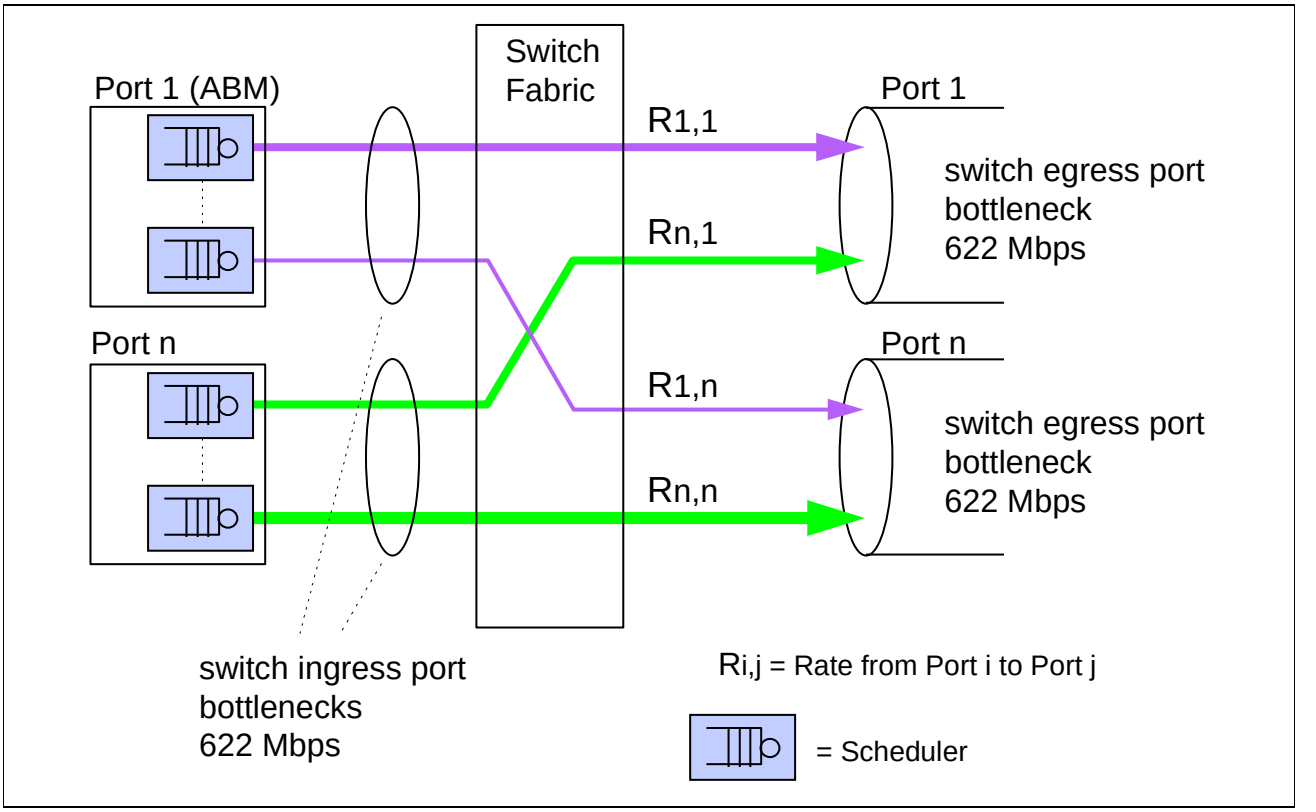


Figure 3-8 Scheduler Usage at Switch Input

There are two options for Scheduler rate adjustment:

- After each connection setup or teardown (static bandwidth allocation).
- Dynamic bandwidth allocation using Input Scheduler Buffer fill information to assign Scheduler rates dynamically.

Note: An algorithm for static bandwidth allocation is available on request.

3.1.4 Quality of Service Class Support

As well as rate guarantees, the support of Quality of Service (QoS) classes is related closely to the threshold-based cell acceptance. One set of thresholds for each QoS class is programmed in the traffic class table (**see also Figure 3-10**). The traffic class table contains the following thresholds:

- Maximum non-real time cells in the entire buffer
- EPD threshold for non-real-time cells in the entire buffer
- The 2-fold threshold
  A) Maximum stored cells in each queue of this traffic class (if EPD disabled)
  or
  B) The EPD threshold for each queue of this traffic class (if EPD enabled)
- The triple threshold
  A) Threshold for each queue of the traffic class where the Congestion Indication (CI) for ABR traffic is set
  and
  B) Threshold where low priority cells (CLP=1) are not accepted (if the CLP transparent flag CLPT is set for the connection)
  C) Queue EPD threshold for GFR (CLPT is false). EPD is triggered if both thresholds 4C and 2 are exceeded.
- Threshold for the maximum number of cells of this traffic class which can be buffered
- The 3-fold threshold for the scheduler occupancy
  A) maximum number of cells in the scheduler if EPD not enabled
  or
  B) EPD threshold for cells in the scheduler if EPD enabled
  or
  C) ABR congestion indication (EFCI, CI) if ABR is enabled

Note: All maximum thresholds are automatically also PPD thresholds, that is, if the maximum fill value is reached, PPD is started if enabled. If PPD is not enabled, cells are discarded if the threshold is reached.

Figure 3-9 shows the independent assignment of queues to traffic classes and Schedulers. Because Schedulers contain the routing function, they must be independent of the QoS class contained in the traffic class table.

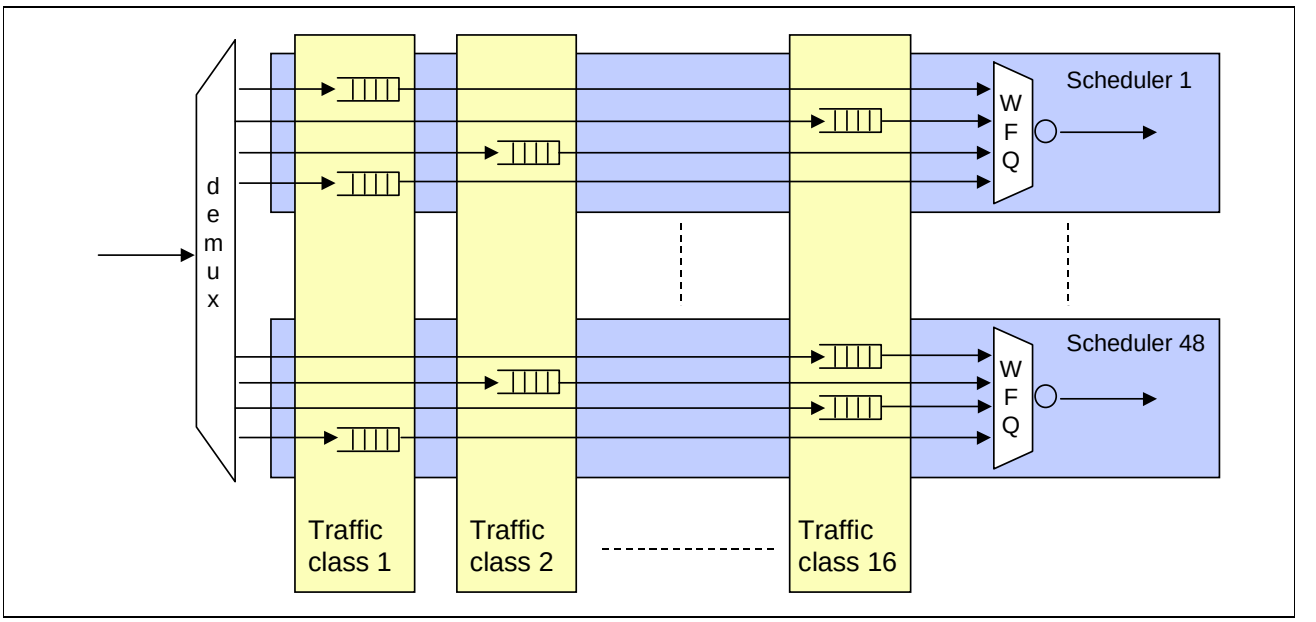


Figure 3-9 Queue Grouping

Examples of traffic classes are

- Real-time traffic
- LAN emulation traffic
- Internet (IP) traffic

Figure 3-10 shows an example of threshold configurations for four traffic classes.

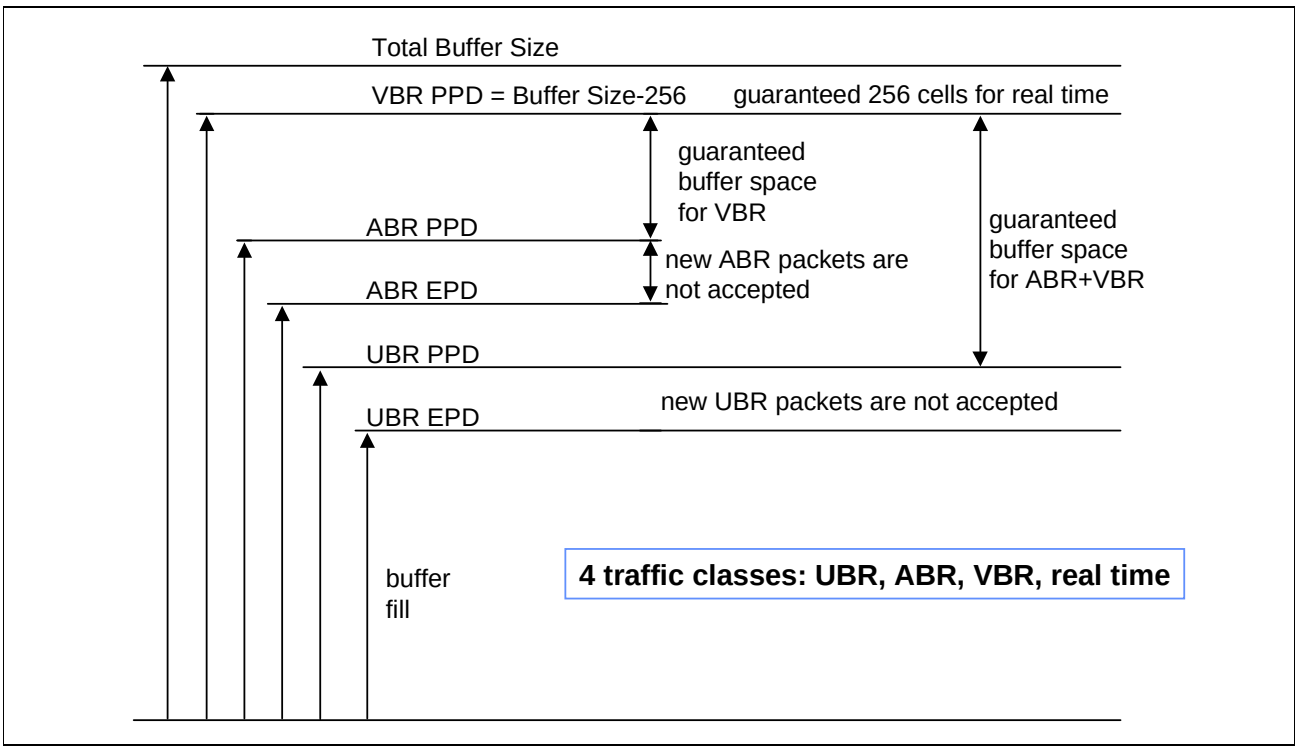


Figure 3-10 Example of Threshold Configuration

3.1.5 EPD/PPD Handling

These functions can be enabled individually per traffic class. The dynamic flags of these functions are stored in the connection specific (LCI) table. For both functions, the ABM looks at the PTI bits of the cells to determine the packet borders of the upper SAR layer.

EPD Threshold Behavior

If the cell fill exceeds an EPD threshold, and EPD is enabled, new packets will not be accepted but will be discarded completely. Cells belonging to packets which have been transmitted partially are accepted.

PPD Threshold Behavior

If the cell fill exceeds a PPD (=max) threshold, the next cell is discarded and, if PPD is enabled, all subsequent cells of the packet are discarded except the last cell. The subsequent cells are discarded even if the cell fill might have dropped below the PPD threshold in the meantime. The last cell is accepted again to convey the discard information to the terminal (cell acceptance is possible only if the queue fill level dropped below the threshold in the meantime). By checking the CRC-32 checksum of AAL5, the terminal can determine rapidly that cells were lost and can immediately ask for retransmission. Otherwise, the terminal would need to wait for a time-out.

3.1.6 Global Thresholds

The following global thresholds are provided:

- Global maximum buffer threshold
  Cells exceeding the threshold will be discarded
- Global maximum threshold for non-real-time cells
- Global congestion indication threshold for ABR
- Global EPD threshold for GFR CLP1 frames (CLPT bit is false)

If the cell fill reaches a maximum threshold, cells are discarded as long as the overflow condition prevails. If the cell fill drops below the maximum threshold, the cells are accepted again immediately.

3.1.7 Scheduler Thresholds

For each upstream direction Scheduler, two individual thresholds can be programmed which are continuously compared by the ABM. The results of all comparisons are provided bit-mapped into microprocessor registers, so that the external controller can rapidly check the fill state of the Schedulers. This feature is provided to enhance the throughput over a switching network by dynamic re-programming of the Scheduler output rates, depending on the actual load. This is more efficient than the static rate adjustment.

3.1.8 Statistical Counters

The ABM chip provides several statistical counters for maintenance purposes.

Global Counters:

- Total stored cells upstream and downstream
- Total stored non-real-time cells upstream and downstream

Per Traffic Class Counters:

- Accepted packets
- Discarded packets or discarded CLP = 1 cells
- Total discarded cells
- Discarded cells due to scheduler overflow
- Discarded cells due to traffic overflow

In addition, two types of sample-hold registers are provided:

- Minimum buffer occupancy value since last readout upstream and downstream
- Maximum buffer occupancy value since last readout upstream and downstream

3.1.9 Supervision Functions

3.1.9.1 Cell Header Protection

To guarantee that the cell header is not corrupted by the external SDRAM, it is protected by a 8-bit interleaved parity octet. It extends over the 5-octet standard header including the UDF1 octet. The BIP-8 octet is calculated for all incoming cells and stored at the place of the UDF2 octet. When a cell is read out, the BIP-8 is calculated again and is compared with the stored BIP-8. In case of a mismatch, an interrupt is signaled and the cell is discarded or not, depending on the configuration.

Note: Due to the usage of the UDF2 field for the BIP-8, the UDF2 octet is not transparent through the ABM.

3.1.9.2 Cell Queue Supervision

The queuing of cells in the ABM is implemented mostly by pointers. To detect pointer errors, the number of the queue in which the cell is stored is appended to the cell in the external cell storage SDRAM. When the cell is read out later, the selected queue number is compared to the QID stored with the cell. In case of a mismatch, an interrupt is signaled.

4 Operational Description

This section describes the ABM from the microprocessor point of view.

4.1 Initialization and Test

These actions are to be performed after reset to prepare the ABM chip for operation.

- Check register Reset salues
- Initialize SDRAM
- Reset internal tables (RAMs)
- Set hardware configuration (UTOPIA configuration)
- Initialize traffic class tables
- Check data path (via adjacent ATM devices)

ABM diagnostic possibilities:

- Check all internal RAMs and register values

4.2 Global Configuration

- Set MODE register
  (Uni-directional Mode or Bi-directional Mode)
- Configure UTOPIA interfaces: mode, number of PHYs
- Set empty rate generator (for SDRAM refresh)
- Set parameter MaxBurstS(3:0), page 6-140 of the output Multiplexer (**Figure 3-1**) and the parameter CDVMAX(8:0), page 6-120 of the Peak Rate Limiter (**Figure 3-1**)
- Set global thresholds
- Programming of Scheduler output rates
- Assignment of Schedulers to PHYs at switch egress side
- Assignment of Schedulers to switch outputs at ingress side

4.3 Connection Setup

To set up a connection, the complete linked list must be established:

LCI → Queue ID → Scheduler and

LCI → Queue ID → Traffic Class

(see **Figure 4-1**). Additionally, the bandwidth and buffer space reservations must be performed (see below). Depending on the traffic class, special functions must be enabled; for example: ABR feedback enable or EPD/PPD for UBR.

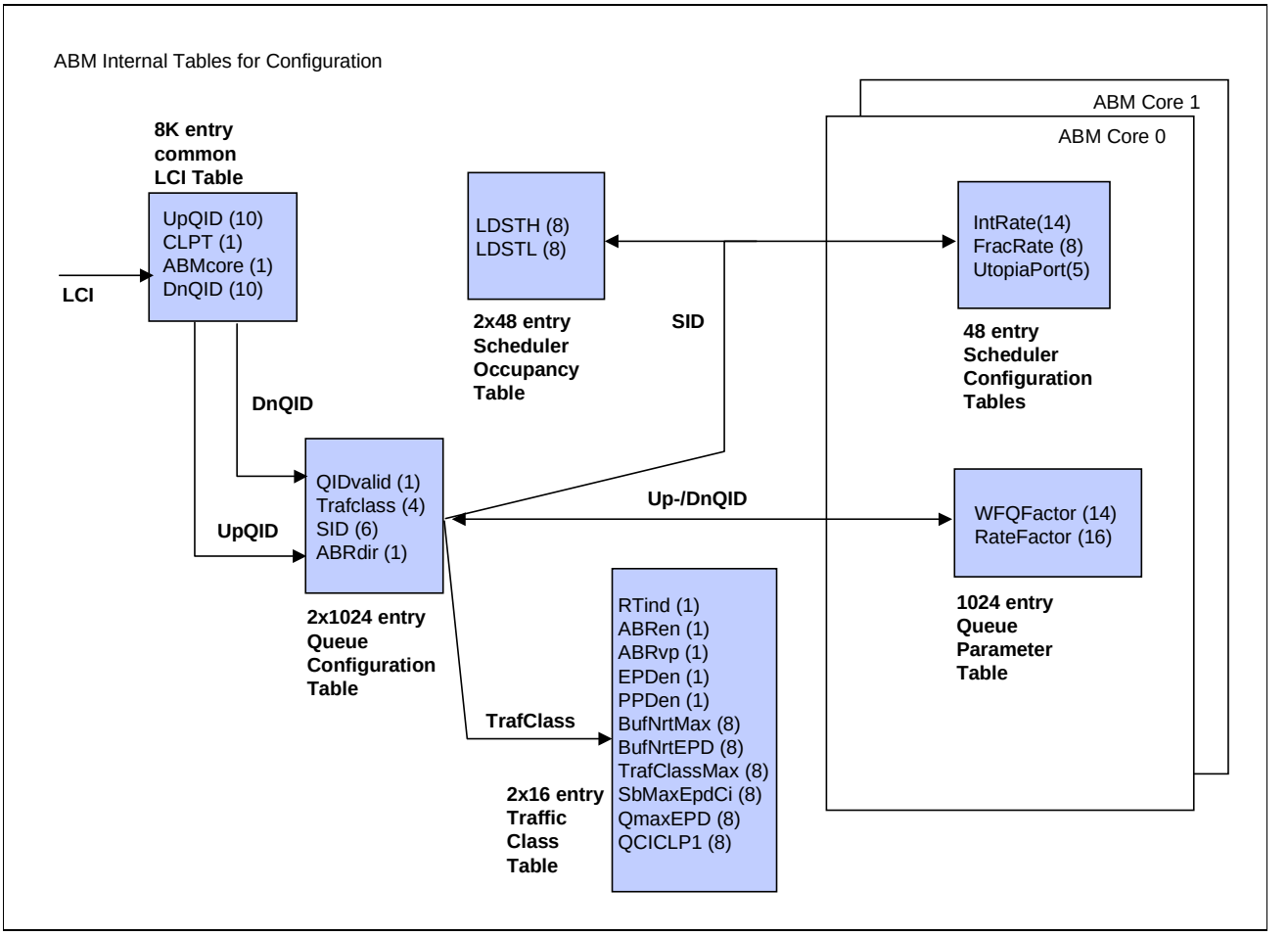


Figure 4-1 Parameters for Connection Setup (Bit width indicated)

Figure 4-1 refers to the following parameters:

Abbreviation	Description	See page
UpQID	Points to queue used for this connection in the upstream direction	6-92
CLPT	If set, the CLP bit of the cells is ignored; not set for GFR, optional for ABR and UBR	6-90
ABMcore	Selects upstream or downstream ABM Core in the Uni-directional Mode	6-90
DnQID	Points to queue used for this connection in the downstream direction	6-90

Abbreviation	Description	See page
QIDvalid	Enables queue; if cleared, cells directed to this queue are discarded and interrupt QIDINV (see 6-149f.) occurs	6-104
TrafClass	Selects the traffic class	6-104
SID	Selects the Scheduler	6-104
ABRdir	Selects the ABM Core in which RM cell update is made for ABR connections	6-104
LDSTH	High threshold for Scheduler occupancy in steps of 256	6-108
LDSTL	Low threshold for Scheduler occupancy in steps of 256	6-108
IntRate	Integer part of incremental value for Scheduler output rate	6-137
FracRate	Fractional part of incremental value for Scheduler output rate	6-131
UtopiaPort	Specify UTOPIA port for this scheduler	6-137
WFQFactor	Weight of multiplexer input in 15,360 steps	6-129
RateFactor	Select value of peak rate limiter	6-128
RTind	Real-time queue indication; set to zero for WFQ queue	6-98
ABRen	If set, EFCI marking is enabled	6-98
ABRvp	(ABR service category) relating to the VP or to the individual VC, respectively; If set, congestion is indicated via VP RM cells (F4 flow)	6-98
EPDen	If set, EPD is enabled	6-98
PPDen	If set, PPD is enabled	6-98

Abbreviation	Description	See page
BufNrtMax	Defines maximum number of non-real-time cells allowed in the entire buffer for this traffic class in steps of 256	6-95
BufNrtEPD	Defines threshold for EPD/maximum[1)] for this traffic class for the entire buffer in steps of 256	6-95
TrafClassMax	Defines maximum number of cells for this traffic class in steps of 256	6-98
SbMaxEpdCi	Defines threshold for EPD/maximum[1)] for this traffic class in the Scheduler in steps of 256	6-98
QueueMaxEPD	Defines threshold for each queue for EPD/maximum[1)] for this traffic class in steps of 64	6-95
QueueCICLP1	Combined threshold for each queue for CI indication (ABR) and CLP=1 cell discard in case of CLPT=0 in steps of 4	6-95

1) mixed threshold: EPD if enabled; otherwise, maximum threshold

4.4 Setup of Queues

Before assigning a connection to a new queue, it should be verified to be empty, as some cells could remain from the previous connection (see **Section 4.5**).

4.5 Teardown of Queues

Disabling a queue via the queue-disable bit does not clear the cells contained in the queue, but:

- The acceptance of the queue for new cells is disabled
- The queue is still served, but the cells are discarded

Normally, at the time a queue is cleared, there will be no more cells in the queue. This can be checked by reading the queue length.

In case of a highly filled queue which is served slowly, the time to empty the queue could be long. To deplete the queue more quickly, its weight can be increased temporarily. However, because the discarded cells produce idle times on the UTOPIA output, the chosen weight factor should not be too high.

4.5.1 ABM Configuration Example

In this section, a popular mini-switch scenario (**Figure 4-2**) is used to describe the most important points for the software configuration of the ABM. Among other things, the following fixed assignments can be made in software by the user:

- Assignment of Schedulers to PHYs and programming of Scheduler output rates
- Definition of the necessary traffic classes
- Assignment of the queues to the traffic classes
- Assignment of the queues (QIDs) to the Schedulers (SIDs)

Assignment of Schedulers and Programming Output Rates:

The ABM has 96 Schedulers (48 in the upstream direction and 48 in the downstream direction). Each ADSL device is assigned to a separate Scheduler (this guarantees each ADSL device a 6-Mbit/s data throughput without bandwidth restrictions caused by the other ADSL devices); then, 95 ADSL devices can be connected. The 96th Scheduler will be occupied by the E3 uplink to the public network. The assignment of the Schedulers to the PHYs is totally independent and even such a strong asymmetrical structure as in (**Figure 4-2**) can be supported. The output rates of the Schedulers must be programmed in such a way that the total sum does not exceed 622 Mbit/s (payload rate). From the example, the following result is derived: 95 x 6 Mbit/s + 1 x 34 Mbit/s = 604 Mbit/s ≤ 622 Mbit/s.

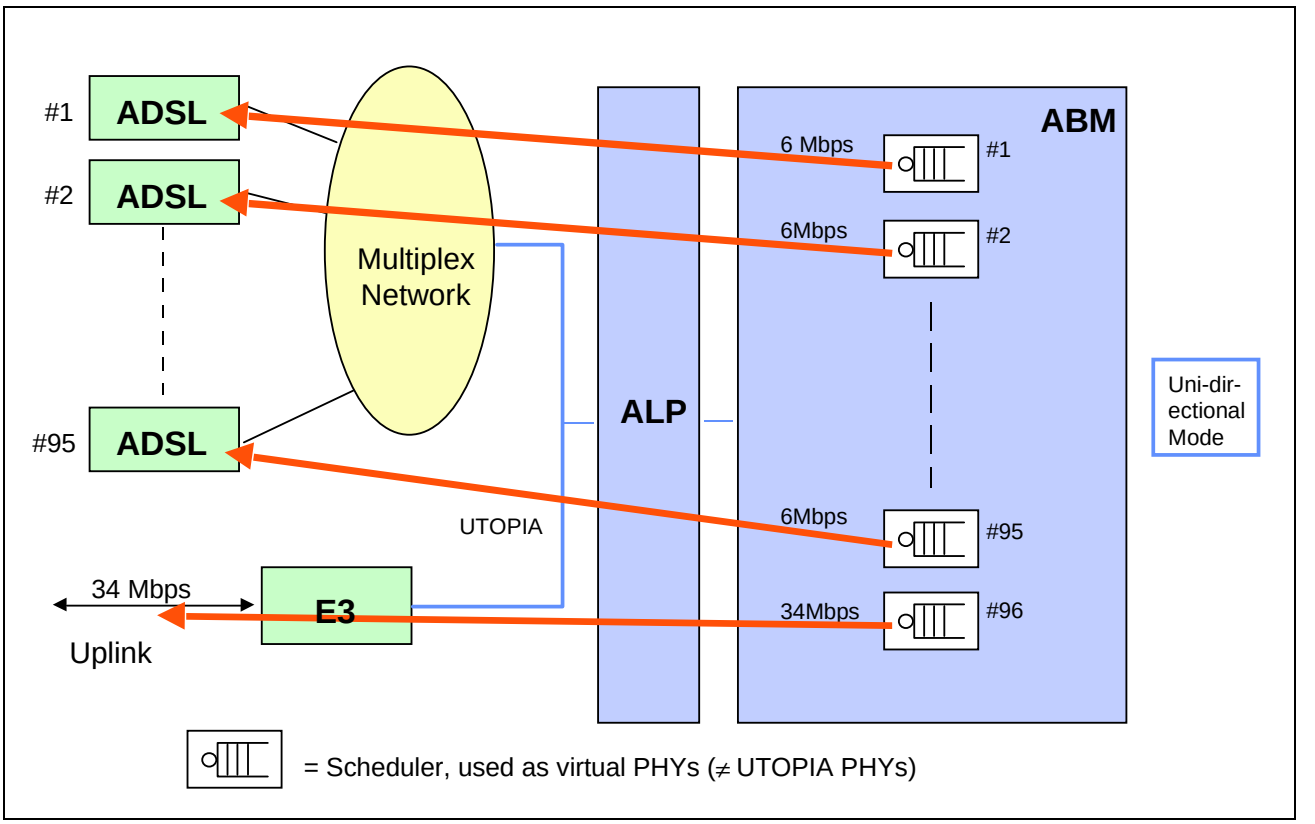


Figure 4-2 ABM Application Example: DSLAM

Definition of Necessary Traffic Classes:

The ABM allows up to 16 traffic classes to be defined by Traffic Class Table RAM entry via the registers TCT0 and TCT1, page 93. In this example, there are 3 traffic classes:

- CBR (real-time) = traffic class 1
- GFR (non-real-time) = traffic class 2
- UBR (non-real-time) = traffic class 3

Assignment of the queues to the traffic classes:

Each queue must relate to a defined traffic class according to the Queue Configuration Table RAM entry via the TrafClass(3:0) bits of the register QCT1, page 6-104.
Figure 4-3 shows that each queue belongs to one of the traffic classes 1..3; for example, Queue 1 belongs to Traffic Class 1, Queue 2 to Traffic Class 2 (just as for Queue 3) and Queue 4 corresponds to Traffic Class 3.

Assignment of the Queues (QIDs) to the Schedulers (SIDs):

Every Scheduler possesses a certain number of queues depending on the assignment by the user of the SID(5:0) bits of register QCT1, page 6-104. In the example, every ADSL device has four data connections so that four queues per Scheduler are necessary. Each Scheduler of the ABM has one real-time queue and an arbitrary number of non-real-time queues. For Schedulers #1..#95, indicate that the first queue belongs to Traffic Class 1, the 2nd and 3rd Queue to Traffic Class 2, and the 4th Queue to Traffic Class 3. There are 380 (1..380) queues altogether for Schedulers #1..#95. The 96th scheduler must be able to serve the 95 ADSL devices (95 Schedulers and appropriate queues). Thus, Scheduler #96 has 95 x 2 = 190 non-real-time queues as every Scheduler from #1..#95 possesses two GFR non-real-time queues (GFR has a guaranteed minimum rate; thus, each GFR queue needs a per VC queueing). The 95 UBR queues of Schedulers #1..#95 need only one UBR queue at the 96th Scheduler as UBR has no guaranteed minimum rate. As every Scheduler has only one real-time queue, the 95 real-time queues from Schedulers #1..#95 flow into the one real-time queue of Scheduler #96. Therefore, Scheduler #96 needs the assignment of 190 (GFR) + 1 (UBR) + 1 (CBR) = 192 queues (only the queue with QID = 400 corresponds with Traffic Class 1).

In **Figure 4-3** the first queue starts with QID = 400 and not with QID = 380 because this makes it easier to recognize the number of queues belonging to Scheduler #96 (also, it shows that the assignment is arbitrary within the given borders (only 1023 queues = QID 1..1023 per ABM Core exist)). The restriction of 1023 queues maximum per ABM Core must be met. The example (**Figure 4-3**) fulfills this condition:

a) Upstream ABM core:
   192 queues (≤ 1023 queues!) are used
b) Downstream ABM core:
   380 queues (≤ 1023 queues!) are used

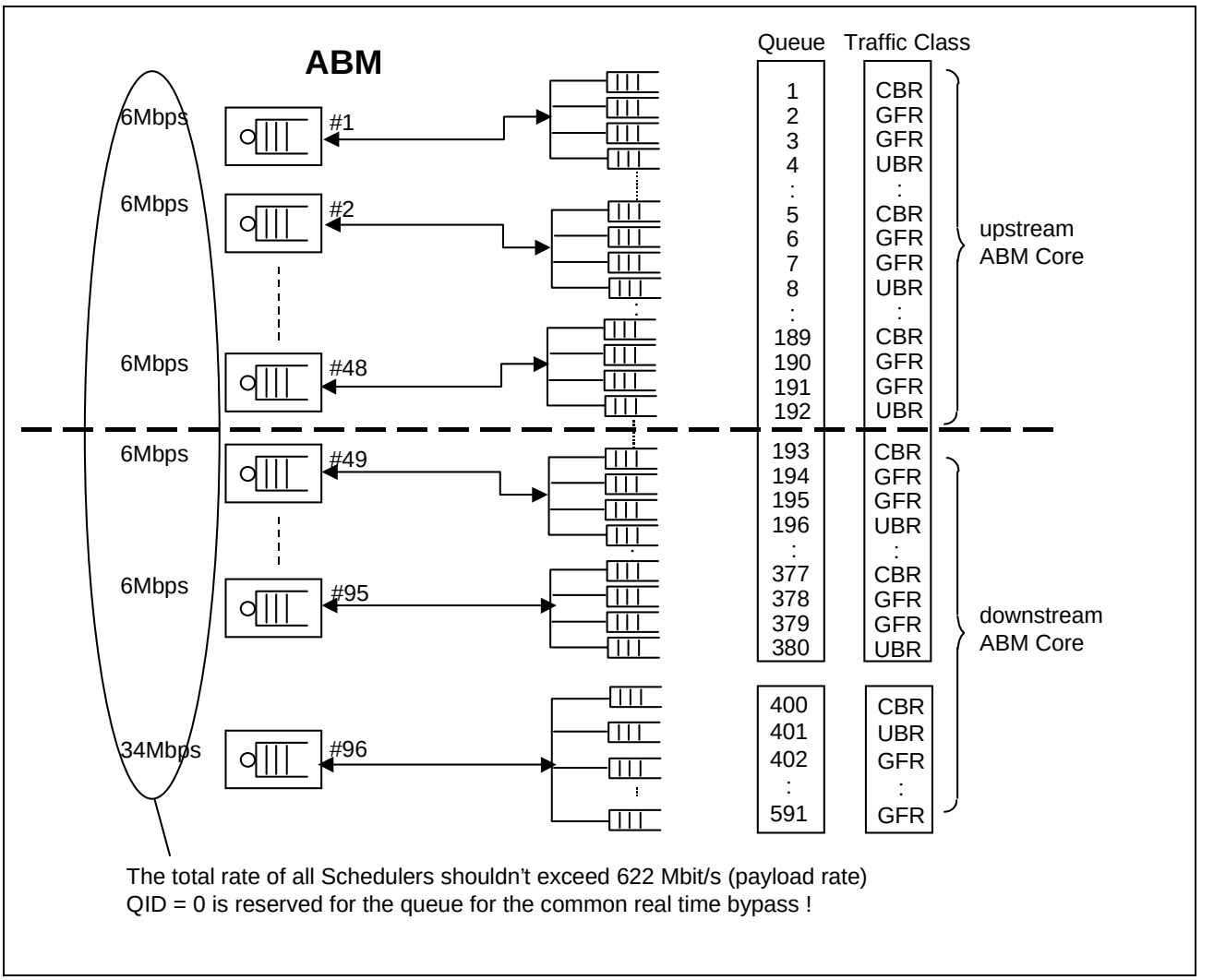


Figure 4-3 ABM Configuration Example: DSLAM

4.6 Normal Operation

In normal operation, no microprocessor interaction is necessary as the ABM chip does all queuing and scheduling automatically. For maintenance purposes, periodically the microprocessor could read out the counters for buffer overflow events. Some overflow events may also be programmed as interrupts.

The only instance of permanent microprocessor interaction is operation of the dynamic bandwidth allocation protocol. In this case, the microprocessor must permanently check the two fill thresholds of the upstream Schedulers and adjust their output rates accordingly.

In case of static bandwidth allocation, all rate adjustments are made only at connection setup or teardown.

4.7 Bandwidth Reservation

Due to the WFQ Scheduler concept of the ABM, the Connection Acceptance Check (CAC) is very simple:

- Check if the Guaranteed Rate of the connection fits within the spare bandwidth of the Scheduler.

For the definition of the Guaranteed Rate, see **Table 3-1.** Mathematically, the CAC can be reduced to the following formulas:

For all connections, verify that the Scheduler is not overbooked:

$$\textbf{Sum of Guaranteed Rates} \leq \textbf{Scheduler output rate} \qquad \textbf{(1)}$$

For real-time connections, (CBR, VBR-rt) in equation **(1)** is the only condition required.

For non-real-time connections or connections using the WFQ Multiplexer, additional conditions must be fulfilled.

VBR, ABR and UBR+ connections must be setup in per-VC queuing configurations, that is, an empty queue must be found for the connection. The Guaranteed Rate determines the weight of the queue:

$$n_i = \mathrm{INT}\left[\frac{GRmin}{GR} \times 2^{14}\right] \qquad \textbf{(2)}$$

with

- $n_i \in \{1, 2, 3, ...15360\}$ is the WFQ factor for the connection i
  ($1/n_i$ is the weight factor W_i)

GR_{min} the defined constant defining the minimum rate to be guaranteed

Note: n_i with a maximum value of 15360 due to hardware limitations.

Note: In addition to the hardware related tasks, a key system constant must be pre-defined: the minimum Guaranteed Rate GR_{min}. This parameter provides an absolute value to the relative weight factors of the WFQ Multiplexers. It is usually identical for all Schedulers in a system, as the Guaranteed Rate is related to the service classes - and these are identical for all users, independent of where they are connected to a network.

- INT(x) the integer part of x.

The integer function in equation **(2)** selects the next smaller value of the integer n, that is to say, the weight factor is higher than required and, thus, the queue is served slightly faster in order to guarantee the rate.

For UBR connections without any rate guarantee, the following procedure is appropriate for the WFQ Multiplexer:

- Reserve one queue per Scheduler for all UBR connections

- Assign minimum weight factor to this queue
- Take the bandwidth of the queue into account using formulas **(1)** and **(2)** as if for a non-real-time connection
- Assign UBR connections to this queue without any further CAC

Note: EPD/PPD functionality is offered by the ABM on a per-VC basis. Hence, these functions can be supported also for UBR connections sharing one queue.

Note: In addition to the bandwidth reservation, buffer space must be assigned by the appropriate setting of thresholds.

4.7.1 Bandwidth Reservation Example

As an example, an access network multiplexer is assumed with ADSL lines and an E3 uplink. CBR and UBR+ connections are supported. A minimum Guaranteed Rate of GR_{min} = 19.2 kbit/s is selected. This allows GR up to 314.57 Mbit/s with increasing granularity for higher values.

This behavior is well suited to the Guaranteed Rates which are minimum or sustainable rates. The values for MCR and SCR will be well below 10 Mbit/s for public networks. In high speed LANs with high MCR and SCR values, a higher minimum rate could be selected.

Additionally, it is assumed that three types of line interfaces (PHY) exist in the system: 34 Mbit/s for the uplink, ADSL rates of 8 Mbit/s downstream, and 0.6 Mbit/s upstream. For each PHY, a maximum possible weight factor 1/n exists: n_{max} = 9, n_{max}= 39, and n_{max} = 524, respectively.

Two types of non-real-time connection are defined with Guaranteed Rates of 100 kbit/s and 20 kbit/s with the weight factors 1/n, n_{100} = 3146 and n_{20} = 15730, respectively. The 100 kbit/s connections would be used for the downstream direction, and the 20 kbit/s connections for the upstream direction. **Table 4-1** provides the maximum number of connections possible on each PHY.

Table 4-1 Number of Possible Connections per PHY

PHY	GR = 100 kbit/s	GR = 20 kbit/s
34 Mbit/s	349	1747
8 Mbit/s	80	403
0.6 Mbit/s	6	30

For example, if the maximum number of connections for each Subscriber is fixed (such as 5 data connections), the queues can be pre-configured for each Subscriber so that only the LCI assignment must be changed when a connection is setup or released.

4.8 Programming of the Peak Rate Limiter / PCR Shaper

For each queue, an optional peak rate shaper can be programmed. The possible peak rate values can be determined with:

$$\mathbf{r} = \frac{\mathbf{rmin}}{\mathbf{m}} \times \mathbf{2^{16}} \quad \textbf{[cells/s]} \qquad \textbf{(3)}$$

with

- m ∈ {1, 2, 3, ...63488} the rate factor
- rmin depending on the total throughput, i.e. the clock frequency:

$$\mathbf{rmin} = \frac{SYSCLK}{\mathbf{2^{19}}} \ \textbf{[cells/s]} \qquad \textbf{(4)}$$

4.9 Scheduler Output Rate Calculation Example

The parameters of the Schedulers must be chosen in relation to the transmission rates of the PHYs, respectively. That means for a Scheduler which transmits in the upstream direction such as 150 Mbit/s output rate and for a Scheduler which transmits in the downstream direction such as 6 Mbit/s output rate for a ADSL device (as depicted in **Figure 4-2**). Within the ABM, the Scheduler output rate is represented by the two parameters: IntRate(14:0), page 73 and FracRate(7:0), page 70. These parameters are without dimension and thus only indirectly represent the output rate. The following part declares how to derive the two parameters by a time parameter T and the correlation between these parameters and the output rate R:

$$\mathbf{T} = \frac{SYSCLK}{32\ cells^{-1} \times R} \quad \textbf{[without dimension]} \qquad \textbf{(5)}$$

with

- ABM core clock SYSCLK = [1/s]
- Scheduler output rate R = [cells/s]

$$\mathbf{IntRate} = \ int(T) \qquad \textbf{(6)}$$

with

- int(T) is integer part of T

$$\mathbf{FracRate} = \{T - int(T)\} \times 256 + 1 \qquad \textbf{(7)}$$

Example:

Chosen values: R_0 = 347000 cells/s (150 Mbit/s), SYSCLK = 50 MHz

with (5)⇒

$$T_0 = \frac{50 \times 10^6}{32 \times 347000} = 4.50288\ldots$$

thus with (6) and (7)⇒

IntRate = 4 and **FracRate** = 130 (rounded up)

Because of rounding the FracRate value, the effective scheduler rate R needs to be calculated by solving equation (7) to T and equation (5) to R:

⇒

$$T = \frac{130 - 1}{256} + \mathrm{IntRate}[T_0] = 4.5039\ldots$$

and

$$R = \frac{50 \times 10^6}{32 \times 4.5039\ldots}\mathrm{cells}^{-1} = 346921\mathrm{cells}^{-1}$$

4.10 Empty Cell Rate Calculation Example

The internal SDRAM refresh generator uses empty cell cycles to perform its refresh cycles. Thus the refresh function is closely related to the scheduler output rate configuration. The empty cell rate generator guarantees a minimum number of empty cell cycles required for refresh cycles. A maximum value for parameter T can be derived by the following term:

$$T_{max} = \frac{SYSCLK \times RefreshPeriod}{32 \times RefreshCycles} \quad (8)$$

with:

- ABM core clock SYSCLK = [1/s]
- SDRAM RefreshPeriod = [s]
- SDRAM RefreshCycles requirement

The empty cell rate parameter definition for fractional and integer parts of T is according to equations (5) and (6).

Example:

Given values: RefreshPeriod = 64ms, RefreshCycles = 4096, SYSCLK = 50 MHz

$\Rightarrow T_{max} = 24.414$

Thus the value of T that is represented by programmed device parameters IntRate and FracRate according to equations (6) and (7), must be less or equal to T_{max} to guarantee sufficient refresh cycles according to the SDRAM specification.

In case of additional bandwidth needs to be reserved (e.g. for multicast operation in subsequent devices), a second maximum condition for parameter T can be derived depending on the empty cell rate required for multicast bandwidth reservation. In this case the value of T must conform the following equation:

$$T = Min\{T_{equation(5)}, T_{MCreservation}, T_{max}\} \quad (9)$$

4.11 Traffic Classes

4.11.1 CBR Connections

These connections should use the real-time bypass of the respective Scheduler. However, if two priority levels for real-time connections must be offered, a slightly lower real-time performance can be achieved by using the WFQ Multiplexer with maximum weight.

In this case, the bandwidth must fit into the WFQ Multiplexer (conditions **(1)** and **(2)** in **"Bandwidth Reservation" on page 4-56**).

4.11.2 VBR-rt Connections

These connections can be treated like CBR connections with a guaranteed cell rate less than or equal to the Peak Cell Rate (PCR). Depending on the behavior of the sources, a statistical benefit could be obtained by reserving less than PCR.

As an example, assume 1000 connections with compressed voice are multiplexed on a link. PCR is 32 kbit/s, but on average only 16 kbit/s. SCR is 8 kbit/s. Hence, instead of reserving 32 Mbit/s for the ensemble of connections, only 16 Mbit/s must be reserved. The large number of connections guarantees that the mean sum rate of 16 Mbit/s is never exceeded.

4.11.3 VBR-nrt Connections

For these connections, the three parameters PCR, SCR, and MBS are given. One queue is reserved for each VBR-nrt connection with SCR programmed as the weight of the respective Scheduler queue. The maximum queue size is set to MBS plus ~100 cells for cell level bursts. If the buffer space reserved for VBR-nrt connections is set to the sum of all MBS, it is guaranteed that no cell is lost. However, with a large number of VBR-nrt connections, the total reserved buffer can be smaller with a negligible number of cell losses.

For the PCR, no adjustment is necessary as the rates of the queues of a Scheduler always adjust automatically to the maximum possible values. As an option for network endpoints, the PCR may be shaped. The output rate of each queue may be limited individually to a programmable value which results in PCR shaping. This could be useful at points where a connection leaves one network and enters the next network which might police the connection (NPC function).

4.11.4 ABR Connections

ABR connections must be setup in per-VC queuing configuration. The queue is assigned a weight guaranteeing the MCR of the connection.

A backward direction connection must be setup. In Bi-directional Mode, the same queue ID must be chosen in order to make the ABR functions work properly.

In Uni-directional Mode, the queue ID value with the toggled LSB must be setup for the backward direction. EFCI marking in forward data cells or CI/NI marking in backward RM cells can be enabled per traffic class.

*Note: Also the LCI is toggled in the Uni-directional Mode (see **"LCI Translation in Mini-Switch Configurations" on page 1-27**).*

4.11.5 UBR+ Connections

UBR+ connections are UBR connections with MCR. They must be setup in individual queues with the weight factor guaranteeing the MCR.

To enhance the overall throughput, the EPD/PPD function is enabled.

4.11.6 GFR Connections

GFR Connections are setup like UBR+ connections with a Guaranteed Rate in individual queues, with the weight factor guaranteeing the rate for the high-priority packets. The threshold for the discard for low-priority packets must be set accordingly.

4.11.7 UBR Connections

As described in **"Bandwidth Reservation" on page 4-56,** one queue per Scheduler is reserved for UBR connections with the smallest weight assigned. All UBR connections share this queue. EPD/PPD can be enabled as the relevant parameters are stored per connection (LCI table).

5 Interface Descriptions

5.1 UTOPIA Interfaces

The ABM has one UTOPIA Receive Interface and one UTOPIA Transmit Interface with Master capability at the PHY side and one Receive Interface and one Transmit Interface with Slave capability at the ATM side (**Figure 5-1**). The interfaces are compliant with the UTOPIA Level 1 and 2 Specification [1, 2] including:

- Bus width is selectable as either 8 bit or 16 bit
- Frequency ranges from 19... 52 MHz
- Single-PHY or multi-PHY configurations are supported
- PHY number enhancement option of UTOPIA Level 2 Appendix 1 is supported.

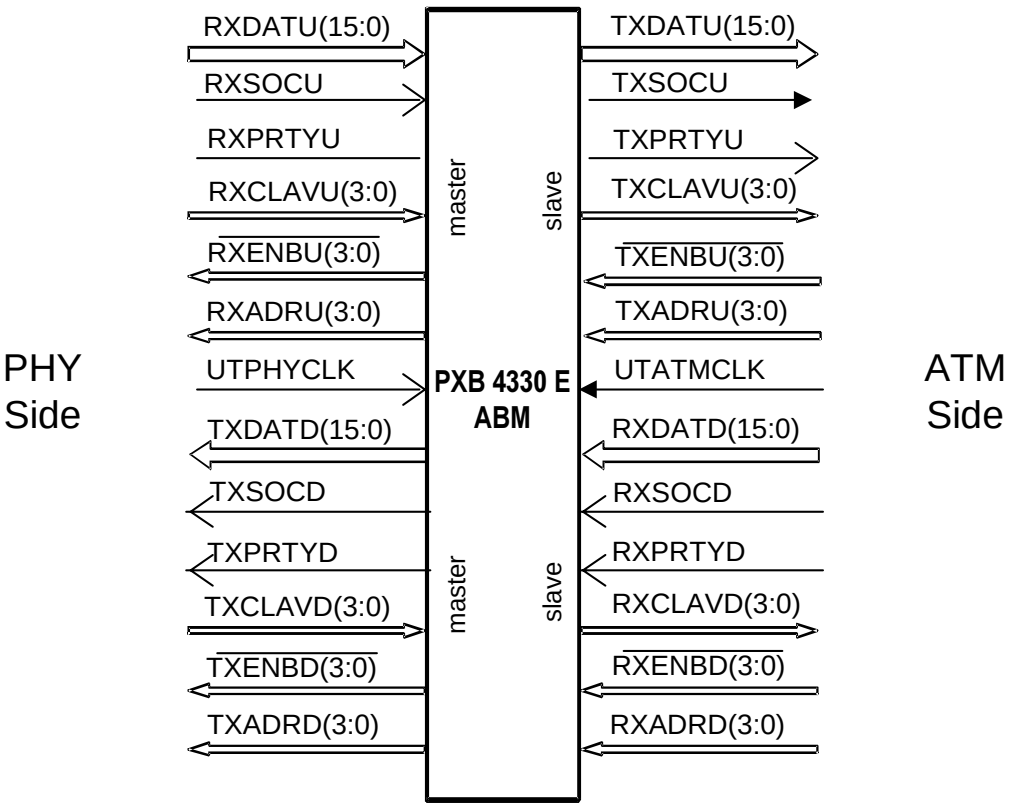


Figure 5-1 UTOPIA Interfaces

The UTOPIA Receive and transmit Interfaces from the ATM and PHY sides operate from one clock which may be completely independent from the main chip clock SYSCLK. The UTOPIA clock frequency must be less than or equal to the main chip clock SYSCLK.

The UTOPIA Interface has both 8-bit and 16-bit options. The 16-bit option features the 54-octet cell format for the standardized format, shown in **Table 5-1**, or the proprietary format, shown in **Table 5-2**. The 8-bit format has 53 octets without the UDF2 octet. The

ATM side and PHY side UTOPIA Interfaces can be configured independently in either the 8-bit or the 16-bit mode.

Note: Octet UDF2 is internally used for BIP8 supervision.

Table 5-1 Standardized UTOPIA Cell Format (16-bit)

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	VPI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	UDF1								UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
:	:								:							
26	Payload Octet 47								Payload Octet 48							
word																

Note: All Fields According to Standards, Unused Octets Shaded

Table 5-2 Proprietary UTOPIA Cell Format (16-bit)

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LCI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	LCI(13:12)		HK(2:0)			PN(2:0)			UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
:	:								:							
26	Payload Octet 47								Payload Octet 48							
word																

Note: PN(2:0) = Port number for PXB 4220 IWE8 (don't care for ABM)
HK(2:0) = Housekeeping bits (for Internal Continuity Check (ICC) only)
LCI(13:0) = Local Connection Identifier
all other fields according to standards.

5.1.1 UTOPIA Multi-PHY Support

To support multi-PHY configurations with or without use of the UTOPIA PHY address, the Infineon ATM switching chip set supports the Appendix 1 option of the UTOPIA Level 2 Standard [2]. It allows the simultaneous polling of up to four groups of PHYs by using four CLAVx/ENBx signal pairs (x=0..3).

During the transfer of a cell, the Master UTOPIA Interface polls 12 PHY addresses. The 27 clock cycles time for the transfer of a cell in 16-bit UTOPIA format allows polling of 12 PHY addresses and selection of one of them for the next cell transfer. The Receive and Transmit UTOPIA Interfaces always poll separately. To allow support of more than 12 PHYs, four pairs of CLAVx/ENBx lines are provided in all Infineon ATM switching chips with UTOPIA Interfaces. However, although 48 PHYs could be polled by this configuration, up to 24 PHYs only are supported.

Note: The number of line interfaces (PHYs) to be supported by an ATM Layer chip basically depends on the number of its UTOPIA queues. The term 'PHY device', however, denotes 'PHY chips'" which may contain more than one PHY. For electrical load considerations, the number of PHY devices is important, as the standard requires that for a 25 MHz clock, a minimum of eight PHY devices must be driven; for a 50 MHz minimum, four PHY devices must be driven.

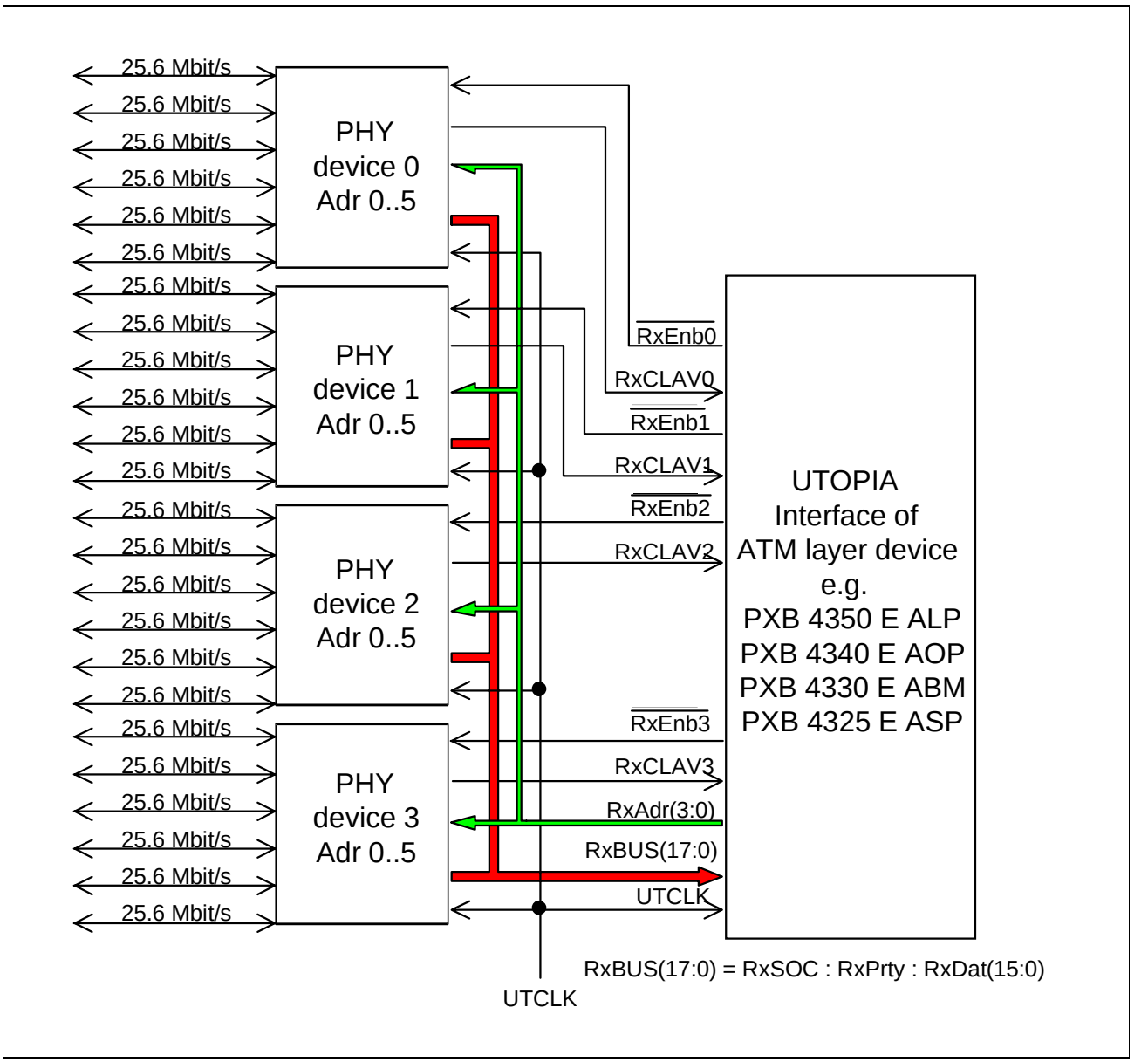


Figure 5-2 Upstream Receive UTOPIA Example: 4 x 6 PHYs

The four CLAVx/$\overline{\text{ENB}}$x lines are connected one-to-one to different PHY devices, as shown in the example of **Figure 5-2** for the upstream receive side of an ATM Layer chip connected to four PHY devices, each containing six PHYs of 25.6 Mbit/s. In this example, 24 PHYs, the maximum number, are connected.

In the example of **Figure 5-2**, the ABM gets four CLAVx signals with each polled address. All PHY devices have the addresses 0..5 assigned to their PHYs. The upper six addresses (6..11) always deliver CLAVx = 0 when polled. To distinguish the PHYs, the UTOPIA Interface of the ABM chip adds offset numbers 6, 12, and 18, to the PHY numbers from PHY Devices 1, 2, and 3, respectively. Then within the ATM Layer device, the PHY numbers range from 0..23 without ambiguity.

Two other multi-PHY modes with UTOPIA addresses are selectable. One additional mode is provided to connect Level 1 PHY chips without address inputs. All modes are summarized in **Table 5-3**.

Table 5-3 UTOPIA Polling Modes

	Mode 2 x 12	Mode 3 x 8	Mode 4 x 6	Level 1 Mode
$\overline{\text{ENB0}}$ / CLAV0	0	0	0	0
$\overline{\text{ENB1}}$ / CLAV1	12	8	6	0
$\overline{\text{ENB2}}$ / CLAV2	do not connect	16	12	0
$\overline{\text{ENB3}}$ / CLAV3	do not connect	do not connect	18	0

Note: The numbers 0, 6, 8, 12, 16 and 18, indicate the Offset added to the PHY number.

- In Level 1 Mode, the PHY numbers are identical to the CLAV/$\overline{\text{ENB}}$ group: 0, 1, 2, 3.
- The user must program the PHY numbers in such a way as to avoid ambiguous PHY numbers inside the ATM Layer device.
- Mode selection can be done independently for the PHY side and the ATM side UTOPIA interfaces.
- If 12 PHYs or fewer are to be polled, Mode 2 x 12 should be used with only the CLAV0/$\overline{\text{ENB0}}$ pair connected. This minimizes the interconnection lines between the chips.
- The enabling of the PHYs is done with a 24-bit bitmap for each UTOPIA Interface. Polling at the Master Interface always extends over the 4 CLAV/$\overline{\text{ENB}}$ pairs and over all 12 addresses. After conversion to the internal PHY number, the ports not enabled are masked out and one of the available PHYs is selected in a fair way.

Examples:

1. One PHY device, such as 622 Mbit/s PHY:
   16-bit bus width, address lines unconnected, RxCLAV0/$\overline{\text{RxEN0}}$ and TxCLAV0/$\overline{\text{TxEN0}}$ signal pairs connected, all other CLAVx/$\overline{\text{ENB}}$x pairs unconnected.
2. Four PHY devices, 155.52 Mbit/s PHYs: 16-bit bus width, address lines unconnected, all four CLAVx/$\overline{\text{ENB}}$x pairs connected, one to each PHY device.
3. Four PHY devices of 6-fold 25.6 Mbit/s PHYs:
   16-bit bus width, address and all four CLAVx/$\overline{\text{ENB}}$x pairs connected, one to each PHY device (**see Figure 5-2**).
4. Three PXB 4220 IWE8s:
   8-bit bus width, address bus unconnected, three CLAVx/$\overline{\text{ENB}}$x pairs connected, one to each IWE8 (this mode requires the PXB 4350 E ALP).

5.2 RAM Interfaces

The ABM chip uses external, synchronous, dynamic RAM (SDRAM) for the storage of ATM cells and external, synchronous, static RAM (SSRAM) for the storage of cell pointers. Two SDRAM Interfaces and one SSRAM Interface are provided. Each of the two SDRAM Interfaces is associated with one of the ABM Cores. The SSRAM Interface is shared by both ABM Cores. All RAM Interfaces are operated with the system clock of up to 52 MHz.

The size of the SDRAMs is fixed to 32 Mbit per ABM Core; but, the size of the SSRAM depends on the required cell store size:

Table 5-4 External RAMs

Cell Store Size		SDRAM Size		SSRAM Size
Upstream	**Downstream**	**Upstream**	**Downstream**	**Common**
64K cells	64K cells	32Mbit	32Mbit	128K × 16bit
32K cells	32K cells	32Mbit	32Mbit	128K × 16bit
16K cells	16K cells	32Mbit	32Mbit	128K × 16bit
64K cells	0	32Mbit	none	64K × 16bit
32K cells	0	32Mbit	none	32K × 16bit
16K cells	0	32Mbit	none	16K x 16bit

The following pipelined SSRAM types are possible:

1. 2M RAM 128K×16 bit,
   for example: Micron MT58LC128K18 Pipelined or Samsung KM718V789/L
2. 4M RAM 128K×32/36 bit with only 16 data bits connected
3. 2M RAM 64K×32 bit,
   for example, Toshiba TC55V2325 with only 16 data bits connected
4. 1M RAM 32K×32 bit with only 16 data bits connected
5. 1M RAM 64K×16 bit.

For the SDRAM, the Infineon 16 M type HYB39S16160AT-12 [6], IBM0316169C-13, or equivalent are recommended. Devices faster than 13 ns (77 MHz) are usable as well.

Figure 5-3 shows an example of the maximum SSRAM size with 2 Mbit devices.

5.2.1 SSRAM Interface

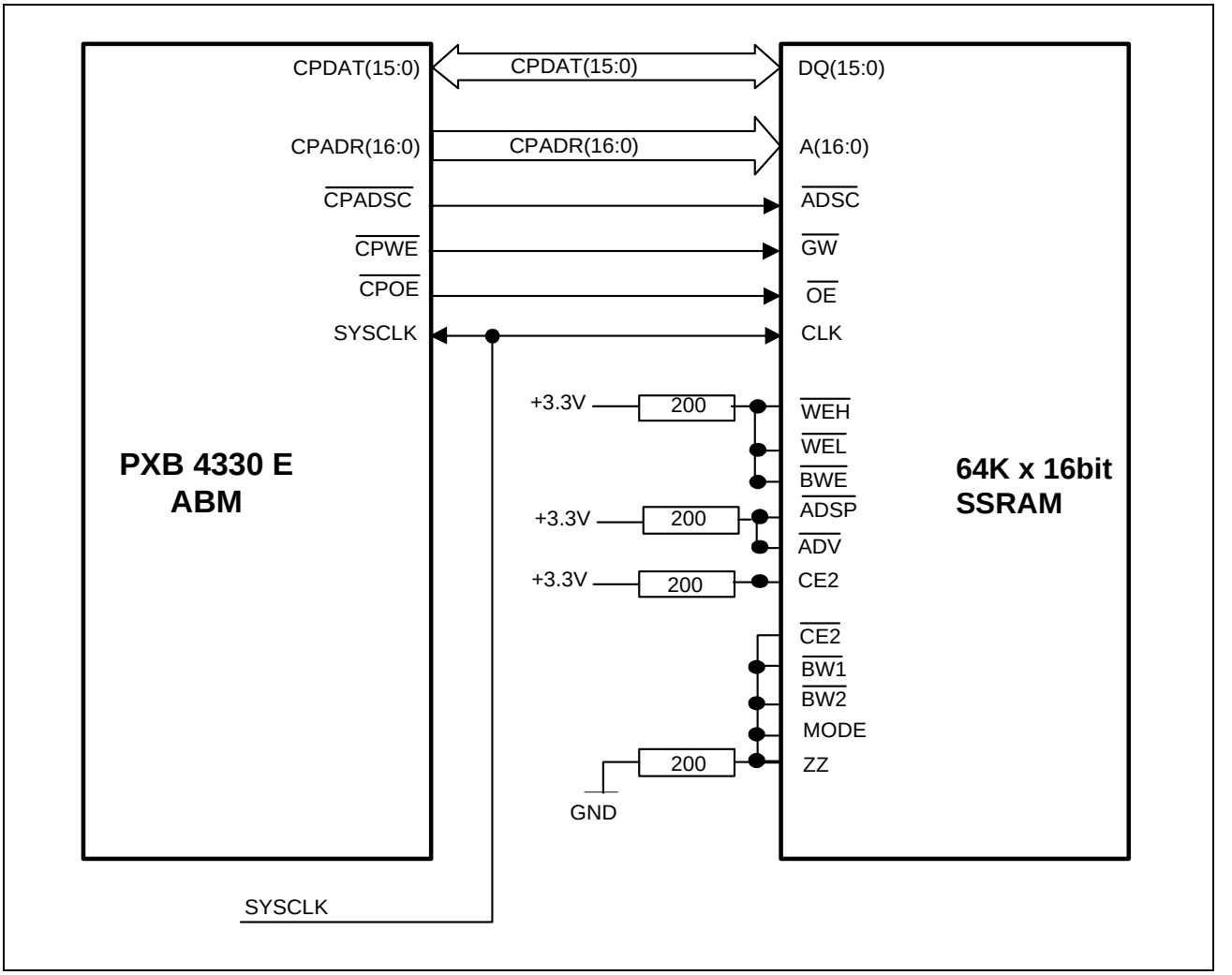


Figure 5-3 SSRAM Interface Using 2 Mbit RAM

Note: The clock cycle for all RAMs is supplied by SYSCLK.

5.2.2 SDRAM Interfaces

The two cell storage SDRAM interfaces are completely separate, but have identical signal and configuration set. Two 16M SDRAM devices in 1M×16 bit configuration must be connected to each interface. As an option for Uni-directional Mode, the downstream SDRAM can be omitted if only one ABM Core is used. The upstream SDRAM must be configured always, as otherwise no cell could be transmitted.

Figure 5-4 shows the connection of the SDRAMs to the ABM.

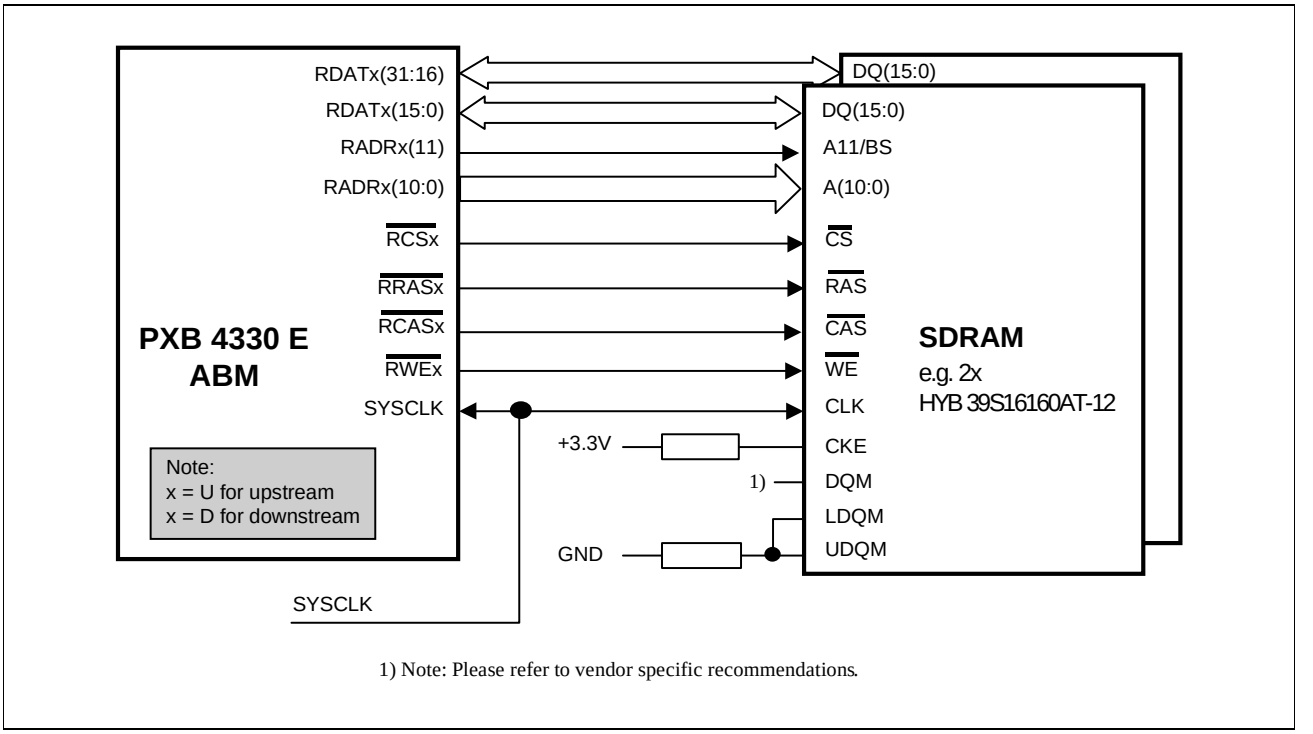


Figure 5-4 SDRAM Interfaces

5.3 Microprocessor Interface

The ABM has a 16-bit Microprocessor Interface for control and operation. The Interface can be configured for either Intel or Motorola Mode. Interconnection to an Intel processor is shown in **Figure 5-5**, with the 386EX embedded controller as an example.

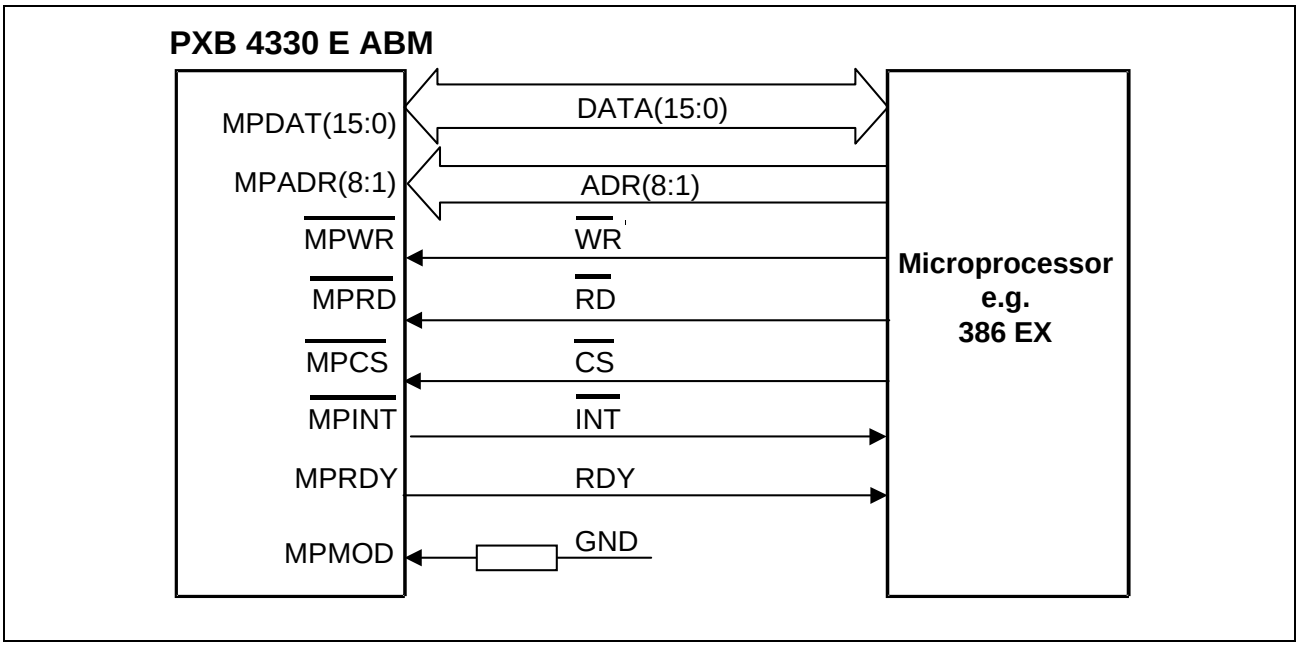


Figure 5-5 Microprocessor Interface: Intel Mode

A typical configuration in Motorola Mode is shown in **Figure 5-6**.

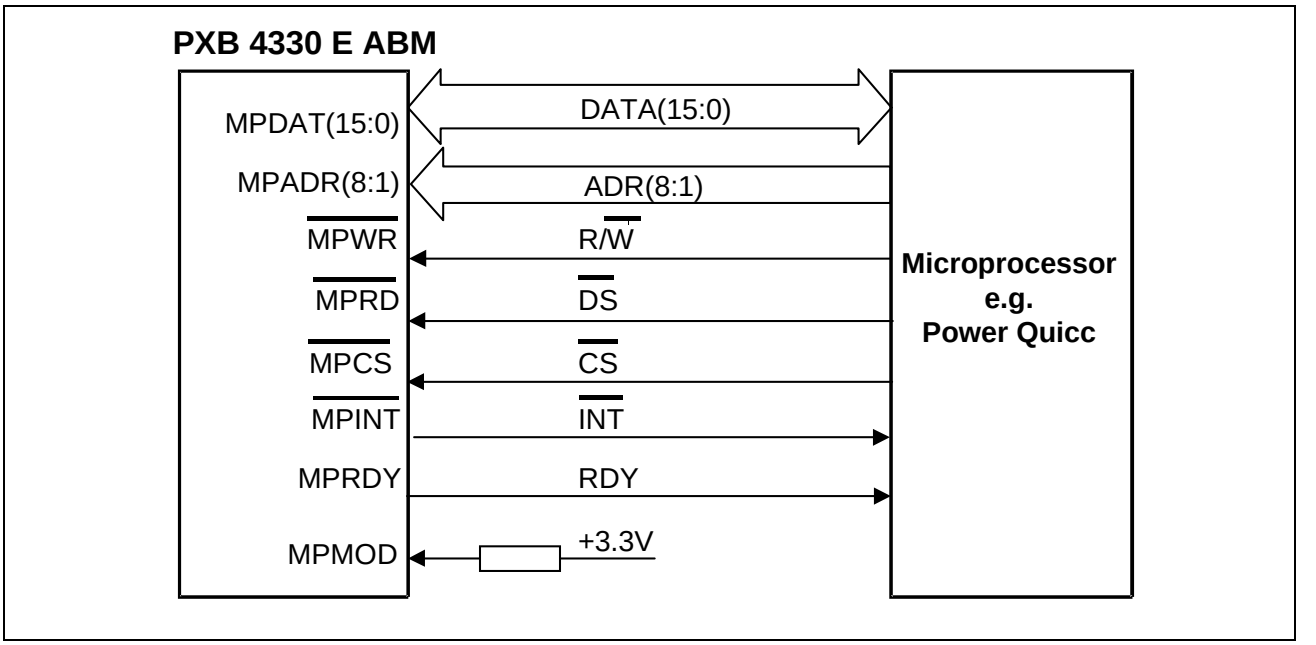


Figure 5-6 Microprocessor Interface: Motorola Mode

The Interface operates completely asynchronous to the system clock SYSCLK.

5.4 JTAG Interface

This interface contains the boundary scan of all signal pins according to the Joint Test Action Group (JTAG) Standard [4]. It consists of the pins shown in **Figure 5-7**.

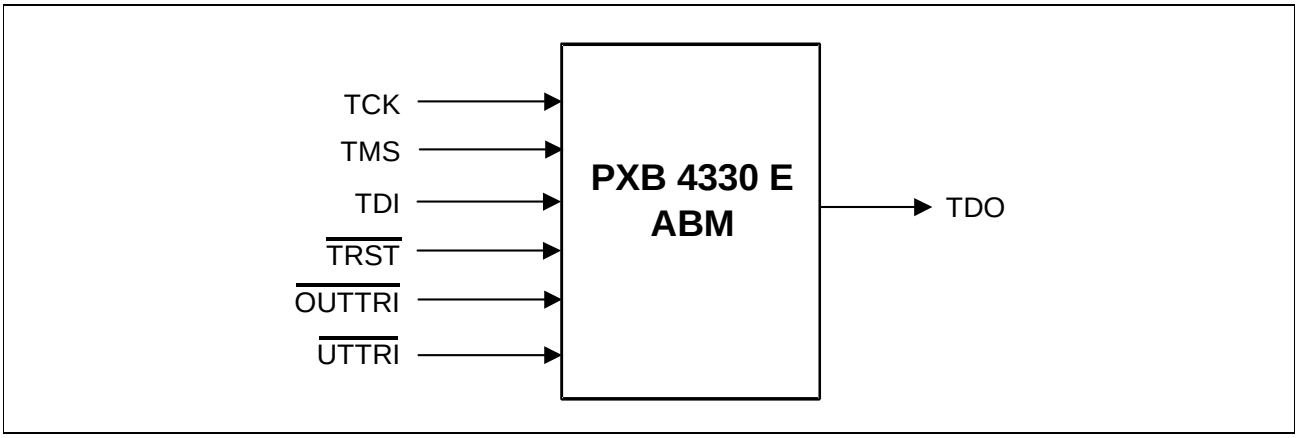


Figure 5-7 JTAG Interface

In addition to the standard boundary scan pins, following pins are provided for board test:

- $\overline{\text{OUTTRI}}$: If this signal is low, all other signal pins of the ABM device are put into high impedance mode.
- $\overline{\text{UTTRI}}$: If this signal is low, all pins of the UTOPIA Interfaces are put into high impedance mode.

5.5 Clock Supply

The ABM Core is operated with a main chip clock, SYSCLK, with a frequency between 25 MHz and 52 MHz, as shown in **Figure 5-8**. The UTOPIA Interfaces have different clocks: one for the PHY side interfaces (towards the PHY side in **Figure 5-8**), and one for the ATM side interfaces (towards the ATM side in **Figure 5-8**). Both UTOPIA clocks may be independent (asynchronous) to each other and also asynchronous to the System Clock. The only restriction is that their frequency must be less than or equal to the System Clock.

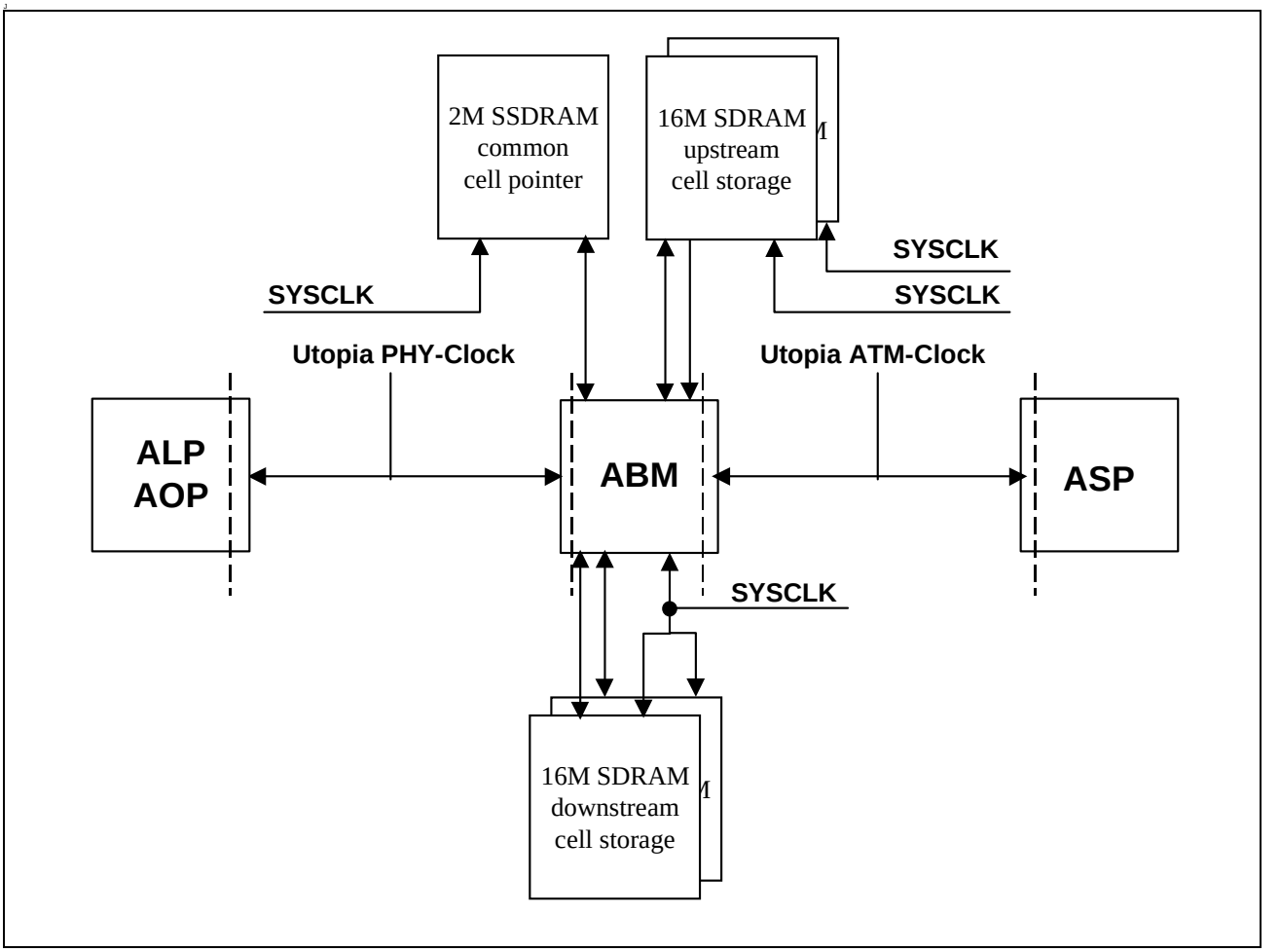


Figure 5-8 Clock Concept

A further asynchronous interface is the Microprocessor Interface. Its speed is limited to less or equal than SYSCLK/2.

Note: The clock cycle for all RAMs is supplied by SYSCLK.

6 Register Descriptions

This chapter provides both an overview of the ATM Buffer Manager PXB 4330 Register Set and detailed register descriptions and Table Access descriptions.

6.1 Overview of the ABM Register Set

Control and operation of the ABM chip can be done by directly configuring Status Registers or, to a large extent, by programming the internal tables. Access to these tables is not direct, but occurs via Transfer Registers and Transfer Commands. Any transfer must be prepared by writing appropriate values to the Transfer Registers. Bit positions named ’don’t Write’ must be masked by writing **1** to the corresponding bit positions in the Mask Register. This avoids overwriting these table bit positions with the Transfer Register contents, which would cause fatal malfunction. The specific table position which should be modified with the Transfer Register contents is selected via Register WAR. Transfer is started by writing the table address to Register MAR and also setting the ’Start’ bit. The ABM device will reset the ’Start’ bit after transfer completion.

The ABM contains the following internal tables for configuration:

- LCI Table
- Traffic Class Table
- Queue Configuration Table
- Queue Parameter Table (consisting of 4 tables)
- Scheduler Block Occupancy Table
- Scheduler Rate Table (consisting of 4 tables)

The Status Registers and Transfer Registers are described below in **Table 6-1**. This register overview table is organized by functional groups and, thus, not always in sequence to the offset addresses. Offset addresses are 16-bit word addresses. Addresses not listed in this table are either associated with Reserved Registers or are unused. Performing Write accesses to those addresses is not recommended in order to prevent malfunctions and to guarantee upwards compatibility to future versions of the device.

Table 6-1 ABM Registers Overview

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
Cell Flow Test Registers					
01/11	UCFTST/ DCFTST	Upstream/Downstream Cell Flow Test Registers	0000	R/W	80
SDRAM Configuration Registers					
02/12	URCFG/ DRCFG	Upstream/Downstream SDRAM Configuration Registers	0033	R/W	82
Buffer Occupation Counter Registers					
20	UBOC	Upstream/Downstream Buffer Occupation Registers	0000	R	82
21	DBOC		0000	R	82
22	UNRTOC	Upstream/Downstream Non-Real-Time Buffer Occupation Registers	0000	R	83
23	DNRTOC		0000	R	83
Buffer Threshold Registers					
24	UBMTH	Upstream/Downstream Buffer Maximum Threshold Registers	0000	R/W	84
25	DBMTH		0000	R/W	84
26	UCIT	Upstream/Downstream ABR Congestion Indication Threshold Registers	0000	R/W	85
27	DCIT		0000	R/W	85
2C	UEC	Upstream/Downstream EPD CLP1 Threshold Registers	0000	R/W	88
2D	DEC		0000	R/W	88
Occupation Capture Registers					
28	UMAC	Upstream/Downstream Maximum Occupation Capture Registers	0000	R	86
29	DMAC		0000	R	86
2A	UMIC	Upstream/Downstream Minimum Occupation Capture Registers	FFFF	R	87
2B	DMIC		FFFF	R	87
LCI Table Transfer Registers LCI0, LCI1					
30	LCI0	LCI Transfer Register 0	0000	R/W	90
31	LCI1	LCI Transfer Register 1	0000	R/W	92
Traffic Class Table Transfer Registers TCT0, TCT1					
32	TCT0	TCT Transfer Register 0	0000	R/W	95
33	TCT1	TCT Transfer Register 1	0000	R/W	98

Table 6-1 ABM Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
Queue Configuration Table Transfer Registers QCT0..3					
34	QCT0	Queue Configuration Transfer Register 0	0000	R/W	103
35	QCT1	Queue Configuration Transfer Register 1	0000	R/W	104
36	QCT2	Queue Configuration Transfer Register 2	0000	R/W	106
37	QCT3	Queue Configuration Transfer Register 3	0000	R/W	106
Scheduler Occupancy Table Transfer Registers SOT0, SOT1					
38	SOT0	SOT Transfer Register 0	0000	R/W	108
39	SOT1	SOT Transfer Register 1	0000	R/W	110
Mask Registers for Read/Write transfer access control of LCI-, Traffic Class-, Queue Configuration- and Scheduler Occupancy Tables					
3B/3C	MASK0/ MASK1	Table Access Mask Registers 0/1	0000	R/W	111
3D/3E	MASK2/ MASK3	Table Access Mask Registers 2/3	0000	R/W	112
ABR CI/NI Marking Registers					
41	CONFIG	Configuration Register	0000	R/W	113
Upstream Scheduler Level/Threshold Exceed Detection Indication Registers					
45	LEVL0	Upstream Scheduler Lower Threshold Reached Indication Register 0	0000	R	114
46	LEVL1	Upstream Scheduler Lower Threshold Reached Indication Register 1	0000	R	115
47	LEVL2	Upstream Scheduler Lower Threshold Reached Indication Register 2	0000	R	116
48	LEVH0	Upstream Scheduler High Threshold Reached Indication Register 0	0000	R	117
49	LEVH1	Upstream Scheduler High Threshold Reached Indication Register 1	0000	R	118
4A	LEVH2	Upstream Scheduler High Threshold Reached Indication Register 2	0000	R	119
Rate Shaper CDV Registers					

Table 6-1 ABM Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
52	CDVU	Upstream/Downstream Rate Shaper CDV Registers	0000	R/W	120
72	CDVD		0000	R/W	120
Queue Parameter Table Mask Registers					
55	QMSKU0	Upstream Queue Parameter Table Mask Registers 0/1	0000	R/W	121
56	QMSKU1		0000	R/W	121
75	QMSKD0	Downstream Queue Parameter Table Mask Registers 0/1	0000	R/W	122
76	QMSKD1		0000	R/W	122
Queue Parameter Table Transfer Registers					
60/80	QPTLU0/ QPTLD0	QPT Upstream/Downstream Low Word Transfer Register 0	0000	R/W	126
61/81	QPTLU1/ QPTLD1	QPT Upstream/Downstream Low Word Transfer Register 1	0000	R/W	127
62/82	QPTHU0/ QPTHD0	QPT Upstream/Downstream High Word Transfer Register 0	0000	R/W	128
63/83	QPTHU1/ QPTHD1	QPT Upstream/Downstream High Word Transfer Register 1	0000	R/W	129
Upstream/Downstream Scheduler Configuration Table Transfer/Mask Registers					
90/B0	SADRU/ SADRD	Upstream/Downstream SCTI Address Registers	0000	R/W	136
91/B1	SCTIU/SCTID	Upstream/Downstream SCTI Transfer Registers	0000	R/W	137
95/B5	SMSKU/ SMSKD	Upstream/Downstream SCTF Mask Registers	0000	R/W	133
96/B6	SCTFU/ SCTFD	Upstream/Downstream SCTF Transfer Registers	0000	R/W	131
SDRAM Refresh Registers					
92/B2	ECRIU/ECRID	Upstream/Downstream Empty Cycle Rate Integer Part Registers	0000	R/W	140
93/B3	ECRFU/ ECRFD	Upstream/Downstream Empty Cycle Rate Fractional Part Registers	0000	R/W	143
UTOPIA Port Select of Common Real Time Queue Registers					

Table 6-1 ABM Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
94/B4	CRTQU/ CRTQD	Upstream/Downstream Common Real Time Queue UTOPIA Port Select Registers	0000	R/W	145
Scheduler Enable Registers					
98/B8	SCEN0U/ SCEN0D	Upstream/Downstream Scheduler Enable 0 Registers	0000	R/W	146
99/B9	SCEN1U/ SCEN1D	Upstream/Downstream Scheduler Enable 1 Registers	0000	R/W	147
9A/BA	SCEN2U/ SCEN2D	Upstream/Downstream Scheduler Enable 2 Registers	0000	R/W	148
Interrupt Status/Mask Registers					
D0	ISRU	Interrupt Status Register Upstream	0000	R/W	149
D1	ISRD	Interrupt Status Register Downstream	0000	R/W	152
D2	IMRU	Interrupt Mask Register Upstream	0000	R/W	155
D3	IMRD	Interrupt Mask Register Downstream	0000	R/W	156
RAM Select Registers					
D7	MAR	Memory Address Register	0000	R/W	157
D8	WAR	Word Address Register	0000	R/W	159
UTOPIA FIFO Fill Level Register					
D9	UTRXFILL	Upstream UTOPIA Receive FIFO Fill Level Register	0000	R	161
ABM Mode Register					
DA	MODE	ABM Mode Register	0000	R/W	162
UTOPIA Configuration Registers					
DC	UTOPHY0	UTOPIA Configuration Register 0 (PHY Side)	0000	R/W	165
DD	UTOPHY1	UTOPIA Configuration Register 1 (PHY Side)	0000	R/W	166
DE	UTOPHY2	UTOPIA Configuration Register 2 (PHY Side)	0000	R/W	167
DF	UTATM0	UTOPIA Configuration Register 0 (ATM Side)	0000	R/W	168

Table 6-1 ABM Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
E0	UTATM1	UTOPIA Configuration Register 1 (ATM Side)	0000	R/W	169
E1	UTATM2	UTOPIA Configuration Register 2 (ATM Side)	0000	R/W	170
Test Registers/Special Mode Registers					
01/11	UCFTST/ DCFTST	Upstream/Downstream Cell Flow Test Registers	0000	R/W	80
F0	TEST	TEST Register	0000	R/W	171
50	-	Reserved Register	0000	R/W	
51	-	Reserved Register	0000	R/W	
53	-	Reserved Register	0000	R/W	
54	-	Reserved Register	0000	R/W	
70	-	Reserved Register	0000	R/W	
71	-	Reserved Register	0000	R/W	
73	-	Reserved Register	0000	R/W	
74	-	Reserved Register	0000	R/W	
97	-	Reserved Register	----	R	
B7	-	Reserved Register	----	R	
ABM Version Code Registers					
F1	VERH	Version Number High Register	1003	R	172
F2	VERL	Version Number Low Register	9083	R	172

6.2 Detailed Register Description

Register 1 UCFTST/DCFTST

Upstream/Downstream Cell Flow Test Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UCFTST** **01_H** **DCFTST** **11_H**

Typical Usage: Written by CPU to test internal integrity functions during special system test scenarios

Bit	15	14	13	12	11	10	9	8
	Unused(15:8)							

Bit	7	6	5	4	3	2	1	0
	Unused(7:2)						TSTBIP	TSTQID

TSTBIP **Test BIP-8 Supervision**
(see **"Cell Header Protection" on page 3-48**)

0 **Normal Operation**:
BIP-8 for cell protection is generated normally. No ’BIP8ER’ interrupt should occur indicating a cell storage failure.

1 **Test Mode**:
Least Significant Bit (LSB) of BIP-8 is inverted to test BIP-8 checking function. An ’BIP8ER’ (**Register 46: ISRU**, **Register 47: ISRD**) interrupt is generated whenever a cell is Read out of the Cell Buffer RAM.

TSTQID **Test Queue ID Supervision**
(see **"Cell Queue Supervision" on page 3-48**)

0 **Normal Operation**:
A correct QID is generated. No ’BUFER5’ interrupt should occur indicating an internal queue pointer failure.

1 **Test Mode**:
The LSB of the QID is inverted to test the QID checking function. A ’BUFER5’ (**Register 46: ISRU**, **Register 47: ISRD**) interrupt is generated whenever a cell is Read out out the Cell Buffer RAM.

Note: The respective QID value is stored with each cell when written to the appropriate queue in the cell storage RAM. The ABM checks the stored QID value against the supposed QID when a cell is read back from the cell storage RAM.

Register 2 URCFG/DRCFG
Upstream/Downstream SDRAM Configuration Registers

CPU Accessibility: **Read/Write**
Reset Value: **0033_H**
Offset Address: **URCFG** **02_H** **DRCFG** **12_H**
Typical Usage: (Reserved)

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Note: These registers are for internal use only. Do not to Write a value different from the Reset Value 0033_H to Registers URCFG/DRCFG.

Register 3 UBOC/DBOC
Upstream/Downstream Buffer Occupation Registers

CPU Accessibility: **Read only**
Reset Value: **0000_H**
Offset Address: **UBOC** **20_H** **DBOC** **21_H**
Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	UBOC/DBOC(15:8)							

Bit	7	6	5	4	3	2	1	0
	UBOC/DBOC(7:0)							

UBOC(15:0) **Upstream Buffer Occupation Counter**

DBOC(15:0) **Downstream Buffer Occupation Counter**

These 16-bit counter values reflect the number of cells currently stored in the dedicated cell storage RAM.

Register 4 UNRTOC/DNRTOC
Upstream/Downstream Non-Real-Time Buffer Occupation Registers

CPU Accessibility: **Read only**

Reset Value: **0000_H**

Offset Address: **UNRTOC** **22_H** **DNRTOC** **23_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	UNRTOC/DNRTOC(15:8)							

Bit	7	6	5	4	3	2	1	0
	UNRTOC/DNRTOC(7:0)							

UNRTOC(15:0) **Upstream Non-Real-Time Buffer Occupation Counter**

DNRTOC(15:0) **Downstream Non-Real-Time Buffer Occupation Counter**

These 16-bit counter values reflect the number of non-real-time cells currently stored in the dedicated cell storage RAM. Non-real-time cells belong to traffic classes with the real-time indication bit ’RTind’ cleared in the traffic class table (Transfer Register TCT1).

Register 5 UBMTH/DBMTH

Upstream/Downstream Buffer Maximum Threshold Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UBMTH** **24_H** **DBMTH** **25_H**

Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	UBMTH/DBMTH(15:8)							

Bit	7	6	5	4	3	2	1	0
	UBMTH/DBMTH(7:0)							

UBMTH(15:0) **Upstream Buffer Maximum Threshold**

DBMTH(15:0) **Downstream Buffer Maximum Threshold**

These bit fields determine a threshold for the total upstream and downstream buffer size. The values depend on:

- The size of the external cell pointer RAM,
- Whether the downstream cell storage RAM is connected.

See **Table 6-2** for recommended values.

Table 6-2 UBMTH/DBMTH Threshold Values

Cell Pointer RAM	Downstream Cell RAM	UBMTH	DBMTH
128 k x 16 bit	1 M x 32 bit	$FFFF_H$	$FFFF_H$
64 k x 16 bit	1 M x 32 bit	$7FFF_H$	$7FFF_H$
32 k x 16 bit	1 M x 32 bit	$3FFF_H$	$3FFF_H$
64 k x 16 bit	none	$FFFF_H$	0000_H
32 k x 16 bit	none	$7FFF_H$	0000_H
16 k x 16 bit	none	$3FFF_H$	0000_H

Note: An upstream cell storage RAM of size 1 M x 32 bit must be connected always.

Register 6 UCIT/DCIT

Upstream/Downstream ABR Congestion Indication Threshold Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UCIT** **26_H** **DCIT** **27_H**

Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	UCIT/DCIT(15:8)							

Bit	7	6	5	4	3	2	1	0
	UCIT/DCIT(7:0)							

UCIT(15:0) **Upstream ABR Congestion Indication Threshold**

DCIT(15:0) **Downstream ABR Congestion Indication Threshold**

These 16-bit counters determine a threshold for the total buffer fill level with non-real-time cells to indicate ABR Congestion.

Congestion indication ’CI’ will be marked in cells belonging to ABR traffic class if the number of stored non-real-time cells exceeds the threshold value.

Register 7 UMAC/DMAC
Upstream/Downstream Maximum Occupation Capture Registers

CPU Accessibility: **Read only, self-clearing on Read**

Reset Value: **0000_H**

Offset Address: **UMAC** **28_H** **DMAC** **29_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	UMAC/DMAC(15:8)							

Bit	7	6	5	4	3	2	1	0
	UMAC/DMAC(7:0)							

UMAC(15:0) **Upstream Maximum Occupation Capture Counter**

DMAC(15:0) **Downstream Maximum Occupation Capture Counter**

These 16-bit counters measure the absolute maximum number of cells stored in the respective external cell buffer since the last Read access (peak cell filling level within measurement interval). The counter value is automatically cleared to 0000_H after Read.

Register 8 UMIC/DMIC
Upstream/Downstream Minimum Occupation Capture Registers

CPU Accessibility: **Read only, self-clearing on Read**

Reset Value: **$FFFF_H$**
(may be modified by chip logic immediately after reset)

Offset Address: **UMIC** **$2A_H$** **DMIC** **$2B_H$**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	UMIC/DMIC(15:8)							

Bit	7	6	5	4	3	2	1	0
	UMIC/DMIC(7:0)							

UMIC(15:0) **Upstream Minimum Occupation Capture Counter**

DMIC(15:0) **Downstream Minimum Occupation Capture Counter**

These 16-bit counters measure the absolute minimum number of cells stored in the respective external cell buffer since the last Read access (minimum cell filling level within measurement interval). The counter value is automatically cleared to $FFFF_H$ after Read.

Note: The reset value may be modified by chip logic immediately after reset or clearing read.

Register 9 UEC/DEC
Upstream/Downstream EPD CLP1 Threshold Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UEC** **$2C_H$** **DEC** **$2D_H$**

Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	UEC/DEC(15:8)							

Bit	7	6	5	4	3	2	1	0
	UEC/DEC(7:0)							

UEC(15:0) **Upstream EPD CLP1 Threshold value**

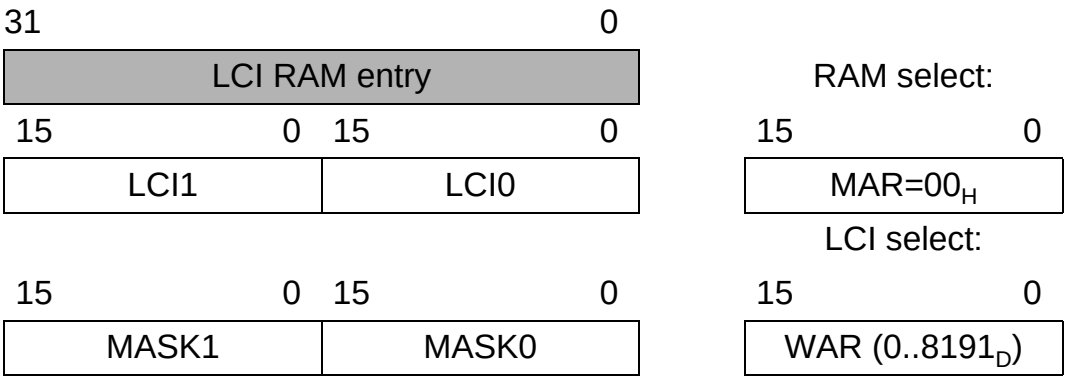
DEC(15:0) **Downstream EPD CLP1 Threshold value**

These 16-bit values determine a global cell filling level threshold that triggers explicit packet discard (EPD) for CLP=1 tagged frames used by GFR traffic class service (low watermark).

Internal Table 1: LCI Table Transfer Registers LCI0, LCI1

These registers are used to access the internal Local Connection Identifier (LCI) table containing 8192 entries. **Table 6-3** shows an overview of the registers involved.

Table 6-3 Registers for LCI Table Access



LCI0 and LCI1 are the transfer registers for one 32-bit LCI table entry. The LCI value representing the table entry which needs to be Read or modified must be written to the Word Address Register (WAR). The dedicated LCI table entry is Read into the LCI1/LCI0 Registers or modified by the LCI1/LCI0 Register values with a Read-Modify-Write mechanism. The associated Mask Registers MASK0 and MASK1 allow a bit-by-bit selection between Read (1) and Write (0) operation. In case of Read operation, the dedicated LCI1/LCI0 register bit will be overwritten by the respective LCI table entry bit value. In case of Write operation, the dedicated LCI1/LCI0 register bit will modify the respective LCI table entry bit value.

The Read-Modify-Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR select the memory/table that will be accessed; to select the LCI table bit field MAR(4:0) must be set to 0. Bit 5 of the MAR starts the transfer and is automatically cleared after execution of the Read-Modify-Write process.

Table 6-4 WAR Register Mapping for LCI Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(2:0)			LCISel(12:8)				

Bit	7	6	5	4	3	2	1	0
	LCISel(7:0)							

LCISel(12:0) Selects an LCI entry within the range (0..8191).

Register 10 LCI0

LCI Transfer Register 0

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **LCI0** **30_H**

Typical Usage: Written and Read by CPU to maintain the LCI table

Bit	15	14	13	12	11	10	9	8
	Unused	CLPT	ABMcore	DnQID(9:5)				

Bit	7	6	5	4	3	2	1	0
	DnQID(4:0)					flags(2:0)		

CLPT **CLP Transparent**:
Specifies whether the CLP bit of cells is evaluated or not in threshold checks. Valid for both upstream and downstream cores.

0 CLP bit is evaluated.

1 CLP bit is not evaluated; all cells are treated as high priority cells assuming CLP=0.

ABMcore **ABM Core Selection**:
This bit is valid in Uni-directional Mode only and specifies the core responsible for cells of this LCI.

0 Schedulers 0..47 are selected (core 0).

1 Schedulers 48..95 are selected (core 1).

DnQID(9:0) **Downstream Queue Identifier**.
Specifies the queue in which the cells of the connection are stored.

flag 2 **Last cell of packet flag for downstream direction**;
This bit is autonomously used by the EPD function of the ABM.
Initialize to 1 at connection setup.
Do not Write during normal operation.

flag 1 — **Discard packet flag in downstream direction**;
This bit is autonomously used by the EPD function of the ABM.
Initialize to 0 at connection setup.
Do not Write during normal operation.

flag 0 — **Discard rest of packet flag in downstream direction**;
This bit is autonomously used by the EPD function of the ABM.
Initialize to 0 at connection setup.
Do not Write during normal operation.

Register 11 LCI1

LCI Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **LCI1** **31_H**

Typical Usage: Written and Read by CPU to maintain the LCI table

Bit	15	14	13	12	11	10	9	8
	Unused(2:0)			UpQID(9:5)				

Bit	7	6	5	4	3	2	1	0
	UpQID(4:0)					flags(2:0)		

UpQID(9:0) **Upstream Queue Identifier**.
Specifies the queue in which the cells of the connection are stored.

flag 2 **Last cell of packet flag for upstream direction**;
This bit is autonomously used by the EPD function of the ABM.
Initialize to 1 at connection setup.
Do not Write during normal operation.

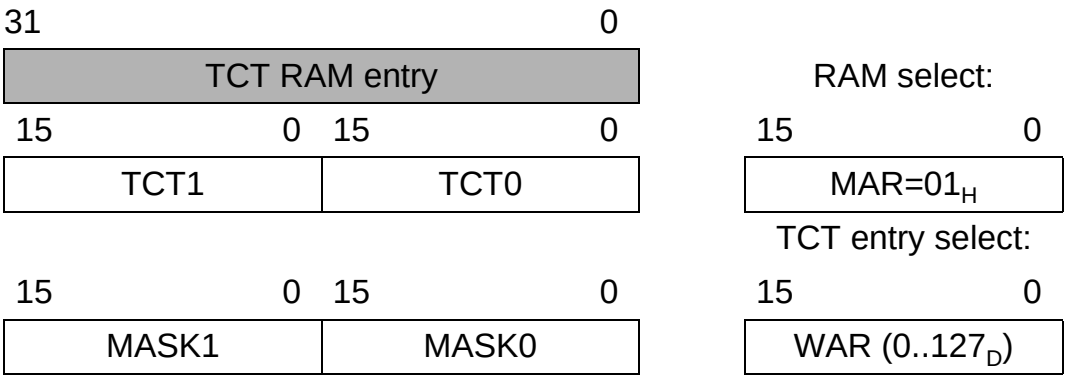
flag 1 **Discard packet flag in upstream direction**;
This bit is autonomously used by the EPD function of the ABM.
Initialize to 0 at connection setup.
Do not Write during normal operation.

flag 0 **Discard rest of packet flag in upstream direction**;
This bit is autonomously used by the EPD function of the ABM.
Initialize to 0 at connection setup.
Do not Write during normal operation.

Internal Table 2: Traffic Class Table Transfer Registers TCT0, TCT1

The Traffic Class Table Transfer Registers are used to access the internal Traffic Class Table (TCT) containing 2*16 entries of 128 bits each (16 traffic classes per ABM core). **Table 6-5** shows an overview of the registers involved.

Table 6-5 Registers for TCT Table Access



TCT0 and TCT1 are the transfer registers used to access the 128 bit TCT table entries.

Core selection, traffic class number, and 32-bit word selection of the table entry which needs to be Read or Modified must be programmed to the Word Address Register (WAR). The dedicated TCT table entry 32-bit word is Read into the TCT1/TCT0 registers or Modified by the TCT1/TCT0 register values with a Read-Modify-Write mechanism. The associated Mask Registers MASK0 and MASK1 allow a bit-by-bit selection between Read (1) and Write (0) operations. In case of Read operation, the dedicated TCT1/TCT0 register bit will be overwritten by the respective TCT table entry bit value. In case of Write operation, the dedicated TCT1/TCT0 register bit will modify the respective TCT table entry bit value.

The Read-Modify-Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR select the memory/table that will be accessed; to select the TCT table bit field MAR(4:0) must be set to 1. Bit 5 of MAR starts the transfer and is automatically cleared after execution of the Read-Modify-Write process.

Table 6-6 WAR Register Mapping for TCT Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	Unused	CoreSel	TrafClass(3:0)				DwordSel(1:0)	

CoreSel **Selects the ABM core for TCT table access**:

0 Upstream core selected (core 0)

1 Downstream core selected (core 1)

TrafClass(3:0) **Selects The Traffic Class** for the TCT table access in the range (0..15).

DwordSel(1:0) **Selects The 32-Bit Word** of the 128-bit TCT table entry for access:

00 Bit field (31..0) of traffic class entry is selected.

01 Bit field (63..32) of traffic class entry is selected.

10 Bit field (95..64) of traffic class entry is selected.

11 Bit field (127..96) of traffic class entry is selected.

The meaning of registers TCT0 and TCT1 depends on the dword selection bit field 'DwordSel(1:0)' in the WAR, because 128-bit TCT entries are mapped to 32 bits of registers TCT0/TCT1 by this selection:

WAR modulo 4

	31 … 24	23 … 16	15 … 8	7 … 0
3	DiscardedCells(15:0)[1]		LostCells TrafClass (3:0)[1]	LostCells Scheduler (3:0)[1]	DiscardedPackets/ CLP1Cells(7:0)[1]
2	Accepted/Transmitted Packets(15:0)[1]		TrafClassOcc(15:0)	
1	TrafClassMax(7:0)	SbMaxEpdCi(7:0)	QueueMaxEPD(7:0)	QueueCiCLP1(7:0)
0	28	27	26	25	24		BufNrtMax(7:0)	BufNrtEPD(7:0)

TCT1(15:0)	TCT0(15:0)

[1] All 5 statistical counters stop at maximum value. Automatically reset after Read access, that is, it is not necessary to Write them to 0.

Register 12 TCT0

TCT Transfer Register 0

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **TCT0** **32_H**

Typical Usage: Written and Read by CPU to maintain the TCT table; the meaning of register TCT0 depends on the bit-field 'DWordSel' in WAR;

Register WAR.DwordSel(1:0) = '00':

Bit	15	14	13	12	11	10	9	8
	BufNrtMax(7:0)							

Bit	7	6	5	4	3	2	1	0
	BufNrtEPD(7:0)							

BufNrtMax(7:0) **Maximum Buffer Fill Threshold for a non-real-time traffic class configuration** (register TCT1, DwordSel=00, RTind=0).
The first cell exceeding this threshold is discarded and if also PPD is enabled for this traffic class (register TCT1, DwordSel=00, PPDen=1) PPD is applied on a per connection (LCI) basis.
The threshold is defined with a granularity of 256 cells:
Threshold = BufNrtMax(7:0) * 256 Cells

BufNrtEPD(7:0) **EPD threshold for a non-real-time traffic class configuration** (register TCT1, DwordSel='00', RTind=0).
If the buffer fill exceeds this threshold and EPD is enabled for this traffic class (register TCT1, DwordSel=00, EPDen=1) EPD is applied on a per connection (LCI) basis.
The threshold is defined with a granularity of 256 cells:
Threshold = BufNrtEPD(7:0) * 256 Cells

Register WAR.DwordSel(1:0) = ’01’:

Bit	15	14	13	12	11	10	9	8
	QueueMaxEPD(7:0)							

Bit	7	6	5	4	3	2	1	0
	QueueCiCLP1(7:0)							

QueueMax EPD(7:0)

Combined Threshold for each Queue of this Traffic Class for the following cases:

a) if EPDen=1

⇒ EPD queue threshold on a connection (LCI) basis for CLP=0/1 frames
(frames with CLP=0 or 01 are discarded)

b) if EPDen=0

⇒ Maximum queue fill threshold for CLP=0/1 cells
(cells with CLP=0 or 1 are discarded as the maximum queue fill for CLP=0/1 cells was exceeded)

The threshold is defined with a granularity of 64:
Threshold = QueueMaxEPD(7:0) * 64 Cells
(This is the high watermark of GFR)

QueueCiCLP1 (7:0)

Combined Queue Threshold of this Traffic Class for the following cases:

a) if ABRen=1 for the traffic class

⇒ ABR Congestion Indication CI/EFCI is triggered

b) if CLPT=0 (CLP transparent bit is not true) and EPDen=0

⇒ CLP1 queue threshold for CLP=1 cells
(cells with CLP=1 are discarded)

c) if CLPT=0 and EPDen=1

⇒ EPD GFR queue threshold. If that threshold and additionally BufNrtEPD (of the respective traffic class) is exceeded then EPD is triggered.

The threshold is defined with a granularity of 4:
Threshold = QueueCiCLP1(7:0) * 4 Cells

Register WAR.DwordSel(1:0) = ’10’:

Bit	15	14	13	12	11	10	9	8
	TrafClassOcc(15:8)							

Bit	7	6	5	4	3	2	1	0
	TrafClassOcc(7:0)							

TrafClassOcc (15:0) **Current Buffer Occupation** in number of cells for this traffic class. Do not Write in normal operation.

Register WAR.DwordSel(1:0) = ’11’:

Bit	15	14	13	12	11	10	9	8
	LostCellsTrafClass(3:0)				LostCellsScheduler(3:0)			

Bit	7	6	5	4	3	2	1	0
	DiscardedPackets/CLP1Cells(7:0)							

LostCellsTrafClass(3:0) **Count of Lost Cells due to Buffer Overflow** for this traffic class. Automatically reset after Read access.

LostCells Scheduler(3:0) **Count of Lost Cells due to Scheduler Overflow** for this traffic class.
Automatically reset after Read access.

Discarded Packets/ CLP1Cells(7:0) **Count of Lost Packets due to EPD Overflow** for this traffic class or count of lost CLP=1 cells due to CLP threshold overflow. Automatically reset after Read access.

Register 13 TCT1

TCT Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **TCT1** **33_H**

Typical Usage: Written and Read by CPU to maintain the TCT table; the meaning of register TCT1 depends on the bit-field 'DWordSel' in WAR;

Register WAR.DwordSel(1:0) = '00':

Bit	15	14	13	12	11	10	9	8
	Unused(10:8)			RTind	ABRen	ABRvp	EPDen	PPDen

Bit	7	6	5	4	3	2	1	0
	Unused(7:0)							

RTind **Real-time or Non-Real-time Indicator** for the traffic class connections:

0 Traffic class consists of non-real-time connections.

1 Traffic class consists of real-time connections.

ABRen **Congestion indication** in user cells (EFCI marking) within every ABR connection (LCI) that belongs to the individual traffic class:

0 Congestion indication disabled.

1 Congestion indication enabled.

ABRvp **Indication for update of RM cells** (ABR service category) relating to the VP or to the individual VC, respectively:

0 Congestion is indicated via VC RM cells (F5 flow). VC RM cells are identified with PTI=110 and VCI <> 6.

1 Congestion is indicated via VP RM cells (F4 flow). VP RM cells are identified with VCI=6 (regardless of the value of the PTI field)

Note: According to the standards, VP RM cells MUST have VCI=6 and PTI=110. If cells with PTI=110 and VCI <> 6 are contained in the cell stream they are ignored. This is the correct behavior for an ABR VC within an ABR VP.

EPDen **EPD for the individual traffic class**. EPD is used for every connection (LCI) within that traffic class:

0 EPD is disabled.

1 EPD is enabled.

PPDen **PPD for the individual traffic class**. PPD is used for every connection (LCI) within that traffic class:

0 PPD is disabled

1 PPD is enabled

Register WAR.DwordSel(1:0) = ’01’:

Bit	15	14	13	12	11	10	9	8
	TrafClassMax(7:0)							

Bit	7	6	5	4	3	2	1	0
	SbMaxEpdCi(7:0)							

TrafClassMax (7:0)

Maximum Traffic Class Fill Threshold (determines the maximum number of cells in all queues associated with this traffic class). The threshold is defined with a granularity of 256:
Threshold = TrafClassMax(7:0) * 256 Cells

SbMaxEpdCi (7:0)

Combined Threshold of the Maximum Number of Buffered Cells in the Scheduler; that is, all cells which are in the traffic classes (= cells in the corresponding queues) of the Scheduler) for the following cases:

a) If EPDen=0 and ABRen=0
⇒ Maximum Scheduler fill threshold for CLP=’0/1’ cells

b) If EPDen=1 and ABRen=0
⇒ EPD Scheduler threshold

c) If ABRen=1
⇒ CI Scheduler threshold for ABR connections
(Set CI-Bit (Congestion Indication) in the RM cells)

The threshold is defined with a granularity of 256:
Threshold = SbMaxEpdCi(7:0) * 256 Cells

Register WAR.DwordSel(1:0) = ’10’:

Bit	15	14	13	12	11	10	9	8
	Accepted/TransmittedPackets(15:8)							

Bit	7	6	5	4	3	2	1	0
	Accepted/TransmittedPackets(7:0)							

Accepted/ Transmitted Packets(15:0) — **Count of Accepted AAL5 Units** within this traffic class. This counter is incremented when a user data cell with AAL_ indication=1 is accepted (Packet end indication in AAL5: PTI= xx1). Do not Write in normal operation. Automatically reset after Read access.

Register WAR.DwordSel(1:0) = ’11’:

Bit	15	14	13	12	11	10	9	8
	DiscardedCells(15:8)							

Bit	7	6	5	4	3	2	1	0
	DiscardedCells(7:0)							

DiscardedCells (15:0) — Count of all discarded cells for this traffic class. Do not Write in normal operation. Automatically reset after Read access.

Internal Table 3: Queue Configuration Table Transfer Registers QCT0..3

Queue Configuration Table Transfer Registers are used to access the internal Queue Configuration Table (QCT) containing 2*1024 entries. The lower 1K entries control the upstream core queues and the upper 1K entries control the downstream core queues. **Table 6-7** shows an overview of the registers involved.

Table 6-7 Registers for Queue Configuration Table Access

63 … 0
QCT RAM entry

15 … 0	15 … 0	15 … 0	15 … 0
QCT3	QCT2	QCT1	QCT0

15 … 0	15 … 0	15 … 0	15 … 0
MASK3 =$FFFF_H$	MASK2 =$FFFF_H$	MASK1	MASK0 =$FFFF_H$

RAM select:

15 … 0
MAR=02_H

Queue select:

15 … 0
WAR (0..2047_D)

QCT0...QCT3 are the transfer registers for one 64 bit QCT table entry. The core selection and queue number representing the table entry which needs to be Read or modified must be written to the Word Address Register (WAR). The dedicated QCT table entry is Read into the QCT0..QCT3 registers or modified by the QCT0..QCT3 register values with a Read-Modify-Write mechanism. The associated Mask Registers MASK0..MASK3 allow a bit-by-bit selection between Read (1) and Write (0) operation. In case of Read operation, the dedicated QCT0..QCT3 register bit will be overwritten by the respective QCT table entry bit value. In case of Write operation, the dedicated QCT0..QCT3 register bit will modify the respective QCT table entry bit value.

Note: It is recommended not to Write to bit fields (64:32) and (15:0) of the QCT table entries; that is, registers MASK0, MASK2 and MASK3 should always be programmed with $FFFF_H$.

The 10 LSBs (= Bit 9..0) of the WAR register select the queue-specific entry that will be accessed and bit 'CoreSel' of the ABM core.

The Read-Modify-Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR select the memory/table that will be accessed; to select the QCT table, bit field MAR(4:0) must be set to 2. Bit 5 of MAR starts the transfer and is automatically cleared after execution of the Read-Modify-Write process.

Table 6-8 WAR Register Mapping for LCI Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(4:0)					CoreSel	QSel(9:8)	

Bit	7	6	5	4	3	2	1	0
	QSel(7:0)							

CoreSel **Selects an ABM Core**:

0 Upstream core selected

1 Downstream core selected

QSel(9:0) **Selects a Queue Entry** within the range (0..1023).

Register 14 QCT0

Queue Configuration Transfer Register 0

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QCT0** **34_H**

Typical Usage: Read by CPU to maintain the QCT table

Bit	15	14	13	12	11	10	9	8
	Unused(1:0)		QueueLength(13:8)					

Bit	7	6	5	4	3	2	1	0
	QueueLength(7:0)							

QueueLength (13:0) Represents the **Current Number of Cells Stored in this Queue**. Do not Write in normal operation.

Register 15 QCT1

Queue Configuration Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QCT1** **35_H**

Typical Usage: Written and Read by CPU to maintain the LCI table

Bit	15	14	13	12	11	10	9	8
	Unused	QIDvalid	TrafClass(3:0)				SID(5:4)	

Bit	7	6	5	4	3	2	1	0
	SID(3:0)				ABRdir	flags(2:0)		

QIDvalid **Queue Enable**:

0 Queue disabled.
An attempt to store a cell to a disabled queue leads to a discard of the cell and a QIDINV interrupt is generated. If a filled queue gets disabled, cells may still be in the queue and they will be Read out. Actual filling of the queue can be obtained via QueueLength(13:0) parameter in the QCT entry.

1 Queue enabled.
Cells are allowed to enter the queue.

TrafClass(3:0) **Traffic Class Number** (0..15)
Assigns the queue to one of the 16 traffic classes defined in the traffic class table TCT for this core.

SID(5:0) **Scheduler Number** (0..47)
Assigns the queue to one of the 48 schedulers of this core.

ABRdir **ABR CI/NI update** of backward RM cells:

0 RM cells of the same core are updated.

1 RM cells of the opposite core are updated.

Note: ABR Congestion Indication is done in RM cells of the backward ABR connection. In Bi-directional Mode, these cells are handled by the opposite core (therefore ABRdir must be 1 for each ABR QID). In Mini-switch Mode, these cells can be handled from the same or opposite core depending on configuration. (If only one core will be used ,ABRdir must be 0 for each ABR QID.)

flag 2 **CI-Flag:**

Whenever a cell is accepted the respective queue threshold values are checked. In case a CI condition is detected, this condition is stored in flag2 for further recognition by resource monitoring operation (ABR).
It is recommended to set this bit to 0 during queue setup.
Do not Write during normal operation.

flag 1 **NI-Flag:**

Whenever a cell is accepted the respective queue threshold values are checked. In case a NI condition is detected, this condition is stored in flag1 for further recognition by resource monitoring operation (ABR).
It is recommended to set this bit to 0 during queue setup.
Do not Write during normal operation.

flag 0 **EFCI-Flag:**

Whenever a cell is accepted the respective queue threshold values are checked. In case a EFCI condition is detected, this condition is stored in flag0 for further recognition by resource monitoring operation (ABR).
It is recommended to set this bit to 0 during queue setup.
Do not Write during normal operation.

Register 16 QCT2

Queue Configuration Transfer Register 2

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QCT2** **36_H**

Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(15:8)							

reserved(13:0) Do not Write in normal operation.

Register 17 QCT3

Queue Configuration Transfer Register 3

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QCT3** **37_H**

Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

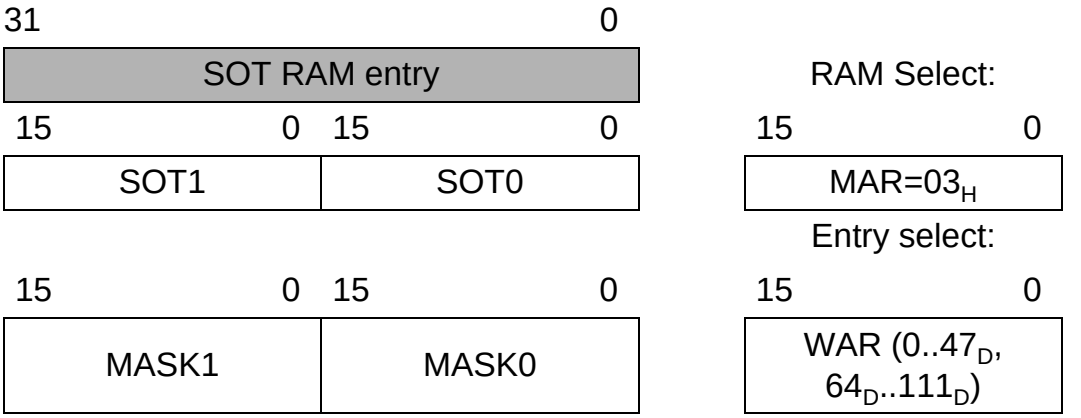
Bit	7	6	5	4	3	2	1	0
	Reserved(15:8)							

reserved(13:0) Do not Write in normal operation.

Internal Table 4: Scheduler Occupancy Table Transfer Registers SOT0, SOT1

The Scheduler Occupancy Table Transfer Registers are used to access the internal Scheduler Occupancy Table (SOT) containing 2*48 entries. **Table 6-9** shows an overview of the registers involved.

Table 6-9 Registers for SOT Table Access



SOT0 and SOT1 are the transfer registers for one 32-bit SOT table entry. The Scheduler number representing the table entry which needs to be Read or modified must be written to the Word Address Register (WAR). The dedicated SOT table entry is Read into the SOT1/SOT0 Registers or modified by the SOT1/SOT0 register values with a Read-Modify-Write mechanism. The associated Mask Registers MASK0 and MASK1 allow a bit-by-bit selection between Read (1) and Write (0) operation. In case of Read operation, the dedicated SOT1/SOT0 register bit will be overwritten by the respective SOT table entry bit value. In case of Write operation, the dedicated SOT1/SOT0 register bit will modify the respective SOT table entry bit value.

The Read-Modify-Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the SOT table, bit field MAR(4:0) must be set to 3. Bit 5 of MAR starts the transfer and is automatically cleared after execution of the Read-Modify-Write process.

Table 6-10 WAR Register Mapping for SOT Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(8:1)							

Bit	7	6	5	4	3	2	1	0
	Unused(0)	CoreSel	SchedSel(5:0)					

CoreSel **Selects an ABM core**:

0 Upstream core selected

1 Downstream core selected

SchedSel(5:0) **Selects one of the 48 core-specific Schedulers**. Only values in the range $0..47_D$ are valid.

Register 18 SOT0

SOT Transfer Register 0

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SOT0** **38_H**

Typical Usage: Written and Read by CPU to maintain the LCI table

Bit	15	14	13	12	11	10	9	8
	LDSTH(7:0)							

Bit	7	6	5	4	3	2	1	0
	LDSTL(7:0)							

LDSTH(7:0) **Level Detection Scheduler Threshold High**.
If the upstream counter SchedOcc(15:0) (SOT1) equals or exceeds this threshold, the corresponding indication bit for this Scheduler in the registers LEVH0..LEVH2 is set to 1. The threshold is defined with a granularity of 256:
Threshold = LDSTH(7:0) * 256 Cells

LDSTL(7:0) **Level Detection Scheduler Threshold Low**.
If the upstream counter SchedOcc(15:0) (SOT1) equals or exceeds this threshold, the corresponding indication bit for this Scheduler in the registers LEVL0..LEVL2 is set to 1. The threshold is defined with a granularity of 256:
Threshold = LDSTL(7:0) * 256 Cells

Note: As soon as the Scheduler fill level falls below a threshold, the corresponding indication bit in registers LEVH0..2 or LEVL0..2 is cleared.

Note: Bit fields LDSTH and LDSTL are provided in the SOT table for the upstream and downstream core as well. But, automatic level detection, by comparing these values with the respective counters SchedOcc(15:0) *and status indication in registers LEVH0..2 and LEVL0..2, is supported* ***for upstream Schedulers only****.*

Register 19 SOT1

SOT Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SOT1** **39_H**

Typical Usage: Read by CPU to maintain the SOT table

Bit	15	14	13	12	11	10	9	8
	SchedOcc(15:8)							

Bit	7	6	5	4	3	2	1	0
	SchedOcc(7:0)							

SchedOcc(15:0) **Count of all cells within this Scheduler** (in all queues and for all traffic classes).
Read only. Do not Write in normal operation.

Register 20 MASK0/MASK1

Table Access Mask Registers 0/1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **MASK0** **$3B_H$** **MASK1** **$3C_H$**

Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	MASK(15:8)							

Bit	7	6	5	4	3	2	1	0
	MASK(7:0)							

MASK0(15:0) **Mask Register 0**

MASK1(15:0) **Mask Register 1**

Mask Registers 0..3 control the Read-Modify-Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (LCI0/LCI1, TCT0/TCT1, QCT0..3, SOT0/SOT1):

0 The dedicated bit of the transfer register is *not* overwritten by the corresponding table entry bit during Read; but overwrites the table entry bit during the Modify-Write process.
This is a Write access to the internal table entry.

1 The dedicated bit of the transfer register is overwritten by the corresponding table entry bit during Read and is written back to the table entry bit during Modify-Write.
This is a Read access to the internal table entry.

Register 21 MASK2/MASK3

Table Access Mask Registers 2/3

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **MASK2** **$3D_H$** **MASK3** **$3E_H$**

Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	MASK(15:8)							

Bit	7	6	5	4	3	2	1	0
	MASK(7:0)							

MASK2(15:0) **Mask Register 2**

MASK3(15:0) **Mask Register 3**

Mask Registers 0..3 control the Read-Modify-Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The Mask Registers correspond to the respective transfer registers (LCI0/LCI1, TCT0/TCT1, QCT0..3, SOT0/SOT1):

0 The dedicated bit of the transfer register is not overwritten by the corresponding table entry bit during Read; but overwrites the table entry bit during the Modify-Write process.
This is a Write access to the internal table entry.

1 The dedicated bit of the transfer register is overwritten by the corresponding table entry bit during Read and is written back to the table entry bit during Modify-Write.
This is a Read access to the internal table entry.

Note: Registers MASK2 and MASK3 are only involved when accessing the Queue Control Table (QCT). Due to the fact that only Read access is recommended for this part of the QCT entries (see Queue Configuration Table Transfer Registers QCT0..3), MASK2 and MASK3 should be programmed to $FFFF_H$ during initialization and should not be changed during operation.

Register 22 CONFIG
Configuration Register

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **41_H**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(13:6)							

Bit	7	6	5	4	3	2	1	0
	Unused(5:0)						Reserved1	ABRTQ

Reserved1 **this bit is for internal use only** and must be set at 0 during normal operation.

ABRTQ **ABR Toggle Queue ID:**
This global bit controls treatment of RM cells for uni-directional (miniswitch) mode.

0 Normal Operation (set for bi-directional mode).

1 Only RM cells with toggled LCI and QID are modified.

Note: The following conditions must apply for proper CI/NI operation:
In Bi-directional Mode, the same LCI and the same queue identifier QID must be used for the ABR connection in forward and backward directions; for example, in forward direction LCI=2 and QID=7, in backward direction LCI=2 and QID=7.
In Uni-directional Mode, LCI and QID must have the LSB inverted; for example, in forward direction LCI=3 and QID=7, in backward direction LCI=2 and QID=6.
The LCI inversion (toggle) is activated by setting the LCI toggle bit in the MODE register to 1.

Register 23 LEVL0

Upstream Scheduler Lower Threshold Reached Indication Register 0

CPU Accessibility: **Read**

Reset Value: **0000_H**

Offset Address: **45_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	SchedIndLow(15:8)							

Bit	7	6	5	4	3	2	1	0
	SchedIndLow(7:0)							

SchedIndLow (15:0) These bits represent the respective upstream scheduler(15:0) and indicate that its lower scheduler threshold configured in the SOT0 table is reached or exceeded; that is, at least as many cells are currently stored as specified by the LDSTL threshold value:

bit i=1 Scheduler i lower threshold reached or exceeded.

Register 24 LEVL1

Upstream Scheduler Lower Threshold Reached Indication Register 1

CPU Accessibility: **Read**

Reset Value: **0000_H**

Offset Address: **46_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	SchedIndLow(31:24)							

Bit	7	6	5	4	3	2	1	0
	SchedIndLow(23:16)							

SchedIndLow (31:16) These bits represent the respective upstream scheduler(31:16) and indicate that its lower scheduler threshold configured in the SOT0 table is reached or exceeded; that is, more cells are currently stored than specified by the LDSTL threshold value:

bit i=1 Scheduler i lower threshold reached or exceeded.

Register 25 LEVL2

Upstream Scheduler Lower Threshold Reached Indication Register 2

CPU Accessibility: **Read**

Reset Value: **0000_H**

Offset Address: **47_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	SchedIndLow(47:40)							

Bit	7	6	5	4	3	2	1	0
	SchedIndLow(39:32)							

SchedIndLow (47:32) These bits represent the respective upstream scheduler(47:32) and indicate that its lower scheduler threshold configured in the SOT0 table is reached or exceeded; that is, more cells are currently stored than specified by the LDSTL threshold value:

bit i=1 Scheduler i lower threshold reached or exceeded.

Register 26 LEVH0

Upstream Scheduler High Threshold Reached Indication Register 0

CPU Accessibility: **Read**

Reset Value: **0000_H**

Offset Address: **48_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	SchedIndHigh(15:8)							

Bit	7	6	5	4	3	2	1	0
	SchedIndHigh(7:0)							

SchedIndHigh (15:0) These bits represent the respective upstream scheduler(15:0) and indicate that its higher scheduler threshold configured in the SOT0 table is reached or exceeded; that is. more cells are currently stored than specified by the LDSTH threshold value:

bit i=1 Scheduler i higher threshold reached or exceeded.

Register 27 LEVH1

Upstream Scheduler High Threshold Reached Indication Register 1

CPU Accessibility: **Read**

Reset Value: **0000_H**

Offset Address: **49_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	SchedIndHigh(31:24)							

Bit	7	6	5	4	3	2	1	0
	SchedIndHigh(23:16)							

SchedIndHigh (31:16) These bits represent the respective upstream scheduler(31:16) and indicate that its lower scheduler threshold configured in the SOT0 table is reached or exceeded; that is, more cells are currently stored than specified by the threshold value:

bit i=1 Scheduler i higher threshold reached or exceeded.

Register 28 LEVH2

Upstream Scheduler High Threshold Reached Indication Register 2

CPU Accessibility: **Read**

Reset Value: **0000_H**

Offset Address: **$4A_H$**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	SchedIndHigh(47:40)							

Bit	7	6	5	4	3	2	1	0
	SchedIndHigh(39:32)							

SchedIndHigh (47:32) These bits represent the respective upstream scheduler(47:32) and indicate that its lower scheduler threshold configured in the SOT0 table is reached or exceeded; that is, more cells are currently stored than specified by the threshold value:

bit i=1 Scheduler i higher threshold reached or exceeded.

Register 29 CDVU/CDVD

Upstream/Downstream Rate Shaper CDV Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **CDVU** **52_H** **CDVD** **72_H**

Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(6:0)							CDV Max(8)

Bit	7	6	5	4	3	2	1	0
	CDVMax(7:0)							

CDVMax(8:0) Maximal Cell Delay Variation (without notice)

This bit-field determines a maximum CDV value for peak rate limited queues that can be introduced without notice.

The CDVMax is measured in multiples of 16-cell cycles.

If this maximum CDV is exceeded, a CDVOV (see registers ISRU/ ISRD) interrupt is generated to indicate an unexpected CDV value. This can occur if multiple peak rate limited queues are scheduled to emit a cell in the same Scheduler time slot.

No cells are discarded due to this event.

Register 30 QMSKU0/QMSKU1
Upstream Queue Parameter Table Mask Registers 0/1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QMSKU0** **55_H** **QMSKU1** **56_H**

Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	QMSKU(15:8)							

Bit	7	6	5	4	3	2	1	0
	QMSKU(7:0)							

QMSKU0(15:0) **Upstream QPT Mask Register 0**

QMSKU1(15:0) **Upstream QPT Mask Register 1**

Mask 0 and 1 control the Read-Modify-Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (QPTHU0/QPTHU1, QPTLU0/QPTLU1):

0 The dedicated bit of the transfer register is not overwritten by the corresponding table entry bit during Read; but overwrites the table entry bit during the Modify-Write process.
This is a Write access to the internal table entry.

1 The dedicated bit of the transfer register is overwritten by the corresponding table entry bit during Read and is written back to the table entry bit during Modify-Write.
This is a Read access to the internal table entry.

Register 31 QMSKD0/QMSKD1

Downstream Queue Parameter Table Mask Registers 0/1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QMSKD0** **75_H** **QMSKD1** **76_H**

Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	QMSKD(15:8)							

Bit	7	6	5	4	3	2	1	0
	QMSKD(7:0)							

QMSKD0(15:0) **Downstream QPT Mask Register 0**

QMSKD1(15:0) **Downstream QPT Mask Register 1**

Mask 0 and 1 control the Read-Modify-Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (QPTHD0/QPTHD1, QPTLD0/QPTLD1):

0 The dedicated bit of the transfer register is not overwritten by the corresponding table entry bit during Read; but overwrites the table entry bit during the Modify-Write. process
This is a Write access to the internal table entry.

1 The dedicated bit of the transfer register is overwritten by the corresponding table entry bit during Read and is written back to the table entry bit during Modify-Write.
This is a Read access to the internal table entry.

Internal Table 5: Queue Parameter Table Transfer Registers

Queue Parameter Table Transfer Registers are used to access the internal Upstream and Downstream Queue Parameter Tables (QPT) containing 2*1024 entries. In both **Table 6-11** and **Table 6-12** provide an overview of the registers involved. Each QPT entry consists of 64 bits, splitted into two 32-bit internal RAMs.

Table 6-11 Registers for QPT Upstream Table Access

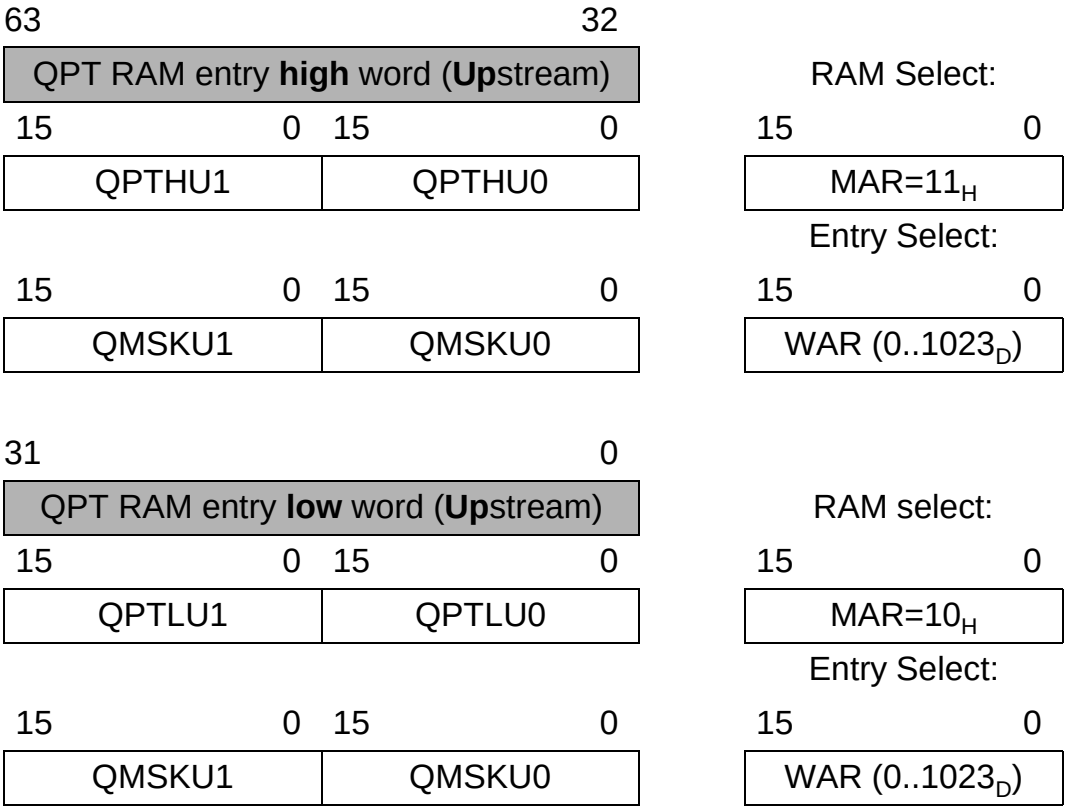
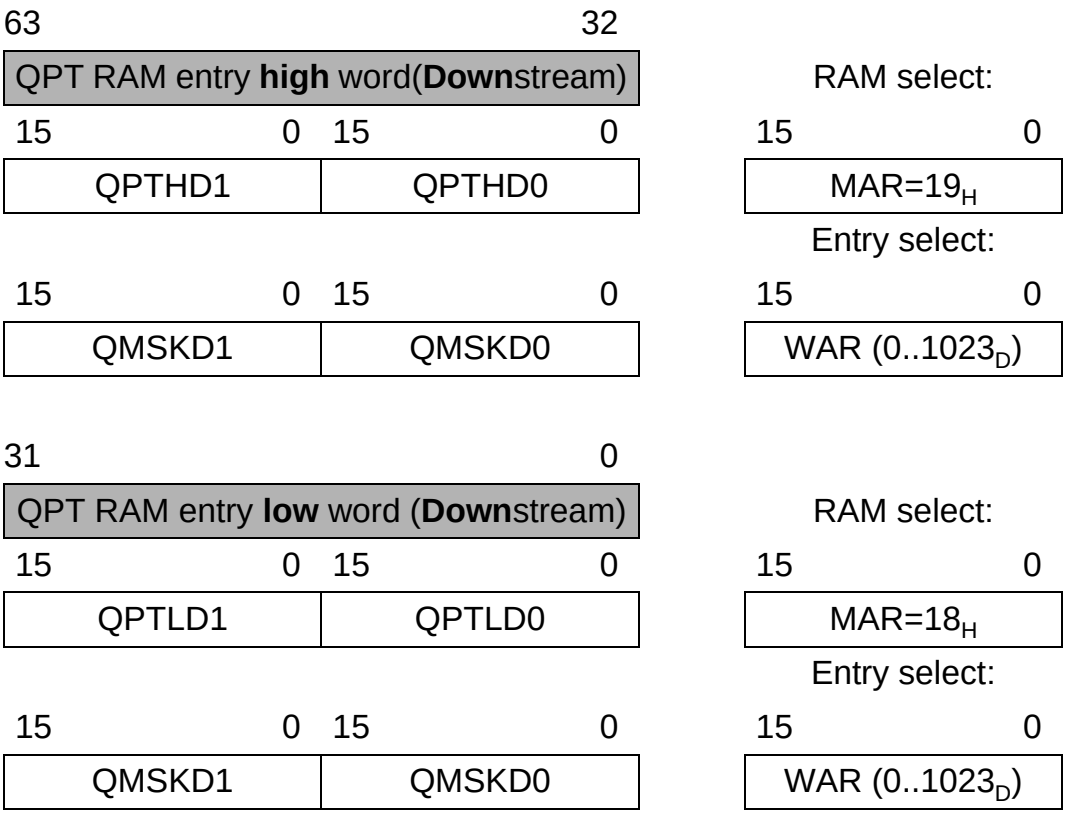


Table 6-12 Registers for QPT Downstream Table Access



QPTHU1 and QPTHU0 are the transfer registers for the 32-bit high word of one upstream QPT table entry. QPTLU1 and QPTLU0 are the transfer registers for the 32-bit low word of one upstream QPT table entry. Access to high and low word are both controlled by mask registers QMSKU1 and QMSKU0.

The register set for accessing the downstream QPT table entries is equal to the upstream set.

The queue number representing the table entry which needs to be Read or modified must be written to the Word Address Register (WAR). The dedicated QPT table entry is Read into the QPTxy1/QPTxy0 registers (x=H,L; y=U,D) or modified by the QPTxy1/ QPTxy0 register values with a Read-Modify-Write mechanism. The associated mask registers QMSKy0 and QMSKy1 allow a bit-by-bit selection between Read (1) and Write (0) operation. In case of Read operation, the dedicated QPTxy1/QPTxy0 register bit will be overwritten by the respective QPT table entry bit value. In case of Write operation, the dedicated QPTxy1/QPTxy0 register bit will modify the respective QPT table entry bit value.

The Read-Modify-Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the QPT table bit field MAR(4:0) must be set to

11_H for QPT upstream table high word,

10_H for QPT upstream table low word,

19_H for QPT downstream table high word,

18_H for QPT downstream table low word.

Bit 5 of MAR starts the transfer and is cleared automatically after execution of the Read-Modify-Write process.

Table 6-13 WAR Register Mapping for QPT Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(5:0)						QueueSel9:8)	

Bit	7	6	5	4	3	2	1	0
	QueueSel(7:0)							

QueueSel(9:0) Selects one of the 1024 queue parameter table entries.

Register 32 QPTLU0/QPTLD0

QPT Upstream/Downstream Low Word Transfer Register 0

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QPTLU0** **60_H** **QPTLD0** **80_H**

Typical Usage: Written by CPU during queue initialization

Bit	15	14	13	12	11	10	9	8
	Reserved(13:6)							

Bit	7	6	5	4	3	2	1	0
	Reserved(5:0)						flags(1:0)	

Reserved(13:0) These bits are used by the device logic. Do not Write to this field as that could lead to complete malfunctioning of the ABM which can be corrected by chip reset only.

flags(1:0) These bits must be written to 0 when initializing the queue. Do not Write during normal operation.

Register 33 QPTLU1/QPTLD1
QPT Upstream/Downstream Low Word Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QPTLU1** **61_H** **QPTLD1** **81_H**

Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Reserved(15:0) These bits are used by the device logic. Do not Write to this field; it could lead to complete malfunctioning of the ABM which can be corrected by chip reset only.

Register 34 QPTHU0/QPTHD0
QPT Upstream/Downstream High Word Transfer Register 0

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QPTHU0** **62_H** **QPTHD0** **82_H**

Typical Usage: Written and Read by CPU to maintain the QPT table

Bit	15	14	13	12	11	10	9	8
	RateFactor(15:8)							

Bit	7	6	5	4	3	2	1	0
	RateFactor(7:0)							

RateFactor(15:0) Controls the Peak Cell Rate of the queue. It is identical to the Rate factor ’m’ described in **"Programming of the Peak Rate Limiter / PCR Shaper" on page 4-58**. The value 0 disables the PCR limiter, that is, the cells from this queue bypass the shaper circuit (see **Figure 3-1**).

Register 35 QPTHU1/QPTHD1
QPT Upstream/Downstream High Word Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QPTHU1** **63_H** **QPTHD1** **83_H**

Typical Usage: Written and Read by CPU to maintain the QPT table

Bit	15	14	13	12	11	10	9	8
	Unused(1:0)		WFQFactor(13:8)					

Bit	7	6	5	4	3	2	1	0
	WFQFactor(7:0)							

WFQFactor (13:0) Determines the weight factor W of the queue at the WFQ multiplexer input to which it is connected. It is identical to the WFQ factor ’n’ in **"Programming of the Peak Rate Limiter / PCR Shaper" on page 4-58**. 1/n = W is the weight factor. The value WFQ factor = 0 connects the queue directly to the priority multiplexor bypassing the WFQ Multiplexer (see **Figure 3-3**). (If more then one queue is connected to the priority multiplexer, then scheduled queues are served with LIFO bahavior).

Internal Table 6: Scheduler Configuration Table Fractional Transfer Registers

The Scheduler Configuration Table Fractional Transfer Registers are used to access the internal Upstream/Downstream Scheduler Configuration Tables Fractional Part (SCTF) containing 48 entries each. **Table 6-14** and **Table 6-15** summarize the registers.

Table 6-14 Registers SCTF Upstream Table Access

15 0	
SCTF RAM Entry (Upstream)	RAM Select:
15 0	15 0
SCTFU	MAR=17_H
	Entry Select:
15 0	15 0
SMSKU	WAR (0..47_D)

Table 6-15 Registers SCTF Downstream Table Access

15 0	
SCTF RAM Entry (Downstream)	RAM Select:
15 0	15 0
SCTFD	MAR=$1F_H$
	Entry Select:
15 0	15 0
SMSKD	WAR (0..47_D)

SCTFU and SCTFD are transfer registers for one 16-bit SCTF upstream/downstream table entry. The upstream and downstream Schedulers use different tables (internal RAMs) addressed via the MAR. The Scheduler number representing the table entry which needs to be Read or modified must be written to the WAR (Word Address Register). The dedicated SCTFU/D table entry is Read into the SCTFU/D registers or modified by the SCTFU/D register value with a Read-Modify-Write mechanism. The associated mask registers, SMSKU and SMSKD, allow a bit-by-bit selection between Read (1) and Write (0) operation. In case of Read operation, the dedicated SCTFU/D register bit will be overwritten by the respective SCTFU/D table entry bit value. In case

of Write operation, the dedicated SCTFU/D register bit will modify the value of the respective SCTFU/D table entry bit.

The Read-Modify-Write process is controlled by the MAR (Memory Address Register). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the SCTF Upstream table, bit field MAR(4:0) must be set to 17_H and $1F_H$ for the SCTF Downstream table respectively. Bit 5 of MAR starts the transfer and is automatically cleared after execution of the Read-Modify-Write process.

Table 6-16 WAR Register Mapping for SCTFU/SCTFD Table access

Bit	15	14	13	12	11	10	9	8
	Unused(9:2)							

Bit	7	6	5	4	3	2	1	0
	Unused(1:0)		SchedSel(5:0)					

SchedSel(5:0) Selects one of the 48 core specific Schedulers. Only values in the range $0..47_D$ are valid.

Register 36 SCTFU/SCTFD

Upstream/Downstream SCTF Transfer Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SCTFU** **96_H** **SCTFD** **$B6_H$**

Typical Usage: Written and Read by CPU to maintain the SCTF tables

Bit	15	14	13	12	11	10	9	8
	Init(7:0)							

Bit	7	6	5	4	3	2	1	0
	FracRate(7:0)							

Init(7:0) **Scheduler Initialization Value**
This bit-field must be written to 00_H at the time of Scheduler configuration/initialization and should not be written during normal operation.

FracRate(7:0) **Fractional Rate**
This value determines the fractional part of the Scheduler output rate.

Note: Recommendation for changing the UTOPIA port number or scheduler rate during operation:
Disable specific scheduler by read-modify-write operation to corresponding bit in registers SCEN0U/SCEN0D... SCEN2U/SCEN2D.
Modify scheduler specific UTOPIA port number and rates via Table 7 "Scheduler Configuration Table Integer Transfer Registers" on page 6-134, registers SCTIU/SCTID and Table 6 "Scheduler Configuration Table Fractional Transfer Registers" on page 6-130, registers SCTFU/SCTFD.
Enable specific scheduler by read-modify-write operation to corresponding bit in registers SCEN0U/SCEN0D... SCEN2U/SCEN2D.

The following formulars explain how the two parameters **IntRate** and **FracRate** determine the scheduler output rate R via an auxiliary parameter T:

$$\mathbf{T} = \frac{\mathrm{SYSCLK}}{32\ \mathrm{cells}^{-1} \times \mathrm{R}} \quad \textbf{[without dimension]}$$

with

- ABM core clock, [SYSCLK} = 1/s
- Scheduler output rate, [R] = cells/s

$$\mathbf{IntRate} = \mathrm{int}(T)$$

with

- int(T) is integer part of T

$$\mathbf{FracRate} = \{T - \mathrm{int}(T)\} \times 256 + 1$$

Thus **IntRate** and **FracRate** can be calculated for a given scheduler output rate R.

Register 37 SMSKU/SMSKD
Upstream/Downstream SCTF Mask Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SMSKU** **95_H** **SMSKD** **$B5_H$**

Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	SMSK(15:8)							

Bit	7	6	5	4	3	2	1	0
	SMSK(7:0)							

SMSKU(15:0) **Upstream SCTF Mask Register**

SMSKD(15:0) **Downstream SCTF Mask Register**

SMSKU and SMSKD control the Read-Modify-Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (SCTFU, SCTFD):

0 The dedicated bit of the transfer register is not overwritten by the corresponding table entry bit during Read; but does overwrite the table entry bit during the Modify-Write process.
This is a Write access to the internal table entry.

1 The dedicated bit of the transfer register is overwritten by the corresponding table entry bit during Read and is written back to the table entry bit during the Modify-Write process.
This is a Read access to the internal table entry.

Internal Table 7: Scheduler Configuration Table Integer Transfer Registers

The Scheduler Configuration Table Integer Transfer Registers are used to access the internal Upstream/Downstream Scheduler Configuration Tables Integer Part (SCTI) containing 48 entries each.

These tables are not addressed by the MAR and WAR regisers, but are addressed via dedicated address registers (SADRU/SADRD) and data registers (SCTIU/SCTID).

Table 6-17 and **Table 6-18** show an overview of the registers involved.

Table 6-17 Registers SCTI Upstream Table Access

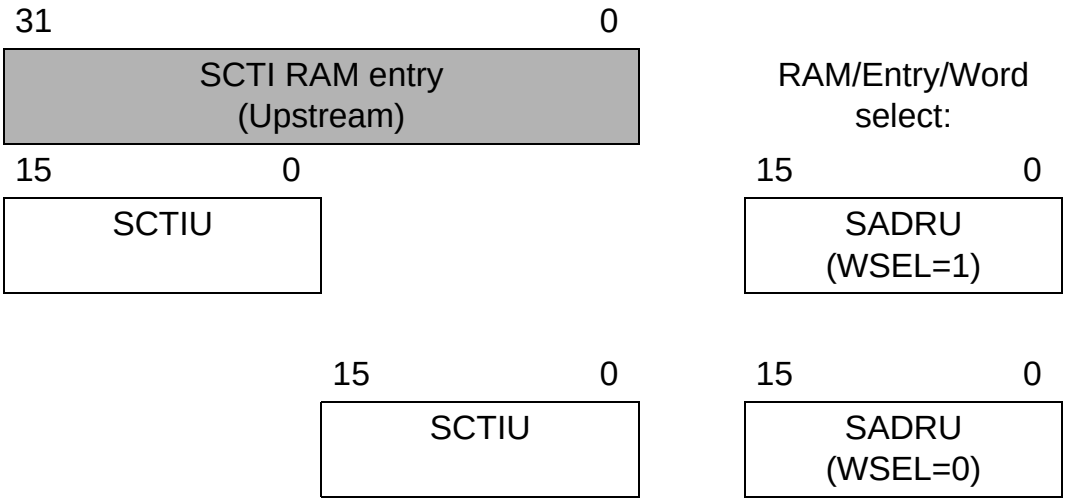
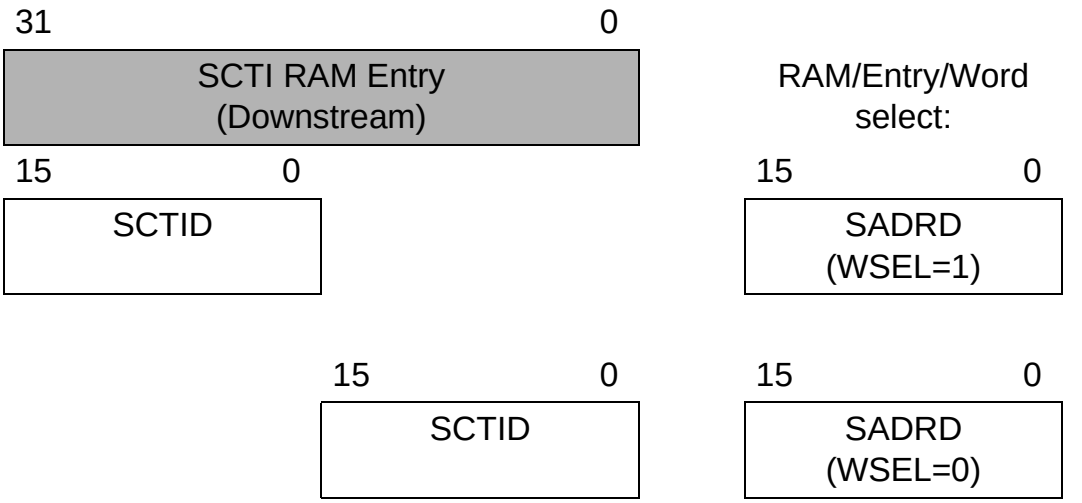


Table 6-18 Registers SCTI Downstream Table Access



SCTIU and SCTID are the transfer registers for the 32-bit SCTI upstream/downstream table entries. The upstream and downstream Schedulers use different tables (internal RAMs) addressed via dedicated registers, SADRU/SADRD. The address registers select the scheduler-specific entry as well as the high or low word of a 32-bit entry to be accessed. Further, there is no command bit, but transfers are triggered via Write access of the address registers and the data registers:

- To initiate a Read access, the Scheduler number must be written to the address register SADRU (upstream) or to the address register SADRD (downstream). One system clock cycle later, the data can be Read from the respective transfer register SCTIU or SCTID.
- To initiate a Write access, it is sufficient to Write the desired Scheduler number to the address registers, SADRU and SADRD, and then Write the desired data to the respective transfer register, SCTIU or SCTID, respectively. The transfer to the integer table is executed one system clock cycle after the Write access to SCTIU or SCTID. Thus, consecutive Write cycles may be executed by the microprocessor.

The SCTI table entries are either read or written. Thus, no additional mask registers are provided for bit-wise control of table entry accesses.

Register 38 SADRU/SADRD

Upstream/Downstream SCTI Address Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SADRU** **90_H** **SADRD** **$B0_H$**

Typical Usage: Written and Read by CPU to maintain the SCTI tables

Bit	15	14	13	12	11	10	9	8
	unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	WSel	0	SchedNo(5:0)					

WSel SCTI table entry **Word Select**

- 1 Selects the high word (bit 31..16) for next access via register SCTIU/SCTID
- 0 Selects the low word (bit 15..0) for next access via register SCTIU/SCTID

SchedNo(5:0) **Scheduler Number**
Selects one of the 48 core-specific Schedulers for next access via register SCTIU/SCTID. Only values in the range $0..47_D$ are valid.

Register 39 SCTIU/SCTID

Upstream/Downstream SCTI Transfer Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SCTIU** **91_H** **SCTID** **$B1_H$**

Typical Usage: Written by CPU to maintain the SCTI tables

Register SADRx.WSel = 0:

Bit	15	14	13	12	11	10	9	8
	unused(1:0)		IntRate(13:8)					

Bit	7	6	5	4	3	2	1	0
	IntRate(7:0)							

IntRate(13:0) **Integer Rate**

This value determines the integer part of the Scheduler output rate.

Note: Recommendation for changing the UTOPIA port number or scheduler rate during operation:
Disable specific scheduler by read-modify-write operation to corresponding bit in registers SCEN0U/SCEN0D... SCEN2U/SCEN2D.
Modify scheduler specific UTOPIA port number and rates via Table 7 "Scheduler Configuration Table Integer Transfer Registers" on page 6-134, registers SCTIU/SCTID and Table 6 "Scheduler Configuration Table Fractional Transfer Registers" on page 6-130, registers SCTFU/SCTFD.
Enable specific scheduler by read-modify-write operation to corresponding bit in registers SCEN0U/SCEN0D... SCEN2U/SCEN2D.

Note: Read access to bit-field IntRate(13:0) is not supported and will return undefined values.

The following formulars explain how the two parameters **IntRate** and **FracRate** determine the scheduler output rate R via an auxiliary parameter T:

$$\mathbf{T} = \frac{\mathrm{SYSCLK}}{32\ \mathrm{cells}^{-1} \times \mathrm{R}} \quad \textbf{[without dimension]}$$

with

- ABM core clock, [SYSCLK} = 1/s
- Scheduler output rate, [R] = cells/s

$$\mathbf{IntRate} = \mathrm{int}(T)$$

with

- int(T) is integer part of T

$$\mathbf{FracRate} = \{T - \mathrm{int}(T)\} \times 256 + 1$$

Thus **IntRate** and **FracRate** can be calculated for a given scheduler output rate R.

Register SADRx.WSel = 1:

Bit	15	14	13	12	11	10	9	8
	Init(10:3)							

Bit	7	6	5	4	3	2	1	0
	Init(2:0)			UtopiaPort(4:0)				

Init(10:0) **Initialization Value**
It is recommended to Write this bit-field to all zeroes during Scheduler configuration/initialization (see note below for further details).

UtopiaPort(4:0) **UTOPIA Port Number**
Specifies one of the 24 UTOPIA ports to which the Scheduler is assigned to. Only values in the range $0..23_D$ are valid. The UTOPIA port number value can be changed during operation (see note below).

The UTOPIA port number can be modified during operation; (port) switch-over is e.g. used for ATM protection switching. The following Notes explain switch-over and rate adaption during operation:

Note: This SCTI table entry should be programmed during Scheduler configuration/ initialization. However the UTOPIA port number value can be modified during operation (e.g. for port switching). In this case the Init(10:0) value can be reset to zero. This bit-field contains a 4 bit counter incrementing the number of unused scheduler cell cycles. Unused cell cycles occur whenever a scheduled event cannot be served, because a previously generated event is still in service (active cell transfer at UTOPIA interface). This counter value is used (and decremented accordingly) to determine the allowed cell burst size for following scheduler events. Such bursts are treated as 'one event' to allow a near 100% scheduler rate utilization. The maximum burst size is programmed in registers ECRIU/ ECRID on page 6-140.
Thus overwriting bit-field Init(10:0) with zero during operation may invalidate some stored cell cycles, only if maximum burst size is programmed >1 for this port.
Only saved scheduler cell cycles can get lost, in no means stored cells can get lost or discarded by these operations.
To minimize even this small impact, value Init(10:0) can be read and written back with the new UTOPIA port number.

Note: Recommendation for changing the UTOPIA port number or scheduler rate during operation:
Disable specific scheduler by read-modify-write operation to corresponding bit in registers SCEN0U/SCEN0D... SCEN2U/SCEN2D.
Modify scheduler specific UTOPIA port number and rates via Table 7 "Scheduler Configuration Table Integer Transfer Registers" on page 6-134, registers SCTIU/ SCTID and Table 6 "Scheduler Configuration Table Fractional Transfer Registers" on page 6-130, registers SCTFU/SCTFD.
Enable specific scheduler by read-modify-write operation to corresponding bit in registers SCEN0U/SCEN0D... SCEN2U/SCEN2D.

Register 40 ECRIU/ECRID
Upstream/Downstream Empty Cycle Rate Integer Part Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **ECRIU** **92_H** **ECRID** **$B2_H$**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	MaxBurstS(3:0)				Unused(1:0)		ECIntRate(9:8)	

Bit	7	6	5	4	3	2	1	0
	ECIntRate(7:0)							

MaxBurstS(3:0) **Maximum Burst size for a Scheduler**

Per scheduler cell bursts can occur due to previously unused cell cycles. Each scheduler has an event generator that determines when this scheduler should be served based on the programmed scheduler rates. Because several schedulers share one UTOPIA interface, it may happen that events cannot be served immediately due to active cell transfers of previous events. Such ’unused cell cycles’ are counted (see also registers SCTIU/SCTID on page 6-137) and can be used for later cell bursts allowing a near 100% scheduler rate utilization. Cell bursts due to this mechanism are not rate limited.

The maximum burst size, generated due to previously counted ’unused cell cycles’, is controlled by bit field MaxBurstS(3:0) in the range 0..15 cells (a minimum value of 1 is recommended).

Maximum burst size dimensioning depends on the burst tolerance of subsequent devices (buffer capacity and backpressure capability).

E.g. if PHY(s) connected to the ABM do not support backpressure and provide a 3 cell transmit buffer, a value in the range 1..3 is recommended to avoid PHY buffer overflows resulting in cell losses (e.g. typical for ADSL PHYs connected to the ABM).

If a PHY is connected that supports port specific backpressure to prevent its transmit buffers from overflowing or provides sufficient buffering, the maximum value of 15 can be programmed guaranteeing a near 100% scheduler rate utilization.

ECIntRate(9:0) **Integer part of Empty Cycle Rate**
The empty cycles are required by internal logic to perform the refresh cycles of the SDRAMS.
Minimum value is 10_H and should be programmed during configuration.

The following formulars explain how the two parameters **ECIntRate** and **ECFracRate** determine the scheduler output rate R via an auxiliary parameter T:

$$T_{max} = \frac{SYSCLK \times RefreshPeriod}{32 \times RefreshCycles} \qquad (8)$$

with:

- ABM core clock SYSCLK = [1/s]
- SDRAM RefreshPeriod = [s]
- SDRAM RefreshCycles requirement

$$\textbf{ECIntRate} = \text{int}(T)$$

with

- int(T) is integer part of T

$$\textbf{ECFracRate} = \{T - \text{int}(T)\} \times 256 + 1$$

Thus **ECIntRate** and **ECFracRate** can be calculated for a given scheduler output rate R.

Register 41 ECRFU/ECRFD

Upstream/Downstream Empty Cycle Rate Fractional Part Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **ECRFU** **93_H** **ECRFD** **$B3_H$**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	ECFracRate(7:0)							

ECFracRate(7:0) **Fractional part of Empty Cycle Rate**
The empty cycles are required by internal logic to perform the refresh cycles of the SDRAMS.
Recommended value is 00_H and should be programmed during configuration.

The following formulars explain how the two parameters **ECIntRate** and **ECFracRate** determine the scheduler output rate R via an auxiliary parameter T:

$$T_{max} = \frac{SYSCLK \times RefreshPeriod}{32 \times RefreshCycles} \qquad (8)$$

with:

- ABM core clock SYSCLK = [1/s]
- SDRAM RefreshPeriod = [s]
- SDRAM RefreshCycles requirement

$$\textbf{ECIntRate} = int(T)$$

with

- int(T) is integer part of T

$$\textbf{ECFracRate} = \{T - int(T)\} \times 256 + 1$$

Thus **ECIntRate** and **ECFracRate** can be calculated for a given scheduler output rate R.

Register 42 CRTQU/CRTQD

Upstream/Downstream Common Real Time Queue UTOPIA Port Select Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **CRTQU** **94_H** **CRTQD** **$B4_H$**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	Unused(10:3)							

Bit	7	6	5	4	3	2	1	0
	Unused(2:0)			CrtqUtopia(4:0)				

CtrqUtopia(4:0) Common Real Time Queue UTOPIA Port Number.
Specifies one of the 24 UTOPIA ports to which the common real time queue is assigned. Only values in the range $0..23_D$ are valid.

Register 43 SCEN0U/SCEN0D
Upstream/Downstream Scheduler Enable 0 Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SCEN0U** **98_H** **SCEN0D** **$B8_H$**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	SchedEn(15:8)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(7:0)							

SchedEn(15:0) **Scheduler Enable**

Each bit position enables/disables the respective Scheduler (15..0):

1 Scheduler enabled

0 Scheduler disabled

Register 44 SCEN1U/SCEN1D
Upstream/Downstream Scheduler Enable 1 Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SCEN1U** **99_H** **SCEN1D** **$B9_H$**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	SchedEn(31:24)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(23:16)							

SchedEn(31:16) **Scheduler Enable**
Each bit position enables/disables the respective Scheduler (31..16):

1 Scheduler enabled

0 Scheduler disabled

Register 45 SCEN2U/SCEN2D
Upstream/Downstream Scheduler Enable 2 Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SCEN2U** **$9A_H$** **SCEN2D** **BA_H**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	SchedEn(47:40)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(39:32)							

SchedEn(47:32) **Scheduler Enable**
Each bit position enables/disables the respective Scheduler (47..32):

1 Scheduler enabled

0 Scheduler disabled

Register 46 ISRU

Interrupt Status Register Upstream

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **ISRU** **$D0_H$**

Typical Usage: Read by CPU to evaluate interrupt events related to the upstream core. Interrupt indications must be cleared by writing a 1 to the respective bit locations; writing a 0 has no effect;

Bit	15	14	13	12	11	10	9	8
	Unused	RAMER	QIDINV	BUFER 1	LCI INVAL	PARITY ER	SOCER	BUFER 2

Bit	7	6	5	4	3	2	1	0
	BUFER 3	CDVOV	MUXOV	BUFER4/ CNTUF	RMCER	BIP8ER	BUFER 5	VCRM ER

RAMER Configuration of common Cell Pointer RAM has been changed after cells have been received (see Register MODE, bit field CPR). (This is a global interrupt shared by both cores. That is, it is not exclusively related to the Upstream Core.)

QIDINV This interrupt is generated if the ABM tries to write a cell into a disabled queue. The cell is discarded in this case. (Typically occurs on queue configuration errors.)

BUFER1 Unexpected buffer error number 1. Should never occur in normal operation. Immediate reset of the chip recommended.

LCIINVAL Cell with invalid LCI received, that is, a LCI value > 8191. The cell is discarded.

PARITYER Parity error at UTOPIA receive upstream (PHY) Interface detected.

SOCER Start of Cell Error at UTOPIA receive upstream (PHY) Interface detected.

BUFER2 Unexpected Buffer Error number 2. Should never occur in normal operation. Immediate reset of the chip is recommended.

BUFER3 Unexpected Buffer Error number 3. Should never occur in normal operation. Immediate reset of the chip is recommended.

CDVOV The maximum upstream CDV value for shaped connections given in CDVU register has been exceeded. This interrupt is a notification only; that is, no cells are discarded due to this event.

MUXOV Indicates that a Scheduler lost a serving time slot. (Can indicate a static backpressure on one port).
The 'MUXOV' interrupt is generated when the number of lost serving time slots exceeds the number specified in bit field MaxBurstS(3:0) (see register ECRIU/ECRID).
No further action is required upon this interrupt.

BUFER4/ CNTUF Indicates that a scheduler specific counter for 'unused cell cycles' has falsely been set to its maximum value by device logic (maximum value is determined by parameter MaxBurstS(3:0) programmed in register ECRIU/ECRID).
This can occur when either the scheduler rate or the UTOPIA port number are changed during operation without disabling the scheduler.
As a consequence a burst of up to MaxBurstS(3:0) cells can be sent out that is not justified by previously saved cell cycles.
No cells are discarded due to this event and no further action is required upon this interrupt.

RMCER ABR RM Cell received with corrupted CRC-10.

BIP8ER BIP-8 error detected when reading a cell from the upstream external SDRAM. BIP-8 protects the cell header of each cell. The cell is discarded. One single sporadic event can be ignored. Hardware should be taken out of service when the error rate exceeds 10^{-10}.

BUFER5 Unexpected Buffer Error number 5. Should never occur in normal operation. Immediate reset of the chip recommended.
For consistency check the ABM stores the queue ID with each cell written to the respective queue within the cell storage RAM. When reading a cell from the cell storage RAM, the queue ID is compared to the stored queue ID.
A queue ID mismatch would indicate a global buffering/pointer problem.

VCRMER VC RM Cell received erroneously when traffic class is configured for ABR VPs using bit ABRvp in Register TCT1
(see **Register 13: TCT1**).

Note: Several mechanisms are implemented in the ABM to check for consistency of pointer operation and internal/external memory control. The interrupt events BUFFER1..BUFFER5 indicate errors detected by these mechanisms.
It is recommended that these interrupts be classified as "fatal device errors."

Register 47 ISRD

Interrupt Status Register Downstream

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **ISRD** **$D1_H$**

Typical Usage: Read by CPU to evaluate interrupt events related to the upstream core. Interrupt indications must be cleared by writing a 1 to the respective bit locations; writing a 0 has no effect;

Bit	15	14	13	12	11	10	9	8
	Unused(1:0)		QIDINV	BUFER 1	LCI INVAL	PARITY ER	SOCER	BUFER 2

Bit	7	6	5	4	3	2	1	0
	BUFER 3	CDVOV	MUXOV	BUFER4/ CNTUF	RMCER	BIP8ER	BUFER 5	VCRM ER

QIDINV This interrupt is generated if the ABM tries to Write a cell into a disabled queue. The cell is discarded.
(Typically occurs on queue configuration errors.)

BUFER1 Unexpected Buffer Error number 1. Should never occur in normal operation. Immediate reset of the chip is recommended.

LCIINVAL Cell with invalid LCI received, i.e. a LCI value >8191. The cell is discarded.

PARITYER Parity Error at UTOPIA receive downstream (PHY) interface detected.

SOCER Start of Cell Error at UTOPIA receive downstream (PHY) interface detected.

BUFER2 Unexpected Buffer Error number 2. Should never occur in normal operation. Immediate reset of the chip is recommended.

BUFER3 Unexpected Buffer Error number 3. Should never occur in normal operation. Immediate reset of the chip recommended.

CDVOV The maximum downstream CDV value for shaped connections given in CDVU register has been exceeded.
This interrupt is a notification only; that is, no cells are discarded due to this event.

MUXOV Indicates that a Scheduler lost a serving time slot. (Can indicate a static backpressure on one port).
The 'MUXOV' interrupt is generated when the number of lost serving time slots exceeds the number specified in bit field MaxBurstS(3:0) (see register ECRIU/ECRID).
No further action is required upon this interrupt.

BUFER4/ CNTUF Indicates that a scheduler specific counter for 'unused cell cycles' has falsely been set to its maximum value by device logic (maximum value is determined by parameter MaxBurstS(3:0) programmed in register ECRIU/ECRID).
This can occur when either the scheduler rate or the UTOPIA port number are changed during operation without disabling the scheduler.
As a consequence a burst of up to MaxBurstS(3:0) cells can be sent out that is not justified by previously saved cell cycles.
No cells are discarded due to this event and no further action is required upon this interrupt.

RMCER ABR RM cell received with corrupted CRC-10.

BIP8ER BIP-8 error detected when reading a cell from the downstream external SDRAM. BIP-8 protects the cell header of each cell. The cell is discarded. One single sporadic event can be ignored. Hardware should be taken out of service when the error rate exceeds 10^{-10}.

BUFER5 Unexpected Buffer Error number 5. Should never occur in normal operation. Immediate reset of the chip is recommended.
For consistency check the ABM stores the queue ID with each cell written to the respective queue within the cell storage RAM. When reading a cell from the cell storage RAM, the queue ID is compared to the stored queue ID.
A queue ID mismatch would indicate a global buffering/pointer problem.

VCRMER VC RM Cell received erroneously, when traffic class is configured for ABR VPs using bit ABRvp TCT1(see **Register 13: TCT1**).

Note: Several mechanisms are implemented in the ABM to check for consistency of pointer operation and internal/external memory control. The interrupt events BUFFER1..BUFFER5 indicate errors detected by these mechanisms.
It is recommended that these interrupts be classified as "fatal device errors."

Register 48 IMRU

Interrupt Mask Register Upstream

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **IMRU** **$D2_H$**

Typical Usage: Written by CPU to control interrupt signal effective events

Bit	15	14	13	12	11	10	9	8
	IMRU(15:8)							

Bit	7	6	5	4	3	2	1	0
	IMRU(7:0)							

IMRU(15:0) Interrupt Mask Upstream
Each bit controls whether the corresponding interrupt indication in register ISRU (same bit location) activates the interrupt signal:

1 Interrupt indication masked.
The interrupt signal is not activated upon this event.

0 Interrupt indication unmasked.
The interrupt signal is activated upon this event.

Register 49 IMRD

Interrupt Mask Register Downstream

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **IMRD** **$D3_H$**

Typical Usage: Written by CPU to control interrupt signal effective events

Bit	15	14	13	12	11	10	9	8
	IMRD(15:8)							

Bit	7	6	5	4	3	2	1	0
	IMRD(7:0)							

IMRD(15:0) **Interrupt Mask Downstream**

Each bit controls whether the corresponding interrupt indication in register ISRD (same bit location) activates the interrupt signal:

1 Interrupt indication masked.
The interrupt signal is not activated upon this event.

0 Interrupt indication unmasked.
The interrupt signal is activated upon this event.

Register 50 MAR

Memory Address Register

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **MAR** **$D7_H$**

Typical Usage: Written by CPU to address internal RAMs/tables for Read-Modify-Write operation via transfer registers

Bit	15	14	13	12	11	10	9	8
	Unused(9:2)							

Bit	7	6	5	4	3	2	1	0
	Unused(1:0)		Start	MAR(4:0)				

Start This command bit starts the Read-Modify-Write procedure to the internal RAM/table addressed by bit-field MAR(4:0). The specific data transfer and mask registers must be prepared appropriately in advance.
This bit is automatically cleared after completion of the Read-Modify-Write procedure.

MAR(4:0) **Memory Address**
This bit-field selects one of the internal RAMs/tables for Read-Modify-Write operation:

00000	LCI: LCI Table RAM (see page 89)
00001	TCT: Traffic Class Table (see page 93)
00010	QCT: Queue Configuration Table (see page 102)
00011	SOT: Scheduler Occupation Table (see page 107)
10001	QPT High Word Upstream: Queue Parameter Table (see page 123)
11001	QPT High Word Downstream: Queue Parameter Table (see page 123)
10000	QPT Low Word Upstream: Queue Parameter Table(see page 123)

11000 QPT Low Word Downstream:
Queue Parameter Table (see page 123)

10111 SCTF Upstream:
Scheduler Configuration Table Fractional Part
(see page 130)

11111 SCTF Downstream:
Scheduler Configuration Table Fractional Part
(see page 130)

Note: The SCTI Table (Scheduler Configuration Table Integer Part) is addressed via dedicated address registers and thus not listed in bit-field MAR(4:0) (see page 134).

Note: MAR(4:0) values not listed above are invalid and reserved. It is recommended to not use invalid/reserved values.

Register 51 WAR

Word Address Register

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **WAR** **$D8_H$**

Typical Usage: Written by CPU to address entries of internal RAMs/ tables for Read-Modify-Write operation via transfer registers.

Bit	15	14	13	12	11	10	9	8
	WAR(15:8)							

Bit	7	6	5	4	3	2	1	0
	WAR(7:0)							

WAR(15:0) **Word Address**

This bit-field selects an entry within the internal RAM/table selected by the MAR reegister.
In general, it can address up to 64K entries.
The current range of supported values depends on the size and organization of the selected RAM/table.
Thus, the specific WAR register meaning is listed in the overview part of each internal RAM/table description:

LCI	LCI Table RAM (see page 89)
TCT	Traffic Class Table (see page 93)
QCT	Queue Configuration Table (see page 107)
SOT	Scheduler Occupation Table (see page 107)
QPTHU	QPT High Word Upstream: Queue Parameter Table (see page 123f.)
QPTHD	QPT High Word Downstream: Queue Parameter Table (see page 123f.)
QPTLU	QPT Low Word Upstream: Queue Parameter Table(see page 123)
QPTLD	QPT Low Word Downstream: Queue Parameter Table (see page 123)

SCTFU SCTF Upstream:
Scheduler Configuration Table Fractional Part
(see page 130)

SCTFD SCTF Downstream:
Scheduler Configuration Table Fractional Part
(see page 130)

Note: The SCTI Table (Scheduler Configuration Table Integer Part) is addressed via dedicated address registers and, thus, is not listed in the MAR and WAR registers (see page 134).

Register 52 UTRXFILL

Upstream UTOPIA Receive FIFO Fill Level Register

CPU Accessibility: **Read**

Reset Value: **0000_H**

Offset Address: **UTRXFILL** **$D9_H$**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(12:5)							

Bit	7	6	5	4	3	2	1	0
	Unused(4:0)					ABMSTATE(2:0)		

ABMSTATE(2:0) Number of cells stored within the UTOPIA Receive Upstream Buffer.
Because of the upstream UTOPIA receive FIFO size, this bit field can carry values in the range 0..4 cells.

Register 53 MODE

ABM Mode Register

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **MODE** **DA_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	SWRES	Unused6	CPR(1:0)		Unused5	INIT RAM	SDRAM	CORE

Bit	7	6	5	4	3	2	1	0
	WGS	BIN	EFCI	BIP8	CRC	LCItog	LCIMOD(1:0)	

SWRES **Software Reset** (reset automatically after four cycles).
This bit is automatically cleared after execution.

1 Starts internal reset procedure

(0) self-clearing

CPR(1:0) Cell Pointer Ram **Size** configuration:
(see also Table 5-4 "External RAMs" on page 5-68)

00 64k pointer entries per direction
(corresponds to 64k cells in each cell storage RAM)

01 32k pointer entries per direction
(corresponds to 32k cells in each cell storage RAM)

10 16k pointer entries per direction
(corresponds to 16k cells in each cell storage RAM)

11 reserved

Note: The Cell Pointer RAM Size should be programmed during initialization and should not be changed during operation.

INITRAM Start of Initialization of the internal RAMs.
This bit is automatically cleared after execution.

1 Starts internal RAMs initialization procedure.

Note: The internal RAM initialization process can be activated only once after hardware reset.

(0) self-clearing

SDRAM Initialization and configuration of the external SDRAMs. This bit must be set to 1 after reset (initial pause of at least 200 µs is necessary) and is automatically cleared by the ABM after configuration of the SDRAMs has been executed.

1 Starts SDRAM initialization procedure

(0) self-clearing

CORE This bit disables the downstream ABM Core, which is necessary in some MiniSwitch configurations (Uni-Directional Mode using one core).
It is recommended to set CORE = 0 in Bi-directional operation modes.

1 Downstream ABM core disabled

0 Downstream ABM core enabled

WGS Selects MiniSwitch (Uni-directional) Mode if set to 1.

1 MiniSwitch (Uni-directional) operation mode selected: upstream transmit UTOPIA interface is disabled; downstream receive UTOPIA interface is disabled.

0 Normal (Bi-directional) operation mode

BIN Indicate the usage of the CI/NI mechanism for ABR connections:

1 Enables CI/NI feedback

0 CI/NI feedback disabled

EFCI Indicate the usage of the EFCI mechanism for ABR connections:

1 Enables EFCI feedback

0 EFCI feedback disabled

BIP8 Disables discard of cells with BIP-8 header error.

1	BIP-8 errored cells are not discarded
0	BIP-8 errored cells are discarded

CRC Disables discard of RM cells with defect CRC10.

1	CRC10 errored RM cells are not discarded
0	CRC10 errored RM cells are discarded

LCItog Enables toggling of the LCI(0) bit in outgoing cells in MiniSwitch (uni-directional) mode.

1	LCI bit zero is toggled in outgoing cells in case of MiniSwitch operation mode selected
0	LCI bit zero remains unchanged

LCIMOD(1:0) Specifies the expected mapping of Local Connection Identifier (LCI) field to cell header:

00	LCI(13, 12) = 0, LCI(11:0) mapped to VPI(11:0) field
01	LCI(13:0) mapped to VCI(13:0) field; VCI(13) = LCI(13) must be zero.
1x	LCI(13:12) mapped to UDF1(7:6) field; LCI(11:0) mapped to VPI(11:0) field

Register 54 UTOPHY0

UTOPIA Configuration Register 0 (PHY Side)

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UTOPHY0 DC_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	unused(4:0)					UTQUEUEOV(6:4)		

Bit	7	6	5	4	3	2	1	0
	UTQUEUEOV(3:0)				BUS	UTPAR	UTCONFIG(1:0)	

UTQUEUEOV (6:0) **UTOPIA Queue Overflow** (downstream transmit)
Bit-field UTQUEUEOV determines the queue overflow level for each UTOPIA queue.

Note: The shared UTOPIA buffer size is 64 cells.

BUS The UTOPIA interface can be used with 16-bit or 8-bit bus width:

0 8-bit mode at PHY side.

1 16-bit mode at PHY side.

UTPAR Enables the parity check at UTOPIA receive upstream interface:

0 Parity check disabled at PHY side

1 Parity check enabled at PHY side

UTCONFIG(1:0) Configuration of port mode at PHY side UTOPIA interface:

00 4 x 6 port

01 3 x 8 port

10 2 x 12 port

11 Level 1 mode (4 x 1 port)

Register 55 UTOPHY1

UTOPIA Configuration Register 1 (PHY Side)

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UTOPHY1** **DD_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	UTPortEnable(15..8)							

Bit	7	6	5	4	3	2	1	0
	UTPortEnable(7..0)							

UTPortEnable (15:0) UTOPIA Port Enable (PHY side):
Each bit enables or disables the respective UTOPIA port (15..0):

bit = 0 Port disabled.

bit = 1 Port enabled.

Register 56 UTOPHY2

UTOPIA Configuration Register 2 (PHY Side)

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UTOPHY2** **DE_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	UTPortEnable(23..16)							

UTPortEnable (23:16) UTOPIA Port Enable (PHY side):
Each bit enables or disables the respective UTOPIA port (23..16):

bit = 0 Port disabled.

bit = 1 Port enabled.

Register 57 UTATM0
UTOPIA Configuration Register 0 (ATM Side)

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UTATM0** **DF_H**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(11:4)							

Bit	7	6	5	4	3	2	1	0
	Unused(3:0)				BUS	UTPAR	UTCONFIG(1:0)	

BUS The UTOPIA interface can be used with 16 bit or 8 bit buswidth:

0 8-bit mode at ATM side.

1 16-bit mode at ATM side.

UTPAR Enables the parity check at UTOPIA receive downstream interface:

0 Parity check disabled at ATM side

1 Parity check enabled at ATM side

UTCONFIG(1:0) Configuration of port mode at ATM side UTOPIA interface:

00 4 x 6 port

01 3 x 8 port

10 2 x 12 port

11 Level 1 mode (4 x 1 port)

Register 58 UTATM1

UTOPIA Configuration Register 1 (ATM Side)

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UTATM1** **$E0_H$**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	UTPortEnable(15..8)							

Bit	7	6	5	4	3	2	1	0
	UTPortEnable(7..0)							

UTPortEnable (15:0) UTOPIA Port Enable (ATM side):
Each bit enables or disables the respective UTOPIA port (15..0):

bit = 0 Port disabled.

bit = 1 Port enabled.

Register 59 UTATM2
UTOPIA Configuration Register 2 (ATM Side)

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UTATM2** **$E1_H$**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	UTPortEnable(23..16)							

UTPortEnable (23:16) UTOPIA Port Enable (ATM side):
Each bit enables or disables the respective UTOPIA port (23..16):

bit = 0 Port disabled.

bit = 1 Port enabled.

Register 60 TEST

TEST Register

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **TEST** **$F0_H$**

Typical Usage: Written and Read by CPU for device test purposes

Bit	15	14	13	12	11	10	9	8
	Unused(1:0)		CLKdelay(1:0)		BistRes(4:1)			

Bit	7	6	5	4	3	2	1	0
	BistRes0	StartBist	flags(5:0)					

CLKDelay(1:0) This bit-field adjusts the delay of TSTCLK output with respect to SYSCLK input.

00	Delay 0
01	Delay 2
10	Delay 4
11	Delay 6

BistRes(4:0) Result of BIST of internal RAMs.
After execution, all five bits must be zero; otherwise, an internal RAM failure was detected.

StartBist Starts internal RAM BIST
Automatically cleared after execution of the Bist procedure.

flags(5:0) This bit-field controls special test modes.
It is recommended to Write all 0s to this bit-field.

Register 61 VERH

Version Number High Register

CPU Accessibility: **Read**

Reset Value: **1003_H**

Offset Address: **VERH** **$F1_H$**

Typical Usage: Read by CPU to determine device version number

Bit	15	14	13	12	11	10	9	8
	VERH(15..8)							

Bit	7	6	5	4	3	2	1	0
	VERH(7..0)							

VERH(15..0) **1003_H**

Register 62 VERL

Version Number Low Register

CPU Accessibility: **Read**

Reset Value: **9083_H**

Offset Address: **VERL** **$F2_H$**

Typical Usage: Read by CPU to determine device version number

Bit	15	14	13	12	11	10	9	8
	VERL(15..8)							

Bit	7	6	5	4	3	2	1	0
	VERL(7..0)							

VERL(15..0) **9083_H**

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PXB	T_A	-40 to 85	°C
Storage temperature	T_{stg}	-40 to 125	°C
IC supply voltage with respect to ground	V_{DD}	-0.3 to 3.6	V
Voltage on any pin with respect to ground	V_S	-0.4 to V_{DD} + 0.4	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2500	V

1) According to MIL-Std 883D, method 3015.7 and ESD Association Standard EOS/ESD-5.1-1993. The RF Pins 20, 21, 26, 29, 32, 33, 34 and 35 are not protected against voltage stress > 300 V (versus V_S or GND). The high frequency performance prohibits the use of adequate protective structures.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating Range

Table 7-2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature under bias	T_A	-40	85	°C	
Junction temperature	T_J		125	°C	
Supply voltage	V_{DD}	3.0	3.6	V	
Ground	V_{SS}	0	0	V	
Power dissipation	P		2.5	W	

Note: In the operating range, the functions given in the circuit description are fulfilled.

7.3 DC Characteristics

Table 7-3 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max		
General Interface Levels *(does not apply to Boundary Scan Interface):*						
Input low voltage	V_{IL}	–0.4		0.8	V	
Input high voltage	V_{IH}	2.0		V_{DD} + 0.3	V	LVTTL (3.3V)
Output low voltage	V_{OL}		0.2	0.4	V	I_{OL} = 5 mA
Output high voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = – 5 mA
Boundary Scan Interface Levels*:*						
(BS) Input low voltage	V_{BS_IL}	–0.4		0.7	V	
(BS) Input high voltage	V_{BS_IH}	2.3		V_{DD} + 0.3	V	Pins: TDI, TCK, TMS
		2.7		V_{DD} + 0.3	V	Pin: $\overline{\text{TRST}}$
(BS) Output low voltage	V_{BS_OL}		0.2	0.4	V	I_{OL} = 5 mA
(BS) Output high voltage	V_{BS_OH}	2.4		V_{DD}	V	I_{OH} = – 5 mA
Average power supply current	I_{CC} (AV)		330		mA	V_{DD} = 3.3 V, T_A = 25 °C, SYSCLK = 52MHz; UTPHYCLK = 52MHz; UTATMCLK = 52MHz;
Average power down supply current	I_{CCPD} (AV)			10	mA	V_{DD} = 3.3 V, T_A = 25 °C, no output loads, no clocks

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max		
Average power dissipation	P (AV)		1	1.3	W	V_{DD} = 3.3 V, T_A = 25 °C, SYSCLK = 52MHz; UTPHYCLK = 52MHz; UTATMCLK = 52MHz;
Input current	I_{IIN}	-1		1	µA	$V_{IN} = V_{DD}$ or V_{SS}
		4		8	µA	$V_{IN} = V_{DD}$ for Inputs with internal Pull-Down resistor
		-4		-8	µA	$V_{IN} = V_{SS}$ for Inputs with internal Pull-Up resistor
Input leakage current	I_{IL}			1	µA	V_{DD} = 3.3 V, GND = 0 V; all other pins are floating
Output leakage current	I_{OZ}			1	µA	V_{DD} = 3.3 V, GND = 0 V; V_{OUT} = 0 V

7.4 AC Characteristics

T_A = -40 to 85 °C, V_{CC} = 3.3 V ± 9 %, V_{SS} = 0 V

All inputs are driven to V_{IH} = 2.4 V for a logical 1
and to V_{IL} = 0.4 V for a logical 0

All outputs are measured at V_H = 2.0 V for a logical 1
and at V_L = 0.8 V for a logical 0

The AC testing input/output waveforms are shown below.

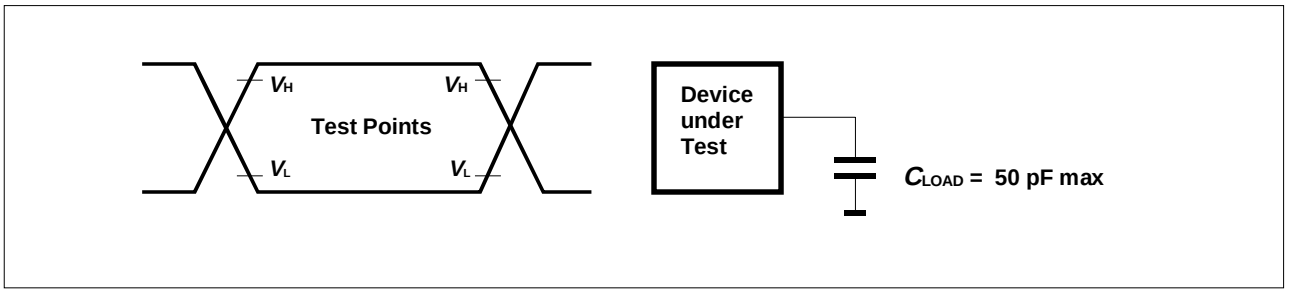


Figure 7-1 Input/Output Waveform for AC Measurements

Table 7-4 Clock Frequencies

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Core clock	SYSCLK	25	52	MHz
UTOPIA clock at PHY-side	UTPHYCLK	$f_{SYSCLK}/2$	$\leq f_{SYSCLK}$	MHz
UTOPIA clock at ATM-side	UTATMCLK	$f_{SYSCLK}/2$	$\leq f_{SYSCLK}$	MHz
µP clock[1)]			$\leq f_{SYSCLK}$	MHz

1) Supplied only to external microprocessor

7.4.1 Microprocessor Interface Timing Intel Mode

7.4.1.1 Microprocessor Write Cycle Timing (Intel)

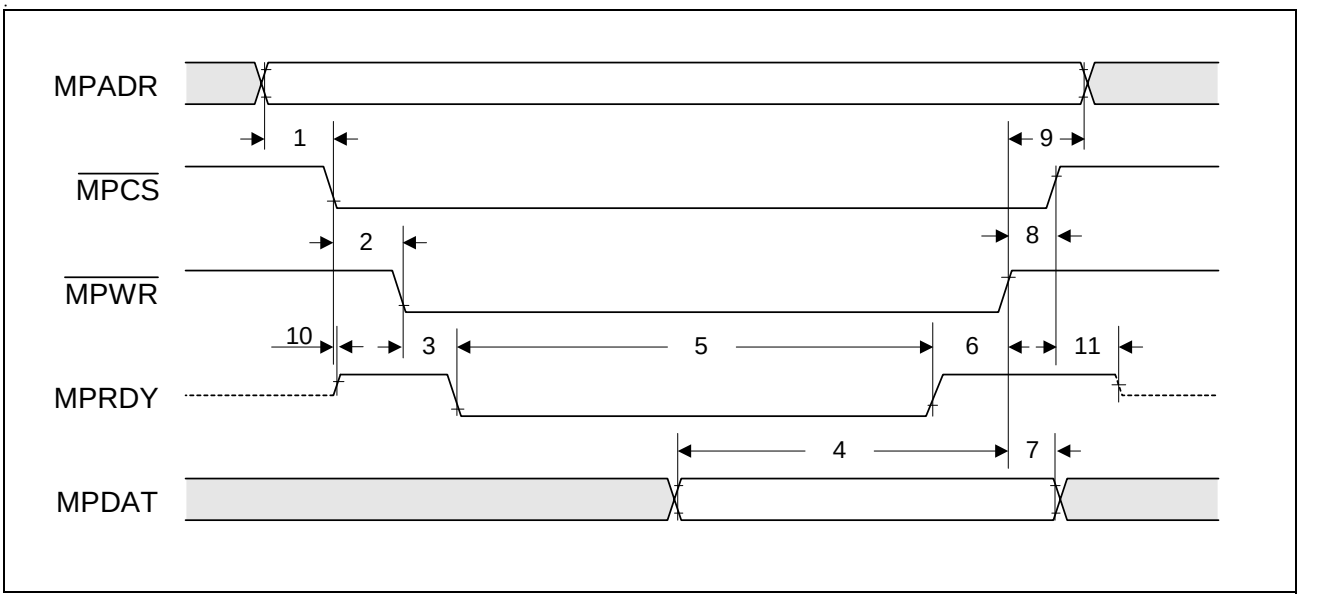


Figure 7-2 Microprocessor Interface Write Cycle Timing (Intel)

Table 7-5 Microprocessor Interface Write Cycle Timing (Intel)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	MPADR setup time before $\overline{\text{MPCS}}$ low	0			ns
2	$\overline{\text{MPCS}}$ setup time before $\overline{\text{MPWR}}$ low	0			ns
3	MPRDY low delay after $\overline{\text{MPWR}}$ low	0		20	ns
4	MPDAT setup time before $\overline{\text{MPWR}}$ high	5			ns
5	Pulse width MPRDY low	3 SYSCLK cycles		4 SYSCLK cycles	
6	MPRDY high to $\overline{\text{MPWR}}$ high	5			ns
7	MPDAT hold time after $\overline{\text{MPWR}}$ high	5			ns
8	$\overline{\text{MPCS}}$ hold time after $\overline{\text{MPWR}}$ high	5			ns
9	MPADR hold time after $\overline{\text{MPWR}}$ high	5			ns
10	$\overline{\text{MPCS}}$ low to MPRDY low impedance	0			ns
11	$\overline{\text{MPCS}}$ high to MPRDY high impedance			15	ns

7.4.1.2 Microprocessor Read Cycle Timing (Intel)

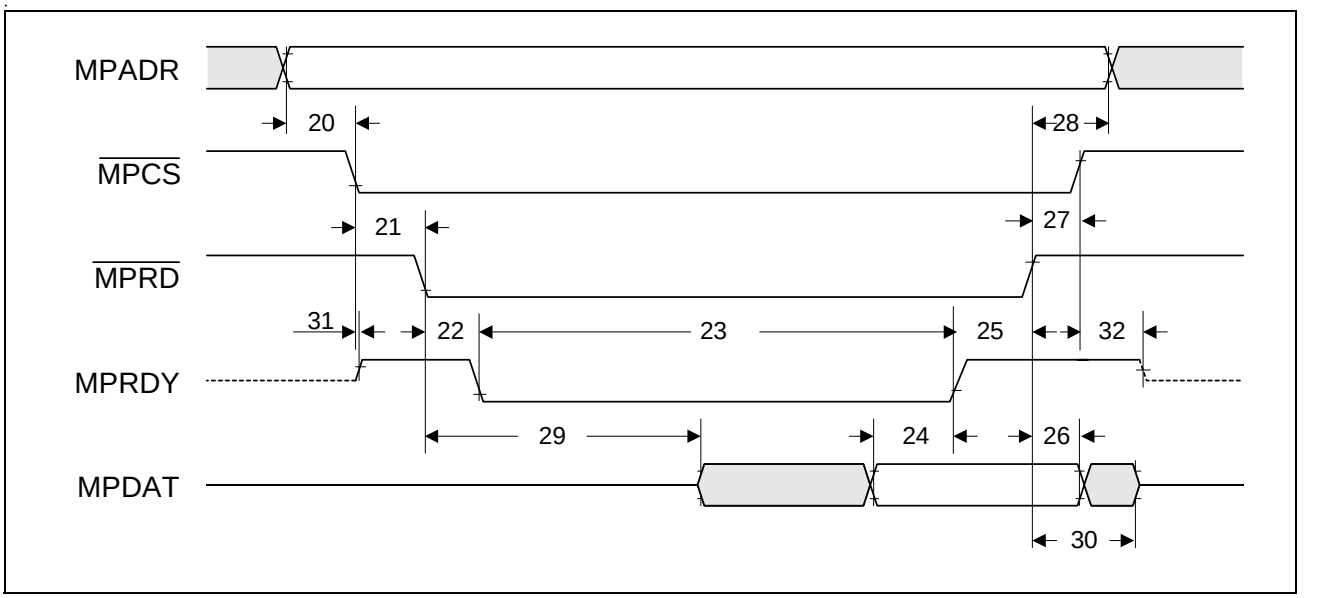


Figure 7-3 Microprocessor Interface Read Cycle Timing (Intel)

Table 7-6 Microprocessor Interface Read Cycle Timing (Intel)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
20	MPADR setup time before $\overline{\text{MPCS}}$ low	0			ns
21	$\overline{\text{MPCS}}$ setup time before $\overline{\text{MPRD}}$ low	0			ns
22	MPRDY low delay after $\overline{\text{MPRD}}$ low	0		20	ns
23	Pulse width MPRDY low	4 SYSCLK cycles		5 SYSCLK cycles	
24	MPDAT valid before MPRDY high	5			ns
25	MPRDY high to $\overline{\text{MPRD}}$ high	5			ns
26	MPDAT hold time after $\overline{\text{MPRD}}$ high	2			ns
27	$\overline{\text{MPCS}}$ hold time after $\overline{\text{MPRD}}$ high	5			ns
28	MPADR hold time after $\overline{\text{MPRD}}$ high	5			ns
29	$\overline{\text{MPRD}}$ low to MPDAT low impedance	0		15	ns
30	$\overline{\text{MPRD}}$ high to MPDAT high impedance	0		17	ns
31	$\overline{\text{MPCS}}$ low to MPRDY low impedance	0			ns
32	$\overline{\text{MPCS}}$ high to MPRDY high impedance			15	ns

7.4.2 Microprocessor Interface Timing Motorola Mode

7.4.2.1 Microprocessor Write Cycle Timing (Motorola)

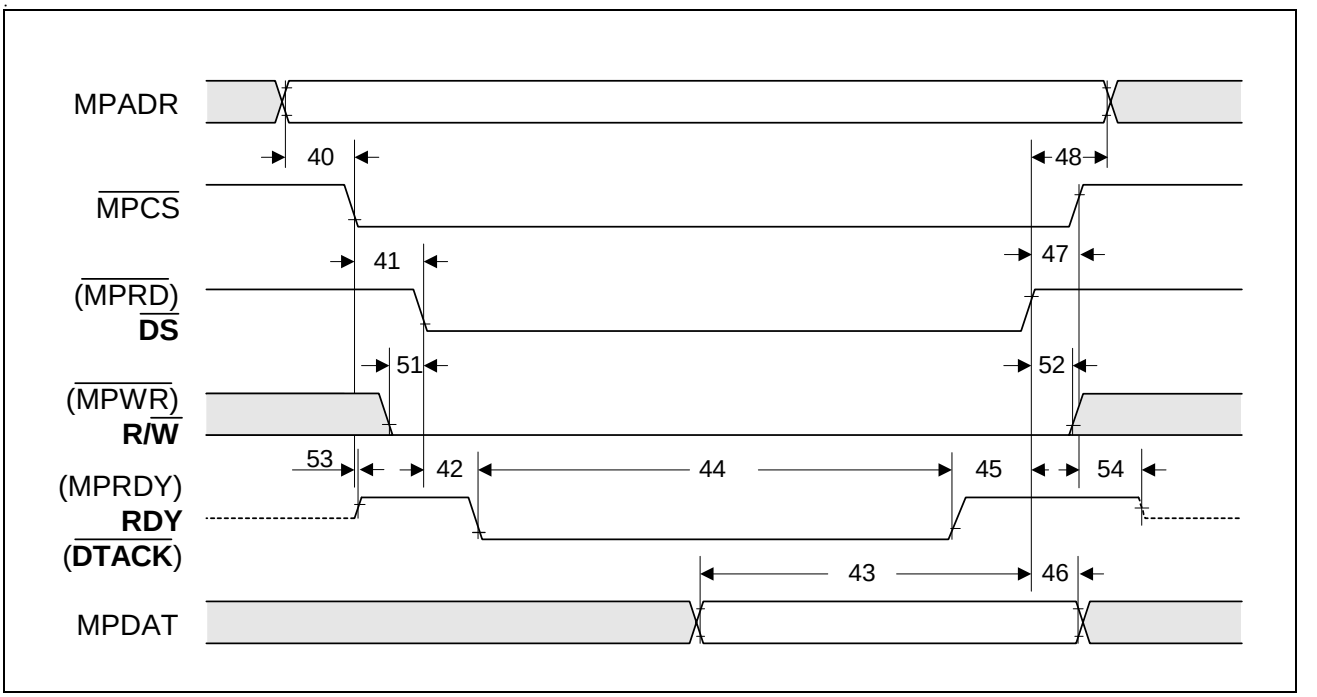


Figure 7-4 Microprocessor Interface Write Cycle Timing (Motorola)

Table 7-7 Microprocessor Interface Write Cycle Timing (Motorola)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
40	MPADR setup time before $\overline{\text{MPCS}}$ low	0			ns
41	$\overline{\text{MPCS}}$ setup time before $\overline{\text{DS}}$ low	0			ns
42	RDY low delay after $\overline{\text{DS}}$ low	0		20	ns
43	MPDAT setup time before $\overline{\text{DS}}$ high	5			ns
44	Pulse width RDY low	3 SYSCLK cycles		4 SYSCLK cycles	
45	RDY high to $\overline{\text{DS}}$ high	5			ns
46	MPDAT hold time after $\overline{\text{DS}}$ high	5			ns
47	$\overline{\text{MPCS}}$ hold time after $\overline{\text{DS}}$ high	5			ns
48	MPADR hold time after $\overline{\text{DS}}$ high	5			ns
51	R/$\overline{\text{W}}$ setup time before $\overline{\text{DS}}$ low	10			ns

Table 7-7 Microprocessor Interface Write Cycle Timing (Motorola)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
52	R/$\overline{W}$ hold time after $\overline{DS}$ high	0			ns
53	$\overline{MPCS}$ low to RDY low impedance	0			ns
54	$\overline{MPCS}$ high to RDY high impedance			15	ns

7.4.2.2 Microprocessor Read Cycle Timing (Motorola)

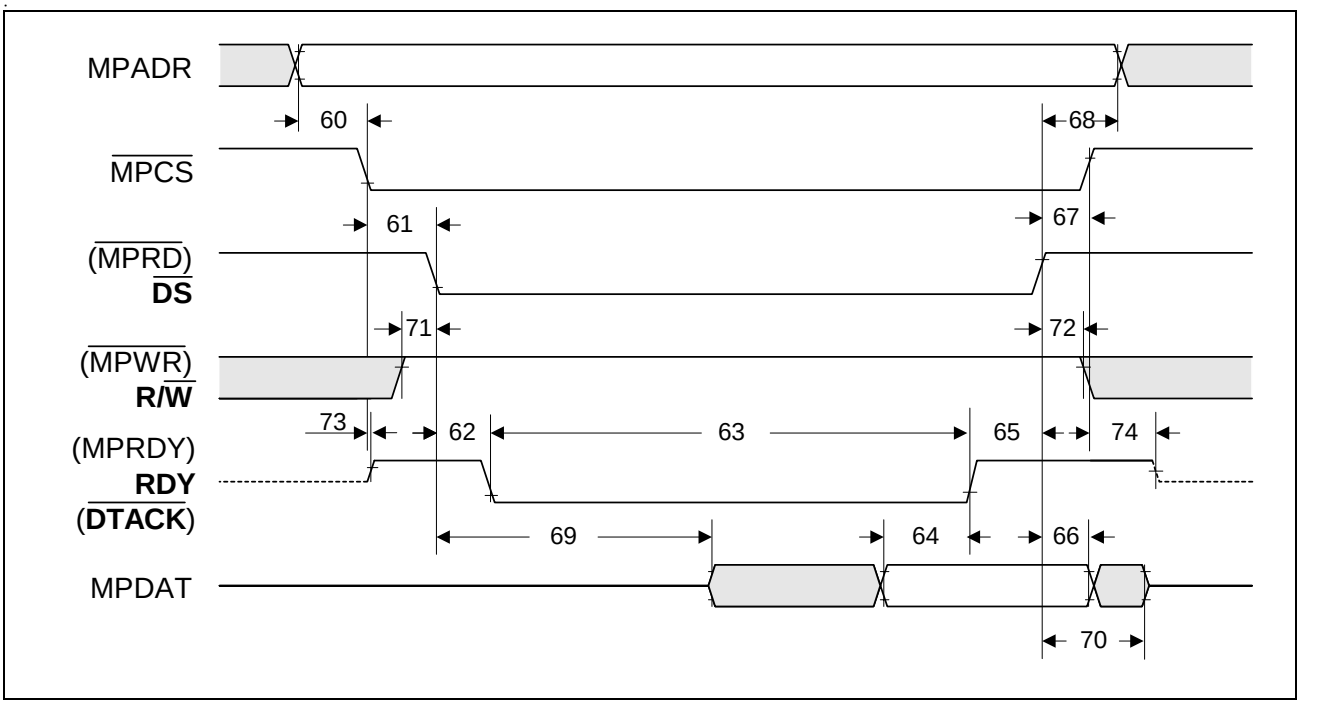


Figure 7-5 Microprocessor Interface Read Cycle Timing (Motorola)

Table 7-8 Microprocessor Interface Read Cycle Timing (Motorola)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
60	MPADR setup time before $\overline{\text{MPCS}}$ low	0			ns
61	$\overline{\text{MPCS}}$ setup time before $\overline{\text{DS}}$ low	0			ns
62	RDY low delay after $\overline{\text{DS}}$ low	0		20	ns
63	Pulse width RDY low	4 SYSCLK cycles		5 SYSCLK cycles	
64	MPDAT valid before RDY high	5			ns
65	RDY high to $\overline{\text{DS}}$ high	5			ns
66	MPDAT hold time after $\overline{\text{DS}}$ high	2			ns
67	$\overline{\text{MPCS}}$ hold time after $\overline{\text{DS}}$ high	5			ns
68	MPADR hold time after $\overline{\text{DS}}$ high	5			ns
69	$\overline{\text{DS}}$ low to MPDAT low impedance	0		15	ns
70	$\overline{\text{DS}}$ high to MPDAT high impedance	0		17	ns
71	R/$\overline{\text{W}}$ setup time before $\overline{\text{DS}}$ low	10			ns

Table 7-8 Microprocessor Interface Read Cycle Timing (Motorola)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
72	R/$\overline{W}$ hold time after $\overline{DS}$ high	0			ns
73	$\overline{MPCS}$ low to RDY low impedance	0			ns
74	$\overline{MPCS}$ high to RDY high impedance			15	ns

7.4.3 UTOPIA Interface

The AC characteristics of the UTOPIA Interface fulfill the standard of [1] and [2]. Setup and hold times of the 50 MHz UTOPIA Specification are valid.

According to the UTOPIA Specification, the AC characteristics are based on the timing specification for the receiver side of a signal. The setup and the hold times are defined with regards to a positive clock edge, see **Figure 7-6**.

Taking into account the actual clock frequency (up to the maximum frequency), the corresponding (min. and max.) transmit side "clock to output" propagation delay specifications can be derived. The timing references (tT5 to tT12) are according to the data found in **Table 7-9** to **Table 7-12**.

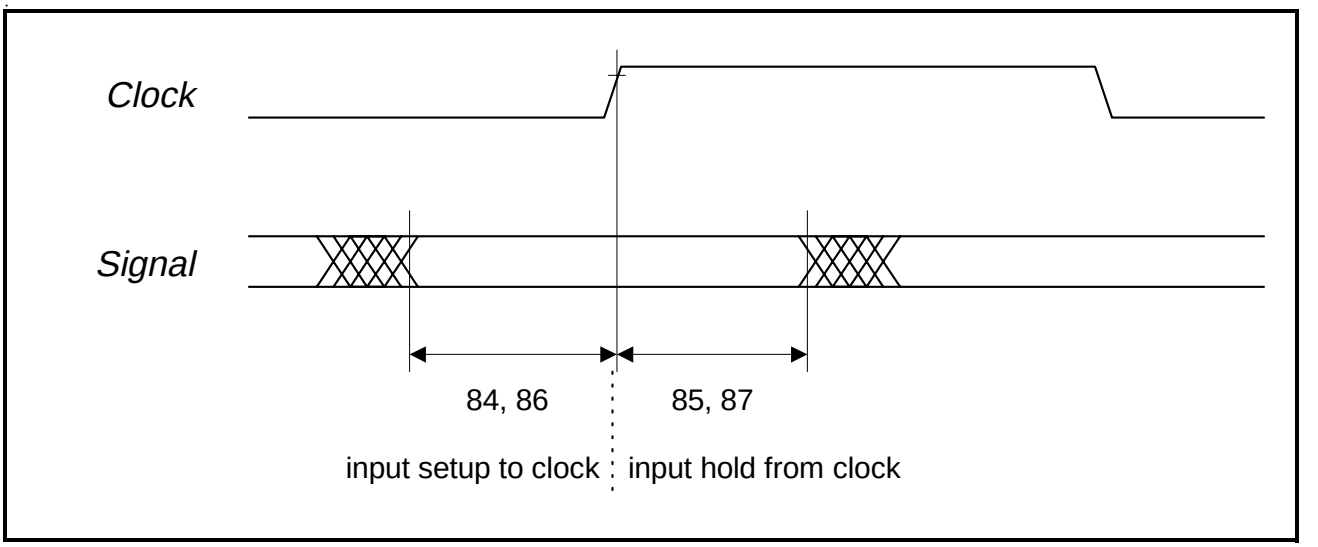


Figure 7-6 Setup and Hold Time Definition (Single- and Multi-PHY)

Figure 7-7 shows the tristate timing for the multi-PHY application (multiple PHY devices, multiple output signals are multiplexed together).

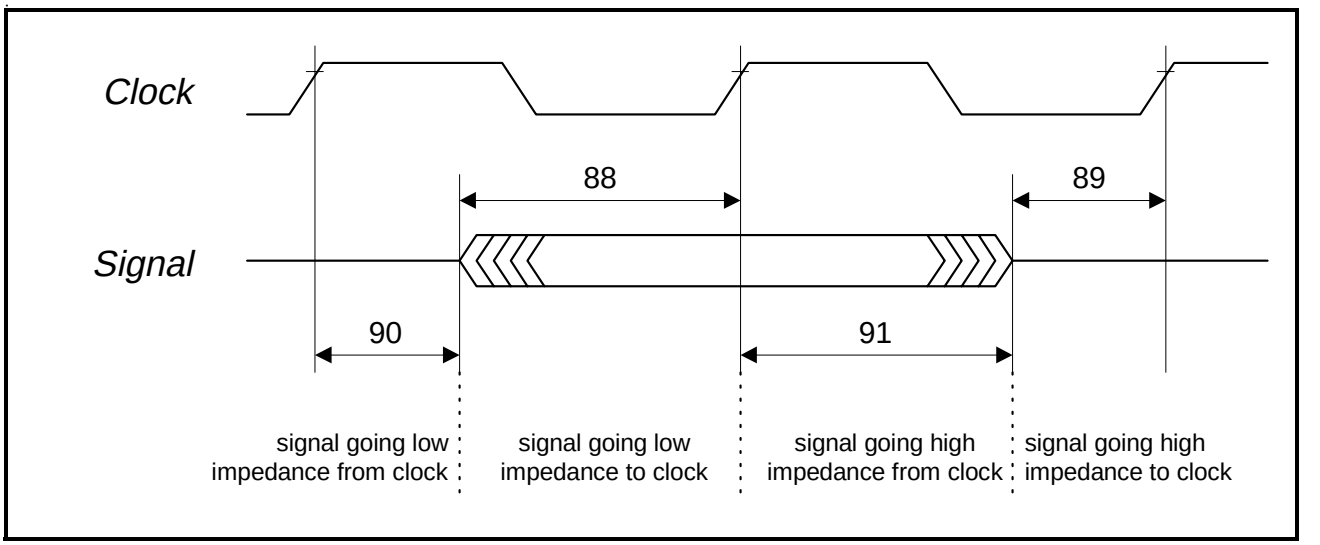


Figure 7-7 Tristate Timing (Multi-PHY, Multiple Devices Only)

In the following tables, A⇒P (column DIR, Direction) defines a signal from the ATM Layer (transmitter, driver) to the PHY Layer (receiver), A⇐P defines a signal from the PHY Layer (transmitter, driver) to the ATM Layer (receiver).

All timings also apply to UTOPIA Level 1 8-bit data bus operation.

Table 7-9 Transmit Timing (16-Bit Data Bus, 50 MHz at Cell Interface, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	TXCLK	A>P	TxClk frequency (nominal)	0	52	MHz
81			TxClk duty cycle	40	60	%
82			TxClk peak-to-peak jitter	-	5	%
83			TxClk rise/fall time	-	2	ns
84	TXDAT[15:0], TXPTY, TXSOC, TXENB	A>P	Input setup to TxClk	4	-	ns
85			Input hold from TxClk	1	-	ns
86	TXCLAV	A<P	Input setup to TxClk	4	-	ns
87			Input hold from TxClk	1	-	ns

Table 7-10 Receive Timing (16-Bit Data Bus, 50 MHz at Cell Interface, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	RXCLK	A>P	RxClk frequency (nominal)	0	52	MHz
81			RxClk duty cycle	40	60	%
82			RxClk peak-to-peak jitter	-	5	%
83			RxClk rise/fall time	-	2	ns
84	$\overline{\text{RXENB}}$	A>P	Input setup to RxClk	4	-	ns
85			Input hold from RxClk	1	-	ns
86	RXDAT[15:0], RXPTY, RXSOC, RXCLAV	A<P	Input setup to RxClk	4	-	ns
87			Input hold from RxClk	1	-	ns

Table 7-11 Transmit Timing (16-Bit Data Bus, 50 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	TXCLK	A>P	TxClk frequency (nominal)	0	52	MHz
81			TxClk duty cycle	40	60	%
82			TxClk peak-to-peak jitter	-	5	%
83			TxClk rise/fall time	-	2	ns
84	TXDAT[15:0], TXPTY, $\underline{\text{TXSOC}}$, TXENB, TXADR[4:0]	A>P	Input setup to TxClk	4	-	ns
85			Input hold from TxClk	1	-	ns

Table 7-11 Transmit Timing (16-Bit Data Bus, 50 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
86	TXCLAV	A<P	Input setup to TxClk	4	-	ns
87			Input hold from TxClk	1	-	ns
88			Signal going low impedance to TxCLK	4	-	ns
89			Signal going high impedance to TxCLK	0	-	ns
90			Signal going low impedance from TxCLK	1	-	ns
91			Signal going high impedance from TxCLK	1	-	ns

Table 7-12 Receive Timing (16-Bit Data Bus, 50 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	RXCLK	A>P	RxClk frequency (nominal)	0	52	MHz
81			RxClk duty cycle	40	60	%
82			RxClk peak-to-peak jitter	-	5	%
83			RxClk rise/fall time	-	2	ns
84	$\overline{\text{RXENB}}$, RXADR[4:0]	A>P	Input setup to RxClk	4	-	ns
85			Input hold from RxClk	1	-	ns

Table 7-12 Receive Timing (16-Bit Data Bus, 50 MHz at Cell Interface, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
86	RXDAT[15:0], RXPTY, RXSOC, RXCLAV	A<P	Input setup to RxClk	4	-	ns
87			Input hold from RxClk	1	-	ns
88			Signal going low impedance to RxCLK	4	-	ns
89			Signal going high impedance to RxCLK	0	-	ns
90			Signal going low impedance from RxCLK	1	-	ns
91			Signal going high impedance from RxCLK	1	-	ns

7.4.4 SSRAM Interface

Timing of the Synchronous Static RAM Interfaces is simplified as all signals are referenced to the rising edge of SYSCLK. In **Figure 7-8**, it can be seen that all signals output by the PXB 4330 E ABM have identical delay times with reference to the clock. When reading from the RAM, the PXB 4330 E ABM samples the data within a window at the rising clock edge.

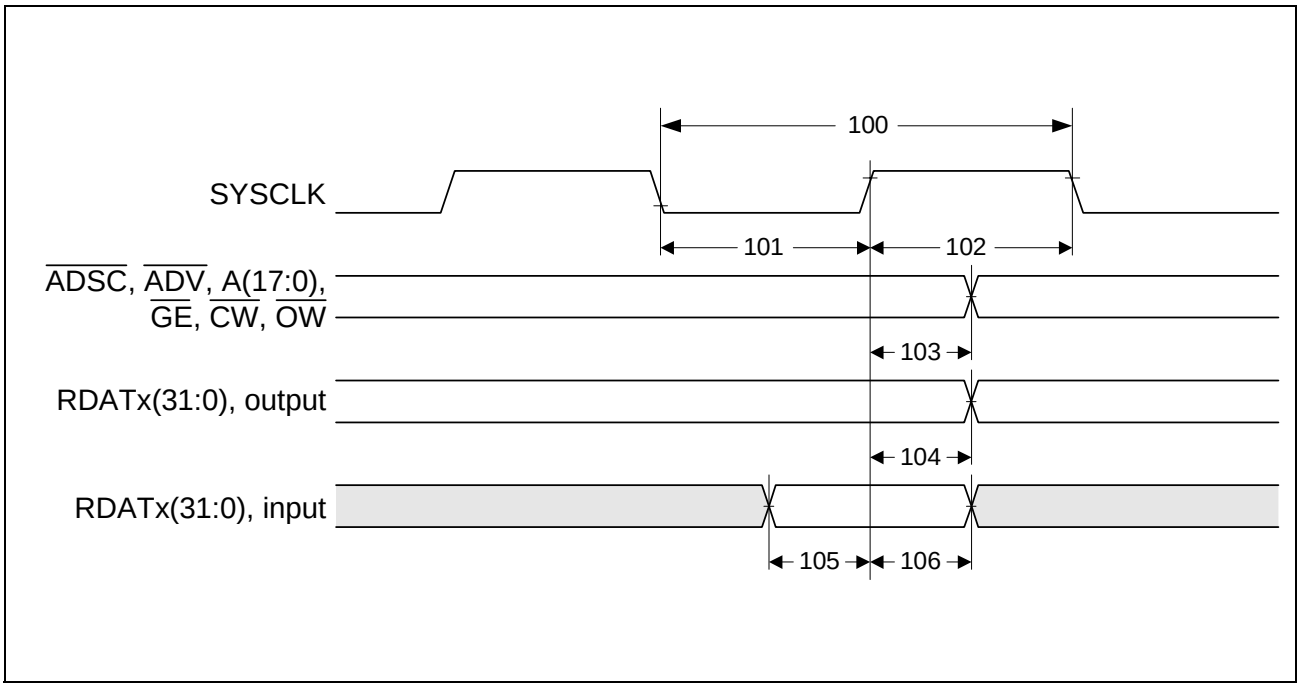


Figure 7-8 SSRAM Interface Generic Timing Diagram

Table 7-13 SSRAM Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
100	T_{SYSCLK} : Period SYSCLK	19.3			ns
100A	F_{SYSCLK} : Frequency SYSCLK			52	MHz
101	SYSCLK Low Pulse Width	7.3			ns
102	SYSCLK High Pulse Width	7.3			ns
103	Delay SYSCLK rising to $\overline{ADSC}$, A(17:0), $\overline{GW}$, $\overline{CE}$, $\overline{OE}$	2		16	ns
104	Delay SYSCLK rising to RDATx Output	2		16	ns

Table 7-13 SSRAM Interface AC Timing Characteristics (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
105	Setup time RDATx Input before SYSCLK rising (read cycles)	5			ns
106	Hold time RDATx Input after SYSCLK rising (read cycles)	3			ns

7.4.5 SDRAM Interface

Timing of the Synchronous Dynamic RAM Interface is simplified as all signals are referenced to the rising edge of SYSCLK. In **Figure 7-9**, it can be seen that all signals output by the PXB 4330 E ABM have identical delay times with reference to the clock. When reading from the RAM, the PXB 4330 E ABM samples the data within a window at the rising clock edge.

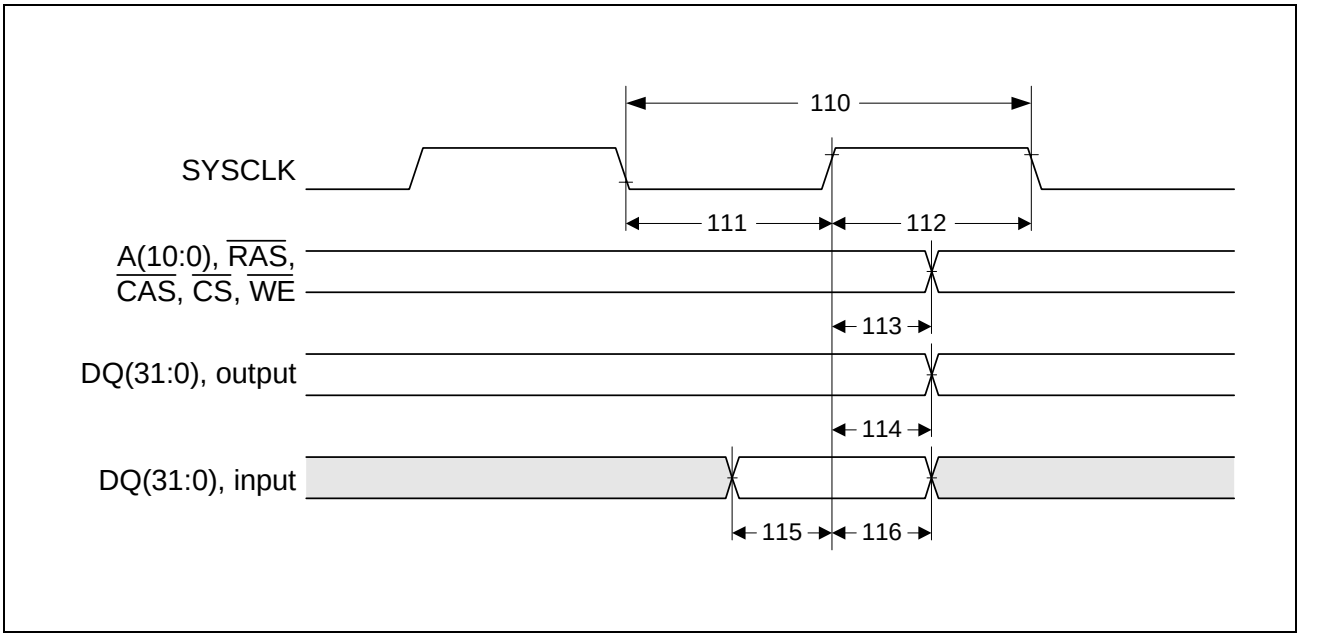


Figure 7-9 Generic SDRAM Interface Timing Diagram

Table 7-14 SDRAM Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
110	T_{SYSCLK} : Period SYSCLK	19.3			ns
110A	F_{SYSCLK} : Frequency SYSCLK			52	MHz

Table 7-14 SDRAM Interface AC Timing Characteristics (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
111	SYSCLK Low Pulse Width	7.3			ns
112	SYSCLK High Pulse Width	7.3			ns
113	Delay SYSCLK rising to $\overline{\text{ADSC}}$, A(17:0), $\overline{\text{GW}}$, $\overline{\text{CE}}$, $\overline{\text{OE}}$	2		16	ns
114	Delay SYSCLK rising to RDATx Output	3		16	ns
115	Setup time RDATx Input before SYSCLK rising (read cycles)	4			ns
116	Hold time RDATx Input after SYSCLK rising (read cycles)	2			ns

7.4.6 Reset Timing

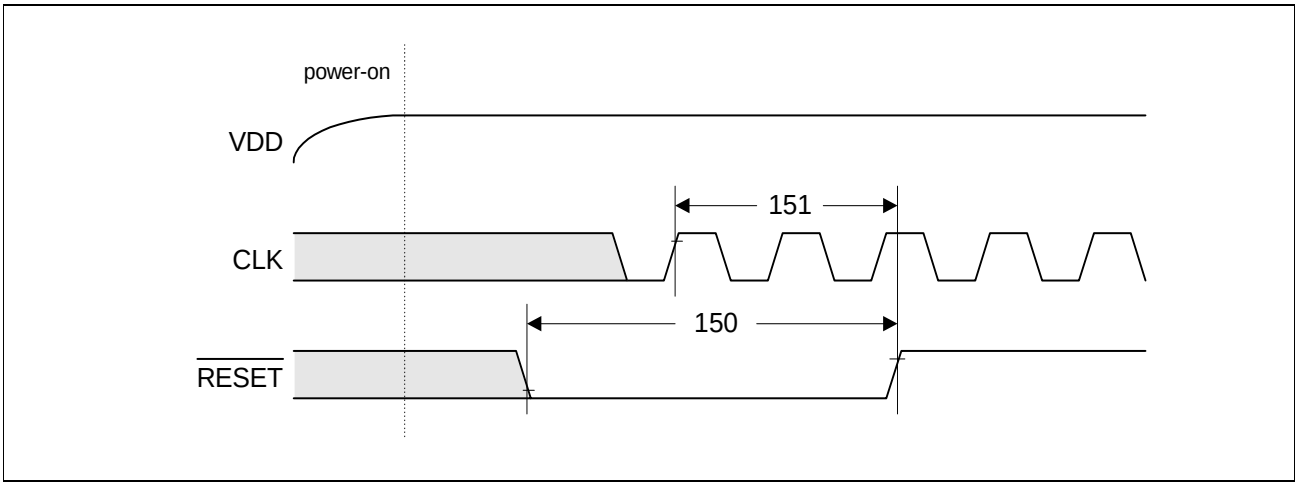


Figure 7-10 Reset Timing

Table 7-15 Reset Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
150	RESET pulse width	120		ns
151	Number of SYSCLK cycles during RESET active	2		SYSCLK cycles

Note: RESET may be asynchronous to CLK when asserted or deasserted. RESET may be asserted during power-up or asserted after power-up. Nevertheless, deassertion must be at a clean, bounce-free edge.

7.4.7 Boundary-Scan Test Interface

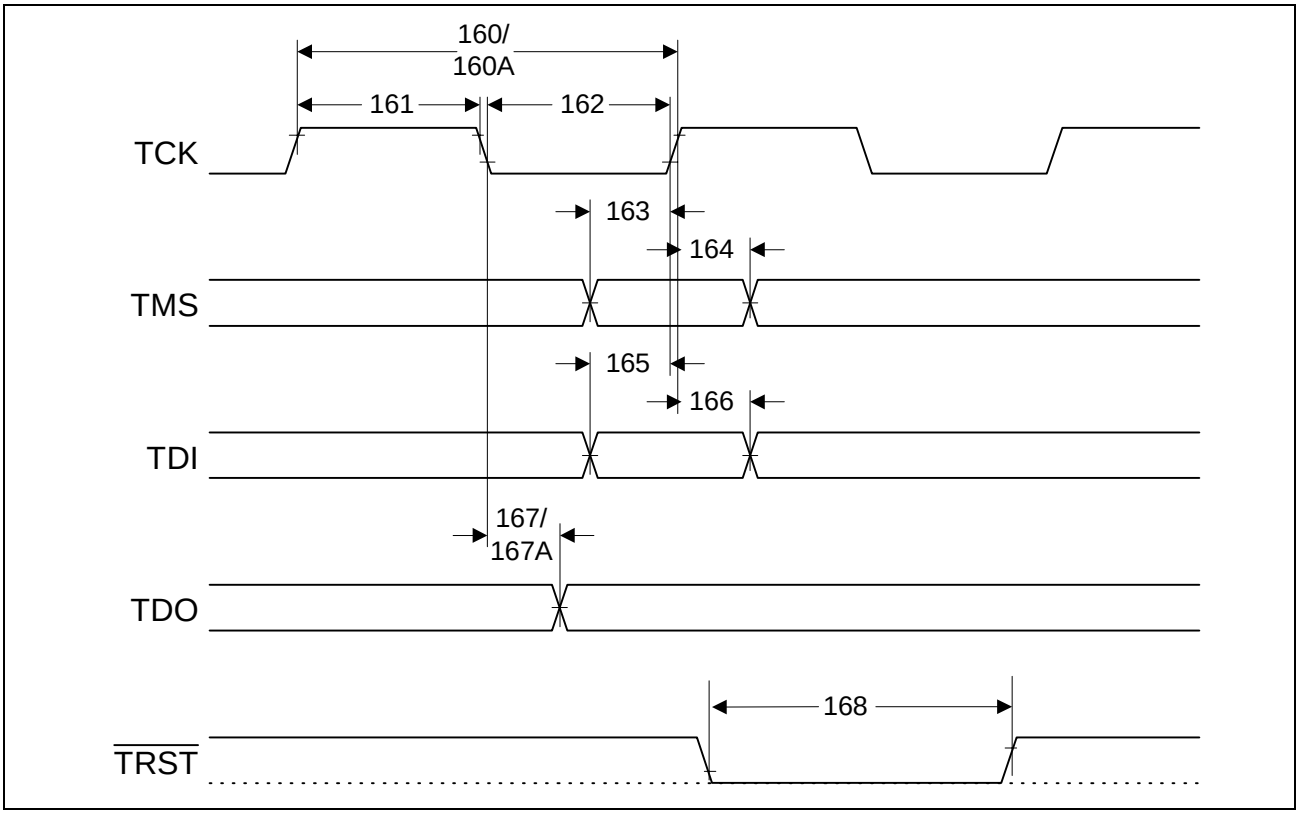


Figure 7-11 Boundary-Scan Test Interface Timing Diagram

Table 7-16 Boundary-Scan Test Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
160	T_{TCK} : Period TCK	100			ns
160A	F_{TCK} : Frequency TCK			10	MHz
161	TCK high time	40			ns
162	TCK low time	40			ns
163	Setup time TMS before TCK rising	10			ns
164	Hold time TMS after TCK rising	10			ns
165	Setup time TDI before TCK rising	10			ns
166	Hold time TDI after TCK rising	10			ns
167	Delay TCK falling to TDO valid			30	ns

Table 7-16 Boundary-Scan Test Interface AC Timing Characteristics (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
167A	Delay TCK falling to TDO high impedance			30	ns
168	Pulse width $\overline{\text{TRST}}$ low	200			ns

7.5 Capacitances

Table 7-17 Capacitances

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input Capacitance	C_{IN}	2.5	5	pF
Output Capacitance	C_{OUT}	2	5	pF
Load Capacitance at: UTOPIA Outputs MPDAT(15:0), MPRDY other outputs	 C_{FO1} C_{FO2} C_{FO3}		 40 50 20	 pF pF pF

7.6 Package Characteristics

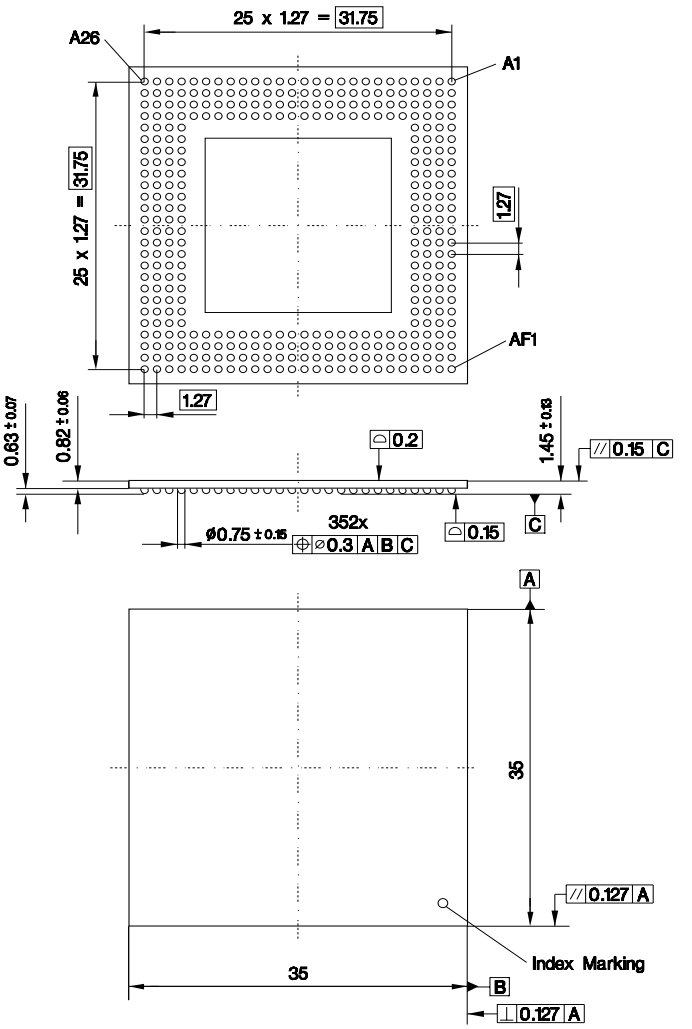
Table 7-18 Thermal Package Characteristics

Parameter		Symbol	Value	Unit
Thermal Package Resistance Junction to Ambient				
Airflow	Ambient Temperature			
No airflow	T_A=25°C	$R_{JA(0,25)}$	12.4	°C/W
Airflow 100 lfpm = 0.5m/s	T_A=25°C	$R_{JA(0,25)}$	10.8	°C/W
Airflow 200 lfpm = 1m/s	T_A=25°C	$R_{JA(0,25)}$	9.6	°C/W
Airflow 300 lfpm = 1.5m/s	T_A=25°C	$R_{JA(0,25)}$	9	°C/W
Airflow 400 lfpm = 2m/s	T_A=25°C	$R_{JA(0,25)}$	8.5	°C/W
Airflow 500 lfpm = 2.5m/s	T_A=25°C	$R_{JA(0,25)}$	8.3	°C/W

8 Package Outlines

P-BGA-352-1

(Super BGA 352 Package with metal heat sink)



GPM05247

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

9 References

1. UTOPIA Level 1 Specification Version 2.01, March 21, 1994, The ATM Forum
2. UTOPIA Level 2 Specification Version 1.0, June 1995, The ATM Forum
3. IEEE 1596.3 Standard for Low-Voltage Differential Signals for SCI, Draft 1.3, November 1995
4. JTAG Joint Test Action Group, IEEE 1149.1
5. Siemens ATM Devices Web Site
   http://www.infineon.com
6. 16M SDRAM Data Sheets, Advance Information
7. Application Note 07.98, 'Cascading of ABM Devices to Increase the Number of Schedulers'

Traffic Management

Two traffic management standards are available from ITU-T and from The ATM Forum:

8. ITU-T Recommendation I.371, "Traffic Control and Congestion Control in B-ISDN", 2nd Release, Geneva, Switzerland, March 1996
9. Traffic Management Specification Version 4.0, April 1996, The ATM Forum

As traffic management has many undefined aspects in research and under investigation, numerous articles about it are published each year. The articles listed below provide the basics for the principles used in the ABM device.

The cell level congestion occurring when several independent sources send random cell traffic into one queue can be solved analytically. This scenario applies to the real-time queue of a Scheduler. The required queue size for a given cell loss probability is calculated in this paper:

10. D. Lampe, "Traffic Studies of a Multiplexer in an ATM Network and Applications to the future Broadband ISDN", International Journal of Digital and Analog Cabled Systems, Vol. 2, 1989

In the case of bursty real-time traffic (VBR-rt), statistical multiplexing gain can be achieved by the fact that it is very unlikely that many uncorrelated sources send bursts simultaneously. The total bit rate to be reserved for an ensemble of such connections can be lower than the sum of the individual peak bit rates. The following articles propose algorithms to calculate the sum rate:

11. E. Wallmeier, "A Connection Acceptance Algorithm for ATM Networks Based on Mean and Peak Bit Rates", International Journal of Digital and Analog Communication Systems, Vol. 3, 1990
12. E. Wallmeier and C. Hauber, "Blocking Probabilities in ATM Pipes controlled by a Connection Acceptance Algorithm base on mean and peak rates", Queuing, Performance and Control in ATM, ITC-13 Workshops, Elsevier Science Publishers B.V., 1991

A general overview of the support of data traffic in ATM networks can be found in:

13.W.Fischer, E. Wallmeier, T. Worster, S. Davis, A. Hayter, “Data Communications using ATM: Architectures, Protocols, and Resource Management”, IEEE Communications Magazine, August 1994

The benefits of weighted fair queuing, referred to as “virtual spacing” in this paper, are described in:

14.J.W. Roberts, “Virtual Spacing for Flexible Traffic Control”, International Journal of Communication Systems, Vol. 7, 1994

To avoid overload in a large switch, various concepts have been proposed, including backpressure. The alternative method of pre-emptive congestion control using dynamic Bandwidth Allocation (DBA) is described in these papers:

15.T. Worster, W. Fischer, S. Davis, A. Hayter, „Buffering and Flow Control for Statistical Multiplexing in an ATM Switch“, International Switching Symposium (ISS’95), April 1995

16.U. Briem, E. Wallmeier, C. Beck, F. Mathiesen, “Traffic Management for an ATM Switch with Per-VC Queuing: Concept and Implementation”, IEEE Communications Magazine, January 1998

10 Acronyms

AAL	**A**TM **A**daptation **L**ayer
ABM	**A**TM **B**uffer **M**anager device, PXB 4330 E
ABR	**A**vailable **B**it **R**ate
ABT	**A**TM **B**lock **T**ransfer
ADSL	**A**symmetric **D**igital **S**ubscriber **L**ine
ALP	**A**TM **L**ayer **P**rocessor device, PXB 4350 E
AOP	**A**TM **O**AM **P**rocessor device, PXB 4340 E
ASF	**A**TM **S**witching **F**abric
ATM	**A**synchronous **T**ransfer **M**ode
BIST	**B**uilt-**I**n **S**elf **T**est
CAC	**C**onnection **A**cceptance **C**ontrol
CAME	**C**ontent **A**ddressable **M**emory **E**lement device, PXB 4360 E
CBR	**C**onstant **B**it **R**ate
CDV	**C**ell **D**elay **V**ariation
CI/NI	**C**ongestion **I**ndication/**N**o **I**ncrease (ABR connections: 2 Bits of a RM cell)
CLP	**C**ell **L**oss **P**riority of standardized ATM cell
CRC	**C**yclic **R**edundancy **C**heck
DBR	**D**eterministic **B**it **R**ate
DSLAM	**D**igital **S**ubscriber **L**ine **A**ccess **M**ultiplexer
dword	**d**ouble **word** (32 bits)
EFCI	**E**xplicit **F**orward **C**ongestion **I**ndication (ABR connections: Header-Bit of a data cell)
EPD	**E**arly **P**acket **D**iscard
FIFO	**F**irst-**I**n-First-**O**ut buffer
GFR	**G**uaranteed **F**rame **R**ate
HK	**H**ouse**K**eeping bits of UDF1 field in UTOPIA cell format
I/O	**I**nput/**O**utput
ITU-T	**I**nternational **T**elecommunications **U**nion—**T**elecommunications standardization sector
LCI	**L**ocal **C**onnection **I**dentifier
LIC	**L**ine **I**nterface **C**ard or **L**ine **I**nterface **C**ircuit

LIFO	**L**ast-**I**n-**F**irst-**O**ut buffer
LSB	**L**east **S**ignificant **B**it
LVDS	**L**ow **V**oltage **D**ifferential **S**ignaling
MBS	**M**aximum **B**urst **S**ize
MCR	**M**inimum **C**ell **R**ate
MSB	**M**ost **S**ignificant **B**it
NPC	**N**etwork **P**arameter **C**ontrol
octet	byte (8 bits)
OAM	**O**peration **A**nd **M**aintenance
PCR	**P**eak **C**ell **R**ate
PHY	**PHY**sical Line Port
PPD	**P**artial **P**acket **D**iscard
PTI	**P**ayload **T**ype **I**ndication field of standardized ATM cell
QID	**Q**ueue **ID**entifier
QoS	**Q**uality **o**f **S**ervice
RAM	**R**andom **A**ccess **M**emory
RM Cell	**R**esource **M**anagement **Cell** (ABR connections)
SCR	**S**ustainable **C**ell **R**ate
SDRAM	**S**ynchronous **D**ynamic **R**andom **A**ccess **M**emory
SID	**S**cheduler **ID**entifier
SLIF	**S**witch **L**ink **I**nter**F**ace
SSRAM	**S**ynchronous **S**tatic **R**andom **A**ccess **M**emory
tbd	**t**o **b**e **d**efined
TM	**T**raffic **M**anagement
UBR	**U**nspecified **B**it **R**ate
UPC	**U**ser **P**arameter **C**ontrol
UTOPIA	**U**niversal **T**est and **OP**eration **I**nterface for **A**TM
VBR-nrt	**V**ariable **B**it **R**ate - **n**on **r**eal **t**ime
VBR-rt	**V**ariable **B**it **R**ate - **r**eal **t**ime
VC-	**V**irtual **C**hannel specific
VCC	**V**irtual **C**hannel **C**onnection
VCI	**V**irtual **C**hannel **I**dentifier of standardized ATM cell

VP-	**V**irtual **P**ath specific
VPC	**V**irtual **P**ath **C**onnection
VPI	**V**irtual **P**ath **I**dentifier of standardized ATM cell
WFQ	**W**eighted **F**air **Q**ueueing
word	16 bits