HCTL-2001
Quadrature Decoder/Counter Interface ICs

Data Sheet

Description

The HCTL-2001 is a CMOS ICs that performs the quadrature decoder, counter, and bus interface function. The HCTL-20XX family is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The HCTL-20XX consists of a quadrature decoder logic, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2001 contains 12-bit counter and provides TLL/CMOS compatible tri-state output buffers. Operation is specified for a temperature range from –40 to +85°C at clock frequencies up to 14MHz.

The HCTL-2001 is compliant to RoHS directive and had been declared as a lead free product.

Features

- Interfaces Encoder to Microprocessor
- 14 MHz Clock Operation
- High Noise Immunity:
  Schmitt Trigger Inputs and Digital Noise Filter
- 12 -Bit Binary Up/Down Counter
- Latched Outputs
- 8-Bit Tristate Interface
- 8 or 12-Bit Operating Modes
- Substantially Reduced System Software
- 5V Operation (VDD – VSS)
- TTL/CMOS Compatible I/O
- Operating Temperature: -40°C to 85°C
- 16-Pin PDIP

Applications

- Interface Quadrature Incremental Encoders to Microprocessors
- Interface Digital Potentiometers to Digital Data Input Buses

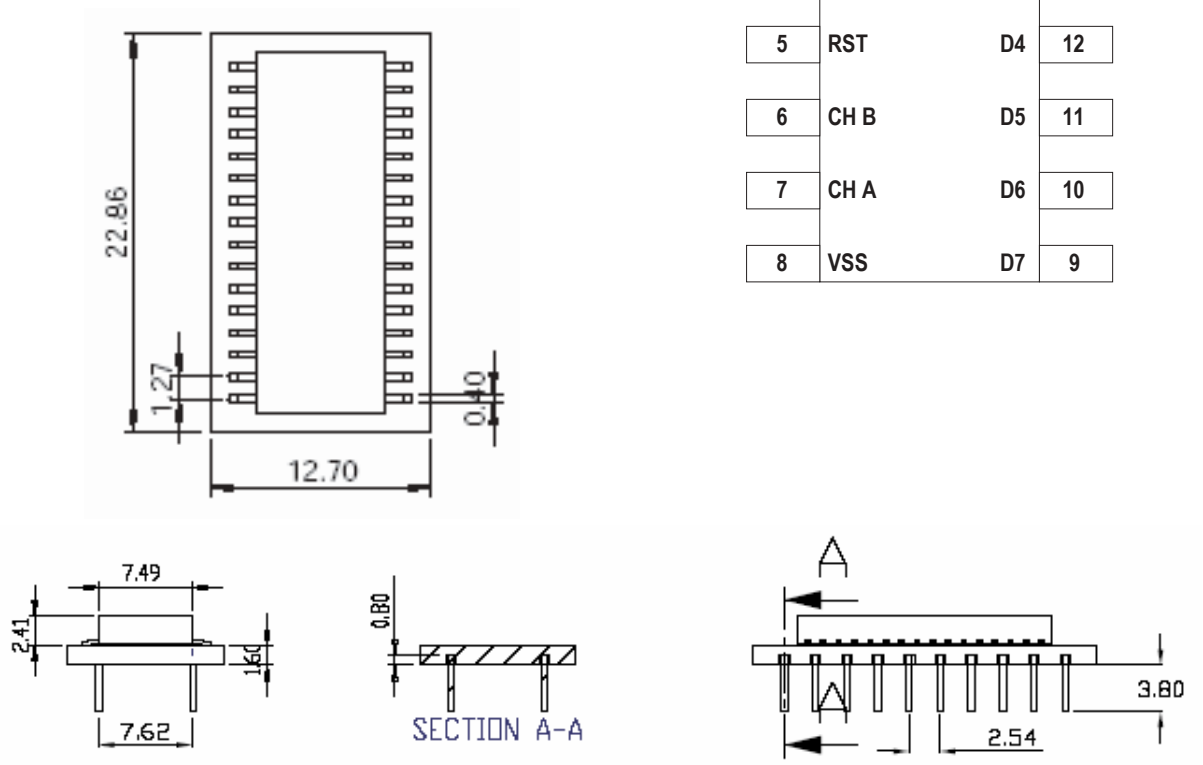
Devices

Part Number	Description	Pinout
HCTL-2001	12-bit counter. 14 MHz clock operation.	PINOUT A

PINOUT A

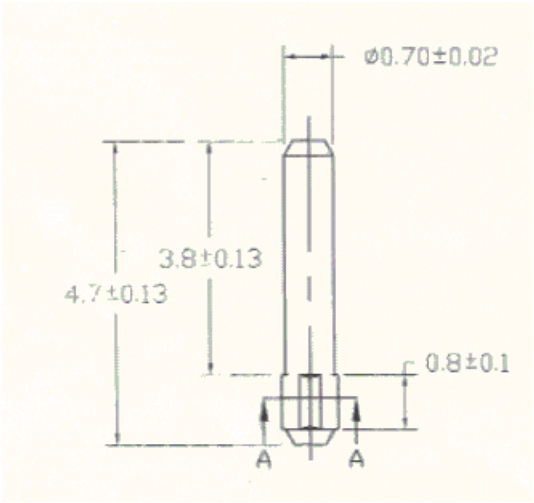
1	D0	VDD	16
2	CLK	D1	15
3	SEL	D2	14
4	OE	D3	13
5	RST	D4	12
6	CH B	D5	11
7	CH A	D6	10
8	VSS	D7	9

Package Dimensions



(dimension in mm)

PIN DRAWING



Package Dimensions with Tolerances

HCTL-2001	Length (L)	Width (W)	Thickness (T)
	22.86 0.5 mm	12.70 0.5 mm	1.67 0.25 mm

Soldering and Mounting Considerations

It is recommended to use manual soldering for HCTL-2001 launch pad devices due to the characteristics of the material used in the launch pad design that not allow wave soldering.

Direct mounting on printed circuit board (PCB) only is recommended for HCTL-2001 launch pad devices.

Operating Characteristics

Table 1. Absolute Maximum Ratings

(All voltages below are referenced to VSS)

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +6.0	V
Input Voltage	V_{IN}	-0.3 to (V_{DD} +0.3)	V
Storage Temperature	T_S	-55 to +150	°C
Operating Temperature [1]	T_A	-40 to +85	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	4.5 to 5.5	V
Ambient Temperature [1]	T_A	-40 to +85	°C

Table 3. DC Characteristics VDD = 5V ± 5%; TA = -40 to 85°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL} [2]	Low-Level Input Voltage				1.5	V
V_{IH} [2]	High-Level Input Voltage		3.5			V
V_{T+}	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
V_{T-}	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_H	Schmitt-Trigger Hysteresis		1.0	2.0		V
I_{IN}	Input Current	V_{IN}=V_{SS} or V_{DD}	-10	1	+10	A
V_{OH} [2]	High-Level Output Voltage	I_{OH} = -3.75 mA	2.4	4.5		V
V_{OL} [2]	Low-Level Output Voltage	I_{OL} = +3.75mA		0.2	0.4	V
I_{OZ}	High-Z Output Leakage Current	V_O=V_{SS} or V_{DD}	-10	1	+10	A
I_{DD}	Quiescent Supply Current	V_{IN}=Vss or V_{DD}		1	100	A
C_{IN} [3]	Input Capacitance	Any Input		5		pF
C_{OUT} [3]	Output Capacitance	Any Output		5		pF

Notes:

1. Free Air
2. In general, for any VDD between the allowable limits (+4.5V to +5.5V), VIL = 0.3VDD and VIH = 0.7VDD; typical values are VOH = VDD – 0.5V and VOL = VSS + 0.2V
3. Including package capacitance but excluding PCB capacitance.

Functional Pin Description

Table 4. Functional Pin Descriptions

Symbol	Pin	Description
	HCTL 2001	
VDD	16	Power Supply
VSS	8	Ground
CLK	2	CLK is a Schmitt-trigger input for the external clock signal.
CHA CHB	7 6	CHA and CHB are Schmitt-trigger inputs that accept the outputs from a quadrature-encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.
$\overline{RST}$	5	This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. RST is asynchronous with respect to any other input signals.
$\overline{OE}$	4	This CMOS active low input enables the tri-state output buffers. The OE/ and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.
SEL	3	These CMOS inputs directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in OE/ above, SEL also control the internal inhibit logic. **SEL** / **BYTE SELECTED** 0 / High 1 / Low
D0	1	These LSTTL-compatible tri-state outputs form an 8-bit output ports through which the contents of the 16-bit position latch may be read in 2 sequential bytes. The High byte is read first followed by the Low bytes.
D1	15	
D2	14	
D3	13	
D4	12	
D5	11	
D6	10	
D7	9	
NC	NA	Not connected - this pin should be left floating.

Switching Characteristics

Table 5. Switching Characteristics Max/Min specifications at VDD = 5.0 ? 5%, TA = -40 to +100 OC, CL = 40 pf

Symbol		Description	Min.	Max.	Units
1	t_{CLK}	Clock Period	70		ns
2	t_{CHH}	Pulse width, clock high	28		ns
3	t_{CD}	Delay time, rising edge of clock to valid, updated count information on D0-7		65	ns
4	t_{ODE}	Delay time, OE fall to valid data		65	ns
5	t_{ODZ}	Delay time, OE rise to Hi-Z state on D0-7		40	ns
6	t_{SDV}	Delay time, SEL valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		65	ns
7	t_{CLH}	Pulse width, clock low	28		ns
8	t_{SS}	Setup time, SEL before clock fall	20		ns
9	t_{OS}	Setup time, OEN before clock fall	20		ns
10	t_{SH}	Hold time, SEL after clock fall	0		ns
11	t_{OH}	Hold time, OE after clock fall	0		ns
12	t_{RST}	Pulse width, RST low	28		ns
13	t_{DCD}	Hold time, last position count stable on D0-7 after clock rise	10		ns
14	t_{DSD}	Hold time, last data byte stable after next SEL state change	10		ns
15	t_{DOD}	Hold time, data byte stable after OE rise	10		ns

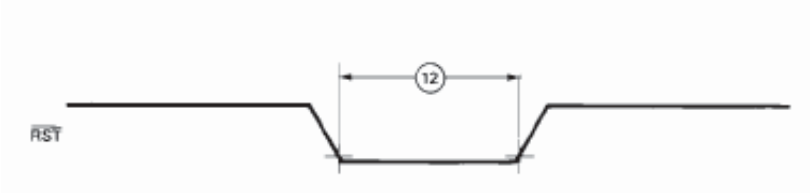


Figure 1. Reset Waveform

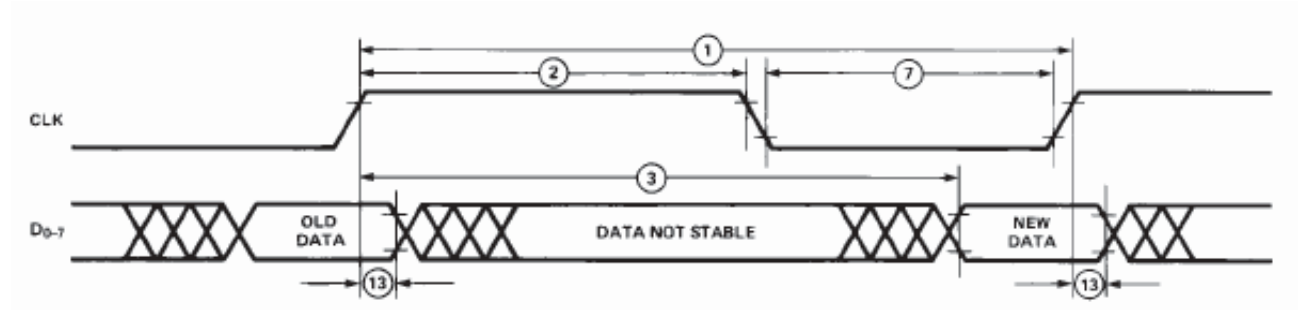


Figure 2. Waveforms for Positive Clock Edge Related Delays

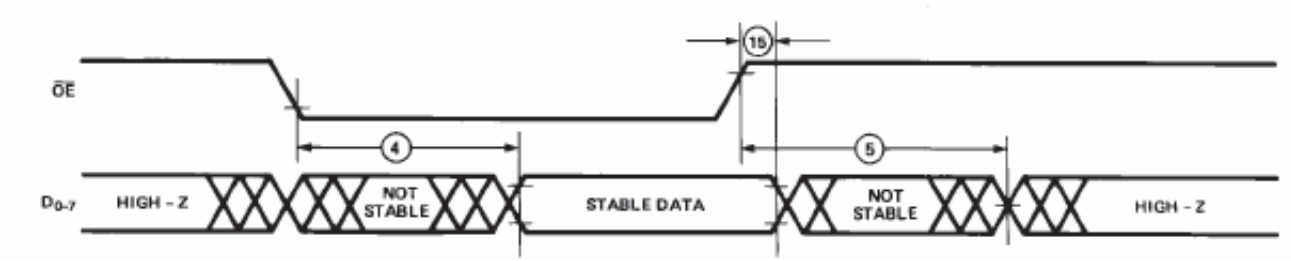


Figure 3. Tri-State Output Timing

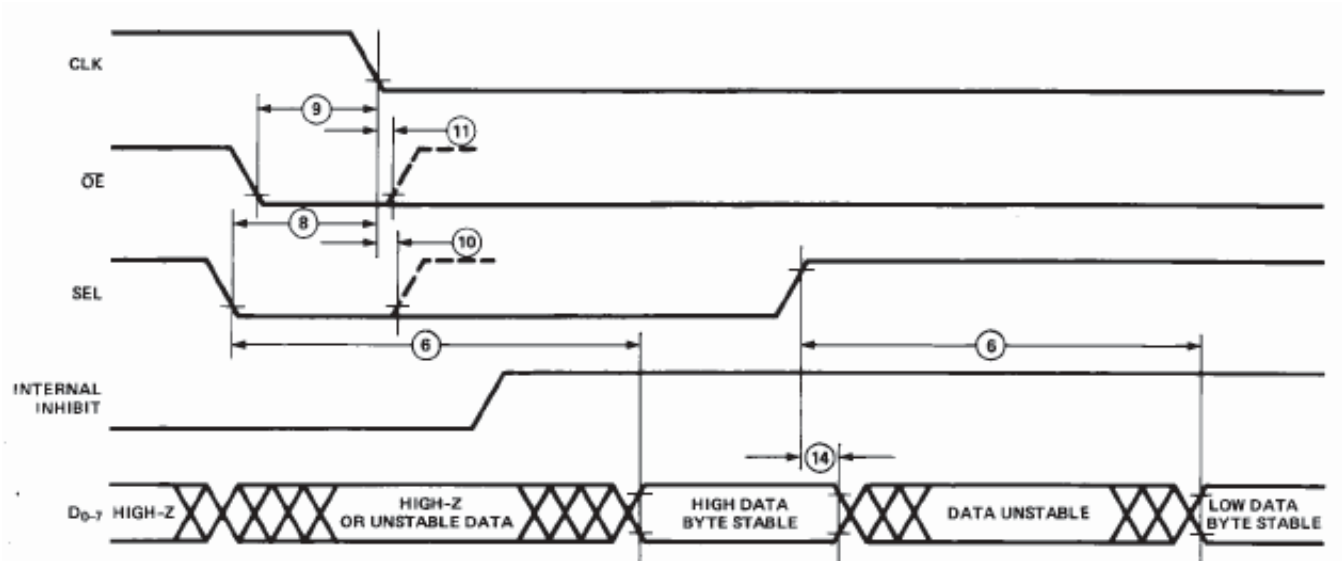


Figure 4. Bus Control Timing

Operation

A block diagram of the HCTL-20XX family is shown in Figure 6. The operation of each major function is described in the following sections.

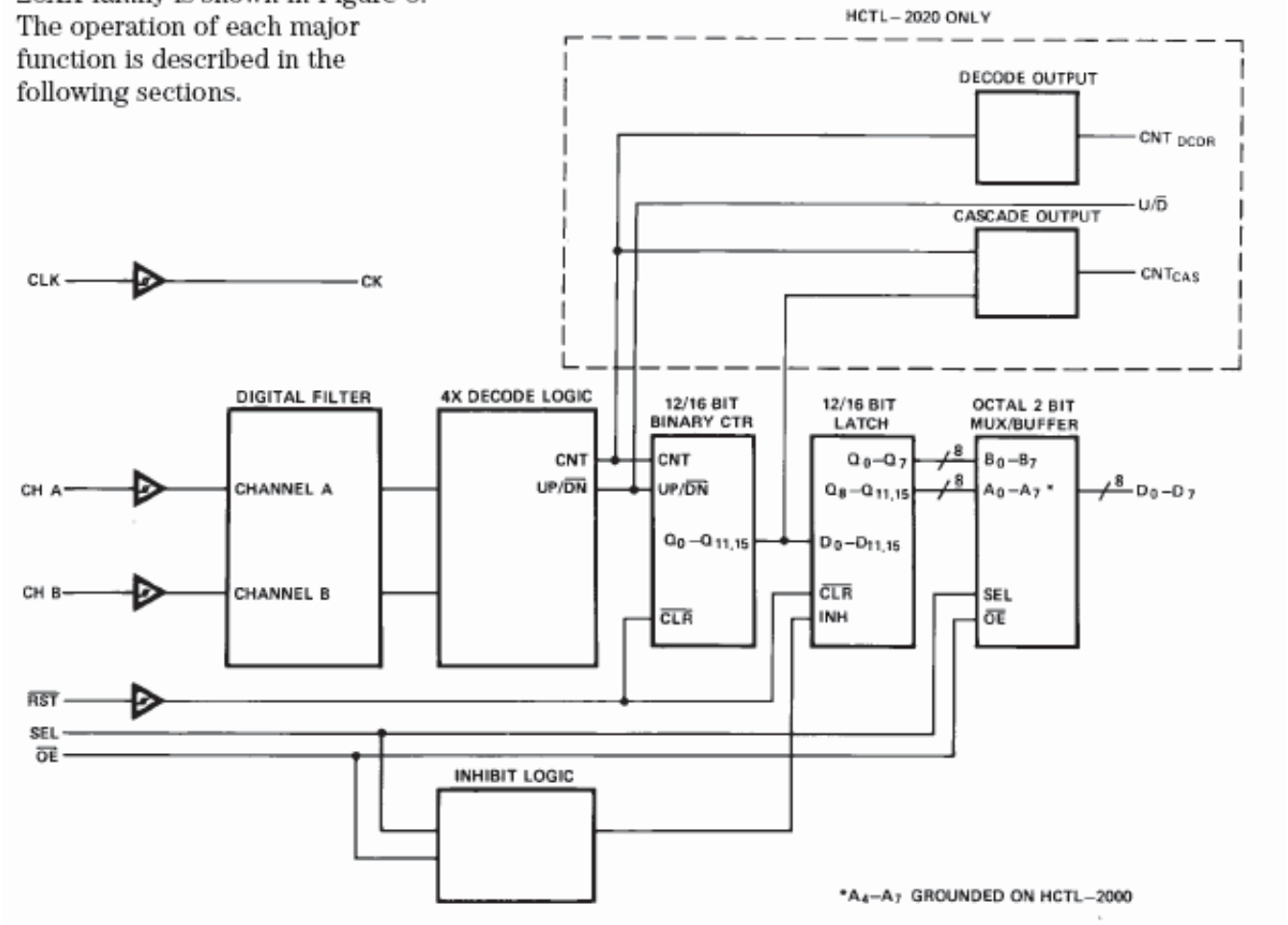


Figure 5. Simplified Logic Diagram

Digital Noise Filter

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a three-clock-cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved integrity of the data in the counter. False counts triggered by noise are avoided.

Figure 6 shows the simplified schematic of the input section. The signals are first passed through a Schmitt-trigger buffer to address the problem of input signals with slow rise times and low-level noise (approximately < 1V). The cleaned up signals are then passed to a four-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges.

Refer to Figure 7, which shows the timing diagram. The result of this circuitry is that short noise spikes between rising clock edges are ignored and pulses shorter than two clock periods are rejected.

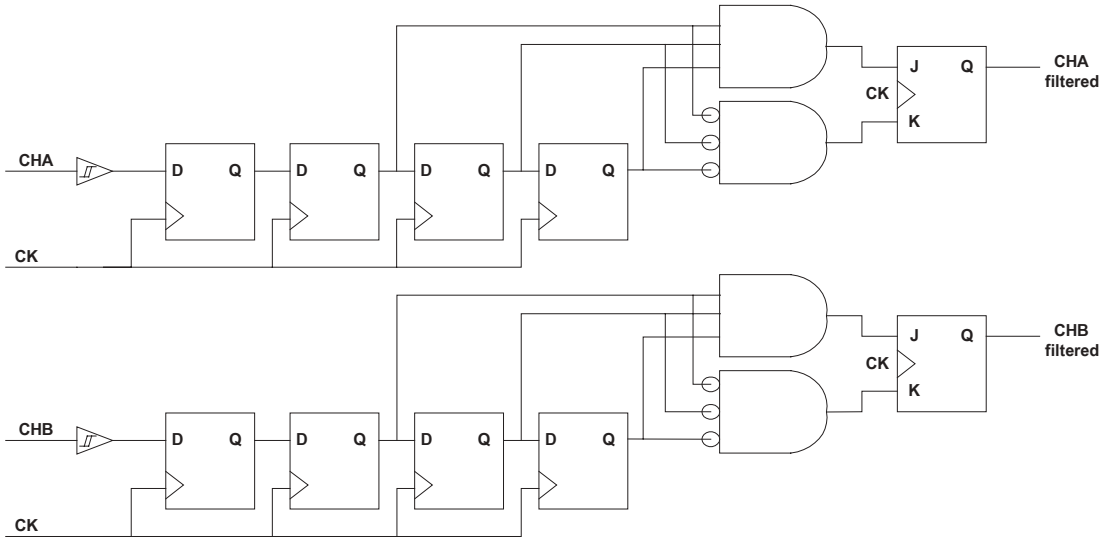


Figure 6. Simplified Digital Noise Filter Logic

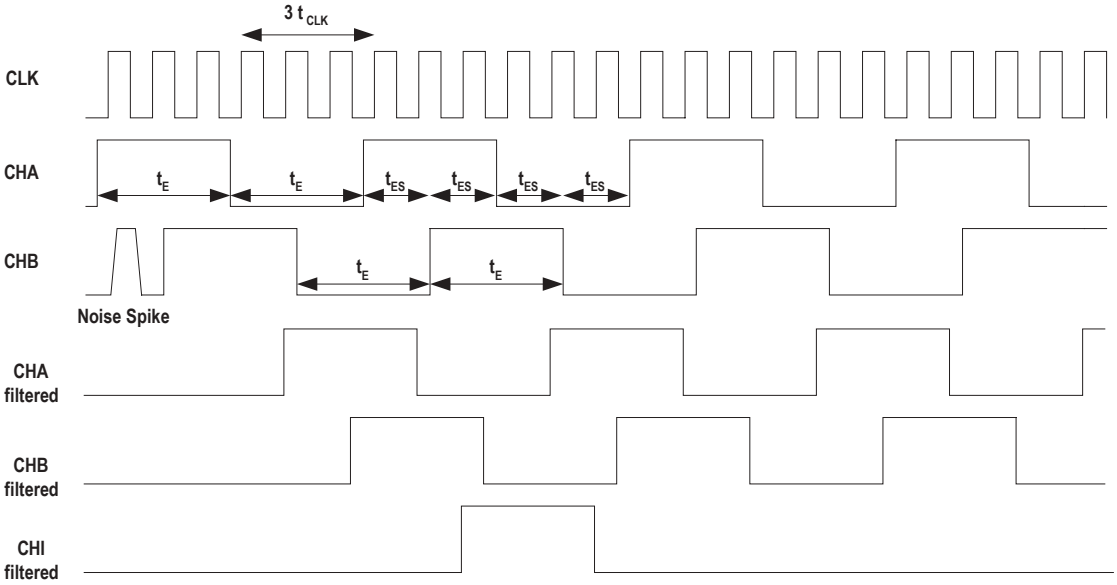


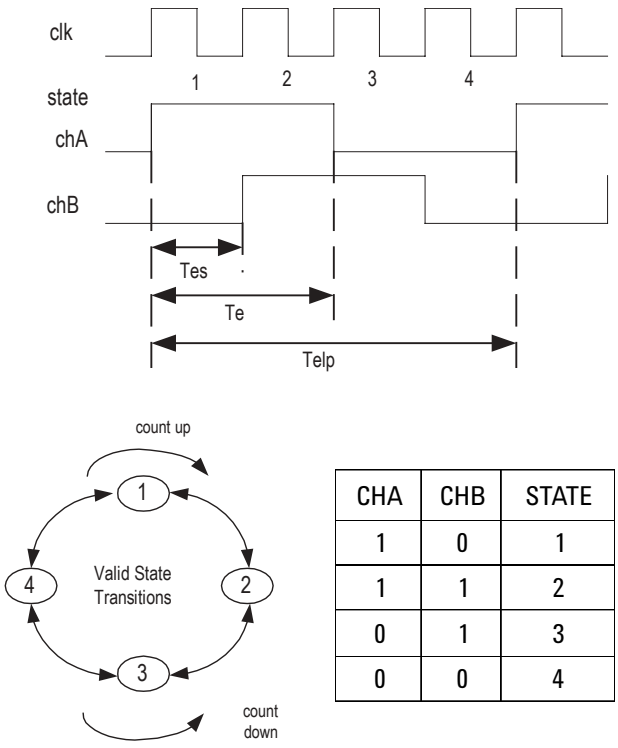
Figure 7. Signal Propagation through Digital Noise Filter

Quadrature Decoder

The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four (4X decoding).

The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the integral position counter.

Figure 8 shows the quadrature states of Channel A and Channel B signals and shows the valid state transitions for 4x decoder. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.



CHA	CHB	STATE
1	0	1
1	1	2
0	1	3
0	0	4

Figure 8. 4x Decoder Mode

Design Considerations

The designer should be aware that the operation of the digital filter places a timing constraint on the relationship between incoming quadrature signals and the external clock. Figure 7 shows the timing waveform with an incremental encoder input. Since an input has to be stable for three rising clock edges, the encoder pulse width (tE - low or high) has to be greater than three clock periods (3tCLK). This guarantees that the asynchronous input will be stable during three consecutive rising clock edges. A realistic design also has to take into account finite rise time of the waveforms, asymmetry of the waveforms, and noise. In the presence of large amounts of noise, tE should be much greater than 3tCLK— to allow for the interruption of the consecutive level sampling by the three-bit delay filter. It should be noted that a change on the inputs that is qualified by the filter will internally propagate in a maximum of seven clock periods.

The quadrature decoder circuitry imposes a second timing constraint between the external clock and the input signals. There must be at least one clock period between consecutive quadrature states. As shown in Figure 7, a quadrature state is defined by consecutive edges on both channels. Therefore, tES (encoder state period) > tCLK-. The designer must account for deviations from the nominal 90 degree phasing of input signals to guarantee that tES > tCLK.

Position Counter

This section consists of a 12-bit (HCTL-2001) binary up/down counter which counts on rising clock edges as explained in the Quadrature Decoder Section. All 12-bit of data are passed to the position data latch. The system can use this count data in several ways:

A. System total range is £ 12 bits, so the count represents "absolute" position.

B. The system is cyclic with £ 12 bits of count per cycle. RSTN (or CHI) is used to reset the counter every cycle and the system uses the data to interpolate within the cycle.

C. System count is > 8 or 12 bits, so the count data is used as a relative or incremental position input for a system software computation of absolute position. In this case counter rollover occurs. In order to prevent loss of position information, the processor must read the outputs of the IC before the count increments one-half of the maximum count capability. Two's-complement arithmetic is normally used to compute position from these periodic position updates.

Position Data Latch

The position data latch is a 12-bit latch which captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic section during two-byte read operations. The output data is passed to the bus interface section. When active, a signal from the inhibit logic section prevents new data from being captured by the latch, keeping the data stable while successive reads are made through the bus section. The latch is automatically re-enabled at the end of these reads. The latch is cleared to 0 asynchronously by the RST signal.

Inhibit Logic

The Inhibit Logic Section samples the OE and SEL signals on the falling edge of the clock and, in response to certain conditions (see Figure 9), inhibits the position data latch. The RST signal asynchronously clears the inhibit logic, enabling the latch.

Bus Interface

The bus interface section consists of a 16 to 8 line multiplexer and an 8-bit, three-state output buffer. The multiplexer allows independent access to the low and high bytes of the position data latch. The SEL and OE signals determine which byte is output and whether or not the output bus is in the high-Z state. In the case of HCTL-2001, the data latch is 12 bit wide.

General Interfacing

The 12-bit (HCTL-2001) latch and inhibit logic allows access to 12 bits of count with an 8-bit bus. When only 8-bits of count are required, a simple 8-bit (1-byte) mode is available by holding SEL high continuously. This disables the inhibit logic. OE provides control of the tri-state bus, and read timing is shown in Figure 2 and 3.

For proper operation of the inhibit logic during a two-byte read, OE and SEL must be synchronous with CLK due to the falling edge sampling of OE and SEL.

The internal inhibit logic on the HCTL-20XX family inhibits the transfer of data from the counter to the position data latch during the time that the latch outputs are being read. The inhibit logic allows the microprocessor / microcontroller to first read the high order 4 or 8 bits from the latch and then read the low order 8 bits from the latch. Meanwhile, the counter can continue to keep track of the quadrature states from the CHA and CHB input signals.

Figure 10 shows the simplified inhibit logic circuit. The operation of the circuitry is illustrated in the read timing shown in Figure 11.

Step	SEL	OE	CLK	Inhibit Signal	Action
1	L	L	Falling	1	Set inhibit; read high byte
2	H	L	Falling	1	Read low byte; starts reset
3	X	H	Falling	0	Complete inhibit logic reset

Figure 9. Two Bytes Read Sequence

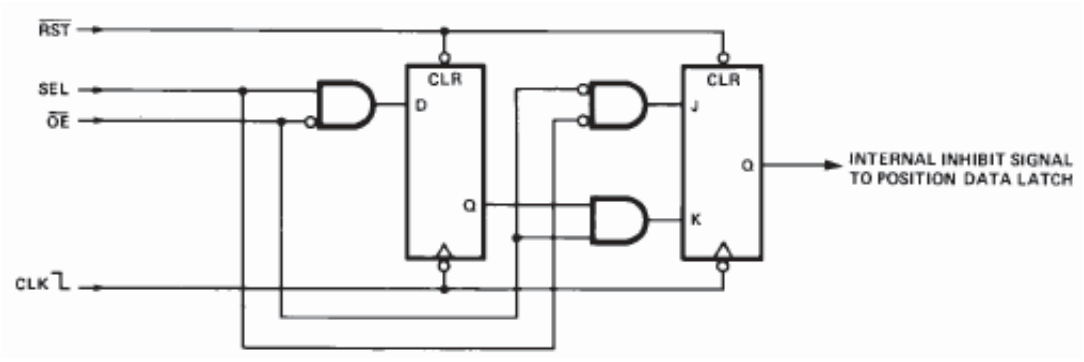


Figure 10. Simplified Inhibit Logic

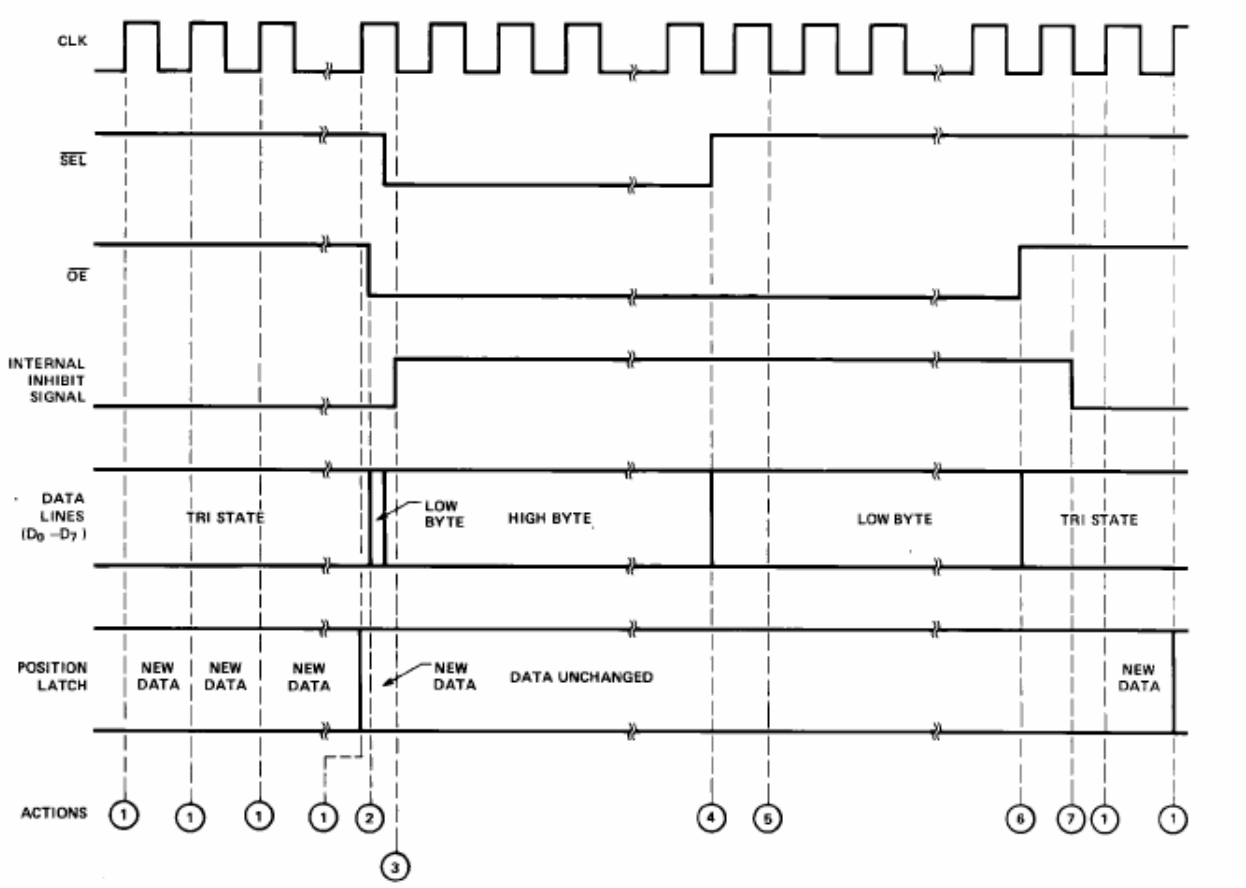


Figure 11. Typical Interface Timing

Actions

1. On the rising edge of the clock, counter data is transferred to the position data latch, provided the inhibit signal is low.
2. When OE goes low, the outputs of the multiplexer are enabled onto the data lines. If SEL is low, then the high order data bytes are enabled onto the data lines. If SEL is high, then the low order data bytes are enabled onto the data lines.
3. When the IC detects a low on OE and SEL during a falling clock edge, the internal inhibit signal is activated. This blocks new data from being transferred from the counter to the position data latch.
4. When SEL goes high, the data outputs change from the high byte to the low byte.
5. The first of two reset conditions for the inhibit logic is met when the IC detects a logic high on SEL and a logic low on OE during a falling clock edge.
6. When OE goes high, the data lines change to a high impedance state.
7. The IC detects a logic high on OE during a falling clock edge. This satisfies the second reset condition for the inhibit logic.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV01-0085EN - August 2, 2006