# 512K x 64 Synchronous Pipeline NBL SRAM

## FEATURES

- Fast clock speed: 166, 150, 133, and 100MHz
- Fast access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Fast OE# access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Seperate +2.5V ± 5% power supplys for core I/O ($V_{CC}$ + $V_{CCQ}$)
- Double Word Write Control
- Clock-controlled and registered addresses, data I/Os and control signals
- Packaging:
  - 119 bump BGA package
- Low capacitive bus loading

## DESCRIPTION

The WEDC SyncBurst - SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process. WEDC's 32Mb Sync SRAM integrate two 512K x 32 SRAMs into a single BGA package to provide 512K x 64 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CK). The NBL or No Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable are synchronized to input clock. Output Enable controls the outputs at any given time and to Asynchronous Input. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

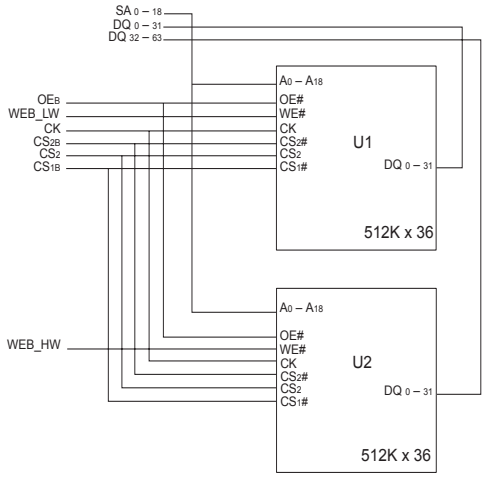
NOTE: NBL = No Bus Latency is equivalent to the industry ZBT™ devices.

## FIG. 1 PIN CONFIGURATION

(TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | $DQ_F$ | $DQ_F$ | $DQ_F$ | $DQ_F$ | NC | $DQ_G$ | $DQ_G$ | $DQ_G$ | $DQ_G$ |
| B | $DQ_F$ | $DQ_F$ | $DQ_F$ | $DQ_F$ | NC | $DQ_G$ | $DQ_G$ | $DQ_G$ | $DQ_G$ |
| C | $DQ_E$ | $DQ_E$ | $DQ_E$ | $DQ_E$ | NC | $DQ_H$ | $DQ_H$ | $DQ_H$ | $DQ_H$ |
| D | $DQ_E$ | $DQ_E$ | $DQ_E$ | $DQ_E$ | NC | $DQ_H$ | $DQ_H$ | $DQ_H$ | $DQ_H$ |
| E | NC | NC | NC | $V_{CCQ}$ | $V_{CCQ}$ | $V_{CCQ}$ | NC | NC | NC |
| F | SA | $V_{CCQ}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CCQ}$ | SA |
| G | SA | CE# | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | SA | SA |
| H | SA | NC | $V_{SS}$ | $WE_1$# | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | SA | SA |
| J | $SA_{18}$ | $CE_2$# | $SS_{CK}$ | OE# | NC | NC | NC | $SA_1$ | $SA_0$ |
| K | SA | $CE_2$ | $V_{SS}$ | $WE_0$# | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | SA | SA |
| L | SA | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | SA | SA |
| M | SA | $V_{CCQ}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CCQ}$ | SA |
| N | NC | NC | NC | $V_{CCQ}$ | $V_{CCQ}$ | $V_{CCQ}$ | NC | NC | NC |
| P | $DQ_D$ | $DQ_D$ | $DQ_D$ | $DQ_D$ | NC | $DQ_A$ | $DQ_A$ | $DQ_A$ | $DQ_A$ |
| R | $DQ_D$ | $DQ_D$ | $DQ_D$ | $DQ_D$ | NC | $DQ_A$ | $DQ_A$ | $DQ_A$ | $DQ_A$ |
| T | $DQ_C$ | $DQ_C$ | $DQ_C$ | $DQ_C$ | NC | $DQ_B$ | $DQ_B$ | $DQ_B$ | $DQ_B$ |
| U | $DQ_C$ | $DQ_C$ | $DQ_C$ | $DQ_C$ | NC | $DQ_B$ | $DQ_B$ | $DQ_B$ | $DQ_B$ |

## BLOCK DIAGRAM



## FUNCTION DESCRIPTION

The WED2ZL64512S is an NBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of OE#) are synchronized to rising clock edges.

Output Enable (OE#) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE# is driven low, the write enable input signals WE# are driven high. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation OE# must be driven low for the device to drive out the requested data.

Write operation occurs when WE# is driven low at the rising edge of the clock. The pipe-lined NBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, WE# and address are registered, and the data associated with that address is required two cycle later.

## TRUTH TABLES

### SYNCHRONOUS TRUTH TABLE

| CEx# | WE# | OE# | CK | Address Accessed | Operation |
|---|---|---|---|---|---|
| H | X | X | ↑ | N/A | Deselect |
| L | H | L | ↑ | Current Address | Read Cycle |
| L | H | H | ↑ | N/A | NOP/Dummy Read |
| X | X | H | ↑ | N/A | Dummy Read |
| L | L | X | ↑ | Current Address | Write Cycle |
| L | L | X | ↑ | N/A | NOP/Write Abort |

NOTES:
1. X means "Don't Care."
2. The rising edge of clock is symbolized by (↑ )
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. WRITE# = L means Write operation in WRITE TRUTH TABLE.
   WRITE# = H means Read operation in WRITE TRUTH TABLE.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on $V_{CC}$ Supply Relative to Vss | -0.3V ≤ $T_A$ ≤ +3.6V |
| $V_{IN}$ (DQx) | -0.3V ≤ $T_A$ ≤ +3.6V |
| $V_{IN}$ (Inputs) | -0.3V ≤ $T_A$ ≤ +3.6V |
| Storage Temperature (BGA) | -55°C ≤ $T_A$ ≤ +125°C |
| Short Circuit Output Current | 100mA |

*Stress greater than those listed under "Absolute Maximum Ratings: may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS (0°C ≤ $T_A$ ≤ 70°C)

| Description | Symbol | Conditions | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | $V_{IH}$ | | 1.7 | $V_{CC}$ +0.3 | V | 1 |
| Input Low (Logic 0) Voltage | $V_{IL}$ | | -0.3 | 0.7 | V | 1 |
| Input Leakage Current | $I_{LI}$ | 0V $V_{IN}$ $V_{CC}$ | -5 | 5 | mA | |
| Output Leakage Current | $I_{LO}$ | Output(s) Disabled, 0V $V_{IN}$ $V_{CC}$ | -5 | 5 | mA | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1.0mA | 2.0 | --- | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1.0mA | --- | 0.4 | V | 1 |
| Supply Voltage | $V_{CC}$ | | 2.375 | 2.625 | V | 1 |

NOTES: 1. All voltages referenced to $V_{SS}$ (GND)

## DC CHARACTERISTICS

| Description | Symbol | Conditions | Typ | 166 MHz | 150 MHz | 133 MHz | 100 MHz | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Power Supply Current: Operating | $I_{CC}$ | Device Selected; All Inputs ≤ $V_{IL}$ or ≥ $V_{IH}$; Cycle Time = $T_{CYC}$ MIN; $V_{CC}$ = MAX; Output Open | | 650 | 600 | 560 | 500 | mA | 1, 2 |
| Power Supply Current: Standby | $I_{SB2}$ | Device Deselected; $V_{CC}$ = MAX; All Inputs ≤ $V_{SS}$ + 0.2 or $V_{CC}$ - 0.2; All Inputs Static; CK Frequency = 0 | 30 | 60 | 60 | 60 | 60 | mA | 2 |
| Clock Running Standby Current | $I_{SB4}$ | Device Deselected; $V_{CC}$ = MAX; All Inputs ≤ $V_{SS}$ + 0.2 or $V_{CC}$ - 0.2; Cycle Time = $T_{CYC}$ MIN | | 140 | 120 | 100 | 80 | mA | 2 |

NOTES: 1. $I_{CC}$ is specified with no output current and increases with faster cycle times. $I_{CC}$ increases with faster cycle times and greater output loading.
2. Typical values are measured at 2.5V, 25°C, and 10ns cycle time.

## BGA CAPACITANCE

| Description | Symbol | Conditions | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Control Input Capacitance | $C_L$ | $T_A$ = 25°C; f = 1MHz | 5 | 7 | pF | 1 |
| Input/Output Capacitance (DQ) | $C_O$ | $T_A$ = 25°C; f = 1MHz | 6 | 8 | pF | 1 |
| Address Capacitance | $C_A$ | $T_A$ = 25°C; f = 1MHz | 5 | 7 | pF | 1 |
| Clock Capacitance | $C_{CK}$ | $T_A$ = 25°C; f = 1MHz | 3 | 5 | pF | 1 |

NOTES: 1. This parameter is sampled.

## AC CHARACTERISTICS

| Parameter | Symbol | 166MHz | | 150MHz | | 133MHz | | 100MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Clock Time | $t_{CYC}$ | 6.0 | | 6.7 | | 7.5 | | 10.0 | | ns |
| Clock Access Time | $t_{CD}$ | -- | 3.5 | -- | 3.8 | -- | 4.2 | -- | 5.0 | ns |
| Output enable to Data Valid | $t_{OE}$ | -- | 3.5 | -- | 3.8 | -- | 4.2 | -- | 5.0 | ns |
| Clock High to Output Low-Z | $t_{LZC}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Output Hold from Clock High | $t_{OH}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Output Enable Low to output Low-Z | $t_{LZOE}$ | 0.0 | -- | 0.0 | -- | 0.0 | -- | 0.0 | -- | ns |
| Output Enable High to Output High-Z | $t_{HZOE}$ | -- | 3.0 | -- | 3.0 | -- | 3.5 | -- | 3.5 | ns |
| Clock High to Output High-Z | $t_{HZC}$ | -- | 3.0 | -- | 3.0 | -- | 3.5 | -- | 3.5 | ns |
| Clock High Pulse Width | $t_{CH}$ | 2.2 | -- | 2.5 | -- | 3.0 | -- | 3.0 | -- | ns |
| Clock Low Pulse Width | $t_{CL}$ | 2.2 | -- | 2.5 | -- | 3.0 | -- | 3.0 | -- | ns |
| Address Setup to Clock High | $t_{AS}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| CKE Setup to Clock High | $t_{CES}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Data Setup to Clock High | $t_{DS}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Write Setup to Clock High | $t_{WS}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Chip Select Setup to Clock High | $t_{CSS}$ | 1.5 | | 1.5 | | 1.5 | | 1.5 | | ns |
| Address Hold to Clock high | $t_{AH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| CKE Hold to Clock High | $t_{CEH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| Data Hold to Clock High | $t_{DH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| Write Hold to Clock High | $t_{WH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| Chip Select Hold to Clock High | $t_{CSH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |

NOTES:

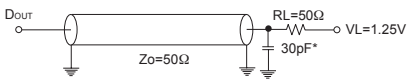
1. All Address inputs must meet the specified setup and hold times for all rising clock (CK) edges when ADV is sampled low and $CE_X$# is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip enable must be valid at each rising edge of CK (when ADV is Low) to remain enabled.
3. A write cycle is defined by WE# low having been registered into the device. A Read cycle is defined by WE# High. Both cases must meet setup and hold times.

## AC TEST CONDITIONS

($0°C \leq T_A \leq 70°C$, $V_{CC} = 2.5V \pm 5\%$, Unless Otherwise Specified)

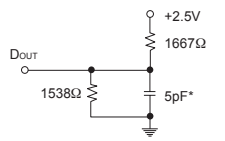
| Parameter | Value |
|---|---|
| Input Pulse Level | 0 to 2.5V |
| Input Rise and Fall Time (Measured at 20% to 80%) | 1.0V/ns |
| Input and Output Timing Reference Levels | 1.25V |
| Output Load | See Output Load (A) |

### OUTPUT LOAD (A)



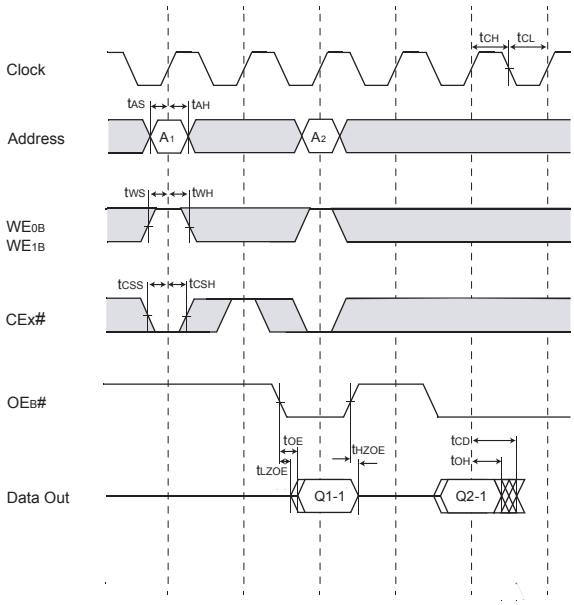

### OUTPUT LOAD (B)

(FOR $t_{LZC}$, $t_{LZOE}$, $t_{HZOE}$, and $t_{HZC}$)




***Including Scope and Jig Capacitance***

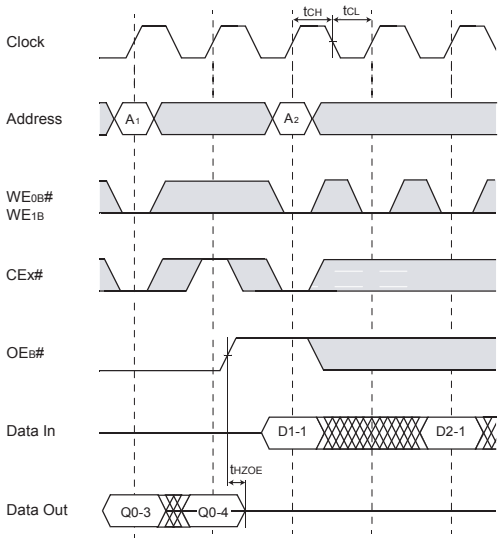
## FIG. 3 TIMING WAVEFORM OF READ CYCLE




NOTES: WRITE# = L means WE# = L, and BWx# = L
CEx# refers to the combination of $CE_1$#, $CE_2$, $CE_2$#.

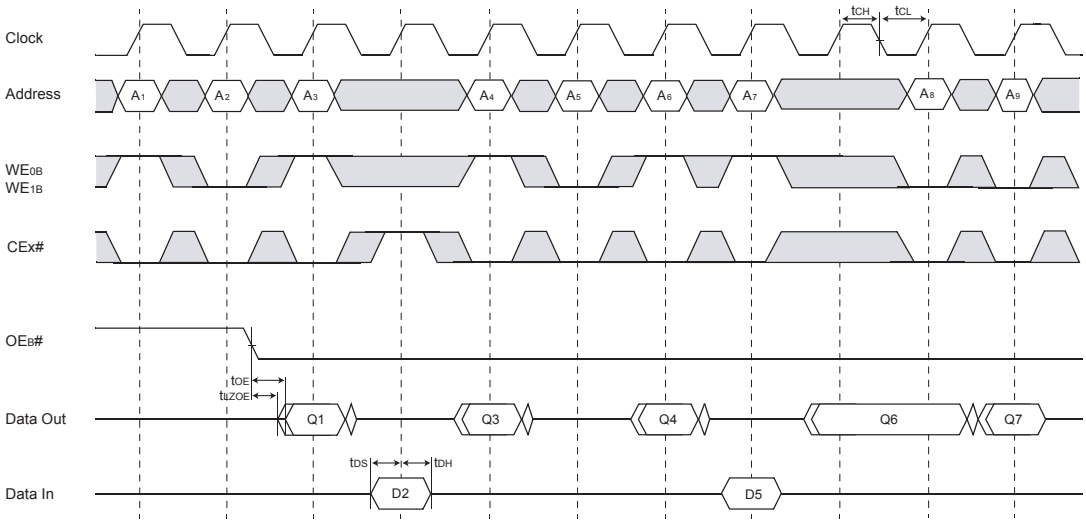
Don't Care
Undefined

## FIG. 4 **TIMING WAVEFORM OF WRITE CYCLE**



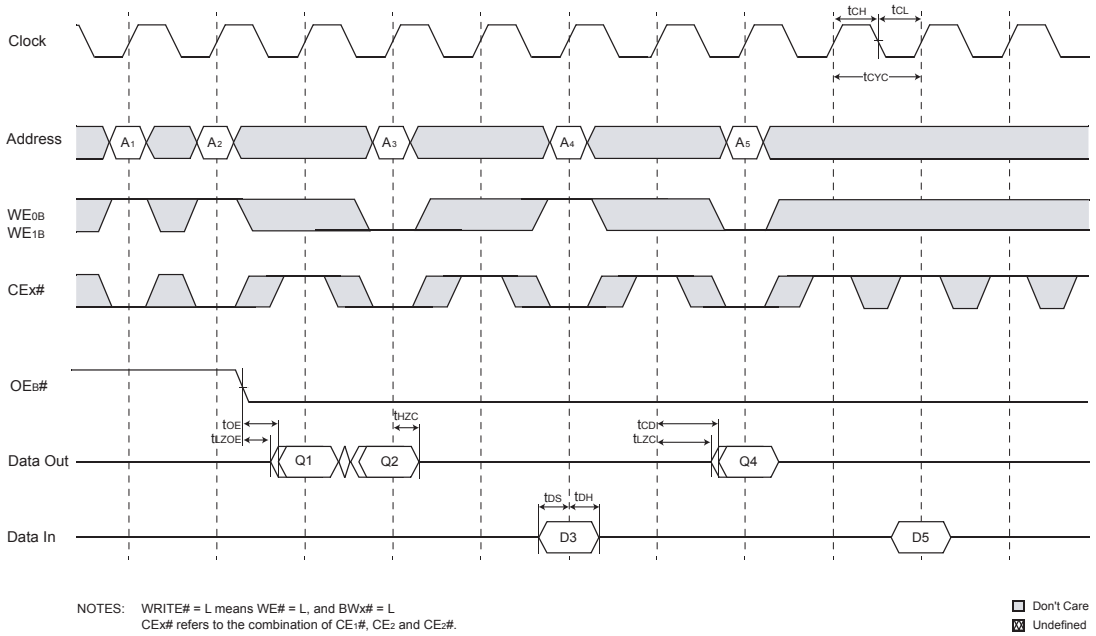

NOTES: WRITE# = L means WE# = L, and BWx# = L
CEx# refers to the combination of $CE_1$#, $CE_2$ and $CE_2$#.

## FIG. 5 **TIMING WAVEFORM OF SINGLE READ/WRITE**




NOTES: WRITE# = L means WE# = L, and BWx# = L
CEx# refers to the combination of $CE_1$#, $CE_2$ and $CE_2$#.

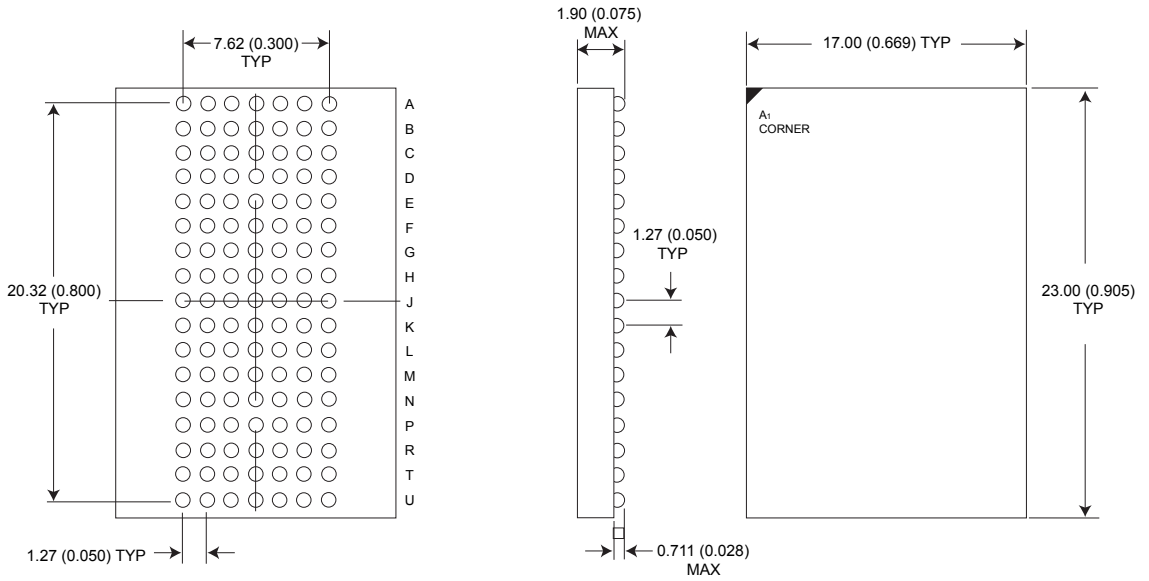
## FIG. 7 **TIMING WAVEFORM OF CE# OPERATION**




NOTES: WRITE# = L means WE# = L, and BWx# = L
CEx# refers to the combination of $CE_1$#, $CE_2$ and $CE_2$#.

Don't Care
Undefined

## PACKAGE DIMENSION: 119 BUMP PBGA




*ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES*

NOTE: Ball attach pad for above BGA package is 620 microns in diameter. Pad is solder mask defined.

## ORDERING INFORMATION

**COMMERCIAL TEMP RANGE (0°C ≤ TA ≤ 70°C)**

| Part Number | Configuration | $t_{CD}$ (ns) | Clock (MHz) |
|---|---|---|---|
| WED2ZL64512S35BC | 512K x 64 | 3.5 | 166 |
| WED2ZL64512S38BC | 512K x 64 | 3.8 | 150 |
| WED2ZL64512S42BC | 512K x 64 | 4.2 | 133 |
| WED2ZL64512S50BC | 512K x 64 | 5.0 | 100 |