*Preliminary Datasheet*

VSC7217

Multi-Gigabit Interconnect Chip

Features

- 4 ANSI X3T11 Fibre Channel and IEEE 802.3z Gigabit Ethernet Compliant Transceivers

- Over 8 Gb/s Duplex Raw Data Rate

- Redundant PECL Tx Outputs and Rx Inputs

- 8B/10B Encoder/Decoder per Channel, Optional Encoder/Decoder Bypass Operation

- "ASIC-Friendly™" Timing Options for Transmitter Parallel Input Data

- Elastic Buffers for Intra/Inter-Chip Cable Deskewing and Channel-to-Channel Alignment

- Tx/Rx Rate Matching via IDLE Insertion/Deletion

- Compatible with VSC7211/7212/7214

- Fast-Locking CRU: 100-Bit Clock Periods

- Received Data Aligned to Local REFCLK or to Recovered Clock

- PECL Rx Signal Detect and Cable Equalization

- Per-Channel Serial Tx-to-Rx and Parallel Rx-to-Tx Internal Loopback Modes

- Clock Multiplier Generates Baud Rate Clock

- Automatic Lock-to-Reference

- JTAG Boundary Scan Support for TTL I/O

- Built-In Self Test

- 3.3V Supply, 3.0W Typ, 3.5W Max.

- 256-pin, 27mm BGA Package

VSC7217 Block Diagram
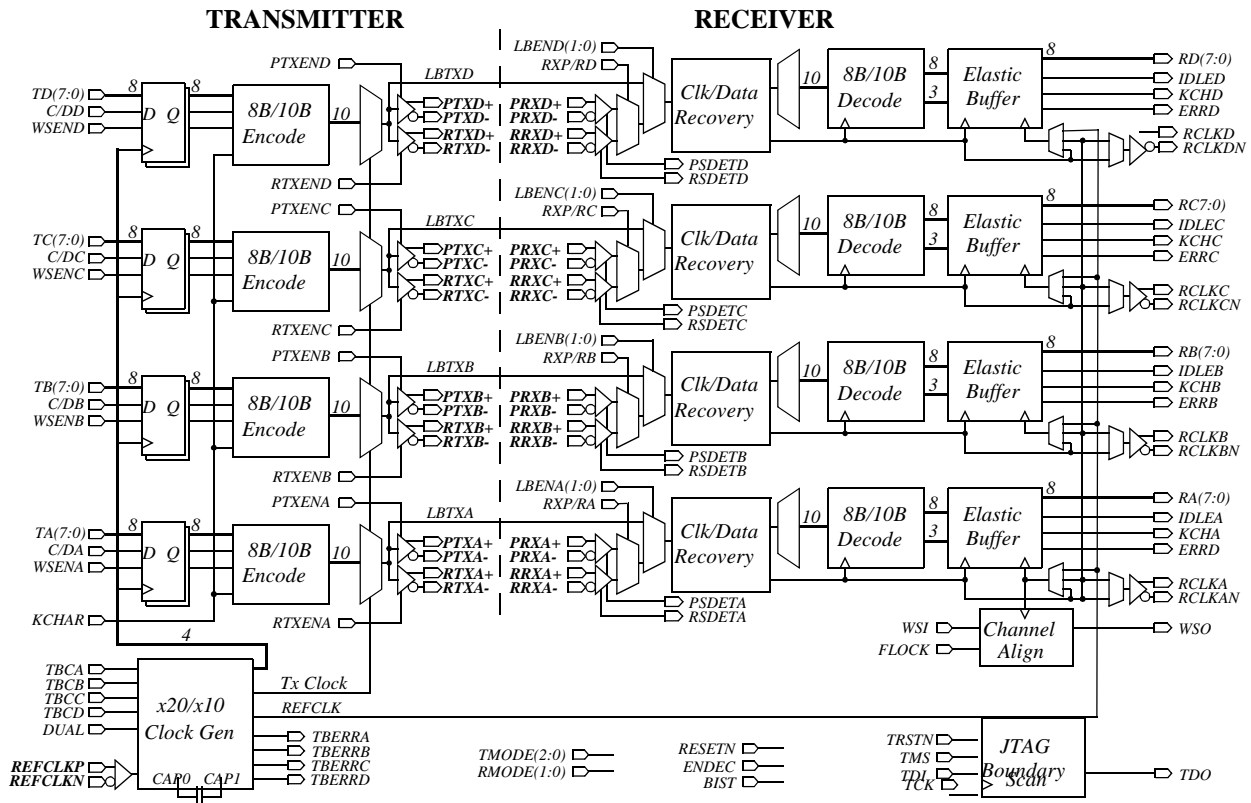
General Description

The VSC7217 is a quad 8-bit parallel-to-serial and serial-to-parallel transceiver chip used for high band-width interconnection between busses, backplanes, or other subsystems. Four Fibre Channel and Gigabit Ethernet compliant transceivers provide up to 8.32Gb/s of duplex raw data transfer. Each channel can be operated at a maximum data transfer rate of 1088Mb/s (8 bits at 136MHz) or a minimum rate of 784Mb/s (8 bits at 98MHz). For the entire chip in duplex mode, the aggregate transfer rate is between 6.3Gb/s and 8.7Gb/s. The VSC7217 contains four 8B/10B encoders, serializers, de-serializers, 8B/10B decoders and elastic buffers which provide the user with a simple interface for transferring data serially and recovering it on the receive side. The device can also be configured to operate as four non-encoded 10-bit transceivers.

Notation

In this document, each of the four channels are identified as channel A, B, C or D. When discussing a signal on any specific channel, the signal will have the channel letter embedded in the name: T$\underline{A}$(7:0). When referring to the common behavior of a signal which is used on each of the four channels, a lower case "n" is used in the signal name: T$\underline{n}$(7:0). Differential signals, such as PTXA+ and PTXA-, may be referred to as a single signal, PTXA, by dropping reference to the "+" and "-". REFCLK refers either to the PECL/TTL input pair REF-CLKP/REFCLKN, which can be differential PECL (using both REFCLKP and REFCLKN) or single-ended TTL (using REFCLKP and leaving REFCLKN open).

Clock Synthesizer

Depending on the state of the **DUAL** input, the VSC7217 clock synthesizer multiplies the reference frequency provided on the **REFCLK** input by 10 (**DUAL** is LOW) or 20 (**DUAL** is HIGH) to achieve a baud rate clock between 0.98GHz and 1.36 GHz. The on-chip Phase Lock Loop (PLL) uses a single external $0.1\mu F$ capacitor, connected between CAP0 and CAP1, to control the Loop Filter. This capacitor should be a multilayer ceramic dielectric, or better, with at least a 5V working voltage rating and a good temperature coefficient. NPO is preferred but X7R may be acceptable. These capacitors are used to minimize the impact of common mode noise on the Clock Multiplier Unit, especially power supply noise. Higher value capacitors provide better robustness in systems. NPO is preferred because if an X7R capacitor is used, the power supply noise sensitivity will vary with temperature. For best noise immunity, the designer may use a three capacitor circuit with one differential capacitor between CAP0 and CAP1, C1, a capacitor from CAP0 to ground, C2, and a capacitor from CAP1 to ground, C3 (Figure 1). Larger values are better but $0.1\mu F$ is adequate. However, if the designer cannot use a three capacitor circuit, a single differential capacitor, C1, is adequate. These components should be isolated from noisy traces.

Figure 1: Loop Filter Capacitors (Best Circuit)
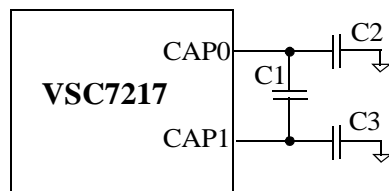
C1=C2=C3= >0.1uF
MultiLayer Ceramic
Surface Mount
NPO (Prefered) or X7R
5V Working Voltage Rating

The **REFCLK** signal can be either single-ended TTL or differential LVPECL. If TTL, connect the TTL input to **REFCLKP** but leave **REFCLKN** open. If LVPECL, connect the inputs to **REFCLKP** and **REF-CLKN**. Internal biasing resistors sets the proper DC Level to $V_{DD}/2$.

Transmitter Functional Description

Transmitter Data Bus

Each VSC7217 transmit channel has an 8-bit input transmit data character, **Tn(7:0)**, and two control inputs, **C/Dn** and **WSENn**. The **C/Dn** input determines whether a normal data character or a special "K-character" is transmitted, and the **WSENn** input initiates transmission of a 16-character "Word Sync Sequence" used to align the receive channels. These data and control inputs are clocked either on the rising edge of **REFCLK**, on the rising edge of **TBCn**, or within the data eye formed by **TBCn**. When not using **REFCLK**, each channel uses either its own **TBCn** input, or the **TBCA** input. The transmit interface mode is controlled by **TMODE(2:0),** as shown in Table 1.

When used, the **TBCn** inputs must be frequency locked to **REFCLK**. No phase relationship is assumed. A small skew buffer is provided to tolerate phase drift between **TBCn** and **REFCLK**. This buffer is recentered by the **RESETN** input, and the total phase drift after recentering must be limited to $\pm180°$ (where $360°$ is one character time). Each channel has an error output, **TBERRn**, that is asserted HIGH to indicate that the phase drift between **TBCn** and **REFCLK** has accumulated to the point that the elastic limit of the skew buffer has been exceeded and a transmit data character has been either dropped or duplicated. This error can not occur when input timing is referenced to **REFCLK**. The **TBERRn** output timing is identical to the low-speed receiver outputs, as selected by **RMODE(1:0)** in Table 5.

Table 1: Transmit Interface Input Timing Mode

| TMODE(2:0)	Input Timing Reference
0 0 0	REFCLK Rising Edge
0 0 1 0 1 0 0 1 1	Reserved
1 0 0	**TBCA** Rising Edge
1 0 1	**TBCn** Rising Edge
1 1 0	**TBCA** Data Eye
1 1 1	**TBCn** Data Eye

The following figures show the possible relationships between data and control inputs and the selected input timing source. Figure 2 shows how **REFCLK** is used as an input timing reference. This mode of operation is used in the VSC7211 and VSC7214. Figure 3 and Figure 4 show how **TBCn** is used as an input timing reference. When **TBCn** is used to define a data eye (see Figure 4), it functions as an additional data input that simply toggles every cycle.

Note that the **REFCLK** and **TBCn** inputs are not used directly to clock the input data. Instead, an internal PLL generates edges aligned with the appropriate clock. The arrows on the rising edges of these signals define the reference edge for the internal phase detection logic. An internal clock is generated at 1/10 the serial trans-

mit data rate that is locked to the selected input timing source. This is an especially important when **DUAL** is HIGH and input timing is referenced to **REFCLK**, since the falling edge is NOT used. The internal clock active edges are placed coincident with the **REFCLK** rising edges and halfway between the **REFCLK** rising edges in this mode.

A similar situation exists when **TBCn** is used to define a data eye. Only the rising edges of **TBCn** are used to define the external data timing. The internal clock active edges are placed at 90° and 270° points between consecutive **TBCn** rising edges (which are assumed to be 360° apart).
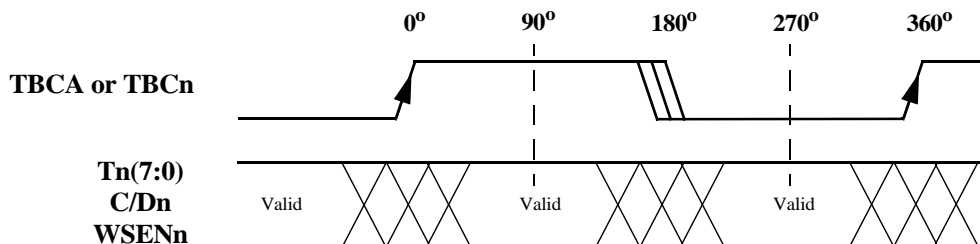
Figure 2: Transmit Timing, *TMODE(2:0)* = 000
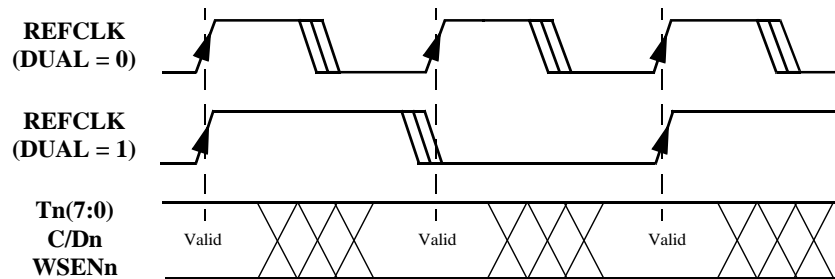
Figure 3: Transmit Timing, *TMODE(2:0)* = 10X
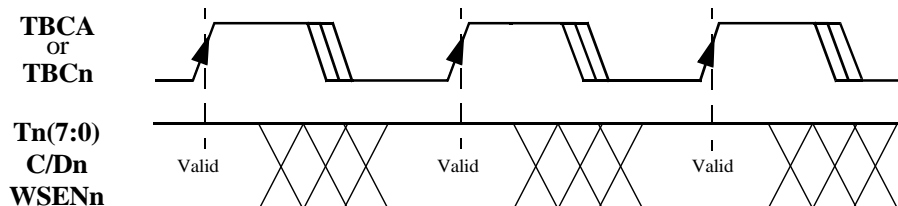
Figure 4: Transmit Timing, *TMODE(2:0)* = 11X ("ASIC-Friendly" Timing

8B/10B Encoder

Each channel contains an 8B/10B encoder which translates the 8-bit input data on **Tn(7:0)** into a 10-bit encoded data character. **C/Dn** inputs are also provided in each channel which, along with **KCHAR**, allow the transmission of special Fibre Channel Kxx.x characters (see Table 2). Note that **KCHAR** is a static input, and does NOT have the same input timing as **Tn(7:0)**, **C/Dn** and **WSENn**. Normally, **C/Dn** is LOW in order to transmit data. If **C/Dn** is HIGH and **KCHAR** is LOW, a Fibre Channel defined IDLE Character (K28.5 = '0011111010' or '1100000101' depending on disparity) is transmitted and **Tn(7:0)** is ignored. If **C/Dn** is HIGH and **KCHAR** is HIGH, a Kxx.x character is transmitted as determined by the data pattern on **Tn(7:0)**. See Table 3. Data patterns other than those defined in Table 3 produce undefined 10B encodings.

Table 2: Transmit Data Controls

WSENn	C/Dn	KCHAR	Encoded 10-bit Output
0	0	X	Data Character
0	1	0	IDLE Character (K28.5)
0	1	1	Special Kxx.x Character
1	X	X	16-Character Word Sync Sequence

Table 3: Special Characters (Selected when C/Dn and KCHAR are HIGH)

Code	Tn(7:0)	Comment	Code	Tn(7:0)	Comment
K28.0	000 11100	User Defined	K28.5-	101 01101	User Defined
K28.1	001 11100	User Defined	K28.6	110 11100	User Defined
K28.2	010 11100	User Defined	K28.7	111 11100	Test Only
K28.3	011 11100	User Defined	K23.7	111 10111	User Defined
K28.4	100 11100	User Defined	K27.7	111 11011	User Defined
K28.5	101 11100	IDLE	K29.7	111 11101	User Defined
K28.5+	101 01100	User Defined	K30.7	111 11110	User Defined

Encoder Bypass Mode

When **ENDEC** is LOW, the 8B/10B encoders are bypassed and a 10-bit input character **Tn(7:0)** is serialized directly in each channel, with bit **Tn0** transmitted first. The **C/Dn** input becomes **Tn8** and **WSENn** becomes **Tn9**. The **KCHAR** input becomes **ENCDET** which is not used in the transmitter but, when HIGH, enables Comma detection in all four receivers. Refer to the "Decoder Bypass Mode" section for a description of this mode of operation in the receiver. The latency through the transmitter is reduced by one character time when **ENDEC** is LOW. This mode of operation is similar to a 10-bit interface commonly found in serializer/deserializers for the Fibre Channel (VSC7125) and Gigabit Ethernet (VSC7135) markets.

Word Sync Generation

The VSC7217 can perform channel alignment (also referred to as "word alignment" or "word sync"). In other words, the four receive data output streams are aligned such that the same 4-byte word presented to the

four transmit channel inputs for serialization will be transferred on the receive channel parallel outputs. The Word Sync Sequence provides a unique synchronization point in the serial data stream that is used to align the receive channels. This sequence consists of 16 consecutive K28.5 IDLE characters with disparity reversals on the second and fourth characters. The Word Sync Sequence is sent either as "I+ I+ I- I- I+ I- I+ I- I+ I- I+ I- I+ I- I+ I-" or as "I- I- I+ I+ I- I+ I- I+ I- I+ I- I+ I- I+ I- I+", depending on the transmitter's running disparity at the time the first IDLE character is serialized.

Transmission of the Word Sync Sequence is initiated independently in each channel when the **WSENn** input is asserted HIGH for one character time (see Figure 5). When **WSENn** is HIGH, the **C/Dn** and **Tn(7:0)** inputs are ignored. The **WSENn**, **C/Dn** and **Tn(7:0)** inputs are also ignored for the subsequent 15 character times. In Figure 5 below, the Word Sync Sequence is initiated in cycle W1 and transmitted through cycle W16. Normal data transmission (or the transmission of another Word Sync Sequence) resumes in cycle D3. Figure 5 is drawn assuming that input timing is referenced to **REFCLK** (e.g., **TMODE(2:0)**=000) with the **DUAL** input LOW. As long as **WSENn** remains asserted, another Word Sync Sequence will be generated.

Figure 5: Word Sync Sequence Generation
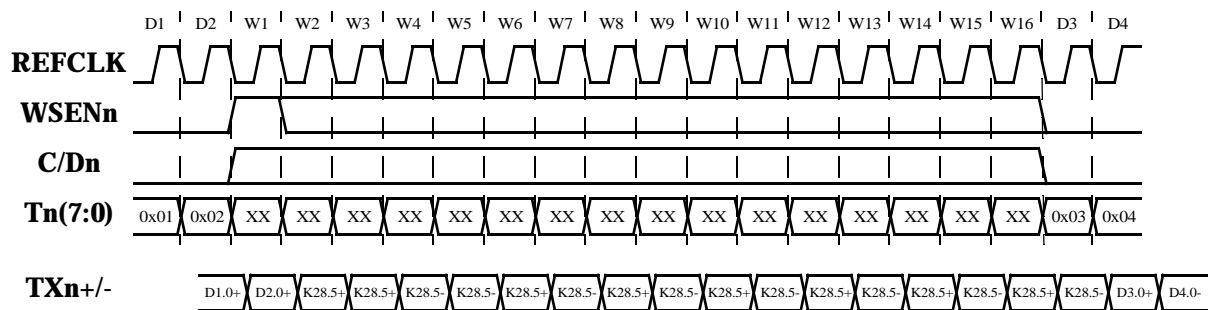
Serializer

The 10-bit output from the encoder (or from the encoder input register if **ENDEC** is LOW) is fed into a multiplexer which serializes the parallel data using the synthesized transmit clock. The least significant bit of the 10B data is transmitted first. Each channel has both primary and redundant serial output ports, **PTXn** and **RTXn**, respectively, which consists of differential PECL output buffers operating at either 10 or 20 times the **REFCLK** rate. The primary and redundant transmitter outputs are controllable separately on each channel. The primary PECL outputs (**PTXn**) are enabled when the **PTXENn** input is HIGH, and the redundant PECL outputs (**RTXn**) are enabled when the **RTXENn** input is HIGH. When a PECL output is disabled, the associated output buffers do not consume power and the attached pins are undriven.

Receiver Functional Description

Serial Data Source

Each receive channel has both primary (**PTXn**) and redundant (**RRXn**) serial input ports, which consists of differential PECL input buffers. Each channel also has a control input, **RXP/Rn**, used to select either the pri-

mary or redundant serial input as the data source for that channel. When **RXP/RC** is HIGH, the C channel serial data source is **PRXC**. When **LBENn(1:0)**=10, the channel's transmitter is looped back and becomes the serial data source regardless of the state of **RXP/Rn** (see Table 4).

Table 4: Serial Data Source Selection

LBENn(1:0)	*RXP/Rn*	*Serial Data Source*
≠ 1 0	0	RRXn
≠ 1 0	1	PRXn
= 1 0	X	LBTXn Loopback fromTransmitters

Signal Detection

Each channel's primary and redundant PECL input buffers have an associated signal detect output, **PSDETn** and **RSDETn**. All eight outputs are available for continuous monitoring of both the selected and non-selected input. Each signal detect output is asserted HIGH when transitions are detected on the associated PECL input and the signal amplitude exceeds 200 mV. A LOW indicates that either no transitions are detected or the signal amplitude is below 100mV. The signal detect outputs are considered undefined when the signal amplitude is in the 100mV to 200 mV range. The signal detect circuitry behaves like a re-triggerable one shot that is triggered by signal transitions, and whose time-out interval ranges from 40 to 80 bit times. The transition density is not checked to ensure that it corresponds to a valid Fibre Channel data stream. The **PSDETn** and **RSDETn** output timing is identical to the low-speed receiver outputs, as selected by **RMODE(1:0)** in Table 5.

Receiver Equalization

Incoming data on the **PRX/RRX** inputs typically contains a substantial amount of Inter Symbol Interference (ISI) or deterministic jitter which reduces the ability of the receiver to recover data without errors. An equalizer has been added to each of the receiver's input buffers in order to compensate for this deterministic jitter. This circuit has been designed to effectively reduce the ISI commonly found in copper cables or backplane traces due to low frequencies traveling faster than high frequencies as a result of the skin effect. The equalizer boosts high-frequency edge response in order to reduce the adverse effects of ISI.

Clock and Data Recovery

At the receiver, each channel contains an independent Clock Recovery Unit (CRU) that accepts the selected serial input source, extracts the high-speed clock and retimes the data. Each CRU automatically locks on data and if the data is not present, will automatically lock to the **REFCLK**. This maintains a very well-behaved recovered clock (**RCLKn/RCLKNn**) which does not contain any slivers and will operate at a frequency of the **REFCLK** reference ±200 ppm. The use of an external Lock-to-Reference pin is not needed.

The Clock Recovery Unit must perform bit synchronization which occurs when the CRU locks onto and properly samples the incoming serial data as described in the previous paragraph. When the CRU is not locked onto the serial data, the 10-bit data out of the decoder is invalid which results in numerous 8B/10B decoding errors or disparity errors. When the link is disturbed (the cable is disconnected or the serial data source is switched), the CRU will require a certain amount of time to lock onto data which is specified in the AC timing specifications for "Data Acquisition Lock Time."

Deserializer and Character Alignment

The retimed serial data stream is converted into 10-bit characters by the deserializer. A special 7-bit "Comma" pattern ('0011111xxx' or '1100000xxx') is recognized by the receiver and allows it to identify the 10-bit character boundary. Note that this pattern is found in three special characters: K28.1, K28.5 and K28.7. However, K28.5 is chosen as the unique IDLE character. Only K28.1 and K28.5 should be used in normal operation. The K28.7 character should be reserved for test and characterization use.

Character alignment occurs when the deserializer synchronizes the 10-bit character framing boundary to a "Comma" pattern in the incoming serial data stream. If the receiver identifies a "Comma" pattern in the incoming data stream, which is misaligned to the current framing boundary, the receiver will re-synchronize the recovered data in order to align the data to the new "Comma" pattern. Re-synchronization ensures that the "Comma" character is output on the internal 10-bit bus so that bits 0 through 9 equal '0011111xxx' or '1100000xxx'. If the "Comma" pattern is aligned with the current framing boundary, re-synchronization will not change the current alignment. Re-synchronization is always enabled and cannot be turned off when **ENDEC** is HIGH. After character re-synchronization the VSC7217 ensures that within a link, the 8-bit data sent to the transmitting VSC7217 will be recovered by the receiving VSC7217 in the same bit locations as the transmitter (e.g., **Tn(7:0)** = **Rn(7:0)**). When ENDEC is LOW, "Comma" detection and alignment are enabled only if **KCHAR** is HIGH.

10B/8B Decoder

The 10-bit character from the deserializer is decoded in the 10B/8B decoder, which outputs the 8B data byte and three bits of status information. If the 10-bit character does not match any valid value, an Out-of-Band Error is generated which is output on the receiver status bus. Similarly, if the running disparity of the character does not match the expected value, a Disparity Error is generated. The decoder also reports when a K-character is received, and distinguishes the K28.5 (IDLE) character from other K-characters. This status information is combined with LOS State Machine status and FIFO error status, to produce the prioritized per-character link status output information (see Table 7).

Elastic Buffer and Channel Deskewing

An elastic buffer is included in each of the four receive channels. Decoded data and status information is written into these buffers on each channel's recovered clock, and is read on the selected output clock. In addition to allowing decoded data to easily cross from a channel's recovered clock domain to its output clock domain, the elastic buffers facilitate channel alignment (the reconstruction of a multi-byte word as presented to the transmitting devices). In addition, the buffers facilitate rate matching via IDLE character insertion/deletion when the channel's recovered clock is not frequency locked to its output clock.

There are three conditions under which a receive channel's elastic buffer is recentered: (1) the **RESETN** input, when asserted, recenters the read/write pointers in each elasticity buffer, (2) whenever a Comma character is received which changes the receive character's framing boundary, and (3) whenever the receiver detects the synchronization point in the Word Sync Sequence. All three of these events are associated with chip initialization or link initialization and will not occur during normal data transfer. Note: recentering can result in the loss or duplication of decoded character data and status information.

When a condition change transmit timing (phase shifts in TBC) or shifts phase/alignment into the receiver, the user should initial a Word Sync Event to recenter all elasticity buffers. Otherwise, data corruption could occur.

The VSC7217 presents recovered data on **Rn(7:0)** and status on **IDLEn**, **KCHn** and **ERRn**. These outputs are timed either to each channel's own recovered clock (**RCLKn/RCLKNn**), to Channel A's recovered clock (**RCLKA/RCLKNA**), or to **REFCLK**. The output timing reference is selected by **RMODE(1:0)** (see Table 5). The transmitter input skew buffer error outputs **TBERRn** and the analog signal detect outputs **PSDETn** and **RSDETn** are also synchronized to the selected output timing reference. There are two choices for **REFCLK**-based timing, which differ in the positioning of the data valid window associated with the output signals timed to **REFCLK**. When **RMODE(1:0)**=00, **REFCLK** is approximately centered in the output data valid window as in the VSC7214. When **RMODE(1:0)**=01, **REFCLK** slightly leads the data valid window so that output data appears to have a more typical "Clock-to-Q" timing relationship to **REFCLK**.

Table 5: Receive Interface Output Timing Mode

RMODE(1:0)	Output Timing Reference
0 0	REFCLK (Centered)
0 1	REFCLK (Leading)
1 0	RCLKA/RCLKNA
1 1	RCLKn/RCLKNn

The term "word clock" is used for whichever clock (**REFCLK**, **RCLKA**/**RCLKNA** or **RCLKn**/**RCLKNn**) is selected as the output timing reference. If **RMODE(1)** is HIGH, each channels' **RCLKn**/**RCLKNn** outputs are complementary outputs at 1/10th or 1/20th the baud rate of the incoming data depending upon **DUAL**. When **RCLKA**/**RCLKNA** is selected as the output timing reference, Channel B, C and D **RCLKn**/**RCLKNn** outputs are copies of **RCLKA**/**RCLKNA**. If **RMODE(1)** is LOW, each channels' **RCLKn**/**RCLKNn** outputs are held in a LOW/HIGH state, respectively, and the data and status outputs are timed to **REFCLK**. If **DUAL** is HIGH, all data at the four output ports are synchronously clocked out on both positive and negative edges of the selected word clock at 1/20th the baud rate. If **DUAL** is LOW, the data is clocked out of the VSC7217 only on the rising edge of the selected word clock at 1/10th the baud rate. Timing waveforms for the output data and status are shown in Figure 6, Figure 7 and Figure 8.

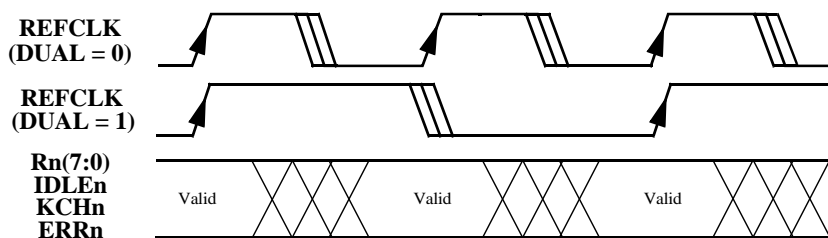**Figure 6: Receive Timing, *RMODE(1:0) = 00***
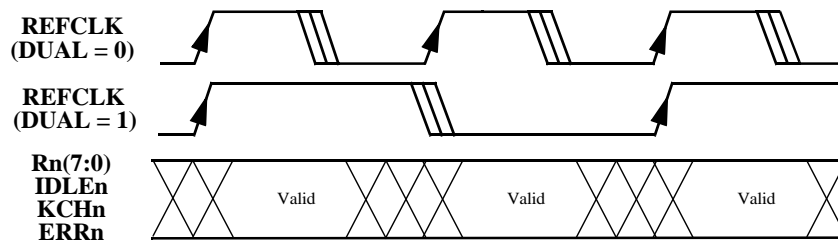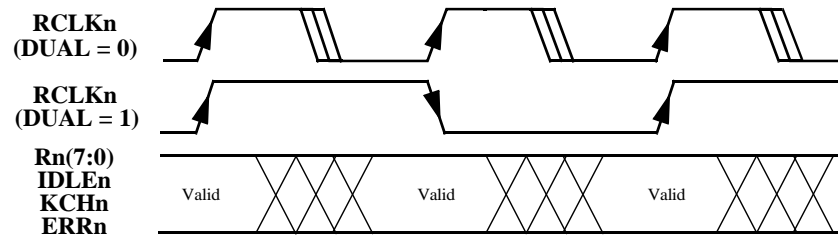
Figure 7: Receive Timing, *RMODE(1:0)* = 01

REFCLK (DUAL = 0)
REFCLK (DUAL = 1)
Rn(7:0) IDLEn KCHn ERRn
Valid   Valid   Valid

Figure 8: Receive Timing, *RMODE(1:0)* = 1X

RCLKn (DUAL = 0)
RCLKn (DUAL = 1)
Rn(7:0) IDLEn KCHn ERRn
Valid   Valid   Valid

The data coming from the decoder is clocked into the elastic buffer by the recovered clock from the channel's CRU. The data is clocked out of the elastic buffers with word clock. If the transmitting device's **REFCLK** is not precisely frequency locked to a receive channel's word clock, then the channel's elastic buffer will tend to gradually fill or empty as the recovered clock (which is by definition frequency locked to the transmitter's **REFCLK**) steadily drifts in phase relative to the word clock.

To accommodate frequency differences between a transmitter's **REFCLK** and the word clock, the VSC7217 can automatically perform rate matching by either deleting or duplicating IDLE characters. The **FLOCK** input must be LOW to enable rate matching which, based on how the **WSI** input is connected, can either be performed in each channel individually or can be performed in parallel across a group of channels that are word-aligned. This is discussed in detail in the following section describing **Word Alignment**. The user must ensure that the frequency at which IDLEs are simultaneously transmitted on each channel accommodates the frequency differences, if any, in their system architecture. Not meeting the IDLE density requirements could result in Underrun/Overrun Errors.

The elastic buffer is designed to allow a maximum phase drift of +2 or -2 serial clock bit times between re-synchronizations, which sets a limit on the maximum data "packet" length allowed between IDLEs. This maximum packet length depends on the frequency difference between the transmitting and receiving devices **REF-CLK**s. Let $\Delta\phi$ represent phase drift in bit times, and let 2π represent one full 10-bit character of phase drift. Limiting phase drift to two bit times means the following inequality must be satisfied:

$$(1) \qquad \Delta\phi \leq (0.2 \times 2\pi)$$

Let *L* be the number of 10-bit characters transmitted, and let Δf be the frequency offset in ppm. The total phase drift in bit times is given by:

$$(2) \qquad \Delta\phi \;=\; (\Delta f / 10^6) \times 2\pi L$$

A simple expression for maximum packet length as a function of frequency offset is derived by substituting Equation (2) in Equation (1) and solving for *L*:

$$(3) \qquad L \leq (0.2 \times 10^6) / \Delta f$$

As an example, if the frequency offset is 200 ppm, the maximum packet length should not be more than 1K bytes. To increase the maximum packet length *L*, decrease the frequency offset Δf. Please note that if only on K28.5 is transmitted between "packets" of data, it might be dropped during compensation for phase drift. If the user must have at least one K28.5 between these two packets, then two K28.5s must be transmitted.

Word Alignment

The VSC7217 performs channel-to-channel word alignment. In this mode of operation, if the data from all four channels on the transmitting VSC7217 (the 4 **Tn(7:0)** busses) is viewed as a 32-bit word, then the receiving VSC7217 will recover an identical word. For example, if a transmit pattern was 'ABCD', 'EFGH', 'IJKL', etc., the receiver should not recover data words as 'ABGD', 'EFKH', 'IJOL', etc. This requires the four transmit channels to obtain input data on a common clock (**TMODE(2:0)**=000 or 1X0) and the four receive channels to present output data on a common word clock (**RMODE(1:0)**=0X or 10).

There are elastic buffers within the receiver used to deskew the four channels and align them to a common word clock. An elastic buffer allows the channels' input to be skewed up to ±6 bit times (12 bit times total skew between any two channels) to accommodate circuit imperfections, differences in transmission delay and jitter. Multiple VSC7217 devices can also be used in synchronous operation if the skew between all serial input pairs is maintained less than ±6 serial clock bit times. This allows easy implementation of robust systems and is discussed in greater detail in the *Using Multiple VSC7217s in Parallel* section.

In order to perform word alignment, a synchronization point must be seen across all aligned receive channels within the ±6 bit time window. The VSC7217 receiver recognizes the first four characters of the Word Sync Sequence (either K28.5+ K28.5+ K28.5- K28.5- or K28.5- K28.5- K28.5+ K28.5+) as the synchronization point. As a model for understanding, consider the case where a VSC7217 transmitter sends 32 bits of data to the receiver via copper media, which has small cable length differences, causing a channel-to-channel skew. All transmit channels that are to be word-aligned transmit the Word Sync Sequence in parallel. On detection of the synchronization point, the receivers will reposition the recovered data within their elastic buffers in order to align all four channels and remove any channel-to-channel skew. All normal data characters following the

Word Sync Sequence will be properly word-aligned. In the process of channel alignment, one or two of the final twelve K28.5 characters in the Word Sync Sequence may be deleted or duplicated. This ensures that each transmitted 32-bit word is recovered correctly.

The VSC7217 is capable of performing rate matching in word-aligned applications by inserting or deleting IDLEs in parallel across the aligned receive channels. This requires that the word-aligned data streams contain IDLEs inserted in parallel on all transmit channels (e.g., an IDLE "word") according to the IDLE density requirement previously described.

Word alignment is enabled by connecting the **WSI** input to a **WSO** output, either from the same device if a single device is used, or from another device if multiple devices are used in parallel to align more than four channels. The **FLOCK** input state and **WSI** input source determine whether or not rate matching (IDLE deletion or duplication) will be performed, and whether it is done independently on each channel or in parallel across aligned channels. Word alignment is disabled when **WSI** is not connected to a **WSO** output. Rate matching is disabled when either **FLOCK** is HIGH or **WSI** is held LOW (see Table 6).

Table 6: Word Alignment and Rate Matching Control

FLOCK	*WSI Source*	*Word Alignment*	*Rate Matching*
0	0	Off	Off
0	1	Off	Enabled, Independent Channels
0	WSO	Enabled	Enabled, Aligned Channels
1	0	Off	Off
1	1	Off	Off
1	WSO	Enabled	Off

There are four distinct modes of operation defined in Table 6. The first row disables both word alignment and rate matching. (The fourth and fifth row configurations function identically to the first row.) The second row configures the channels to operate independently with rate matching. Word alignment is disabled, and IDLEs will be dropped/duplicated independently in each channel as required. The third row configures the part to perform word alignment and rate matching. The receive channels will be aligned per the device driving WSO, and IDLE words will be dropped/duplicated across the aligned channels as required. The last row configures the part to perform word alignment and disables rate matching. This mode of operation is appropriate for a frequency-locked application where it desired to align the receive channels without altering the received data streams.

Using Multiple VSC7217s in Parallel

Multiple VSC7217s can be used in parallel to form wider bus widths. In order for word alignment to function correctly across multiple devices, each transmit channel's input data must be transmitted on a common clock, and each receive channel's output data must also be aligned to a common word clock. This requires that all transmitting devices use either the same or identical **REFCLK**s, and that **TMODE(2:0)**=000 (inputs timed to **REFCLK**) or **TMODE(2:0)**=1X0 (inputs timed to **TBCA**). If inputs are timed to **TBCA**, then all transmitting devices must use either the same or identical **TBCA**s. Since all receive channels must use a common word clock, the receiving devices must also use the same or identical **REFCLK**s and it must be selected as the word clock for all receive channels (**RMODE(1:0)**=0X).

If the transmitting devices' **REFCLK**s are not frequency locked to the receiving devices' **REFCLK**s, IDLEs will have to be added to or dropped from all the channels at the same time. In order to implement this, one VSC7217 is arbitrarily chosen as the "Master" and its **WSO** output is driven to the **WSI** inputs of all the receiving VSC7217s, including itself. **WSO** is asserted prior to the VSC7217 adding/dropping IDLEs so all the VSC7217s will operate simultaneously. **WSO** uses a simple 3-bit serial protocol, synchronous to the Master channel's word clock, for indicating the required synchronization action to other VSC7217s. A steady LOW level indicates no action is required. '101' indicates that Master Channel A has seen a Word Sync Event. The relative timing relationship between receiving a Word Sync Event (on all channels together) and seeing '101' on the **WSI** input in the other channels allows these channels to word-synchronize with Master Channel A. '110' indicates that the next IDLE encountered in the receive data stream should be deleted. '111' indicates that an IDLE should be inserted after the next IDLE encountered in the receive data stream. Note that the arbitrarily chosen Master Channel A must be an active channel.

Decoder Bypass Mode

If **ENDEC** is LOW, the 8B/10B decoder is bypassed and a 10-bit received character **Rn(9:0)** is output from each receive channel. The **KCHn** output becomes **Rn8,** and **ERRn** becomes **Rn9**. Character alignment is handled differently in this mode of operation. As mentioned in the "Encoder Bypass Mode" section, the **KCHAR** input becomes **ENCDET** which enables Comma detection and re-synchronization when HIGH, and disables re-synchronization when LOW. Only the '0011111xxx' version of the Comma pattern is recognized when **ENDEC** is LOW. The **IDLEn** output becomes **COMDET** (Comma Detect) which signals detection of the '0011111xxx' Comma pattern in the current 10-bit output character when high. This mode of operation is equivalent to a 10-bit interface commonly found in serializer/deserializers for the Fibre Channel (VSC7125) and Gigabit Ethernet markets (VSC7135).

The logic used to align the four receive channels and/or insert and delete IDLE characters to compensate for REFCLK variations between transmitting and receiving devices is disabled when **ENDEC** is LOW. In order for this mode of operation to function without errors, the word clock source, as selected by **RMODE(1:0)**, must be frequency-locked to the REFCLK of the remote transmitting device in each channel. This is guaranteed when **RMODE(1:0)** = 11. For other choices of **RMODE(1:0)**, the frequency locked condition must be guaranteed by system design. When **DUAL** is HIGH and **RMODE(1:0)** = 10 or 11, the character containing the '0011111xxx' Comma pattern is aligned to **RCLKn**/**RCLKNn** in each channel so that **COMDET** will be asserted on the falling edge of **RCLKn** (rising edge of **RCLKNn**). This is done by adjusting the latency through the elastic buffer; the recovered clock is never stretched or slivered. When the Comma pattern changes the framing boundary, data characters prior to the assertion of **COMDET** on the falling edge of **RCLKn** may be corrupted.

Receiver State Machine

Each channel contains a Loss of Synchronization State Machine (LSSM) which is responsible for detecting and handling loss of bit, channel, word and word clock synchronization in a controlled manner. There are three states in the LSSM: LOSS_OF_SYNC, RESYNC, and SYNC_ACQUIRED as shown in the state diagram of Figure 9. The RESYNC state is entered when a 10-bit word has been received which contains the 7-bit Comma pattern (e.g., a K28.5 IDLE character). After entering the RESYNC state, the VSC7217 will stay in it until a valid, non-Comma transmission is received, then it transitions to the SYNC_ACQUIRED state indicating a normal operating condition. The RESYNC state is re-entered if four consecutive Commas are received or if a single Comma is received that changes the 10B character framing boundary. The LOSS_OF_SYNC state is

entered whenever four consecutive invalid transmissions have been detected or when the occurrences of invalid transmission outnumber those of valid transmission by four. The relative occurrences of invalid vs. valid transmissions are monitored with a simple up/down counter that increments when an invalid transmission is detected and decrements otherwise. The LSSM transitions to the LOSS_OF_SYNC state when the counter reaches four, and the counter is reset. A state diagram for the invalid transmission counter is shown in Figure 10. The VSC7217 receiver will stay in the LOSS_OF_SYNC state until a valid Comma pattern is detected. Note that the RESYNC state is entered whenever the 10B framing boundary is changed, and whenever the Word Sync Sequence is received. When **ENDEC** is LOW the **ERRn**, **KCHn** and **IDLEn** outputs are re-defined and the decoder and associated LSSM logic in each channel is unused.

Figure 9: State Diagram of the Loss of Synchronization State Machine
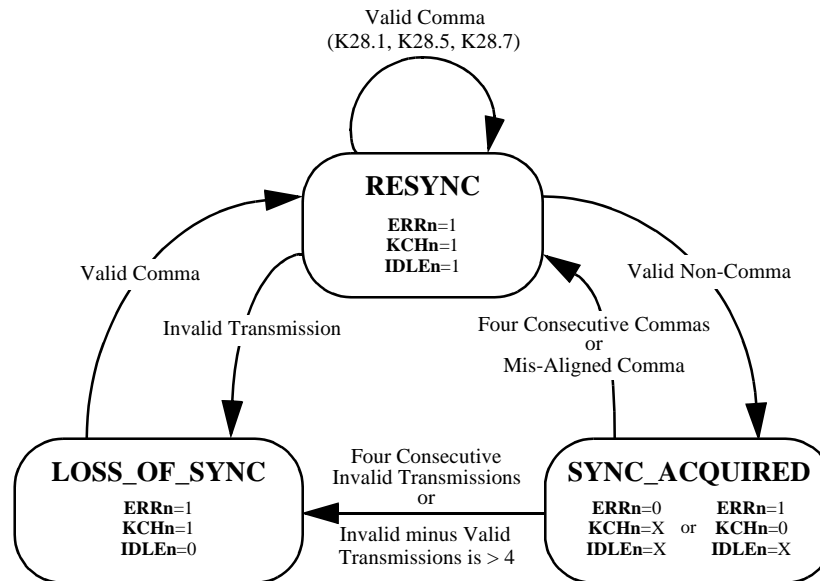
Figure 10: State Diagram of the Invalid Transmission Counter

G52325-0, Rev. 3.0
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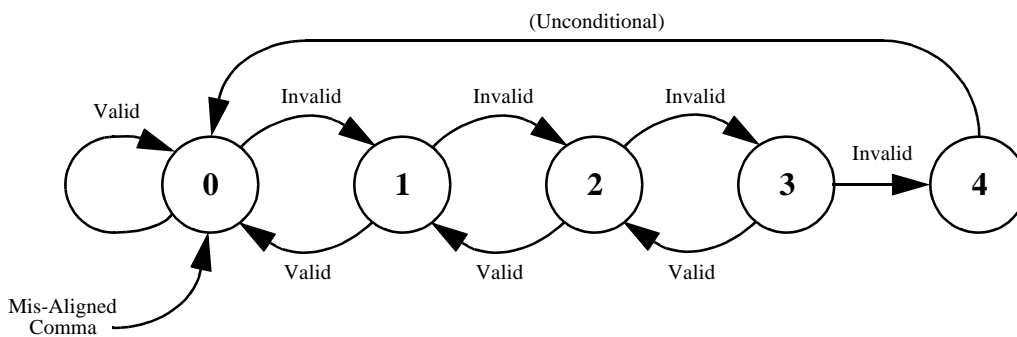
Link Status Outputs

The receiver **ERRn**, **KCHn** and **IDLEn** outputs indicate status for each channel as shown below in Table 7. Since this status is encoded, multiple conditions could occur simultaneously so the states are prioritized as indicated (1 being highest priority). For example, if both Out-of-Band and Disparity Errors occur, only an Out-of-Band Error is reported because it has higher priority.

The **ERRn**, **KCHn** and **IDLEn** status signals apply to the data on **Rn(7:0)** on a per-character basis. The only exception to this is the Underrun/Overrun indication. This indication is asserted coincident with the duplicated character when an underrun occurs, and is asserted following the deleted character (e.g., on the cycle where the deleted character should have appeared) when overrun occurs.

Table 7: Receiver Status Signals

ERRn	KCHn	IDLEn	Priority	Link Status
0	0	0	7	**Valid Data Transmission:** A valid 10B data character with correct disparity was received. The correctly decoded version of this character is on **Rn(7:0)**.
0	0	1	1	**Underrun/Overrun Error:** The elastic buffer has not been able to add/drop an IDLE when required. Data on **Rn(7:0)** is invalid.
0	1	0	6	**Kxx.x Special Character Detected (not IDLE):** A valid 10B special character with correct disparity was received. The correctly decoded version of this character, per Table 3, is on **Rn(7:0)**.
0	1	1	5	**IDLE Detected:** A valid IDLE character (K28.5) with correct disparity was received. The correctly decoded version of this character, per Table 3, is on **Rn(7:0)**.
1	0	0	3	**Out-of-band Error Detected**: A character was received which was not a valid 10B data or control character. Data on **Rn(7:0)** is invalid.
1	0	1	4	**Disparity Error Detected:** A valid 10B character was received which did not have the expected disparity. **Rn(7:0)** is invalid.
1	1	0	2	**Loss of Synchronization:** The receiver state machine is in the Loss-of-Sync state. Data on **Rn(7:0)** is invalid.
1	1	1	2	**RESYNC:** The receiver state machine is in the Re-Synchronization state. Data on **Rn(7:0)** is a decoded version of K28.1, K28.5 or K28.7.

Loopback Operation

Loopback control pins, **LBENn(1:0)**, are provided in each channel to internally loopback data paths for on-chip diagnosis. Both serial and parallel loopback functions are provided.

Table 8: Loopback Mode Selection

LBENn(1:0)	Loopback Mode
0 0	Normal Operation
0 1	Internal Parallel Loopback
1 0	Internal Serial Loopback
1 1	Reserved

When **LBENn(1:0)**=10, Serial Loopback mode is selected. The transmitter's serial transmit data is internally connected to the receiver's CRU input. The serial loopback paths are labelled LBTXn in the VSC7217 block diagram on the first page. This allows parallel data on **Tn(7:0)** to be encoded, serialized, looped back, deserialized and decoded. This mode is intended for the system to verify functionality of the local VSC7217 prior to attempting to establish an external link. The **PTXn** and **RTXn** outputs are unaffected by the state of **LBENn(1:0)**.

When **LBENn(1:0)**=01, Parallel Loopback mode is selected. The **Rn(7:0)** outputs are looped back to the **Tn(7:0)** inputs (see Figure 11). **WSENn** does not have a loopback source and is internally connected to a logic LOW. **KCHAR** does not have a loopback source and is internally connected to a logic HIGH. The **C/Dn** input is obtained by decoding the link status outputs such that either a data character, special character, or IDLE (K28.5) is transmitted. When the link is in the LOS or RESYNC states, **C/Dn** is asserted and the data path is set to 0xBC so that an IDLE will be transmitted. For other link status conditions **C/Dn** follows the **KCHn** status bit. This guarantees that IDLE and special characters will be correctly looped back along with normal data, and also has the effect of looping back the data received as a normal data character when a disparity error, out-of-band character, or underflow/overflow link status condition occurs.

In Parallel Loopback mode, the receiver uses an internal copy of **REFCLK** as the word clock in each receiver. This data is looped back to the transmitter with **TMODE(2:0)** internally set to 000. This guarantees that the parallel loopback data to be re-transmitted will be frequency-locked to the transmitter's **REFCLK**. This also means that the receiver parallel output data timing will not match the normal system timing that is externally selected by **RMODE(1:0)**. The parallel output data should be ignored in this mode of operation.

This internal loopback configuration also allows rate matching to be performed in the receivers' elastic buffers. Rate matching is controlled and operates exactly the same way that it does in normal mode. This is required to avoid receiver Overrun/Underrun errors in the loopback device if the remote transmitting device's **REFCLK** is not frequency-locked to the loopback device's **REFCLK**. Keep in mind that the **LBENn(1:0)**, **RXP/Rn**, **PTXENn**, **RTXENn** and **BIST** inputs must all be configured appropriately in order for end-to-end parallel loopback to function correctly in a user environment. Parallel Loopback mode is internally disabled when BIST mode is enabled.

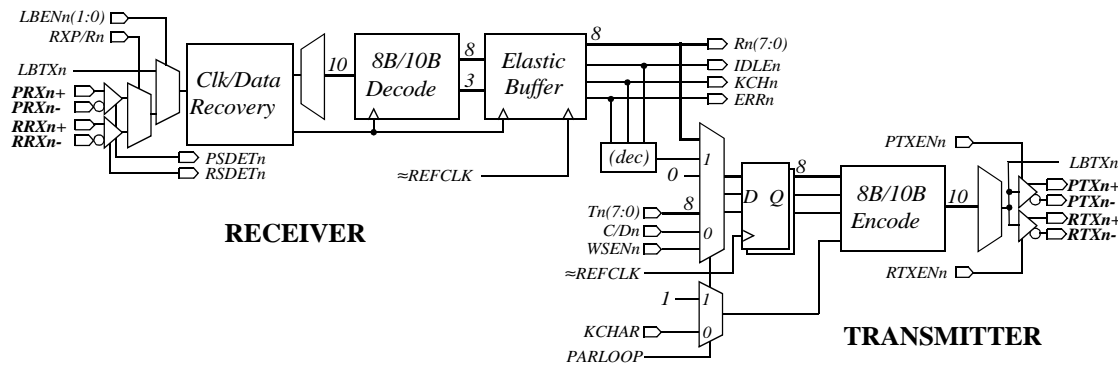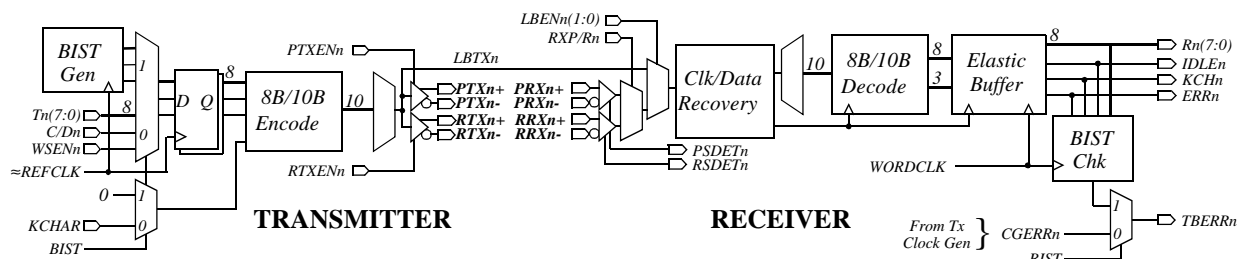**Figure 11: Parallel Loopback Mode Operation**

Figure 12: BIST Mode Operation

Built-In Self-Test Operation

Built-In Self-Test operation is enabled when the **BIST** input is HIGH, which causes **TMODE(2:0)** to be internally set to 000. Upon entering BIST mode, the transmitter will issue a Word Sync Sequence in order to recenter the elasticity buffers in the receive channel. Each transmitter then repeatedly sends a simple 256-byte incrementing data pattern (prior to 8B/10B encoding) followed by three IDLE characters (K28.5). Note that this incrementing pattern plus three IDLEs will cause both disparities of each data character and the IDLE character to be transmitted, and contains a sufficient IDLE density for any application requiring IDLE insertion/deletion. It is up to the user to enable IDLE insertion/deletion if the receiver's word clock is not frequency-locked to the transmitter's **REFCLK**.

Each receiver monitors incoming data for this pattern and indicates if any errors are detected. Correct reception of the pattern is reported on each receiver's **TBERRn** output. A LOW means the pattern is being received correctly and a HIGH means that errors are detected. When **BIST** transitions from LOW to HIGH, each **TBERRn** output is initialized HIGH. It will be cleared LOW whenever one or more IDLE characters, followed by all 256 data characters, are sequentially received without error, and set HIGH whenever a pattern mismatch or receiver error is encountered. Each channel functions independently, no attempt is made to word-align the receive channels. Received data and associated status will be output as in normal operation. Please note that Serial Loopback mode and receiver output timing mode selection via **RMODE(1:0)** operate independently of BIST mode, but BIST mode disables Parallel Loopback mode.

Compatibility with VSC7214 and VSC7211

Care has been taken in the functional definition of the VSC7217 ensure compatiblity with the VSC7211 and VSC7214 at the serial link level, and that the transmitter and receiver low-speed interfaces have compatible modes of operation. It is strongly recommended that the VSC7217 not be connected in any way through the **WSO** and/or **WSI** pins to a VSC7211 or VSC7214.

Serial Link Compatibility

The VSC7217 uses the same Fibre Channel 8b/10b encoding scheme and the same Word Sync Sequence used in the VSC7211 and VSC7214. The only difference in serial link operation is that the VSC7211 and VSC7214 require four consecutive identically-aligned Comma patterns to set the character framing boundary, while the VSC7217 requires a single Comma. This means that from the LOSS_OF_SYNC state, the VSC7217 will make an earlier transition to the RESYNC state (one Comma instead of four) as shown in Figure 9. Once out of the LOSS_OF_SYNC state, there is no difference in receiver behavior in the absence of data link errors. When transmitting in 32-bit mode from a VSC7217 to a VSC7211 or VSC7214, use **TMODE(2:0)**=000 or =1X0 (common transmit interface timing source) to minimize transmitter inter-channel skew.

Parallel Interface Compatibility

In general, the VSC7217 low-speed parallel interfaces can be configured so that there are input and output signals that are compatible with their VSC7211 and VSC7214 counterparts. On the transmit interface, the signals **Tn(7:0)** and **C/Dn** behave identically on the VSC7217 as long as the input timing is referenced to **REF-CLK** (e.g., **TMODE(2:0)**=000). On the receive interface, the signals **Rn(7:0)**, **ERRn**, **KCHn** and **IDLEn** behave identically on the VSC7217 as long as the four receive channels present output data centered around **REFCLK** (**RMODE(1:0)**=00) or timed to **RCLKA**/**RCLKNA** (**RMODE(1:0)**=10). When **RMODE(1:0)**=10 the VSC7217 **RCLKn**/**RCLKNn** outputs provide four copies of **RCLKA**/**RCLKNA**, which are equivalent to the VSC7211 and VSC7214 **RCLK**/**RCLKN** outputs.

The VSC7217 **KCHAR** input is no longer a synchronous input timed to **REFCLK** as on the VSC7211 and VSC7214. It is a static input used to define the control character encoding mode when **C/Dn**=1 as shown in Table 2. The VSC7217 also has a separate **WSENn** input per channel instead of a common **WSYNC** input as on the VSC7211 and VSC7214.

Operational Mode Compatibility

The VSC7211 and VSC7214 specifications define eight operating modes based on the binary combinations of the **RCLKEN**, **FLOCK** and **INDEP** inputs. Note that these mode inputs control VSC7211 and VSC7214 receiver operation only, and have no effect on transmitter operation. For each of these modes, the equivalent VSC7217 receiver configuration is presented.

VSC7214 MODE 0: RCLKEN=LOW, FLOCK=LOW, INDEP=LOW

Receiver **Rn(7:0)**, **ERRn**, **KCHn** and **IDLEn** outputs are synchronous to **REFCLK**, IDLE insertion/deletion is enabled, and the receive channels are word-aligned. The VSC7217 should be configured with **RMODE(1:0)**=00, **FLOCK**=0, and **WSI** connected to its own **WSO** or to the **WSO** of another VSC7217 if multiple devices are to be used in parallel. The **WSI** connection allows IDLE insertion/deletion to occur in parallel across all word-aligned channels.

VSC7214 MODE 1: RCLKEN=LOW, FLOCK=LOW, INDEP=HIGH

Receiver **Rn(7:0)**, **ERRn**, **KCHn** and **IDLEn** outputs are synchronous to **REFCLK**, IDLE insertion/deletion is enabled, and the receive channels are independent. The VSC7217 should be configured with **RMODE(1:0)**=00, **FLOCK**=0, and **WSI**=1. The **WSI** connection inhibits channel alignment, and allows IDLE insertion/deletion to occur independently in each channel.

VSC7214 MODE 2: RCLKEN=LOW, FLOCK=HIGH, INDEP=LOW

Receiver **Rn(7:0)**, **ERRn**, **KCHn** and **IDLEn** outputs are synchronous to **REFCLK**, IDLE insertion/deletion is disabled, and the receive channels are word-aligned. The VSC7217 should be configured with **RMODE(1:0)**=00, **FLOCK**=1, and **WSI** connected to its own **WSO** or to the **WSO** of another VSC7217 if multiple devices are to be used in parallel. The **WSI** connection allows word alignment to occur, and the **FLOCK** connection inhibits IDLE insertion/deletion.

VSC7214 MODE 3: RCLKEN=LOW, FLOCK=HIGH, INDEP=HIGH

Receiver **Rn(7:0)**, **ERRn**, **KCHn** and **IDLEn** outputs are synchronous to **REFCLK**, IDLE insertion/deletion is disabled, and the receive channels are independent. The VSC7217 should be configured with **RMODE(1:0)**=00, **FLOCK**=1, and **WSI**=0. The **WSI** connection inhibits channel alignment, and the **FLOCK** connection inhibits IDLE insertion/deletion.

VSC7214 MODE 4: RCLKEN=HIGH, FLOCK=LOW, INDEP=LOW

This configuration does not require IDLE insertion/deletion, use Mode 6 instead.

VSC7214 MODE 5: RCLKEN=HIGH, FLOCK=LOW, INDEP=HIGH

Receiver **Rn(7:0)**, **ERRn**, **KCHn** and **IDLEn** outputs are synchronous to **RCLKn/RCLKNn**, IDLE insertion/deletion is enabled, and the receive channels are independent. The VSC7217 should be configured with **RMODE(1:0)**=10, **FLOCK**=0, and **WSI**=1. The **WSI** connection inhibits channel alignment, and allows IDLE insertion/deletion to occur independently in each channel. The B, C and D channel **RCLKn**/ **RCLKNn** outputs are copies of **RCLKA/RCLKNA**.

VSC7214 MODE 6: RCLKEN=HIGH, FLOCK=HIGH, INDEP=LOW

Receiver **Rn(7:0)**, **ERRn**, **KCHn** and **IDLEn** outputs are synchronous to **RCLKn/RCLKNn**, IDLE insertion/deletion is disabled, and the receive channels are word-aligned. The VSC7217 should be configured with **RMODE(1:0)**=10, **FLOCK**=1, and **WSI** connected to its own **WSO**. Multiple VSC7217 devices should not be used in parallel when the outputs are synchronous to **RCLKn/RCLKNn**. The **WSI** connection allows word alignment to occur, and the **FLOCK** connection inhibits IDLE insertion/deletion.

VSC7214 MODE 7: RCLKEN=HIGH, FLOCK=HIGH, INDEP=HIGH

Receiver **Rn(7:0)**, **ERRn**, **KCHn** and **IDLEn** outputs are synchronous to **RCLKn/RCLKNn**, IDLE insertion/deletion is disabled, and the receive channels are independent. The VSC7217 should be configured with **RMODE(1:0)**=10, **FLOCK**=1, and **WSI**=0. The **WSI** connection inhibits channel alignment, and the **FLOCK** connection inhibits IDLE insertion/deletion.

AC Specifications

Figure 13: Transmit Input Timing Waveforms with *TMODE* = 000
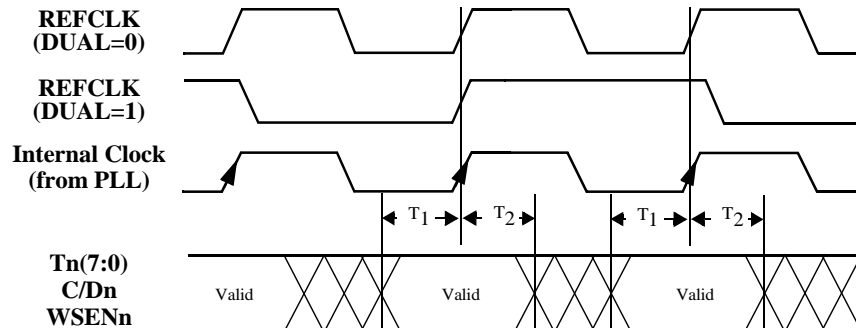
Figure 14: Transmit Input Timing Waveforms with *TMODE* = 10X
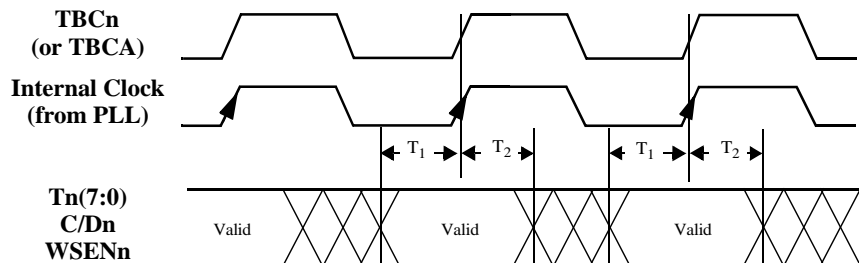
Table 9: Transmit Input AC Characteristics with *TMODE* = 000 or *TMODE* = 10X

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	Input Setup time to the rising edge of **REFCLK** or **TBCn**	1.5	—	ns	Measured between the valid data level of the input and the 1.4V point of **REFCLK** or **TBCn**.
T_2	Input Hold time after the rising edge of **REFCLK** or **TBCn**	1.0	—	ns	

**Figure 15: Transmit Input Timing Waveforms with *TMODE* = 11X ("ASIC-Friendly" Timing)**
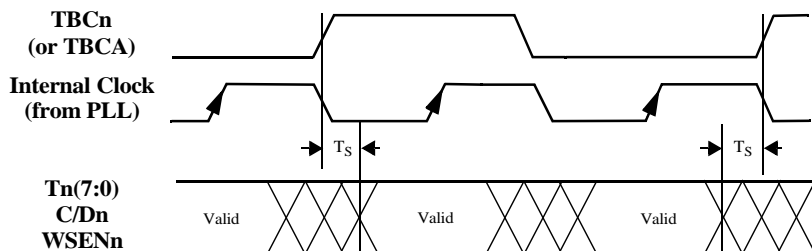
Table 10: Transmit Input AC Characteristics with *TMODE* = 11X

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_S	Input Skew relative to the rising edge of **TBCn** or **TBCA**	—	2.0	bc	Measured between the valid data level of the input and the 1.4V point of **TBCn** or **TBCA**, bc = Bit Clock.

Figure 16: Transmit Serial Timing Waveforms
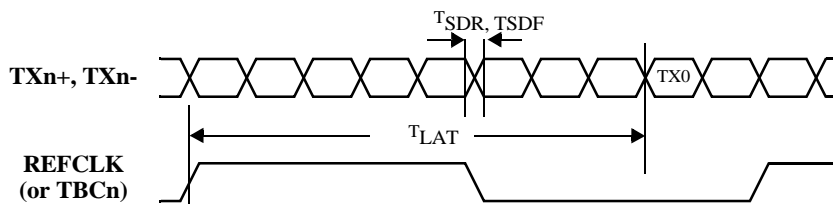
Table 11: Transmit Serial AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_{SDR}, T_{SDF}	**TXn**+/- Rise and Fall Times	—	330	ps	Measured between 20% to 80% of the valid data level.
T_{LAT}	Latency, **REFCLK** to **TX0** Latency, **TBCA** to **TX0** Latency, **TBCB/C/D** to **TX0**	22bc+0.2ns 36bc+0.0ns 32bc+0.1ns	22bc+0.8ns 38bc+0.3ns 42bc+0.6ns	bc + ns	ENDEC=1 TMODE=000 ENDEC=1 TMODE=10X ENDEC=1 TMODE=101
T_J	Serial Data Output Total Jitter (p-p)	—	192	ps	IEEE 802.3z Clause 38.69, tested on a sample basis.
T_{DJ}	Serial Data Output Deterministic Jitter (p-p)	—	80	ps	IEEE 802.3z Clause 38.69, tested on a sample basis.

Figure 17: Receive Output Timing Waveforms with *RMODE* = 00 or 01
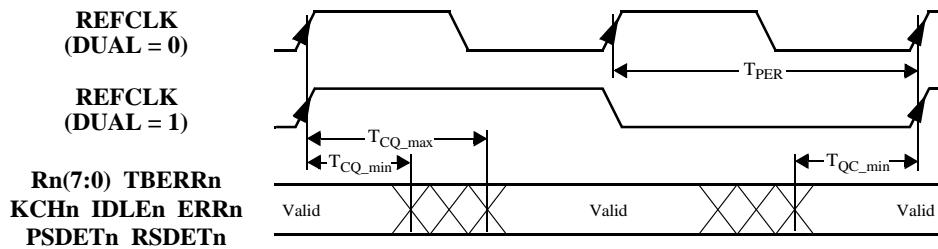
Table 12: Receive Output AC Characteristics with *RMODE* = 00 or 01

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_{CQ}	**REFCLK** Rising Edge to TTL Output Transition	2.58 ns - 0 bc	5.43 ns - 0 bc	ns	RMODE = 00 bc = Bit Clock
T_{CQ}	**REFCLK** Rising Edge to TTL Output Transition	2.58 ns - 2 bc	5.43 ns - 2 bc	ns	RMODE = 01 bc = Bit Clock
T_{QC}	TTL Output Transition to **REFCLK** Rising Edge	$T_{PER} - T_{CQ\_max}$		ns	

Figure 18: Receive Output Timing Waveforms with *RMODE* = 10 or 11
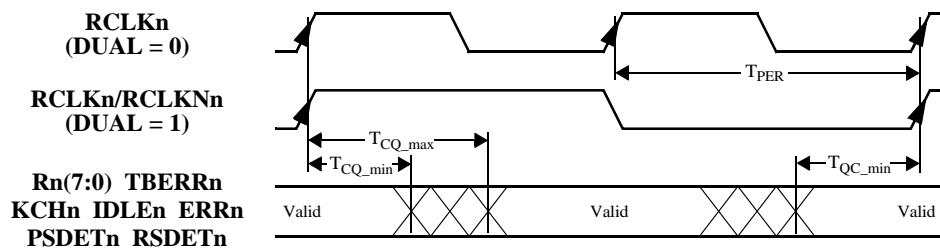
Table 13: Receive Output AC Characteristics with *RMODE* = 10 or 11

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_{CQ}	**RCLKn/RCLKNn** Rising Edge to TTL Output Transition	-1.25 ns + 4 bc	1.25 ns + 4 bc	ns	**RMODE** = 10 or 11 bc = Bit Clock
T_{CQ}	TTL Output Transition to **RCLKn/RCLKNn** Rising Edge	$T_{PER} - T_{CQ\_max}$	$T_{PER} - T_{CQ\_min}$	ns	
DC	**RCLKn/RCLKNn** Duty Cycle	50% - 1 ns	50% + 1 ns	ns	Measured at 1.4. V

Figure 19: RCLKn and RCLKNn Timing Waveforms with *DUAL* = 1
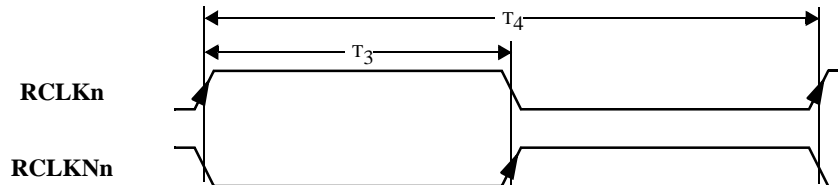
Table 14: General Receive AC Characteristics

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_3	Delay Between Rising Edge of **RCLKn** to Rising Edge of **RCLKNn**	$10 \times T_{RX}$ -500	$10 \times T_{RX}$ +500	ps	T_{RX} is the bit period of the incoming data on Rx.
ΔT_3	**RCLKn** to **RCLKNn** Skew $Delay = \frac{10}{f_{baud}} \pm \Delta T_3$	-500	500	ps	Deviation of **RCLKn** rising edge to **RCLKNn** rising edge. Nominal delay is 10 bit times.
T_4	Period of **RCLKn** and **RCLKNn**	$0.99 \times T_{REFCLK}$	$1.01 \times T_{REFCLK}$	ps	Whether or not locked to serial data, independent of DUAL input.
ΔT_4	Deviation of **RCLK/RCLKN** Period from **REFCLK** Period $T_{RCLK} = T_{REFCLK} \pm \Delta T_4$	-1.0	1.0	%	Whether or not locked to serial data, independent of DUAL input.
T_R, T_F	Output Rise and Fall Time	—	2.4	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$ into 10pf load.
R_{LAT}	Latency from **RX0** to **REFCLK** or **RCLK**	70.5bc-1.6ns 48.5bc-1.6ns	81.5bc+4.1ns 102.5bc+4.1ns	bc+ns	ENDEC=1, Recenter only ENDEC=X, Recenter + Drift
$T_{LOCK}(1)$	Data Acquisition Lock Time	—	100	bc	Using K28.5+/K28.5- pattern. tested on a sample basis.
T_{JTD}	Receive Data Total Jitter Tolerance (p-p)		600	ps	IEEE 802.3z Clause 38.68, tested on a sample basis.
D_{JTD}	Receive Data Deterministic Jitter Tolerance (p-p)		370	ps	IEEE 802.3z Clause 38.69, tested on a sample basis.

NOTE: (1) The probability of correct data acquisition and recovery is 99% per FC-PH 4.3 Section 5.3.

Figure 20: REFCLK Timing Waveforms
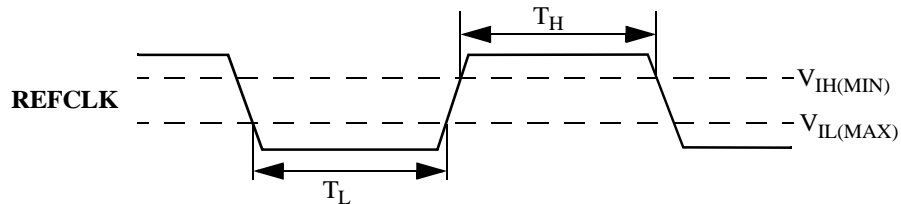
Table 15: Reference Clock Requirements

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR	Frequency Range	98	136	MHz	**DUAL** = 0
		49	68	MHz	**DUAL** = 1
FO	Frequency Offset	-200	200	ppm	| **REFCLK** (Tx) - **REFCLK** (Rx) | = max offset between Tx and Rx device **REFCLK**s on one serial link.
DC	**REFCLK** Duty Cycle	35	65	%	Measured at 1.4V.
T_H, T_L	**REFLCK** and **TBC** Pulse Width	3	—	ns	
T_{RCR}, T_{RCF}	**REFCLK** Rise and Fall Times	—	1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.
REFCLK Jitter	REFCLK Jitter Power $$\int_{100Hz}^{3MHz} PhaseNoise$$	—	100	ps	Peak-to-peak jitter at VSC7217 **REFCLK** input.

Figure 21: Parametric Measurement Information

Serial Input Rise and Fall Time

80%
20%

T_r T_f

TTL Input and Output Rise and Fall Time

$V_{IH(MIN)}$
$V_{IL(MAX)}$

T_r T_f
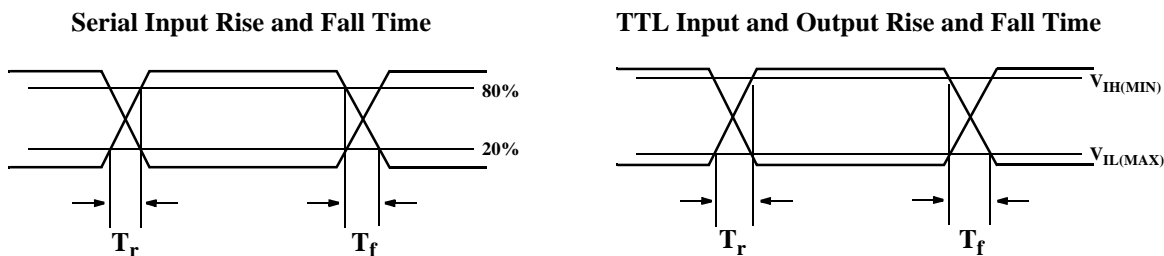
Receiver Input Eye Diagram Jitter Tolerance Mask

Bit Time

Amplitude

Eye Width%
25%
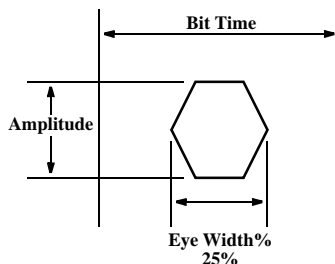
Parametric Test Load Circuit

Serial Output Load

$Z_0 = 50\Omega$

50Ω

$V_{DD} - 2.0V$

TTL AC Output Load

10 pF
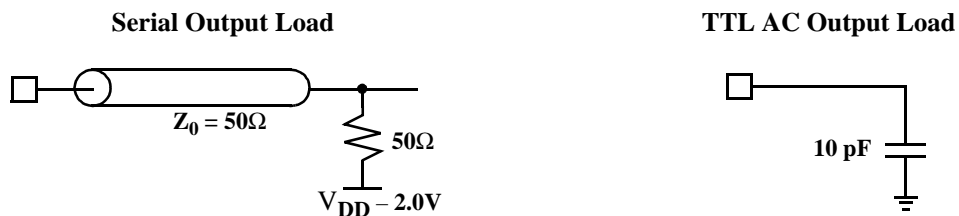
DC Characteristics

Parameters	Description	Min.	Typ	Max.	Units	Conditions
TTL Outputs (Rn(7:0), KCHn, IDLEn, ERRn, RCLKn/RCLKNn, TBERRn, PSDETn, RSDETn, WSO)						
V_{OH}	TTL Output HIGH Voltage	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	TTL Output LOW Voltage	—	—	0.5	V	I_{OL} = +1.0mA
I_{OZ}	TTL Output Leakage Current	—	—	TBD	μA	When set to high-impedance state through JTAG.
TTL Inputs (TBCn, Tn(7:0), C/Dn, WSENn, KCHAR, RATE, BIST, LBENn(1:0), TMODE(2:0), RMODE(1:0), DUAL, PTXENn, RTXENn, RXP/Rn, RESETN, ENDEC, WSI, FLOCK, TRSTN, TDI, TDO, TMS, TCK)						
V_{IH}	TTL Input HIGH Voltage	2.0	—	—	V	
V_{IL}	TTL Input LOW Voltage	0	—	0.8	V	
I_{IH}	TTL Input HIGH Current	—	50	500	μA	V_{IN} =2.4V
I_{IL}	TTL Input LOW Current	—	—	-1000	μA	V_{IN} =0.5V
PECL Inputs (REFCLKP/REFCLKN)						
V_{IH}	PECL Input HIGH Voltage	V_{DD} - 1.1	—	V_{DD} - 0.7	V	
V_{IL}	PECL Input LOW Voltage	V_{DD} - 2.0	—	V_{DD} - 1.5	V	
I_{IH}	PECL Input HIGH Current	—	—	200	μA	V_{IN} =$V_{IH(MAX)}$
I_{IL}	PECL Input LOW Current	- 50	—	—	μA	V_{IN} =$V_{IL(MIN)}$
ΔV_{IN}	PECL Input Differential Peak-to-Peak Voltage Swing	200	—	—	mV	$\mid V_{IH(MIN)}$ - $V_{IL(MAX)} \mid$[a]
V_{CM}	PECL Input Common-Mode Voltage	V_{DD} - 1.5	—	V_{DD} - 0.7	V	
V_{BIAS}	REFCLKP/REFCLKN Internal Input bias voltage	—	V_{DD}/2	—		
PECL Outputs (PTXn+/-, RTXn+/-)						
ΔV_{OUT}	PECL Differential Peak-to-Peak Output Voltage Swing	450	—	1100	mV	$\mid$ **PTXn**+ - **PTXn**- $\mid$[a] 50Ω to V_{DD} - 2.0V
PECL Inputs (PRXn+/-, RRXn+/-)						
ΔV_{IN}	PECL Differential Peak-to-Peak Input Voltage Swing	200	—	1300	mV	$\mid$ **PRXn**+ - **PRXn**- $\mid$[a]
Miscellaneous						
V_{DD}	Power Supply Voltage	3.14	—	3.47	V	3.3V $\pm$ 5%
P_D	Power Dissipation	—	3.0	3.5	W	Maximum at 3.47V, 130MHz redundant I/O OFF
I_{DD}	Supply Current	—	910	1000	mA	Typical at 3.3V, outputs open

a. *Single ended measurement results are quoted here. Differential techniques used in Fibre Channel would yield values that are twice the magnitude. See diagram below.*
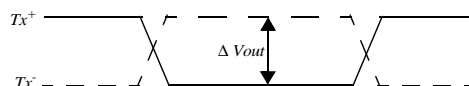
Absolute Maximum Ratings [1]

Power Supply Voltage, (any V_{DDX}) .... 0.5V to +3.8V

PECL Differential Input Voltage .... -0.5V to V_{DD} +0.5V

TTL Input Voltage .... -0.5V to +5.5V

TTL Output Voltage .... -0.5V to V_{DD} + 0.5V

TTL Output Current 50mA

PECL Output Current 50mA

Case Temperature Under Bias, (T_C) .... -55° to +125°C

Storage Temperature, (T_{STG}) .... -65°C to +150°C

Note: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) .... +3.3V$\pm$5%

Operating Temperature Range, ... 0°C Ambient to +95°C Case

Table 16: Pin Table

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	ERRC	RD0	RD3	VSST	RD7	ERRD	VSST	TBERRD	RSDETD	VDDD	WSI	RCLKA	VSST	PSDETA	TBERRA	VSST	RA5	RA4	RA1	RCLKNB
19	VSST	VDDT	RSDETC	RD1	VDDT	RD4	VDDT	IDLED	VDDT	TDO	VSSD	RCLKNA	VDDT	KCHA	RA6	VDDT	RA2	PSDETB	VDDT	VSST
18	RC4	TBERRC	VSST	PSDETC	RCLKC	VSST	RD6	KCHD	VSST	RCLKND	VDDT	VSST	ERRA	RA7	VSST	RA0	RSDETB	VSST	IDLEB	RB5
17	RC3	VDDT	IDLEC	VDDT	RCLKNC	RD2	RD5	VDDT	PSDETD	RCLKD	WSO	RSDETA	IDLEA	VDDT	RA3	RCLKB	VDDT	TBERRB	VDDT	RB4
16	RC0	VSST	RC7	KCHC												ERRB	KCHB	VSST	VSST	RB1
15	TCK	RC2	RC6	RC5												RB6	RB7	RB3	VDDD	VDDD
14	TDI	VDDT	VSST	RC1												RB2	VSST	VDDT	VDDT	RSVD2
13	TRSTN	TMS	VSSD	VDDD												VSSD	RB0	FLOCK	VDDD	RSVD1
12	TC7	C/DC	WSENC	BIST				*NOT POPULATED*								RESETN	ENDEC	KCHAR	WSENB	VDDD
11	VSSD	VDDD	TC6	TC5												TB7	C/DB	TB6	VDDD	VDDD
10	TC4	TC3	TC1	TC2												TB3	TB2	TB4	TB5	TB5
9	TC0	TBCC	TBCD	REFCLKN												TBCA	TBCB	TB0	TB1	TB1
8	REFCLKP	WSEND	TD6	TD7												TA6	VDDD	VSSD	WSENA	WSENA
7	VSSD	TD5	VSSD	TD3												TA2	TA3	TA5	C/DA	C/DA
6	C/DD	TD2	TD1	TMODE1												RMODE0	VSSD	TA1	TA7	TA7
5	TD4	TD0	VDDD	TMODE0												DUAL	VDDD	TA0	TA4	TA4
4	RRXC-	TMODE2	VSSD	VDDD	VSSD	LBENC0	LBEND0	PTXEND	PTXENC	VSSA	VDDA	PTXENB	PTXENA	LBENA0	LBENB0	VSSD	VDDD	VSSD	RMODE1	RRXB-
3	RRXC+	RXP/RC	VSSD	VDDD	LBEND1	VDDRD	RTXEND	RTXENC	VDDPC	VSSD	VDDD	VDDPB	RTXENB	RTXENA	VDDRA	LBENA1	LBENB1	VSSD	RXP/RB	RRXB+
2	PRXC-	RRXD-	LBENC1	RXP/RD	RTXD-	PTXD-	VDDPD	RTXC-	PTXC-	VSSA	VDDA	PTXB-	RTXB-	VDDPA	PTXA-	RTXA-	PRXA-	RXP/RA	RRXA-	PRXB-
1	PRXC+	RRXD+	VDDD	PRXD+	RTXD+	PTXD+	VDDRC	RTXC+	PTXC+	CAP0	CAPI	PTXB+	RTXB+	VDDRB	PTXA+	RTXA+	PRXA+	VDDD	RRXA+	PRXB+

Table 17: Pin Description

Pin	Name	I/O	Type	Pin Description
6Y, 8U, 7W, 5Y, 7V, 7U, 6W, 5W	TA(7:0)	I	TTL	**T**ransmit Data for Channel **n**. Synchronous to REFCLK, TBCA or TBCn.
11U, 11W, 10Y, 10W, 10U, 10V, 9Y, 9W	TB(7:0)	I	TTL	**T**ransmit Data for Channel **n**. Synchronous to REFCLK, TBCB or TBCn.
12A, 11C, 11D, 10A, 10B, 10D, 10C, 9A	TC(7:0)	I	TTL	**T**ransmit Data for Channel **n**. Synchronous to REFCLK, TBCC or TBCn.
8D, 8C, 7B, 5A, 7D, 6B, 6C, 5B	TD(7:0)	I	TTL	**T**ransmit Data for Channel **n**. Synchronous to REFCLK, TBCD or TBCn.
7Y 11V 12B 6A	C/DA C/DB C/DC C/DD	I	TTL	**C**ontrol/**D**ata for Channel **n**. If KCHAR=C/Dn=LOW, then Tn(7:0) is used to generate transmit data. If KCHAR=C/Dn=HIGH, then special Kxx.x characters are transmitted based upon the value of Tn(7:0). If KCHAR=LOW and C/Dn=HIGH, IDLE characters are transmitted. When ENDEC=LOW, this is equivalent to data bit **Tn8**.
8Y 12Y 12C 8B	WSENA WSENB WSENC WSEND	I	TTL	**W**ord **S**ync **EN**able for Channel **n**. Asserted HIGH for one cycle to initiate transmission of the Word Sync Sequence as defined in Figure 5 and related text. When ENDEC=LOW, this is equivalent to data bit **Tn9**.
9U 9V 9B 9C	TBCA TBCB TBCC TBCD	I	TTL	**T**ransmit **B**yte **C**lock for Channel **n**. Optional input data timing reference for Tn(7:0), WSENn and C/Dn.
12W	KCHAR	I	TTL	Special **K**xx.x **CHAR**acter Enable. When C/Dn is HIGH, KCHAR controls data sent to the transmitter. When LOW, IDLE characters are sent. When HIGH, Kxx.x special characters are sent as encoded on Tn(7:0). This is intended to be a static input and cannot be changed on a cycle-by-cycle basis. When ENDEC=LOW, this is equivalent to **ENCDET**.
5D 6D 4B	TMODE0 TMODE1 TMODE2	I	TTL	**T**ransmit Input Data Timing **MODE**. Determines the timing reference for Tn(7:0), WSENn and C/Dn on all channels as defined in Table 1.
20R 17V 18B 20H	TBERRA TBERRB TBERRC TBERRD	O	TTL	**T**ransmit **B**uffer **ERR**or for Channel **n**. When HIGH indicates that the elastic limit of the transmit input skew buffer was exceeded, output timing is same as Rn(7:0). A LOW indicates correct reception of the 256-bye incrementing pattern in BIST mode.

Pin	Name	I/O	Type	Pin Description
1R, 2R 1M, 2M 1J, 2J 1F, 2F	PTXA+/- PTXB+/- PTXC+/- PTXD+/-	O	PECL	**P**rimary Differential **TX** Outputs for Channel **n**. These pins output serialized transmit data when PTXENn is HIGH. AC coupling is recommended.
1T, 2T 1N, 2N 1H, 2H 1E, 2E	RTXA+/- RTXB+/- RTXC+/- RTXD+/-	O	PECL	**R**edundant Differential **TX** Outputs for Channel **n**. These pins output serialized transmit data when RTXENn is HIGH. AC coupling is recommended.
4N 4M 4J 4H	PTXENA PTXENB PTXENC PTXEND	I	TTL	**P**rimary **TX** Output **EN**able for Channel **n**. PTXn+/- is active when HIGH; when LOW, PTXn+/- is powered down and the outputs are undriven.
3P 3N 3H 3G	RTXENA RTXENB RTXENC RTXEND	I	TTL	**R**edundant **TX** Output **EN**able for Channel **n**. RTXn+/- is active when HIGH; when LOW, RTXn+/- is powered down and the outputs are undriven.
18P, 19R 20U, 20V 17R, 19U 20W, 18T	RA(7:0)	O	TTL	**R**eceive Data for Channel A. Synchronous to RCLKA/RCLKNA or REFCLK as selected by RMODE(1:0).
15V, 15U 18Y, 17Y 15W, 14U 16Y, 13V	RB(7:0)	O	TTL	**R**eceive Data for Channel B. Synchronous to RCLKB/RCLKNB or REFCLK as selected by RMODE(1:0).
16C, 15C 15D, 18A 17A, 15B 14D, 16A	RC(7:0)	O	TTL	**R**eceive Data for Channel C. Synchronous to RCLKC/RCLKNC or REFCLK as selected by RMODE(1:0).
20E, 18G 17G, 19F 20C, 17F 19D, 20B	RD(7:0)	O	TTL	**R**eceive Data for Channel D. Synchronous to RCLKD/RCLKND or REFCLK as selected by RMODE(1:0).
17N 18W 17C 19H	IDLEA IDLEB IDLEC IDLED	O	TTL	**IDLE** Detect for Channel **n**. When HIGH, an IDLE character has been detected by the decoder and is on Rn(7:0). When ENDEC=LOW, this is equivalent to **COMDETn**.
19P 16V 16D 18H	KCHA KCHB KCHC KCHD	O	TTL	**K**xx.x **CH**aracter Detect for Channel **n**. When HIGH, a special Kxx.x character has been detected by the decoder and is on Rn(7:0). When ENDEC=LOW, this is equivalent to data bit **Rn8**.

Pin	Name	I/O	Type	Pin Description
18N 16U 20A 20F	ERRA ERRB ERRC ERRD	O	TTL	**ERR**or Detect for Channel **n**. When HIGH, an invalid 10-bit character or disparity error has been detected and the data on Rn(7:0) is invalid. When ENDEC=LOW, this is equivalent to data bit **Rn9**.
20M 19M 17T 20Y 18E 17E 17K 18K	RCLKA RCLKNA RCLKB RCLKNB RCLKC RCLKNC RCLKD RCLKND	O	TTL	**R**ecovered **CL**oc**K** Outputs for Channel **n**. These outputs are driven from either the channel A or channel n recovered clock, at 1/10 or 1/20 the baud rate, as selected by RMODE(1:0) and DUAL. When unused, RCLKn is LOW and RCLKNn is HIGH.
6U 4W	RMODE0 RMODE1	I	TTL	**R**eceive Output Data Timing **MODE**. Determines the timing reference for all receive channels' Rn(7:0), IDLEn, KCHn and ERRn output data, and also for the PSDETn, RSDETn and TBERRn outputs, as defined in Table 5.
1U, 2U 1Y, 2Y 1A, 2A 1D, 2D	PRXA+/- PRXB+/- PRXC+/- PRXD+/-	I	PECL	**P**rimary Differential Serial **RX** Inputs for Channel **n**. These pins receive the serialized input data when LBENn(1) is LOW and RXP/Rn is HIGH; otherwise they are unused. They are internally biased at V_{DD}/2 through a 3.2kΩ resistor to the bias voltage. AC-coupling is recommended.
1W, 2W 3Y, 4Y 3A, 4A 1B, 2B	RRXA+/- RRXB+/- RRXC+/- RRXD+/-	I	PECL	**R**edundant Differential Serial **RX** Inputs for Channel **n**. These pins receive the serialized input data when LBENn(1) is LOW and RXP/Rn is LOW, otherwise they are unused. They are internally biased at V_{DD}/2 through a 3.2kΩ resistor to the bias voltage. AC-coupling is recommended.
4P 3T 4R 3U 4F 3D 4G 3E	LBENA0 LBENA1 LBENB0 LBENB1 LBENC0 LBENC1 LBEND0 LBEND1	I	TTL	**L**oop**B**ack **EN**able for Channel **n**. These inputs control the channel serial or parallel loopback configuration as described in Table 8.
2V 3W 3B 2C	RXP/RA RXP/RB RXP/RC RXP/RD	I	TTL	**RX** Input **P**rimary/**R**edundant Serial Input Select for Channel **n**. When LBENn(1) is LOW, this input selects PRXn+/- as the RX serial input source when HIGH and RRXn+/- as the serial input source when LOW.
20P 19V 18D 17J	PSDETA PSDETB PSDETC PSDETD	O	TTL	**P**rimary Analog **S**ignal **DET**ect, Channel **n**. This output goes HIGH when the amplitude on PRXn is greater than 200mV and goes LOW when the input is less than 100mV. PSDETn is not defined when the input is between 100mV and 200mV. Output timing is same as Rn(7:0).
17M 18U 19C 20J	RSDETA RSDETB RSDETC RSDETD	O	TTL	**R**edundant Analog **S**ignal **DET**ect, Channel **n**. This output goes HIGH when the amplitude on RRXn is greater than 200 mV and goes LOW when the input is less than 100mV. RSDETn is not defined when the input is between 100mV and 200mV. Output timing is same as Rn(7:0).

Pin	Name	I/O	Type	Pin Description
8A 9D	REFCLKP REFCLKN	I	PECL	**REFCLK** Differential **P**ositive and **N**egative PECL or Single-ended TTL Inputs. This rising edge of this clock latches transmit data and control into the input register. It also provides the reference clock, at 1/10th or 1/20th of the baud rate to the PLL as selected by DUAL. If TTL, connect to REFCLKP but leave REFCLKN open. If PECL, connect both REFCLKP and REFCLKN.
1K 1L	CAP0 CAP1		Analog	Loop Filter **CAP**acitor for Clock Generation PLL. Nominally 0.1 μF, amplitude is less than 3V. Refer to the Loop Filter Applications section for further details.
5U	DUAL	I	TTL	**DUAL** Clock Mode. When LOW, REFCLK and RCLKn/RCLKNn are 1/10th the baud rate. When HIGH, they are 1/20th the baud rate.
13W	FLOCK	I	TTL	**F**requency **LOCK**ed Mode. When HIGH, indicates that each transmit channel's REFCLK is frequency-locked to the receive channel's word clock. Controls rate matching (IDLE delete/duplicate) logic along with the WSI input as per Table 6.
12D	BIST	I	TTL	**B**uilt-**I**n **S**elf-**T**est Mode. When HIGH, all transmit channels continuously send a 256 byte incrementing data pattern, and all receive channels signal correct reception of the test pattern with a LOW on the TBERRn outputs.
12V	ENDEC	I	TTL	**EN**coder/**DEC**oder Enable. When HIGH, the VSC7217 is configured for 8 bit operation and internal 8B/10B encoding is enabled. When LOW, a 10-bit interface is used and internal 8B/10B encoding is bypassed.
12U	RESETN	I	TTL	**RESETN** Input. When asserted LOW, the transmitter input skew buffers and receiver elastic buffers are recentered.
20L	WSI	I	TTL	**W**ord **S**ync **I**nput. Used to control channel alignment and IDLE character insertion/deletion as defined in Table 6.
17L	WSO	O	TTL	**W**ord **S**ync **O**utput. Used to set initial channel word alignment, and to maintain alignment by controlling IDLE character insertion/deletion.
15A	TCK	I	TTL	JTAG Test Access Port test clock input.
13B	TMS	I	TTL	JTAG Test Access Port test mode select input.
14A	TDI	I	TTL	JTAG Test Access Port test data input.
19K	TDO	O	TTL	JTAG Test Access Port test data output.
13A	TRSTN	I	TTL	JTAG Test Access Port test logic reset input.
14Y	RSVD	I	N/A	Reserved Inputs for Future Use. Set HIGH for compatibility reasons.
13Y	RSVD	I	N/A	Reserved Inputs for Future Use. Set HIGH for compatibility reasons.
2L, 4L	VDDA		VDD	Analog Power Supply to PLL.
2K, 4K	VSSA		GND	Analog Ground to PLL.
11B, 11Y, 13D, 15Y, 1C, 1V, 20K, 3L, 4D, 4U, 5C, 5V, 8V	VDDD		VDD	Digital Power Supply.

G52325-0, Rev. 3.0
6/14/00

Pin	Name	I/O	Type	Pin Description
11A, 13C, 13U, 19L, 3C, 3K, 3V, 4C, 4E, 4T, 4V, 6V, 7A, 7C, 8W	VSSD		GND	Digital Ground.
14B, 14W, 17B, 17D, 17H, 17P, 17U, 17W, 18L, 19B, 19E, 19G, 19J, 19N, 19T, 19W	VDDT		VDD	TTL Output Power Supply.
14C, 14V, 16B, 16W, 18C, 18F, 18J, 18M, 18R, 18V, 19A, 19Y, 20D, 20G, 20N, 20T	VSST		GND	TTL Output Ground.
2P 3R 3M 1P 3J 1G 2G 3F	VDDPA VDDRA VDDPB VDDRB VDDPC VDDRC VDDPD VDDRD		VDD	PECL Output Power Supply for PTXA. PECL Output Power Supply for RTXA. PECL Output Power Supply for PTXB. PECL Output Power Supply for RTXB. PECL Output Power Supply for PTXC. PECL Output Power Supply for RTXC. PECL Output Power Supply for PTXD. PECL Output Power Supply for RTXD. If use of an output is not necessary, leave the power supply pin open.

Package Thermal Considerations

The VSC7217 is packaged in a 256-pin, 27mm, thermally enhanced BGA in a 20x20 array which offers excellent electrical characteristics, good thermal performance and small size. This package uses an industry-standard footprint. The package construction is shown in Figure 22.
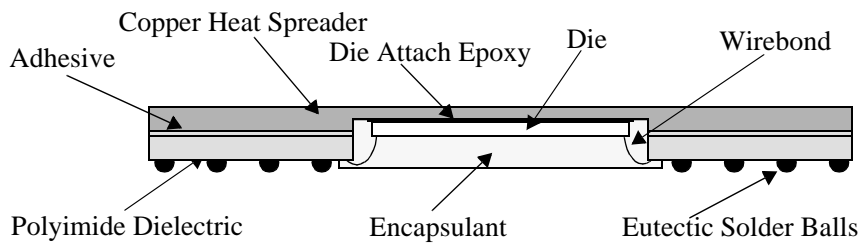
Figure 22: Package Cross Section

Table 18: Thermal Resistance

Symbol	Description	Value	Units
θ_{ca}	Thermal resistance from case-to-ambient in still air including conduction through the leads.	15	^{o}C/W
θ_{ca-100}	Thermal resistance from case-to-ambient with 100 LFM airflow	13	^{o}C/W
θ_{ca-200}	Thermal resistance from case-to-ambient with200 LFM airflow	12	^{o}C/W
θ_{ca-400}	Thermal resistance from case-to-ambient with 400 LFM airflow	10.5	^{o}C/W
θ_{ca-600}	Thermal resistance from case-to-ambient with 600 LFM airflow	10	^{o}C/W

The VSC7217 is designed to operate with a case temperature up to 95°C. The user must guarantee that this case temperature specification is not violated. With the Thermal Resistances listed in Table 18, the VSC7217 can operate in still air ambient temperatures of 50°C [50°C = 95°C - (3.0W * 15°C/W)]. If the ambient air temperature exceeds these limits, some form of cooling through a heat sink or an increase in airflow must be provided.
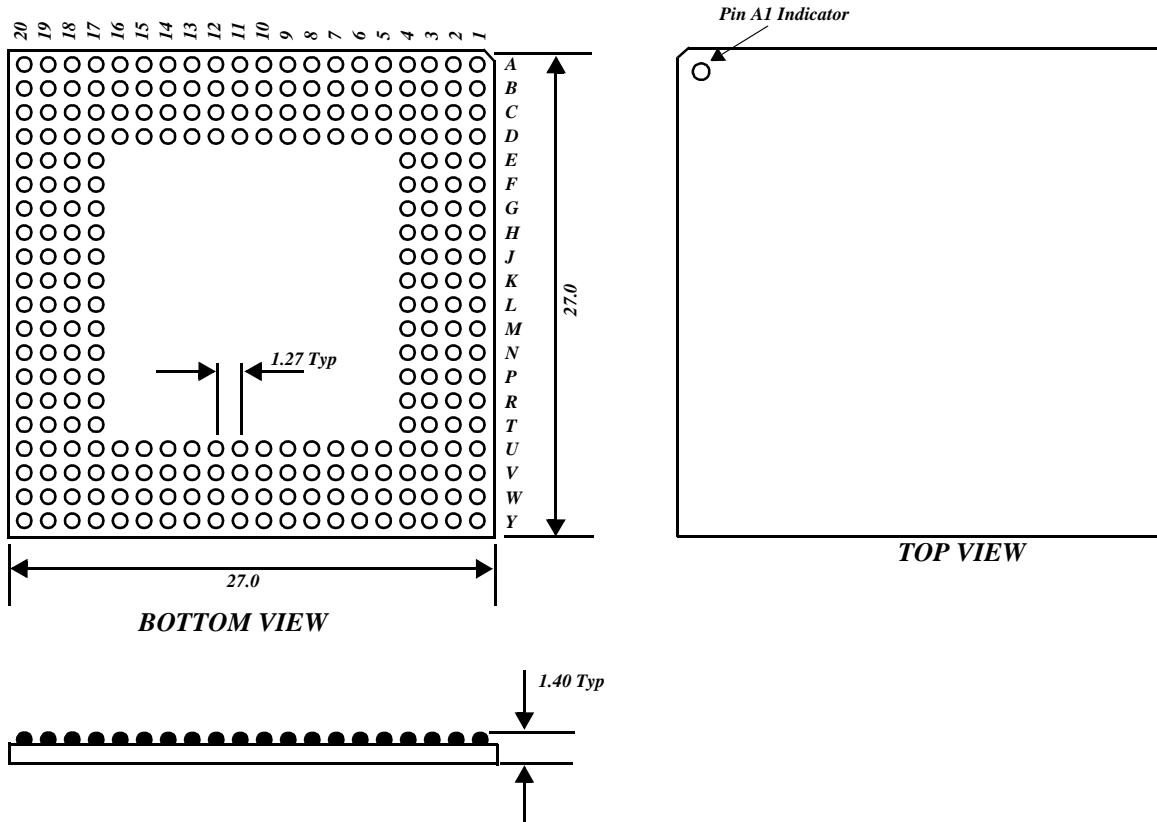
Moisture Sensitivity Level

This device is rated at with a Moisture Sensitivity Level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

Package Information

256-pin BGA

BOTTOM VIEW
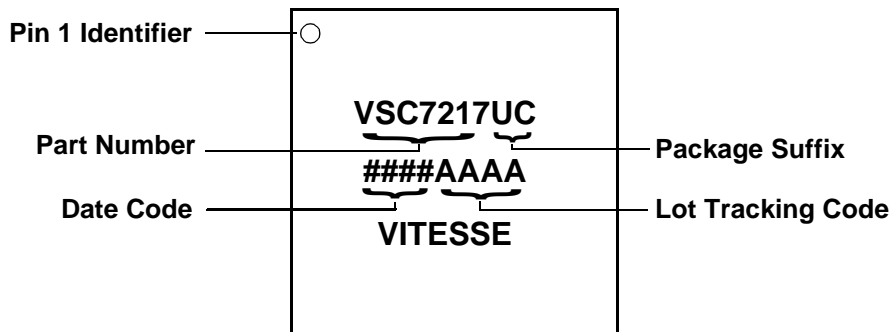
TOP VIEW

Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC7217 **xx**

Device Type
Multi-Gigabit Interconnect Chip

Package
UC: 256-Pin, 27mm BGA
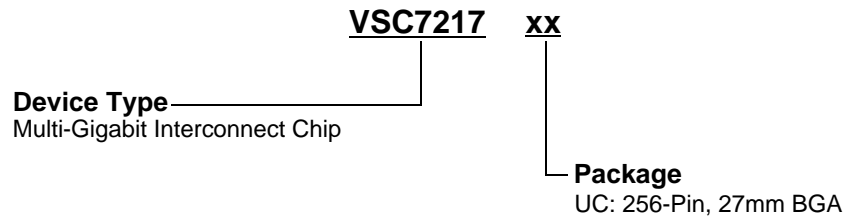
Marking Information

The package is marked with three lines of text as shown:

Pin 1 Identifier

Part Number

Date Code

VSC7217UC

####AAAA

VITESSE

Package Suffix

Lot Tracking Code

Notice

This document contains information about a new product during its fabrication or sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this data sheet is current prior to design or order placement.

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