RM3182

ARINC 429 Differential Line Driver

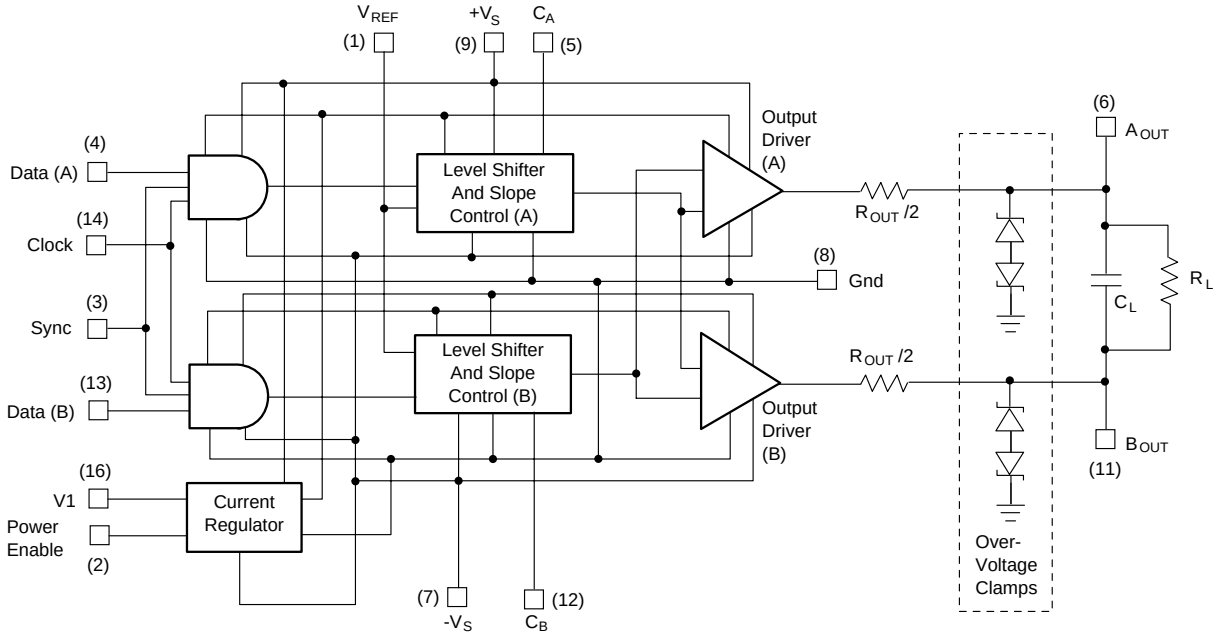
Features

- Adjustable rise and fall times
- Adjustable output voltage swing
- Short circuit protected
- Output overvoltage protected
- Sync and clock enable inputs
- TTL and CMOS compatible inputs
- MIL-STD-883B types available
- 100 Kbits/second data rate

Description

The RM3182 consists of a bus interface line driver circuit plus auxiliary gating and synchronization circuitry. Designed to address the ARINC 429 standard, the RM3182 has output rise and fall times adjustable by the selection of two external capacitor values, and the output voltage swing range can be adjusted through an externally applied V_{REF} signal.
The logic inputs as well as the sync control inputs are TTL-CMOS compatible. The device is constructed on a monolithic IC using a junction-isolated bipolar process. Sputtered SiCr resistors are used in the internal bias circuitry, providing stable internal bias currents. The RM3182 is available in 16-lead ceramic DIP and 28-pad LCC, and can be ordered with MIL-STD883B high reliability screening.

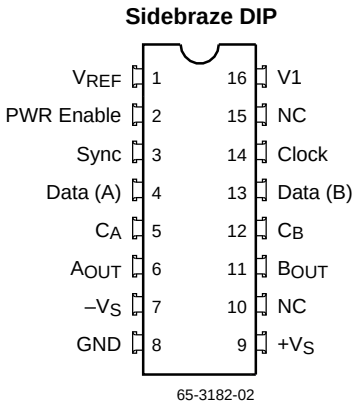
Block Diagram

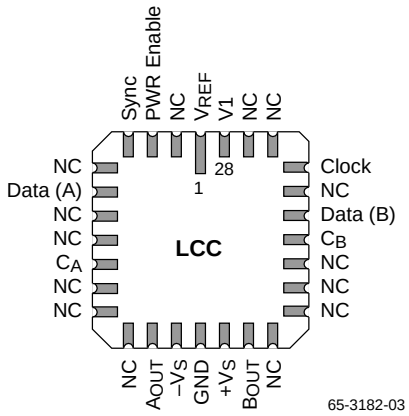


Notes:
1. R_L and C_L are external. Full load values are: $R_L = 400\Omega$, $C_L = 0.03\mu F$.
2. Pin numbers are for 16-lead DIP.

65-3182-01

Pin Assignments





Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply Voltage (+V_S to –V_S)		36	V
V1 Voltage		+7	V
V_{REF} Voltage		+6	V
Logic Input Voltage	-0.3	+V_S + 0.3	V
Output Short Circuit Duration	See Note 1		
Output Overvoltage	–6.5	+6.5	V
Storage Temperature Range	-65	+150	°C
Operating Temperature Range (see Note 2)	-55	+125	°C
Lead Soldering Temperature (60 sec.)		+300	°C

Notes:

1. Heatsinking may he required for output short circuit at +125°C.
2. Heatsinking may be required depending on load and signal frequencies

Thermal Characteristics

(Still air, soldered into PC board)

	Sidebrazed DIP	LCC
Maximum Junction Temperature	+175°C	+175°C
Max. P_D T_A < 50°C	1470 mW	1040 mW
Thermal Resistance θ_{JC}	25°C/W	25°C/W
Thermal Resistance θ_{JA}	85°C/W	120°C/W
For T_A > 50°C Derate at	11.7 mW/°C	8.3 mW/°C

Electrical Characteristics

(V_S = ±15V, V_{REF} = V1 = +5V, PWR Enable = 0V, R_L = open circuit, -55°C ≤ T_A ≤ +125°C)

Parameters	Test Conditlons	Min.	Typ.	Max.	Units
Positive Supply Current	Data Rate = 0 to 100 Kbits/sec		11	16	mA
Negative Supply Current	Data Rate = 0 to 100 Kbits/sec	-16	-10		mA
V1 Supply Current	Data Rate = 0 to 100 Kbits/sec		200	975	µA
V_{REF} Supply Current	Data Rate = 0 to 100 Kbits/sec	-1.0	-0.4	-0.15	mA
Input Logic Level High		2.0			V
Input Logic Level Low				0.5	V
Output Voltage High	With Respect to Ground	4.75	5.0	5.25	V
Output Voltage Low	With Respect to Ground	-5.25	-5.0	-4.75	V
Output Voltage Null	Both Data Input = Logic 0	-250	0	+250	mV
Input Current High	V_{IN} = 2.0V		1	10	µA
Input Current Low	V_{IN} = 0.5V	-20	-1		µA
Output Short Circuit Current	Output in High State, to Gnd		-133	-80	mA
Output Short Circuit Current	Output in Low State, to Gnd	80	133		mA
Positive Supply Current	Output High and Shorted to Gnd			150	mA
Negative Supply Current	Output Low and Shorted to Gnd	-150			mA
Input Capacitance[1]			5	15	pF

Note:

1. Guaranteed by design.

Typical Power Dissipation Characteristics

(V_S = ±15V, V1 = V_{REF} = +5V, Pwr Enable = 0V, T_A = + 25°C)

Data Rate (Kbits/sec)	Load	Positive Supply Current	Negative Supply Current	Pin V1 Supply Current	Internal Power Dissipatlon	Load Power Dissipatlon
0 to 100	Open Circuit	11 mA	-10 mA	200 µA	325 mW	0
12.5 to 14	Full Load[1]	24 mA	-24 mA	200 µA	660 mW	60 mW
100	Full Load[1]	46 mA	-46 mA	200 µA	1000 mW	325 mW

Note:

1. R_L = 400Ω, C_L = 0.03 µF (see Block Diagram).

Principles of Operation

Each device consists of one differential driver and associated gating circuitry. The gating circuitry consists of clock and sync signal inputs which are ANDed with the two data inputs. See the block diagram and truth table. Three power supplies are required to operate the RM3182 in a typical ARINC 429 bus application: +15V, -15V, and +5V. The +5V supply, in addition to powering the internal bus current regulator, provides a reference voltage that determines the output voltage swing. The differential output swing will equal 2 V_{REF}. If a value of V_{REF} other than +5V is used, then a separate +5V supply is required for pin V1.

Figure 1 depicts connections for the ARINC 429 application. The driver output impedance is nominally 75Ω. With the Data(A) input at a logic high and Data (B) input at a logic low, A_{OUT} will swing to +V_{REF} and B_{OUT} will swing to V_{REF} (constituting a logic high state). Reversing the data input states will cause A_{OUT} to swing to -V_{REF} and B_{OUT} to +V_{REF}. With both data input signals at a logic low state, the outputs will both swing to 0V (output in null state).

The slew rate of the outputs, and consequently rise and fall times, can be adjusted through the selection of two external capacitor values. Typical values are $C_A = C_B = 75$ pF for high-speed operation (100 Kbits/sec) and $C_A = C_B = 500$ pF for low-speed operation (12.5 to 14 Kbits/sec).

The device can be powered down by applying a logic high signal to the Power Enable pin. If the power down feature is not used, then the Power Enable pin should be tied directly to ground.

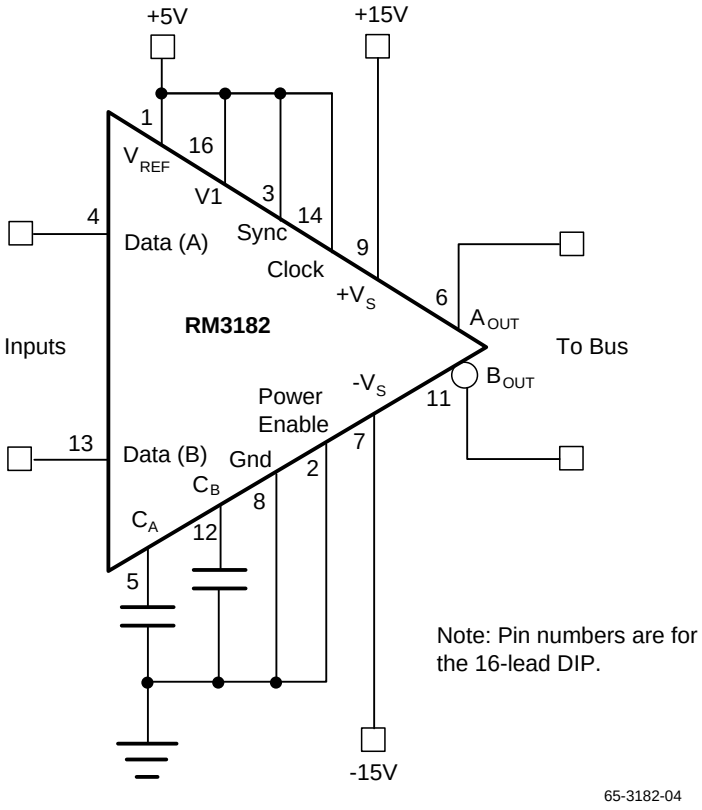


Figure 1. ARINC 429 Bus Application

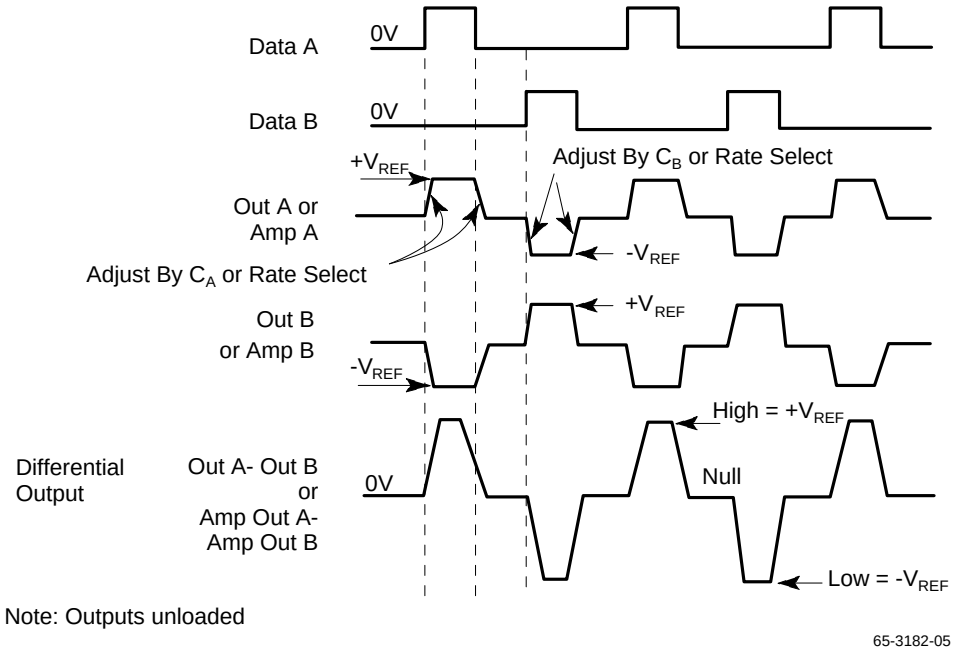


Figure 1. Switching Waveforms

Truth Table

Sync	Clock	Data (A)	Data (B)	AOUT	BOUT	Comments
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	-VREF	+VREF	Low
H	H	H	L	+VREF	-VREF	High
H	H	H	H	0V	0V	Null

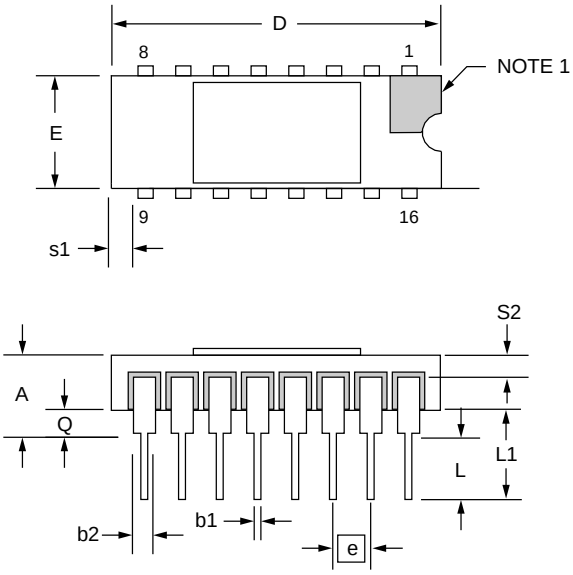
Mechanical Dimensions

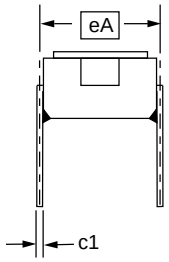
16-Lead Sidebraze DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	7
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	7
D	—	.860	—	21.84	
E	.280	.310	7.11	7.87	
e	.100 BSC		2.54 BSC		4, 8
eA	.300 BSC		7.62 BSC		6
L	.125	.200	3.18	5.08	
L1	.140	—	3.56	—	
Q	.015	.070	.38	1.78	3
s1	.005	—	.13	—	5
s2	.005	—	.13	—	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 16.
5. Applies to all four corners (leads number 1, 8, 9, and 16).
6. "eA" shall be measured at the centerline of the leads.
7. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
8. Fourteen spaces.





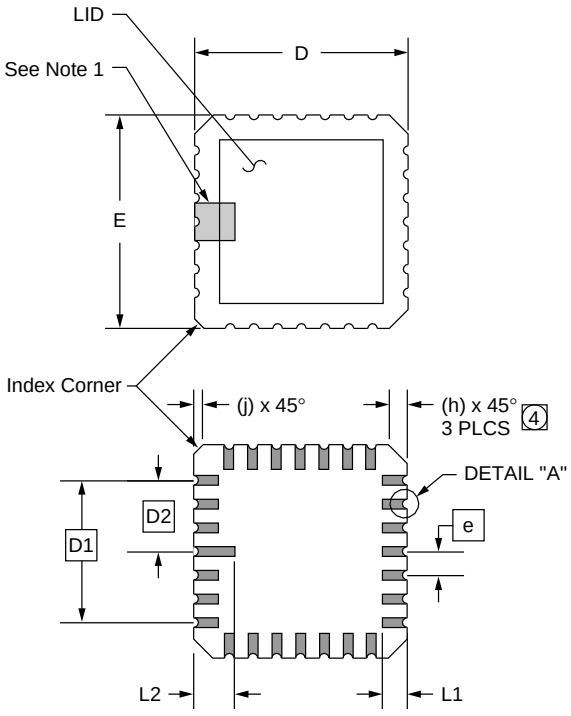
Mechanical Dimensions (continued)

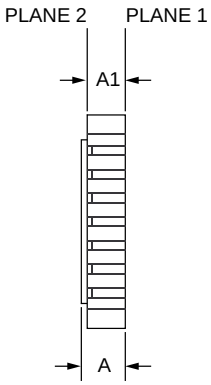
28 Terminal Leadless Chip Carrier (LCC)

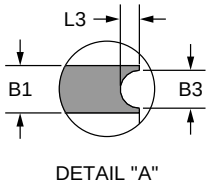
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.060	.100	1.52	2.54	3, 6
A1	.050	.088	1.27	2.24	3, 6
B1	.022	.028	.56	.71	2
B3	.006	.022	.15	.56	2, 5
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
e	.050 BSC		1.27 BSC		
h	.040 REF		1.02 REF		4
j	.020 REF		.51 REF		4
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.91	2.41	
L3	.003	.015	.08	.38	5
ND/NE	7		7		
N	28		28		

Notes:

1. The index feature for terminal 1 identification, optical orientation or handling purposes, shall be within the shaded index areas shown on planes 1 and 2. Plane 1 terminal 1 identification may be an extension of the length of the metallized terminal which shall not be wider than the B1 dimension.
2. Unless otherwise specified, a minimum clearance of .015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.).
3. Dimension "A" controls the overall package thickness. The maximum "A" dimension is the package height before being solder dipped.
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing. The index corner shall be clearly unique.
5. Dimension "B3" minimum and "L3" minimum and the appropriately derived castellation length define an unobstructed three dimensional space traversing all of the ceramic layers in which a castellation was designed. Dimension "B3" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dripping.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.







Ordering Information

Part Number	Package	Operating Temperature Range
RM3182S	S	-55°C to +125°C
RM8182S/883B	S	-55°C to +125°C
RM3182L	L	-55°C to +125°C
RM3182L/883B	L	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S = 16 Lead sidebraze ceramic DIP
L = 28 Terminal Leadless Chip Carrier

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