FAIRCHILD SEMICONDUCTOR®

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FDD8447L
40V N-Channel PowerTrench® MOSFET
40V, 54A, 8.5mΩ

Features

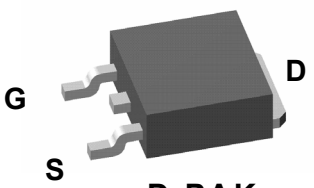
- Max $r_{DS(on)}$ = 8.5mΩ at V_{GS} = 10V, I_D = 14A
- Max $r_{DS(on)}$ = 11mΩ at V_{GS} = 4.5V, I_D = 11A
- Fast Switching
- RoHS Compliant

General Description

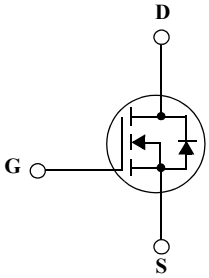
This N-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench® technology to deliver low $r_{DS(on)}$ and optimized BV_{DSS} capability to offer superior performance benefit in the application.

Application

- Inverter
- Power Supplies



D-PAK
(TO-252)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		40	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Continuous Drain Current @ T_C = 25°C	(Note 3)	54	A
	@ T_A = 25°C	(Note 1a)	21	
	Pulsed	(Note 1a)	100	
E_{AS}	Drain-Source Avalanche Energy	(Note 3)	153	mJ
P_D	Power Dissipation @ T_C = 25°C	(Note 3)	45	W
	@ T_A = 25°C	(Note 1a)	3.8	
	@ T_A = 25°C	(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	96	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8447L	FDD8447L	D-PAK(TO-252)	13"	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		35		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{GS} = 0V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 14A		7	8.5	mΩ
		V_{GS} = 4.5V, I_D = 11A		8.5	11	
		V_{GS} = 10V, I_D = 14A, T_J=125°C		10.4	14	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 14A		58		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		1970		pF
C_{oss}	Output Capacitance			250		pF
C_{rss}	Reverse Transfer Capacitance			150		pF
R_g	Gate Resistance	f = 1MHz		1.27		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω		12	21	ns
t_r	Rise Time			12	21	ns
$t_{d(off)}$	Turn-Off Delay Time			38	61	ns
t_f	Fall Time			9	18	ns
$Q_{g(TOT)}$	Total Gate Charge, V_{GS} = 10V	V_{DD} =20V, I_D = 14A, V_{GS} = 10V		37	52	nC
$Q_{g(TOT)}$	Total Gate Charge, V_{GS} = 5V			20	28	
Q_{gs}	Gate to Source Gate Charge			6		nC
Q_{gd}	Gate to Drain “Miller” Charge			7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 14A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 14A, di/dt = 100A/μs		22		ns
Q_{rr}	Reverse Recovery Charge			11		nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a. 40°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 96°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3: Maximun current is calculated as: $\sqrt{\frac{P_D}{r_{DS(on)}}}$

where P_D is maximum power dissipation at T_C = 25°C and $r_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10V. Package current limitation is 21A.

4: Starting T_J = 25°C, L = 1mH, I_{AS} = 17.5A, V_{DD} = 40V, V_{GS} = 10V.

Typical Characteristics

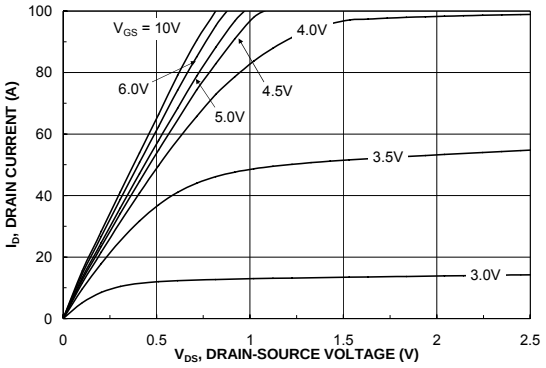


Figure 1. On-Region Characteristics

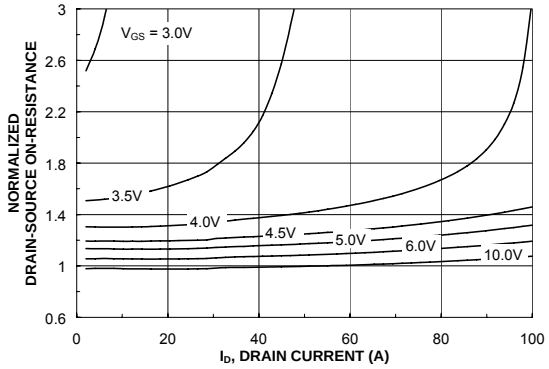


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

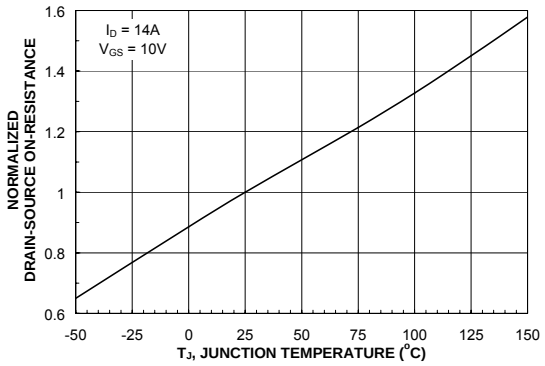


Figure 3. On-Resistance Variation with Temperature

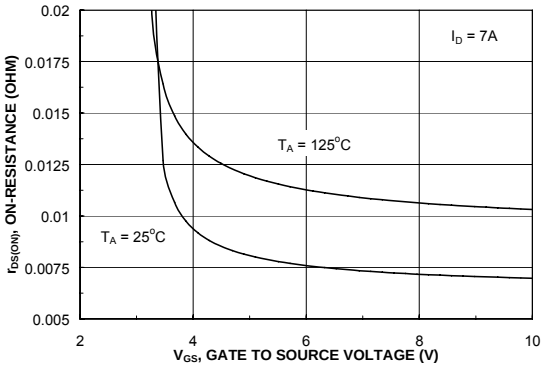


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

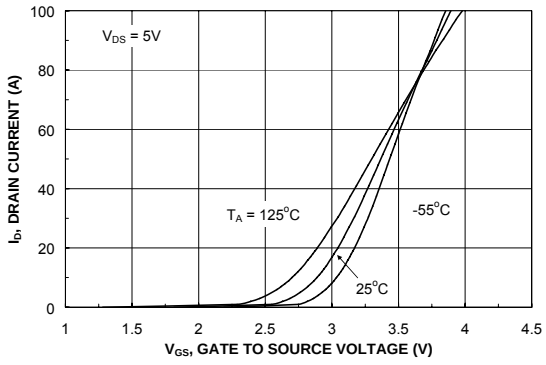


Figure 5. Transfer Characteristics

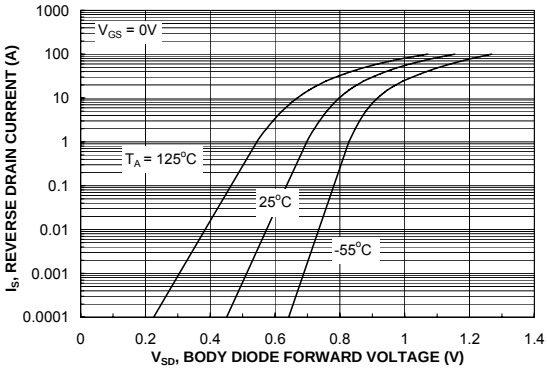


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

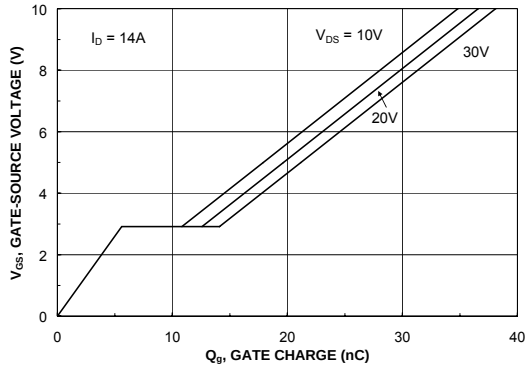


Figure 7. Gate Charge Characteristics

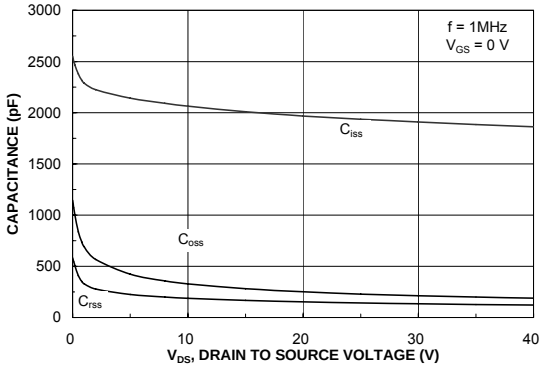


Figure 8. Capacitance Characteristics

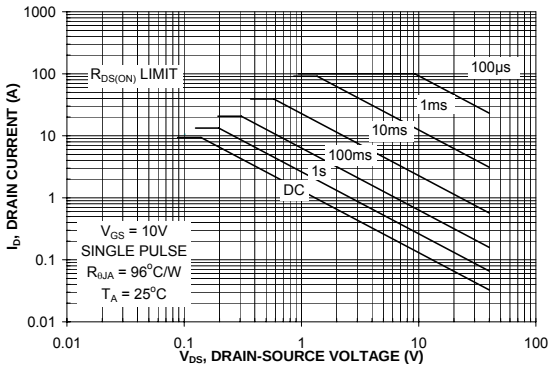


Figure 9. Maximum Safe Operating Area

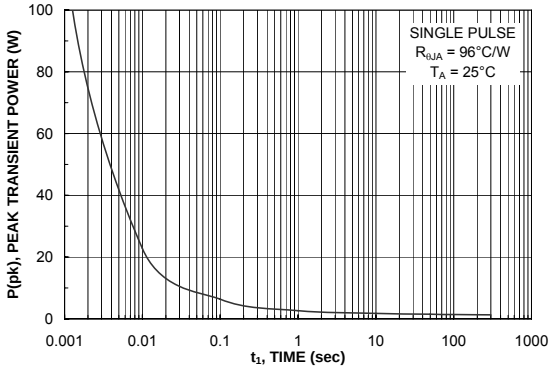


Figure 10. Single Pulse Maximum Power Dissipation

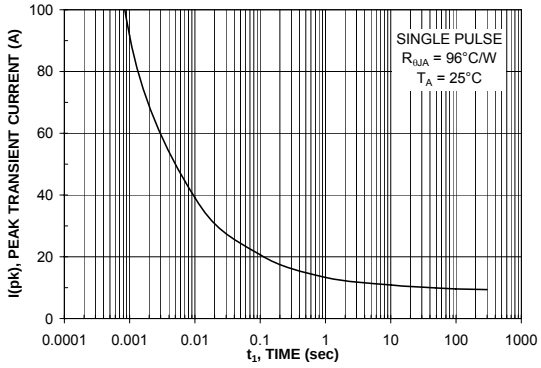


Figure 11. Single Pulse Maximum Peak Current

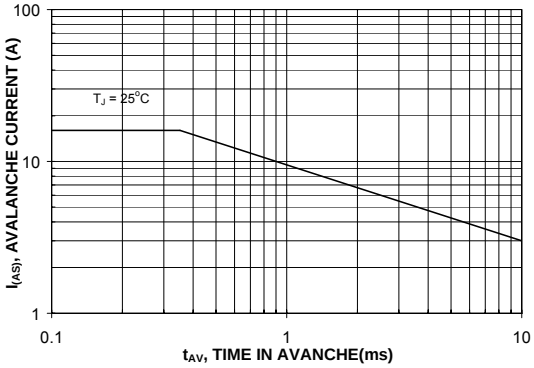


Figure 12. Unclamped Inductive Switching Capability

Typical Characteristics

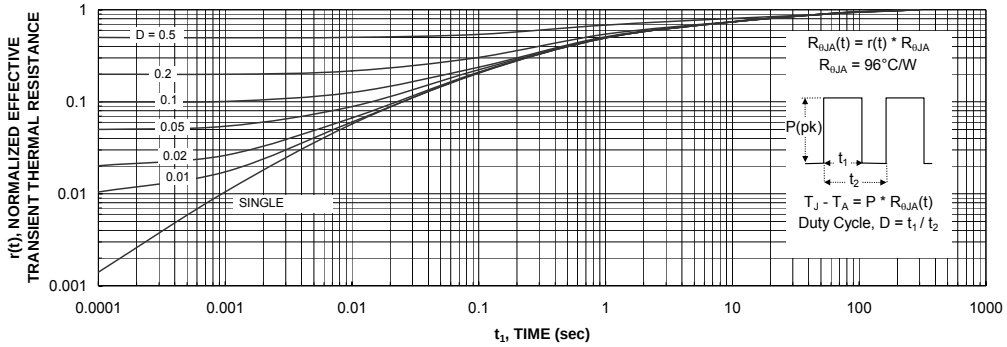


Figure 13. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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FAST®	MicroFET™	QS™	TinyBuck™	
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