STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	1ch Series Regulator Driver IC
PRODUCT SERIES	**BD3508EKN**
FEATURES	・High Accuracy Voltage Regulator(0.65±1%)
	・Non Rush Current on Start up (NRCS)
	・Built in Super low ON resistance (65mΩtyp) Nch PowerMOSFET

○ ABSOLUTE MAXIMUM RATINGS (Ta=100℃)

Parameter	Symbol	Limit	Unit
Supply Voltage 1	VCC	6.0 *1	V
Supply Voltage 2	VIN	6.0 *1	V
Enable Input Voltage	Ven	6.0	V
Power dissipation 1	Pd1	0.5 *2	W
Power dissipation 2	Pd2	0.75 *3	W
Power dissipation 3	Pd3	1.75 *4	W
Power dissipation 4	Pd4	2.0 *5	W
Operating temperature range	Topr	-10～+100	℃
Storage temperature range	Tstg	-55～+125	℃
Junction Temperature	Tjmax	+150	℃

*1 Should not exceed Pd.。

*2 Reduced by 4mW for each increase in Ta of 1℃ over 25℃ (With no heat sink) .

*3 Ta≧25℃ (when mounted on 70mm x 70mm x 1.6mm Glass-epoxy PCB which does not have copper on the back side) .

*4 Ta≧25℃ (when mounted on 70mm x 70mm x 1.6mm Glass-epoxy PCB which has 1 layer (60mm x 60mm) of copper on the back side) 14mW/℃ increase.

*5 Ta≧25℃ (When mounted on board 70mm x 70mm x 1.6mm Glass-epoxy PCB which has 2 layers (60mm x 60mm) of copper on the back side) 16mW/℃ increase.

○ RECOMMENDED OPERATING CONDITIONS(Ta=25℃)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage1	VCC	4.3	5.5	V
Supply Voltage2	VIN	1.2	VCC-1 *6	V
Output Voltage	Vo	VFB	2.5	V
Enable Input Voltage	Ven	-0.3	5.5	V
Capacitor in NRCS pin	CNRCS	0.001	1	uF

*6 Order of VCC and VIN does not matter

★ This product should not be used within a radioactive environment

Status of this document

The Japanese version of this document is the official specification.

This translated version is intended only as a reference, to aid in understanding the official version.

If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

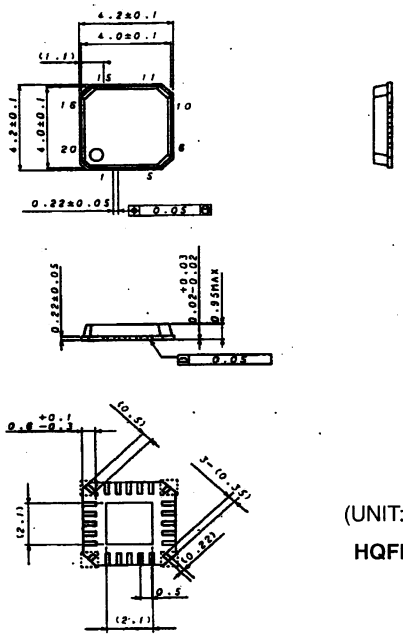
○ ELECTRICAL CHARACTERISTICS

(Unless otherwise specified,Ta=25℃ VCC=5V Ven=3V VIN=1.8V R1=3.9kΩ R2=3.3kΩ)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
Bias current	ICC	-	0.7	1.4	mA	
Shut-Down Mode Current	IST	-	0	10	uA	Ven=0V
Output Voltage	VOUT	-	1.200	-	V	
Maximum Output Current	Io	3.0	-	-	A	
Maximum Short Current	Iost	-	-	4.0	A	Vo=0V
Temperature coefficient of Output Voltage	Tcvo	-	0.01	-	%/℃	
Feed Back Voltage 1	VFB1	0.643	0.650	0.657	V	
Feed Back Voltage 2	VFB2	0.630	0.650	0.670	V	Io=0 to 3A Ta=-10 to 100℃ *7
Line Regulation 1	Reg.I1	-	0.1	0.5	%/V	VCC=4.3V to 5.5V
Line Regulation 2	Reg.I2	-	0.1	0.5	%/V	VIN=1.2V to 3.3V
Load Regulation	Reg.L	-	0.5	10	mV	Io=0 to 3A
Dropout Voltage	dVo	-	65	100	mV	Io=1A,VIN=1.2V Ta=-10 to 100℃ *7
Standby Discharge Current	Iden	1	-	-	mA	Ven=0V, Vo=1V
[Enable]						
High level Enable Input Voltage	Enhi	2	-	-	V	
Low level Enable Input Voltage	Enlow	-0.2	-	0.8	V	
Enable pin Input Current	Ien	-	7	10	uA	Ven=3V
[Voltage Feed Back]						
Feed Back terminal Bias Current	IFB	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	Inrcs	14	20	26	uA	Vnrcs=0.5V
NRCS Standby Voltage	VSTB	-	0	50	mV	Ven=0V
[UVLO]						
VCC UVLO	VccUVLO	3.5	3.8	4.1	V	Vcc:Sweep-up
VCC UVLO Hysterisis	Vcchys	100	160	220	mV	Vcc:Sweep-down
[AMP]						
Gate Source Current	I_{GSO}	-	1.6	-	mA	V_{FB}=0, V_{GATE}=2.5V
Gate Sink Current	I_{GSI}	-	2.4	-	mA	V_{FB}=VCC, V_{GATE}=2.5V

*7 Design Guarantee

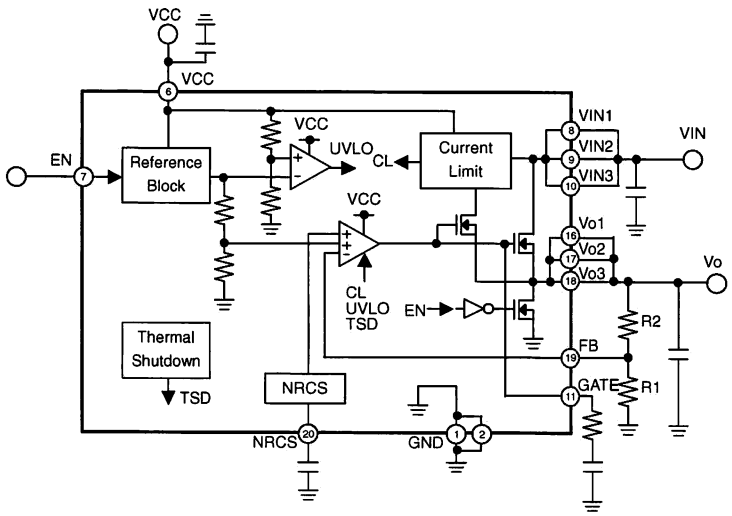
O PHYSICAL DIMENSIONS



(UNIT:mm)

HQFN20

O BLOCK DIAGRAM



O Pin number Pin name

PIN No.	Pin name
1	GND
2	GND
3	N.C
4	N.C
5	N.C
6	VCC
7	EN
8	VIN1
9	VIN2
10	VIN3
11	GATE
12	N.C
13	N.C
14	N.C
15	N.C
16	VO1
17	VO2
18	VO3
19	FB
20	NRCS
-	FIN

ONOTES FOR USE

(1) Absolute maximum range

Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.

(2) Ground potential

Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.

(3) Thermal Design

Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(4) Using in the strong electromagnetic field

Use in strong electromagnetic fields may cause malfunctions.

(5) ASO

Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.

(6) Thermal shutdown circuit

The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off (open) state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC per se or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
175	15

(7) GND pattern

When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(8) Output Voltage Setting (R1, R2)

Output volage is adjusted with resistor R1 and R2. output voltage is calculated as VFBx(R1+R2)/R1. Total 10kohm resistor (R1+R2) is recommended so that the output voltage is not affected by the VFB bias current (Typ. 100nA).

(9) Output Capacitor (C4)

Mount an output capacitor between Vo1 to Vo3 and GND for stability purposes. The output capacitor is for the open loop gain phase compensation and reduces the output voltage load regulation. If the capacitor value is not large enough, the output voltage may oscillate. And if the equivalent series resistance (ESR) is too large, the output voltage rise/drop increases during a sudden load change. A 150uF polymer capacitor is recommended. However, the stability depends on the characteristics of temperature and load. And if several kinds of capacitors are utilized in parallel, the output voltage may oscillate due to lack of phase margin. Please confirm operation across a variety of temperature and load conditions.

(10) Input Capacitor (C1, C2)

The input capacitor reduces the output impedence of the voltage supply source connected in the VCC and VIN. If the output impedence of this power supply increases, the input voltage (VCC,VIN) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. A low ESR 10uF capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

(11) NRCS (Non Rush Current on Start-up) Setting(C3)

The NRCS function is built in this IC to prevent rush current from going through the load (VIN to Vo) for start-up. The constant current comes from the NRCS pin when EN is high or UVLO function is deactivated. Temporary reference voltage is made proportional to time due to current charge the NRCS pin capacitor and make output voltage start up proportional to this reference volatge. To obtain a stable NRCS delay time, a capacitor (X5R or X7R) with susceptiblity to temperature is recommended.

(12) Input Terminal (VCC,VIN,EN)

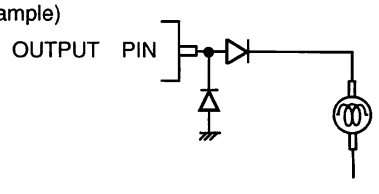
The EN, VIN, and VCC are isolatetd. The UVLO protects incorrect operation when the voltage level of VCC are low. The output becomes high when VCC and EN reach the individual threshold level independent of the start-up pin order.

(13) Heat sink (FIN)

Since the heat sink (FIN) is connected with the Sub, short it to the GND. It is possible to minimize the thermal resistance by soldering it to GND plane of PCB.

(14) Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.

(Example)



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