Winbond

W2416

2K X 8 CMOS STATIC RAM

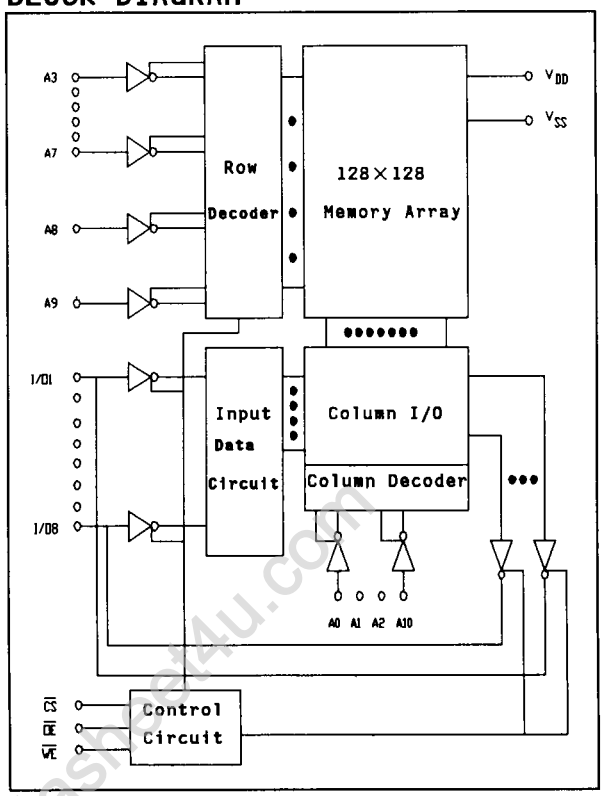
FEATURES

- Low Power Consumption :
  Active : 250mW (Typ.)
  Standby : 10 μW(Typ.)-- L-Version
- Fast Access Time : 70/100 ns (Max.)
- Single +5V Supply
- Fully Static Operation
- Direct TTL Compatible : All Inputs and Outputs
- Three State Outputs
- Capability of Battery Back Up Operation (L-Version)
- Data Retention Voltage : 2V (Min.) (L-Version)
- Available in 24 Pin DIP, SOP, or Skinny DIP Packages

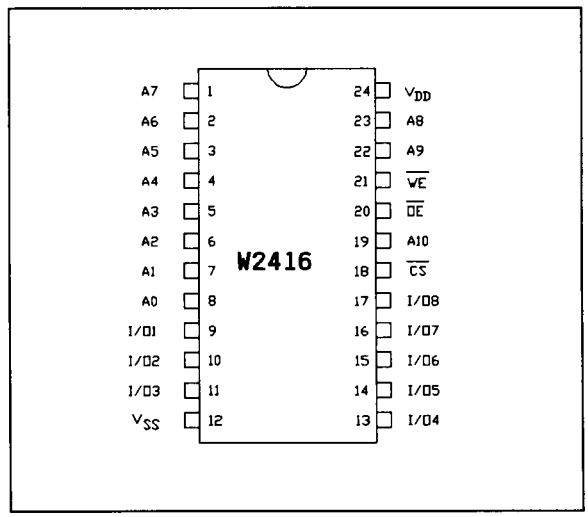
DESCRIPTION

The W2416 is a High Speed, Low Power CMOS Static RAM Organized as 2048×8 Bits and Operates on a Single 5-Volt Supply. It is Manufactured Using WINBOND's High Performance CMOS Technology.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A10	Address Inputs
I/O1-I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply
V_{SS}	Ground

OCTOBER • 1990

DC CHARACTERISTICS

ABSOLUTE MAXIMUN RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Inputs/Outputs to V_{SS} Potential	-0.5 to V_{DD}+0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-55 to +150	℃
Operating Temperature	0 to +70	℃

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 - I/O8	V_{DD} Current
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

OPERATING CHARACTERISTICS

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		- 0.5	-	+ 0.8	V
Input High Voltage	V_{IH}	-		+ 2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN}= V_{SS} to V_{DD}		- 2	-	+ 2	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD} $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		- 2	-	+ 2	μA
Output Low Voltage	V_{OL}	I_{OL} = +4.0mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL}, I/O = 0mA CYCLE = MIN, DUTY = 100%		-	-	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}		-	-	3	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{DD} -0.2V	L	-	2	100	μA
			S	-	-	1000	μA

Note : Typical characteristics are at V_{DD}=5V, Ta=25℃.

CAPACITANCE

(V_{DD}=5V, Ta=25℃, f=1MHz)

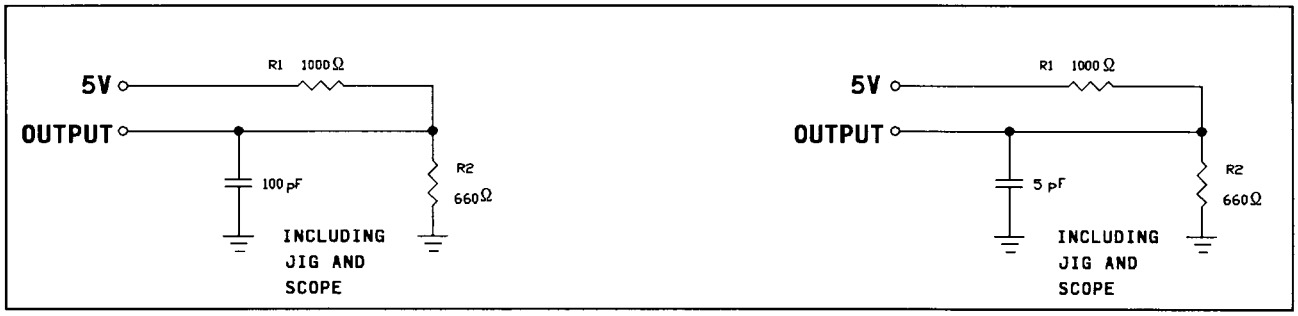
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT}=0V	8	pF

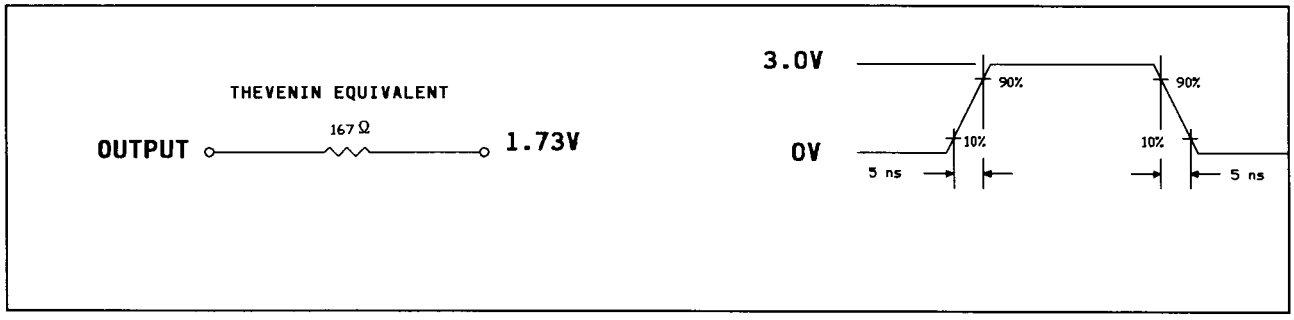
Note : This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100pF, I_{OH}/I_{OL}=-1mA/4mA

AC TEST LOADS AND WAVEFORMS





AC CHARACTERISTICS

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	W2416-70		W2416-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	100	-	ns
Address Access Time	T_{AA}	-	70	-	100	ns
Chip Select Access Time	T_{ACS}	-	70	-	100	ns
Output Enable to Output Valid	T_{AOE}	-	35	-	50	ns
Chip Selection to Output in Low Z	T_{CLZ}	5	-	5	-	ns
Output Enable to Output in Low Z	T_{OLZ}	5	-	5	-	ns
Chip Deselection to Output in High Z	T_{CHZ}	-	35	-	35	ns
Output Disable to Output in High Z	T_{OHZ}	-	30	-	35	ns
Output Hold from Address Change	T_{OH}	5	-	5	-	ns

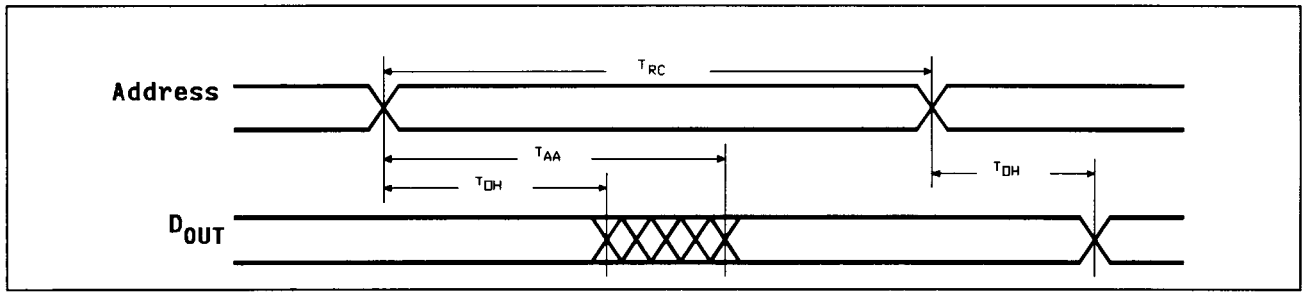
(2) WRITE CYCLE

PARAMETER		SYMBOL	W2416-70		W2416-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	70	-	100	-	ns
Chip Selection to End of Write		T_{CW}	45	-	80	-	ns
Address Valid to End of Write		T_{AW}	50	-	80	-	ns
Address Setup Time		T_{AS}	5	-	5	-	ns
Write Pulse Width		T_{WP}	45	-	60	-	ns
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	T_{WR}	5	-	5	-	ns
Data to Write Time Overlap		T_{DW}	30	-	40	-	ns
Data Hold from Write Time		T_{DH}	5	-	5	-	ns
Write to Output in High Z		T_{WHZ}	0	30	0	35	ns
Output Disable to Output in High Z		T_{OHZ}	0	30	0	30	ns
Output Active from End of Write		T_{OW}	5	-	5	-	ns

TIMING WAVEFORMS

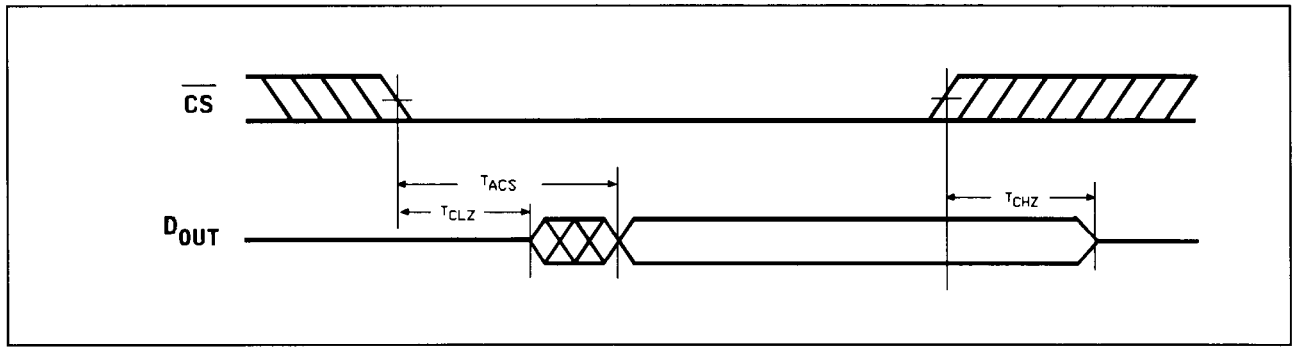
READ CYCLE 1

(Address Controlled)



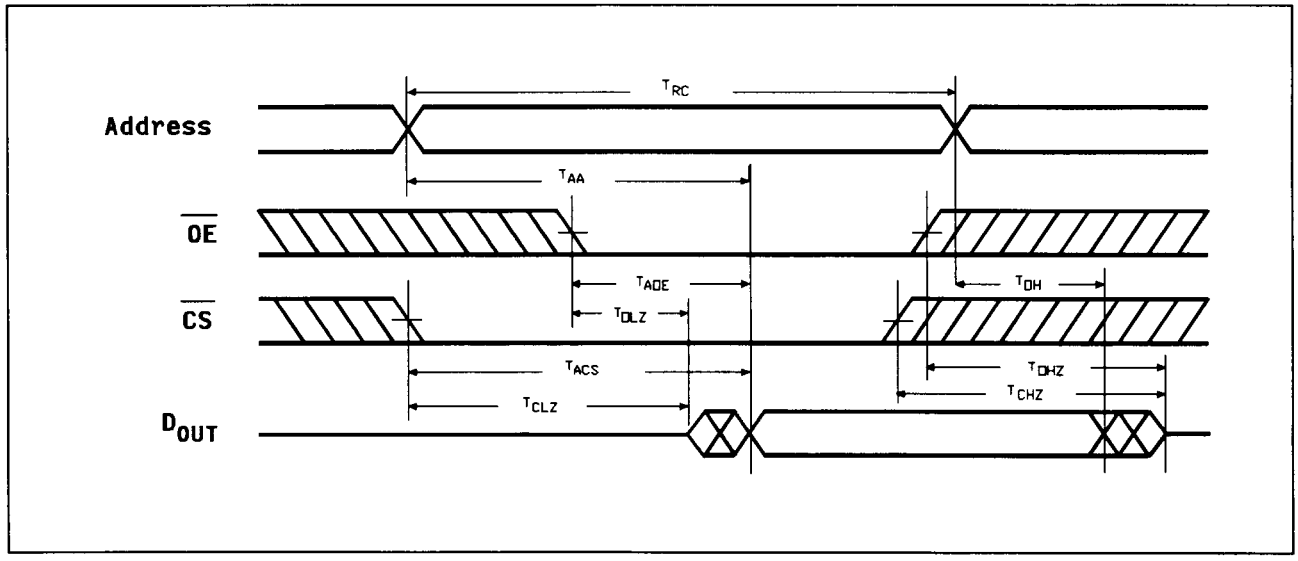
READ CYCLE 2

(Chip Select Controlled)

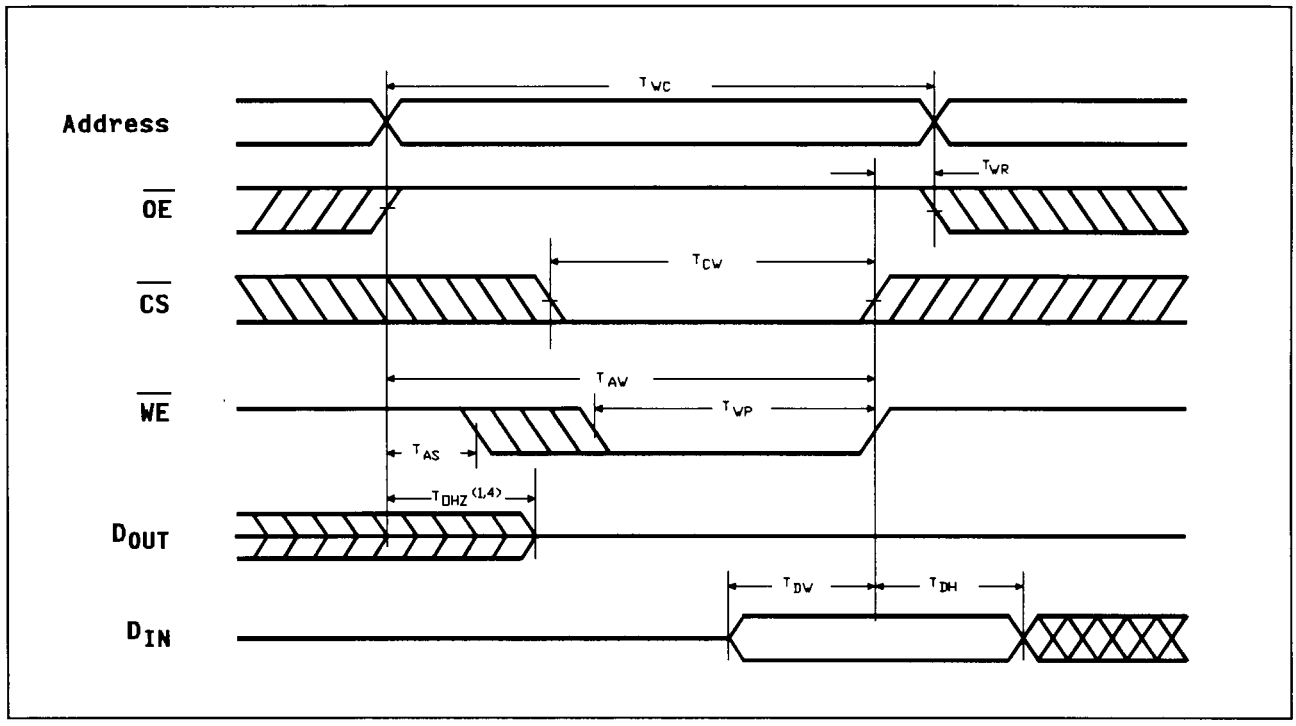


READ CYCLE 3

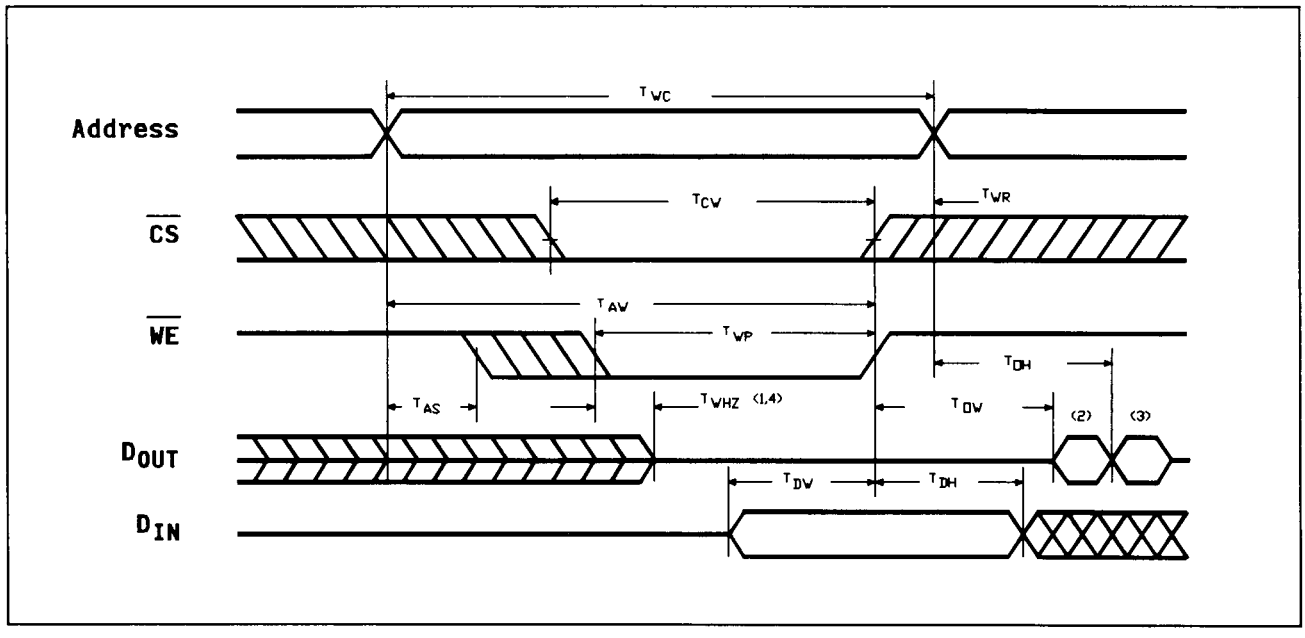
(Output Enable Controlled)



WRITE CYCLE 1



WRITE CYCLE 2



Notes:

1. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
2. D_{OUT} is the same phase of write data of this write cycle.
3. D_{OUT} is the read data of next address.
4. Transition is measured ±500mV from steady state with C_L=5pF. This parameter is guaranteed and not 100% tested.

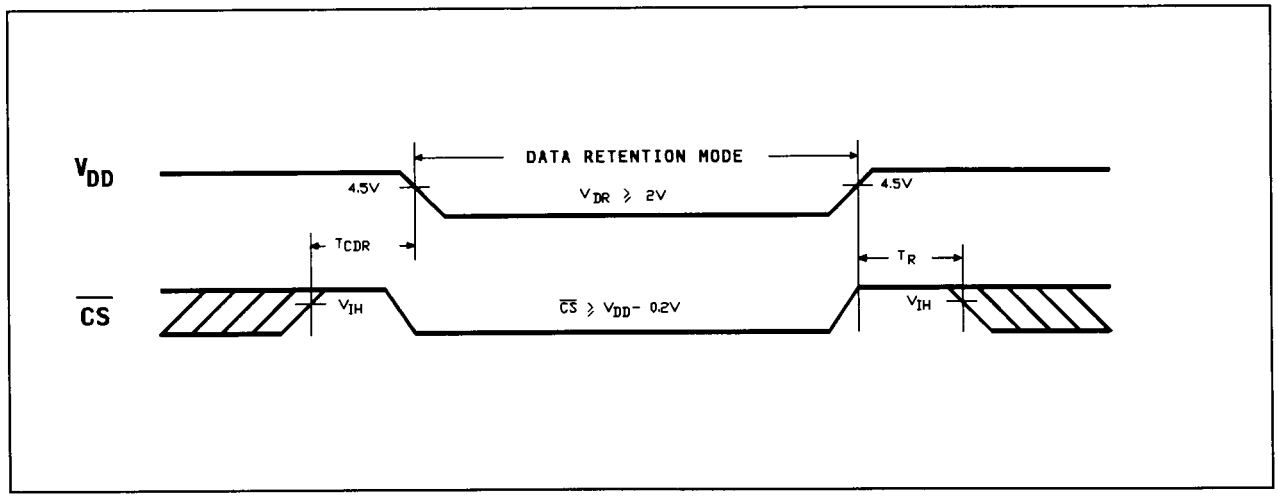
DATA RETENTION CHARACTERISTICS

(Ta=0 to 70℃, Guaranteed Only for L-Version)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{DD}$ - 0.2V	2.0	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS} \geqq V_{DD}$ - 0.2V V_{DD} = 3V	-	2	50	μA
Chip Deselect to Data Retention Time	T_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	T_R		T_{RC} *	-	-	ns

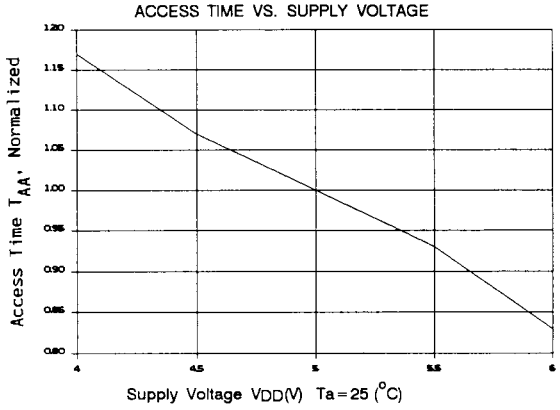
Note:* T_{RC}=Read Cycle Time

DATA RETENTION WAVEFORM

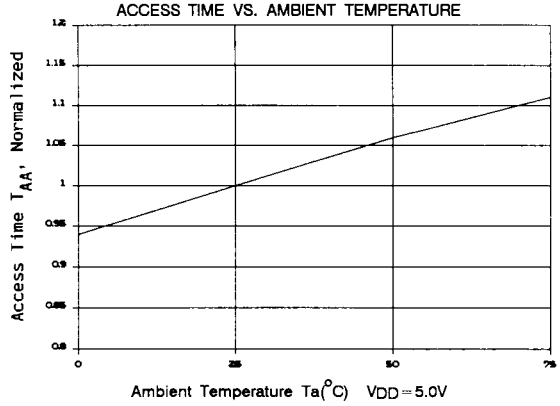


CHARACTERISTICS CURVES

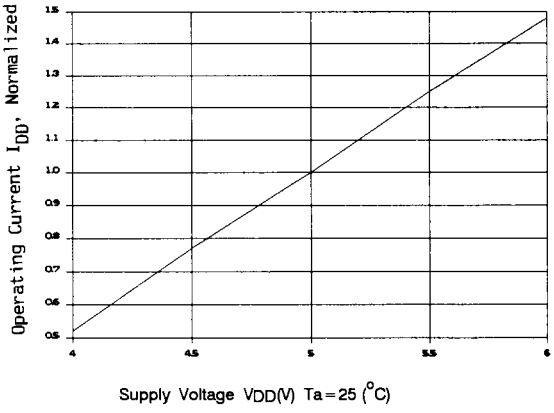
ACCESS TIME VS. SUPPLY VOLTAGE



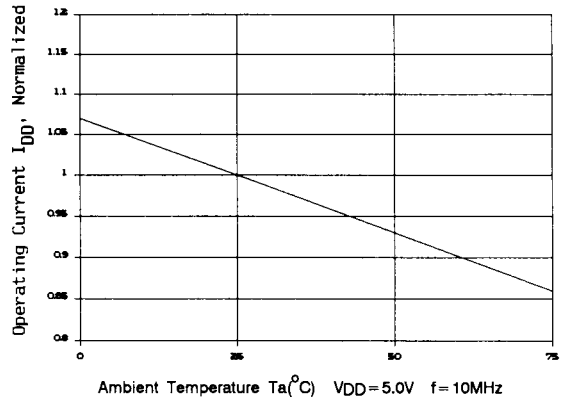
ACCESS TIME VS. AMBIENT TEMPERATURE



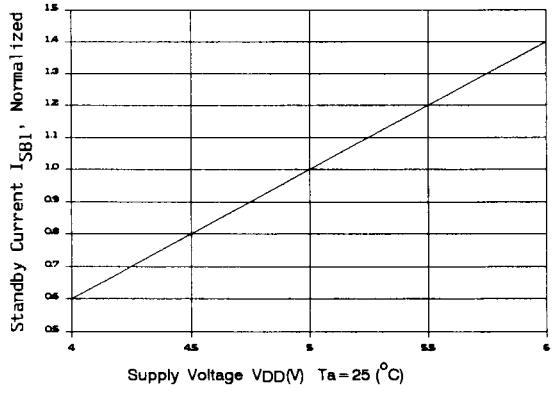
OPERATING SUPPLY CURRENT VS. SUPPLY VOLTAGE



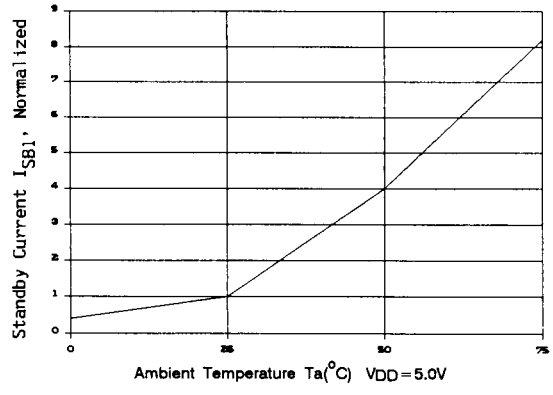
OPERATING CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



ORDERING INFORMATION

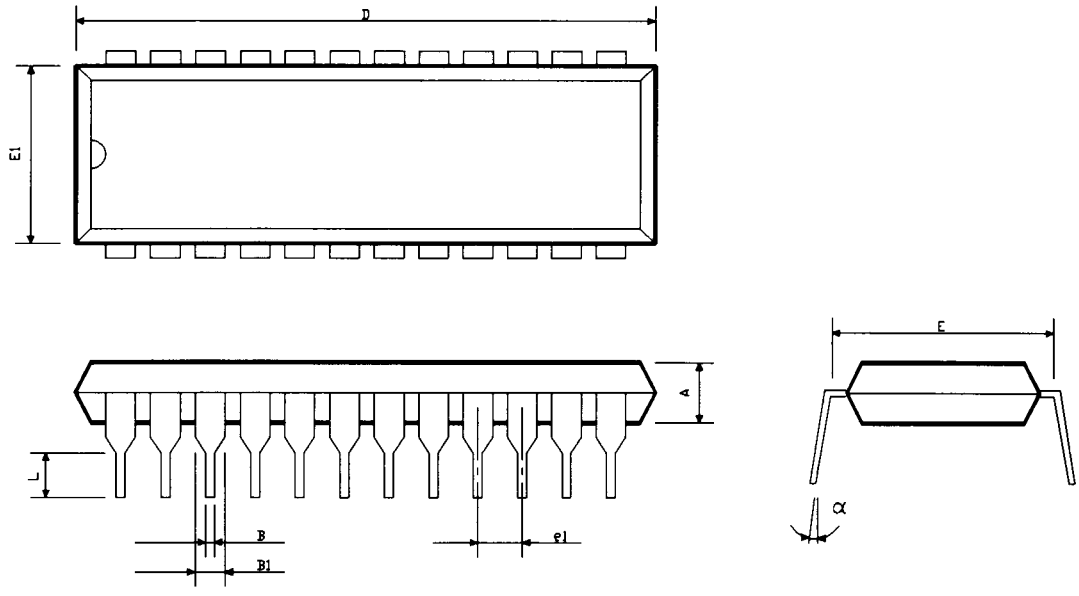
Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package	Remark
W2416-70	70	80	1	600mil DIP	
W2416-70L	70	80	0.1	600mil DIP	Low Power
W2416-10	100	80	1	600mil DIP	
W2416-10L	100	80	0.1	600mil DIP	Low Power
W2416S-70	70	80	1	300mil SOP	
W2416S-70L	70	80	0.1	300mil SOP	Low Power
W2416S-10	100	80	1	300mil SOP	
W2416S-10L	100	80	0.1	300mil SOP	Low Power
W2416K-70	70	80	1	300mil Skinny	
W2416K-70L	70	80	0.1	300mil Skinny	Low Power
W2416K-10	100	80	1	300mil Skinny	
W2416K-10L	100	80	0.1	300mil Skinny	Low Power

Notes:

1. Winbond Electronics Corp. reserves the right to make changes to its products without prior notice, in order to improve design and preformance.
2. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such application.

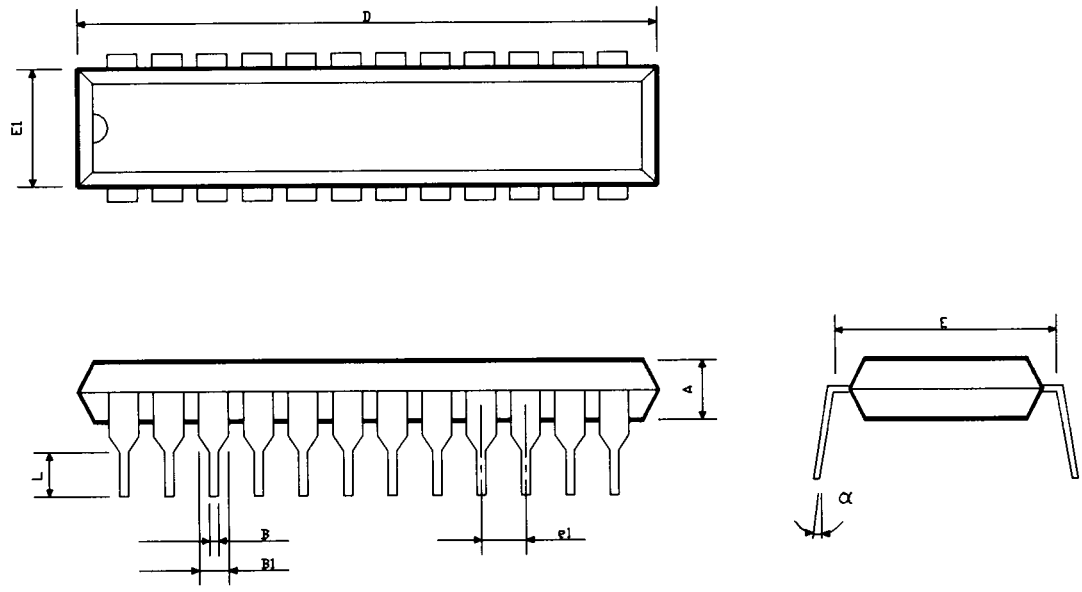
PACKAGE DIMENSION

24 LEAD P-DIP



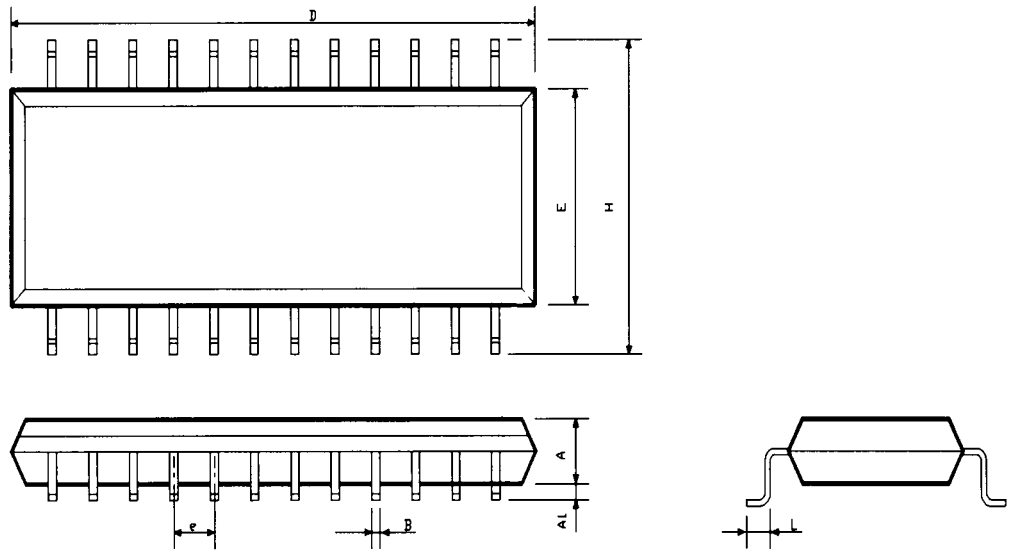
Symbol	Dimensions in inch	Dimensions in mm
A	0.155 ± 0.005	3.937 ± 0.127
B	0.018 ± 0.004	0.457 ± 0.102
B1	0.060 ± 0.004	1.524 ± 0.102
D	1.250 ± 0.010	31.750 ± 0.254
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 ± 0.010	13.970 ± 0.254
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.135 ± 0.010	3.429 ± 0.254
α	0° ~ 7°	0° ~ 7°

24 LEAD P-DIP SKINNY



Symbol	Dimensions in inch	Dimensions in mm
A	0.130 ± 0.005	3.302 ± 0.127
B	0.018 ± 0.004	0.457 ± 0.102
B1	0.060 ± 0.004	1.524 ± 0.102
D	1.250 ± 0.010	31.877 ± 0.254
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.260 ± 0.010	6.604 ± 0.254
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 7°	0° ~ 7°

24 LEAD SO NARROW BODY



Symbol	Dimensions in inch	Dimensions in mm
A	0.091 ± 0.006	2.311 ± 0.152
A1	0.008 ± 0.003	0.203 ± 0.076
B	0.016 ± 0.003	0.406 ± 0.076
D	0.606 ± 0.004	15.392 ± 0.102
E	0.295 ± 0.004	7.493 ± 0.102
e	0.050 ± 0.008	1.270 ± 0.203
H	0.406 ± 0.008	10.312 ± 0.203
L	0.036 ± 0.006	0.914 ± 0.152

Winbond

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