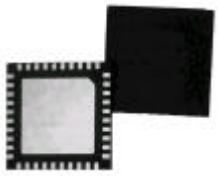
Advanced Information

SVG-2066 / SVG-2066Z

500MHz - 2200MHz 6-Bit Variable Gain Amp



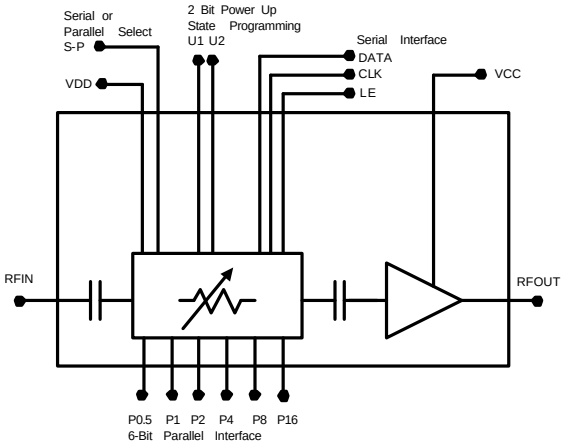
RoHS Compliant & Green Package

6mm x 6mm QFN Package

Product Description

Sirenza Microdevices' SVG-2066 is an IC based 6-bit digital 31.5dB range attenuator cascaded with a linear class A amplifier in a low-cost surface-mountable 6x6 QFN plastic package. This product is specifically designed as a high linearity variable gain amplifier for infrastructure equipment that can be used in either the RF transmit or RF receive path. It features both parallel or serial programmability, programmable power up states, latchable parallel control, 3V or 5V combatible logic and robust Class 1B ESD. The SVG-2066 features configurable pin I/O's for optimizing the part over application specific bands.

Functional Block Diagram



Product Features

- **P1dB = 25dBm @ 2140MHz**
- **OIP3 Typical 41dBm @ 2GHz**
- **Gain = 15dB at 850MHz**
- **31.5dB Attenuation range in 0.5dB steps**
- **Serial or Parallel Controlled**
- **Optional Latched Parallel Control**
- **Programmable Power Up States**
- **Immune to Latch-Up**
- **Positive Supply Voltage**
- **3V or 5V Logic Compatible**

Applications

- **CDMA, W-CDMA Tx and Rx**
- **GSM, EDGE Tx and Rx**
- **High Performance VGA applications**

Key Specifications

Symbol	Parameters: Test Conditions, App circuit page 4 Z_0 = 50Ω, V_{CC} = 5.0V, Vdd=3V, I = 115mA, T_L= 30ºC	Unit	Min.	Typ.	Max.
f_O	Frequency of Operation	MHz	500		2200
P_{1dB}	Output Power at 1dB Compression – 850MHz	dBm		24	
	Output Power at 1dB Compression – 2.14GHz		23.5	25	
S_{21}	Small Signal Gain – 850MHz @ 0dB state	dB		15	
	Small Signal Gain – 2.14GHz @ 0dB state		9.5	11	13.5
IP3	Third Order Intercept (Pout = 9dBm per tone) - 850MHz	dBm		39	
	Third Order Intercept (Pout = 9dBm per tone) - 2.14GHz		39	41	
NF	Noise Figure at 850 MHz @ 0 dB state	dB		5.9	
	Noise Figure at 2140 MHz @ 0 dB state			6.9	7.9
IRL	Input Return Loss 850-2200 MHz (0dB attenuation)	dB	9	12	
ORL	Output Return Loss 850-2200MHz (0dB attenuation)		9	12	
Ts	10%/90% Settling time	nS		320	
Icq	Current (Vcc = 5V,Vdd=3v)	mA	100	115	130
$R_{th, j-l}$	Thermal Resistance (junction - lead)	ºC/W		70	

The information provided herein is believed to be reliable at press time. Sirenza Microdevices assumes no responsibility for inaccuracies or ommisions.
Sirenza Microdevices assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. Sirenza Microdevices does not authorize or warrant any Sirenza Microdevices product for use in life-support devices and/or systems.
Copyright 2002 Sirenza Microdevices, Inc. All worldwide rights reserved.

Specification continued

Symbol	Parameters: Test Conditions Z_0 = 50Ω, V_{CC} = 5.0V,Vdd=3V Iq = 115mA	Unit	Min.	Typ.	Max.
ERR	Atten setting accuracy any state (500MHz-2200MHz)	dB		+/- 0.2	+/- (0.2+3% Atten setting)
DYNR	Attenuation dynamic range	dB	30.3	31.5	32.7
FCLK	Serial Data Clock Frequency	MHz			20
VDD	Drain voltage of Attenuator	V	2.7	3.0	3.3
IDD	Drain Supply Current	uA		40	100
LH	Digital Logic High	V	0.7xVDD		VDD
LL	Digital Logic Low	V	0		0.3xVDD
ILEAK	Digital Logic Leakage	uA			1

Absolute Maximum Ratings

Parameters	Mln	Max	Unit
VCC Bias Current (I_C)		220	mA
VCC Bias Voltage		8	V
Power Dissipation		1.5	W
Drain Voltage (V_{DD})	-0.3	4.0	V
Voltage on any Digital Input	-0.3	VDD+0.3	V
Operating Lead Temperature (T_L)	-40	+85	ºC
Max RF Input Power		21	dBm
Storage Temperature Range	-40	+150	ºC
Operating Junction Temperature (T_J)		+150	ºC
ESD Human Body Model		500	V

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias conditions should also satisfy the following expression:
$I_D V_D < (T_J - T_L) / R_{TH, j-l}$

Caution: ESD Sensitive
Appropriate precaution in handling, packaging and testing devices must be observed.

Digital Interfacing:

Serial or Parallel Mode Selection
The SVG-2066 can be controlled with either a serial or parallel interface. The S-P bit selects the mode: S-P=low for parallel mode and S-P=high for serial mode.

Parallel Mode Operation
For latched parallel interfacing the LE line should be held low while changing attenuation state control logic P0.5 thru P16. To load data pulse LE from low to high and to low again. See Figure 1 and Table 1 on the next page for the parallel mode timing diagram and specifications. For direct parallel mode operation the LE line should be held high and the attenuation state is directly loaded when the parallel line logic changes. The truth table for parallel operation is shown in Table 2.

Serial Mode Operation
Three CMOS compatible signals control the attenuator in this mode: DATA, CLK and LE. When LE is high the latch is enabled and data in the serial shift register gets loaded. When the LE is low the data in the shift register is latched. Refer to Figure 2 for the timing diagram and Table 3 for the timing specifications.

Power up State Programming
At power up in serial mode the six control bits are set to the values available on the six parallel inputs P0.5 thru P16 (see Table 2). For parallel mode the power up state is set with the two bit word defined by U1 and U2. See the truth table in Table 4.

Figure 1: Parallel Mode Timing Diagram (S-P=0)

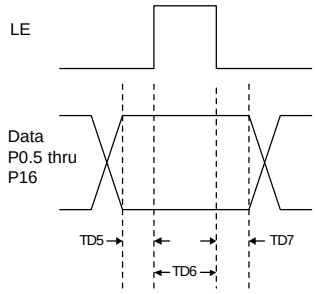


Table 2: Parallel Mode Truth table (S-P=0)

Attenuation State	P0.5	P1	P2	P4	P8	P16
Reference	0	0	0	0	0	0
0.5 dB	1	0	0	0	0	0
1 dB	0	1	0	0	0	0
2 dB	0	0	1	0	0	0
4 dB	0	0	0	1	0	0
8 dB	0	0	0	0	1	0
16 dB	0	0	0	0	0	1
31.5 dB	1	1	1	1	1	1

Table 1: Parallel Mode Timing Specifications (S-P=0)

Parameter	Symbol	Unit	Min	Max
LE minimum pulse width	TD6	nS	10	
Delay set up time before rising LE edge	TD5	nS	10	
Data hold after falling edge of LE	TD7	nS	10	

Figure 2: Serial Mode Timing Diagram (S-P=1)

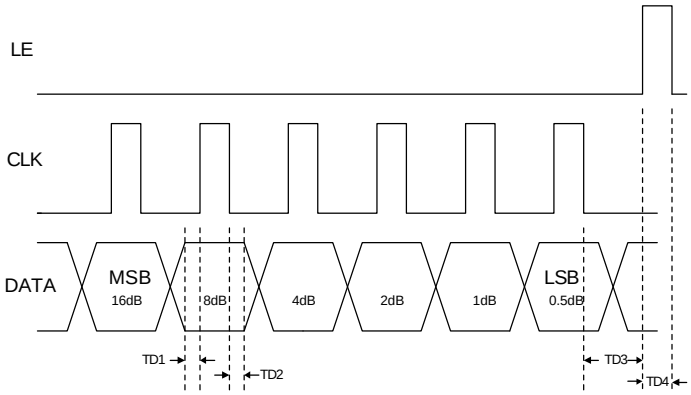


Table 3: Serial Mode Timing Specifications

Parameter	Symbol	Unit	Min	Max
Serial data delay before clock rising edge	TD1	nS	10	
Serial data hold after clock falling edge	TD2	nS	10	
LE delay after last clock falling edge	TD3	nS	10	
LE minimum pulse width	TD4	nS	30	
Serial data clock freq	FCLK	MHz		20
Serial clock high time	TCLKH	nS	30	
Serial clock low time	TCLKL	nS	30	

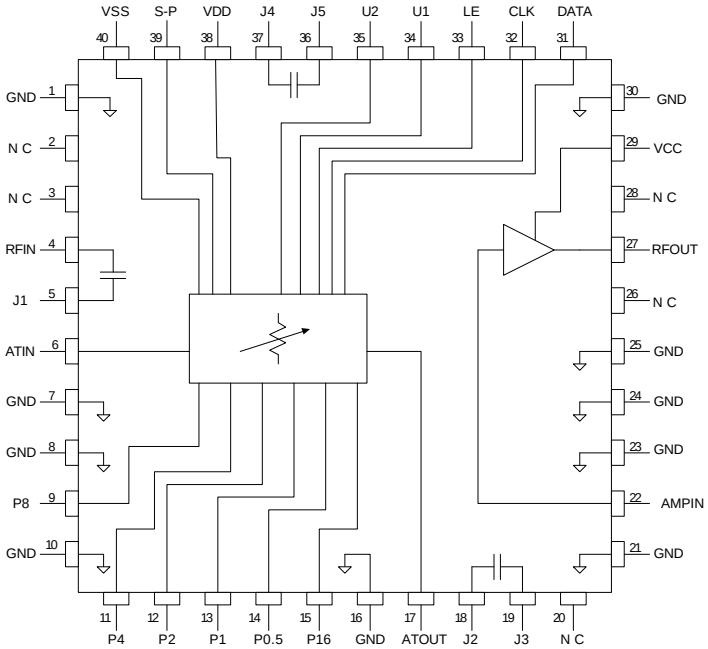
Table 4: Power Up Truth Table for Parallel Mode (S-P=0)

Attenuation State	LE	U1	U2
Reference	0	0	0
8 dB	0	1	0
16 dB	0	0	1
31 dB	0	1	1
Defined by P0.5 Thru P16	1	Not Applicable	Not Applicable

Note: Serial mode power up (S-P=1) state is defined by the parallel input logic shown in Table 2.

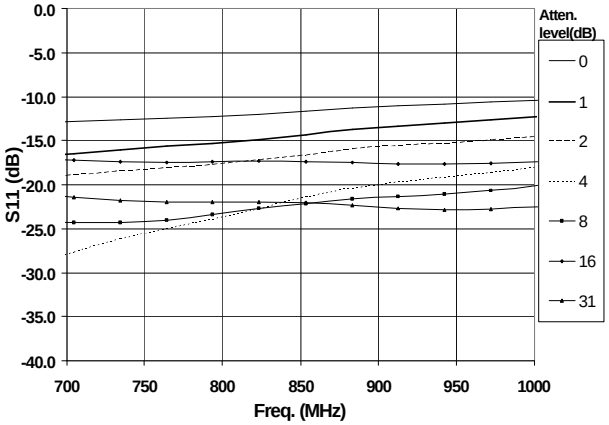
Pin Out Description

Pin #	Label	Description
2,3,20,26,28	N/C	These are unused pins and not wired inside the package. May be grounded or connected to adjacent pins.
1,7,8,10,16, 21,23,24,25,30	GND	Pins are internally grounded
4	RFIN	RF input pin. Connects to 100pF cap inside package.
5	J1	Jumper this pin on the PC board to the attenuator input (ATIN) pin #6. Connects to 100pF cap inside package.
6	ATIN	Attenuator input pin
9	P8	Parallel interface attenuation control bit 8 dB. When in serial mode P0.5, P1, P2, P4, P8 and P16 logic dictate power up state.
11	P4	Parallel interface attenuation control bit 4 dB. When in serial mode P0.5, P1, P2, P4, P8 and P16 logic dictate power up state.
12	P2	Parallel interface attenuation control bit 2 dB. When in serial mode P0.5, P1, P2, P4, P8 and P16 logic dictate power up state.
13	P1	Parallel interface attenuation control bit 1 dB. When in serial mode P0.5, P1, P2, P4, P8 and P16 logic dictate power up state.
14	P0.5	Parallel interface attenuation control bit 0.5dB. When in serial mode P0.5, P1, P2, P4, P8 and P16 logic dictate power up state.
15	P16	Parallel interface attenuation control bit 16dB. When in serial mode P0.5, P1, P2, P4, P8 and P16 logic dictate power up state.
17	ATOUT	Attenuator output pin.
18	J2	Jumper this pin to the attenuator output pin (ATOUT). Connects to 100pF cap inside package.
19	J3	Connect this pin to the amplifier input pin (AMPIN) with the appropriate AMPIN impedance matching
22	AMPIN	Amplifier input pin. Internally connected to base of amplifier (~1.3V)
27	RFOUT	Amplifier RF output pin. Internally connected to 5V. Not matched to 50 ohm. Use appropriate matching circuit.
29	VCC	Power Supply pin to Amplifier. Apply 5.0V to this pin.
31	Data	Serial interface data input.
32	CLK	Serial interface clock input.
33	LE	Latch enable input. Parallel mode can also be latch enabled with this pin.
34, 35	U1 / U2	Parallel mode power-up state logic bits. 0/0 = 0dB, 1/0 = 8dB, 0/1=16dB, 1/1=31dB
36	J5	Jumper this pin to GND on the PC board. Connects to 1000pF cap inside package.
37	J4	Jumper this pin on PC board to VDD pin 38. Connects to 1000pF bypass cap inside package.
38	VDD	Power supply pin to Digital Attenuator. Apply 2.7-3.3V to this pin. May be set from another voltage with a voltage divider (pulls 40uA typ, 100uA max)
39	S-P	Serial or parallel mode select. Logic low for parallel mode. Logic high for serial mode.
40	VSS	Negative supply voltage or GND
EPAD	GND	Exposed area on the bottom side of the package . GND with vias as shown in recommended landing pattern.

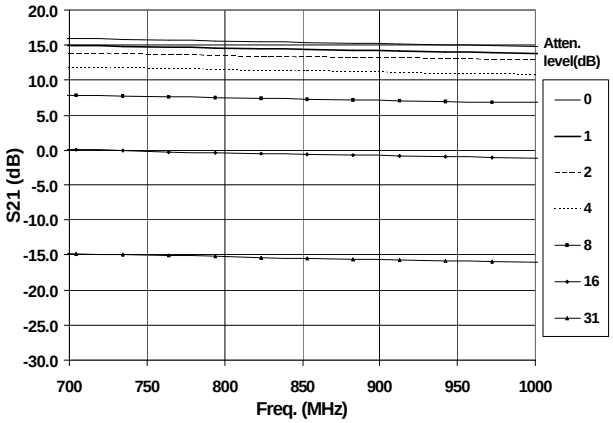


Measured 850MHz Evaluation Board Data (V_{cc} = 5.0V, Vdd=3.0V, I_q =115mA)

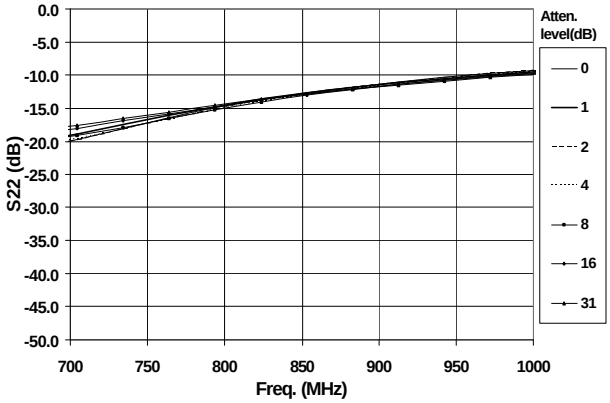
S11 vs. Frequency, T=+25c



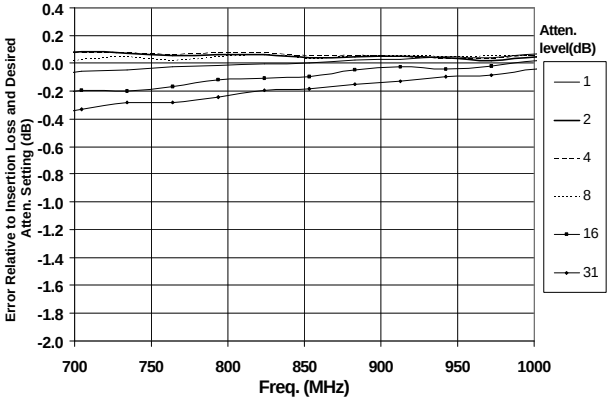
S21 vs. Frequency, T=+25c



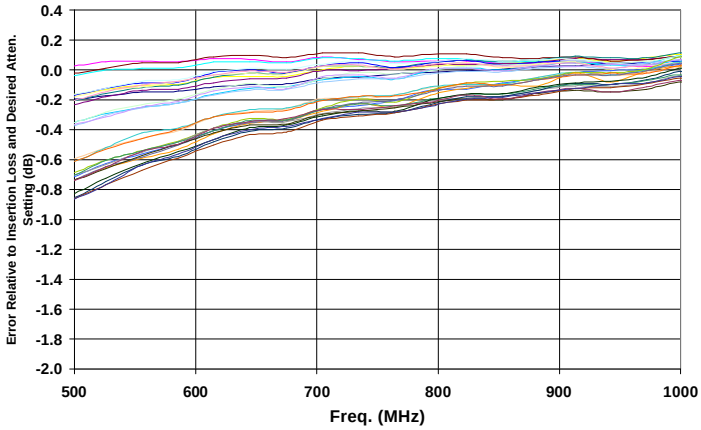
S22 vs. Frequency, T=+25c



850MHz +25c Attenuation Error vs. Frequency

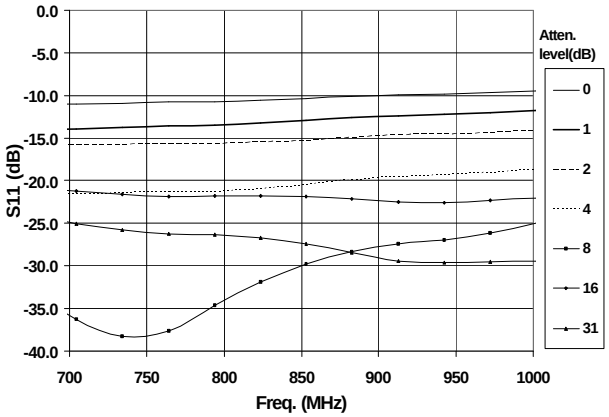


T= +25c, All 1dB Steps,Attenuation Error vs. Frequency

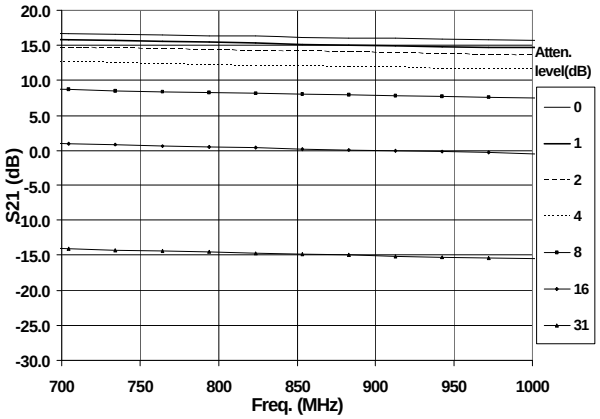


Measured 850MHz Evaluation Board Data (V_{CC} = 5.0V, Vdd=3.0V, I_q =115mA)

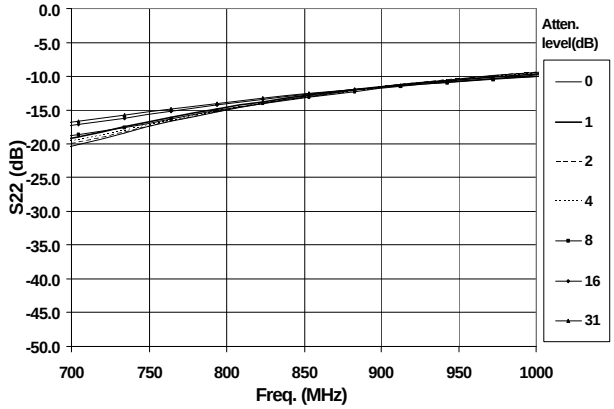
S11 vs. Frequency, T=-40c



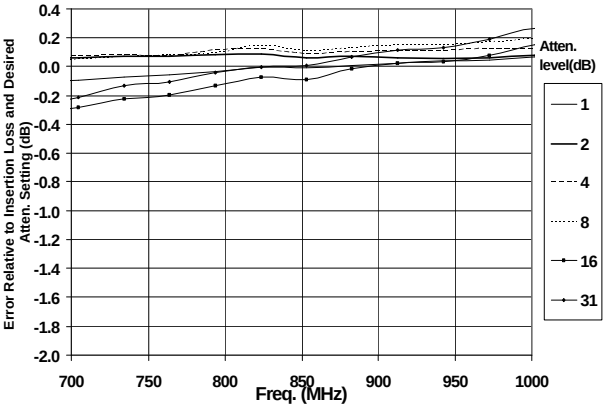
S21 vs. Frequency, T=-40c



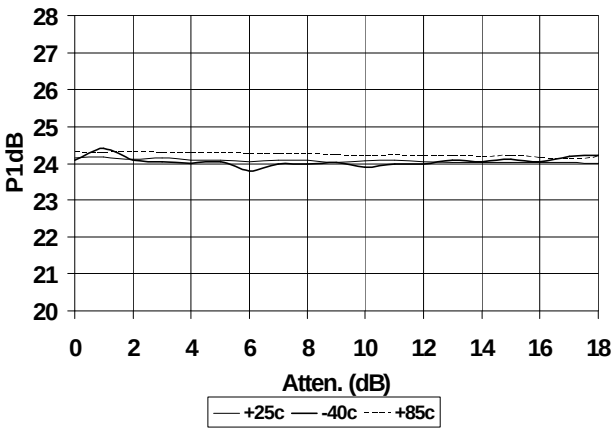
S22 vs. Frequency, T=-40c



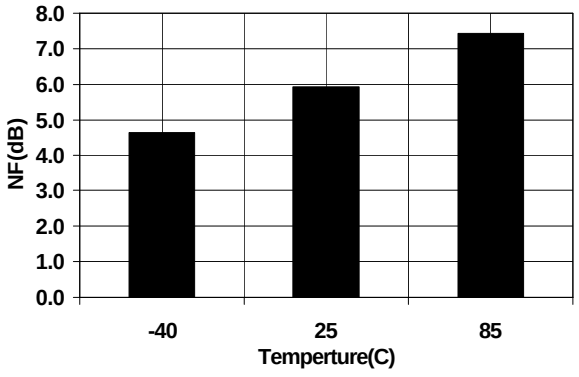
T=-40c Attenuation Error vs. Frequency



850MHz P1dB vs Atten

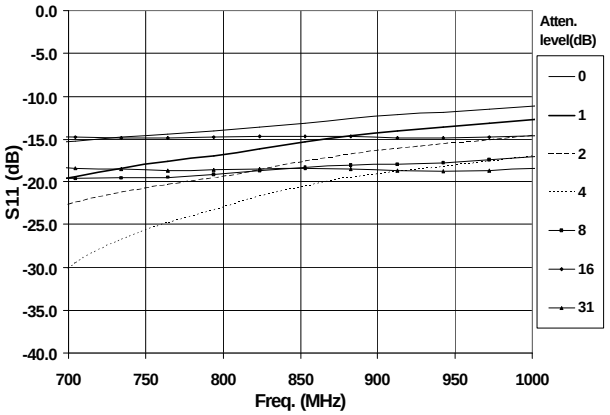


Noise Figure vs Temp, F=850MHz, Atten.=0dB

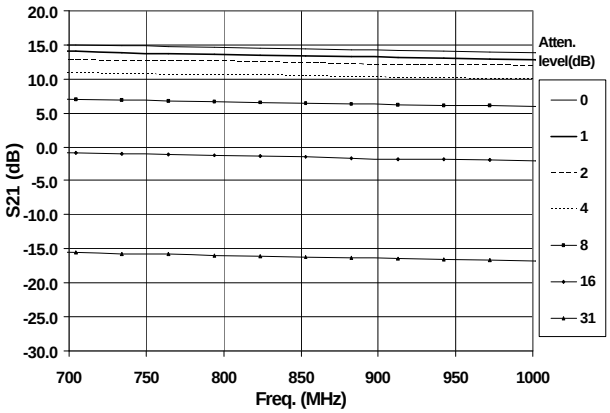


Measured 850MHz Evaluation Board Data (V_{CC} = 5.0V, Vdd=3.0V, I_q =115mA)

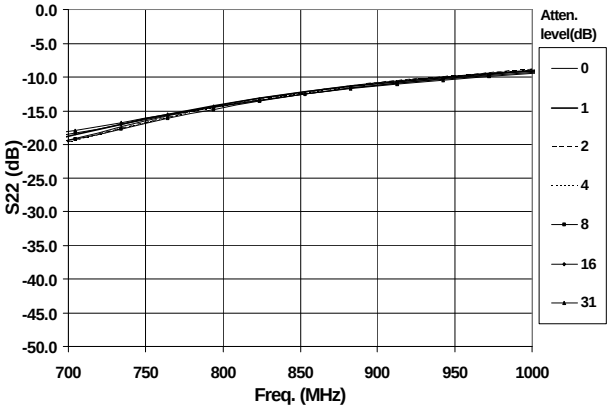
S11 vs. Frequency, T=+85c



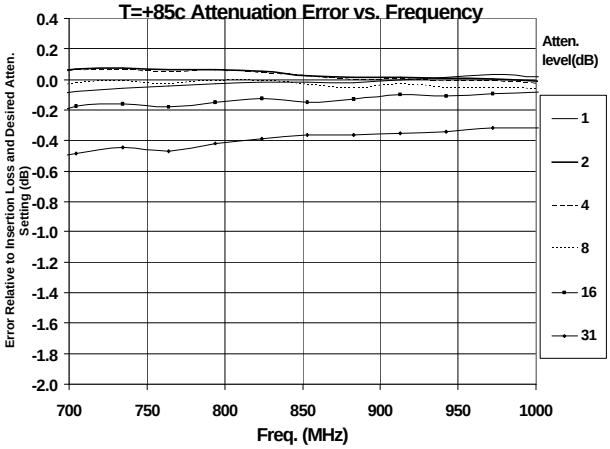
S21 vs. Frequency, T=+85c



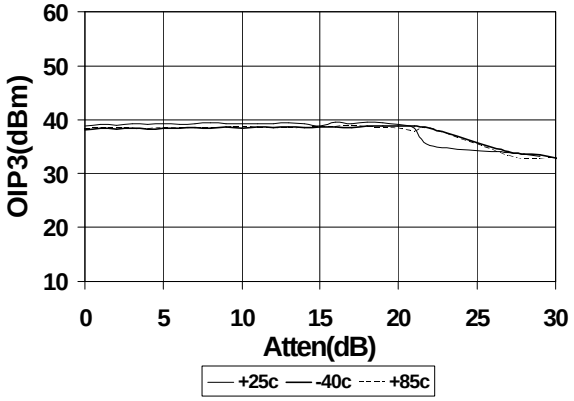
S22 vs. Frequency, T=+85c



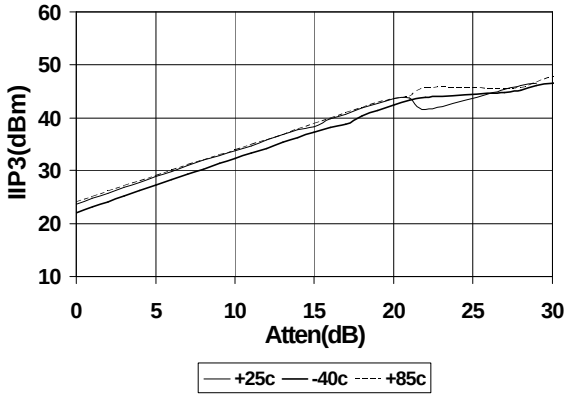
T=+85c Attenuation Error vs. Frequency



Output IP3 vs atten level

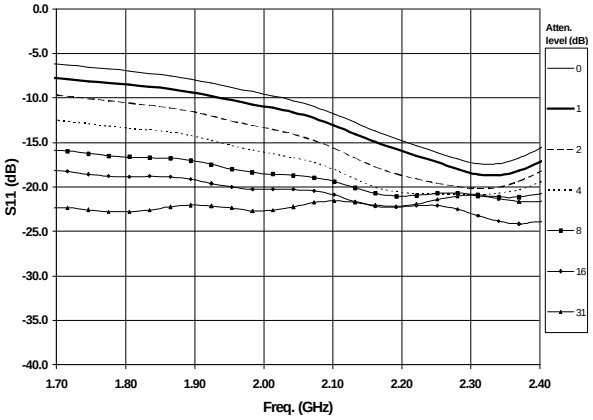


Input IP3 vs atten level

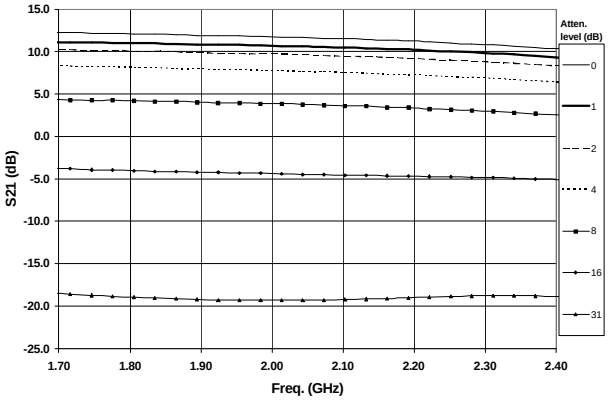


Measured 2.14GHz Evaluation Board Data (V_{cc} = 5.0V, Vdd=3.0V, I_q =115mA)

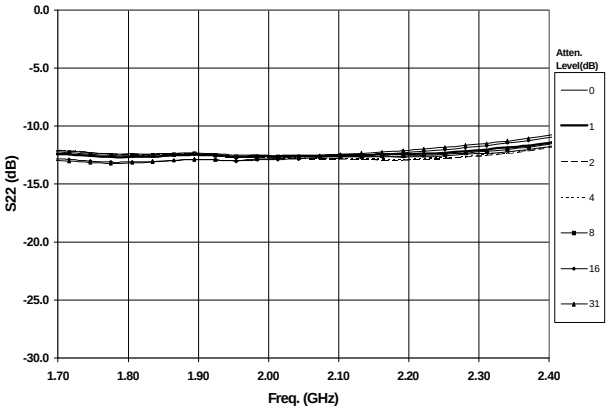
S11 vs. Frequency, T= +25c



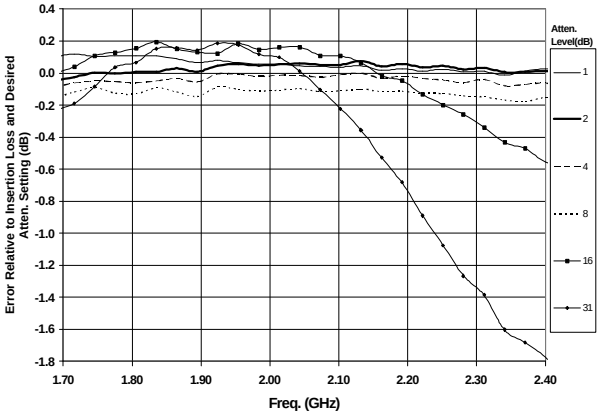
S21 vs. Frequency, T= +25c



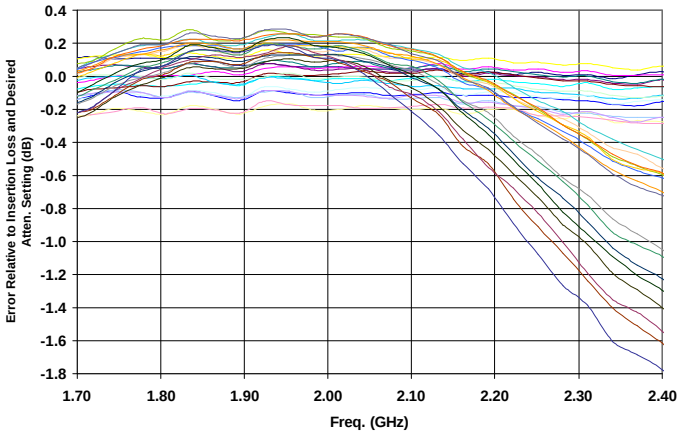
S22 vs. Frequency, T= +25c



T=+25c Attenuation Error vs. Frequency

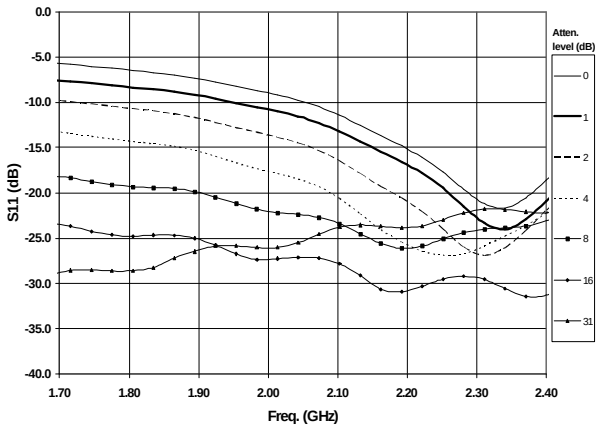


All 1dB Steps, T= +25c Attenuation Error vs. Frequency

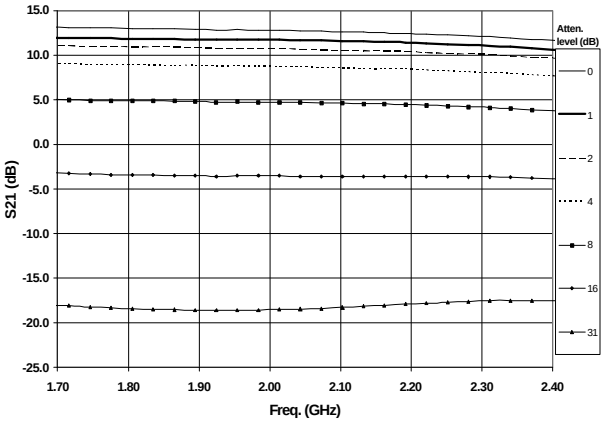


Measured 2.14GHz Evaluation Board Data (V_{cc} = 5.0V, Vdd=3.0V, I_q =115mA)

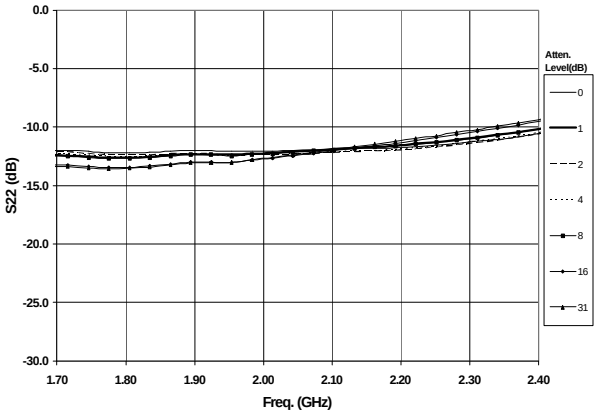
S11 vs. Frequency, T= -40c



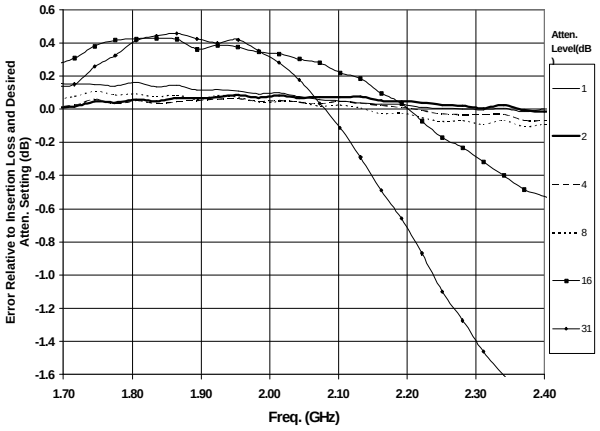
S21 vs. Frequency, T= -40c



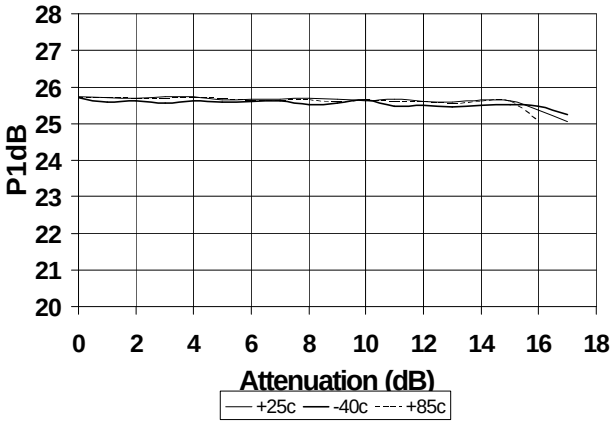
S22 vs. Frequency, T= -40c



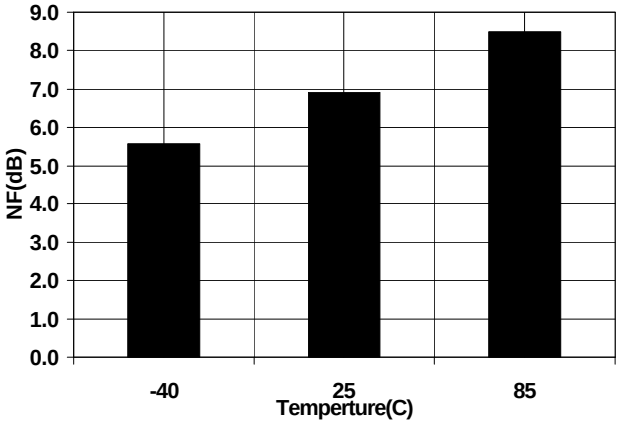
T=-40c Attenuation Error vs. Frequency



P1dB vs Atten

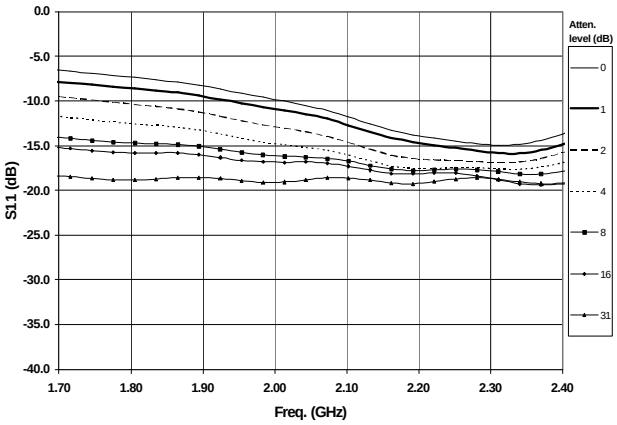


Noise Figure vs Temp, F=2.14GHz, Atten.=0dB

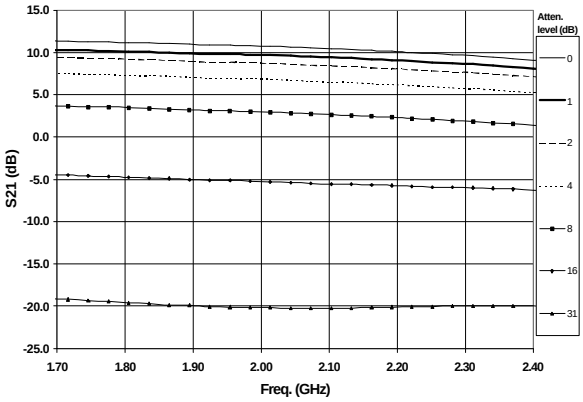


Measured 2.14GHz Evaluation Board Data (V_{cc} = 5.0V, Vdd=3.0V, I_q =115mA)

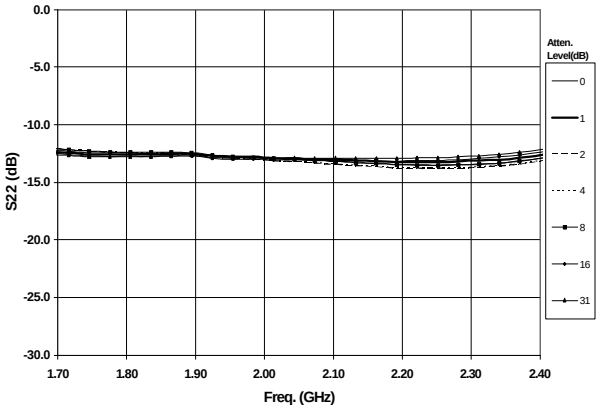
S11 vs. Frequency, T= +85c



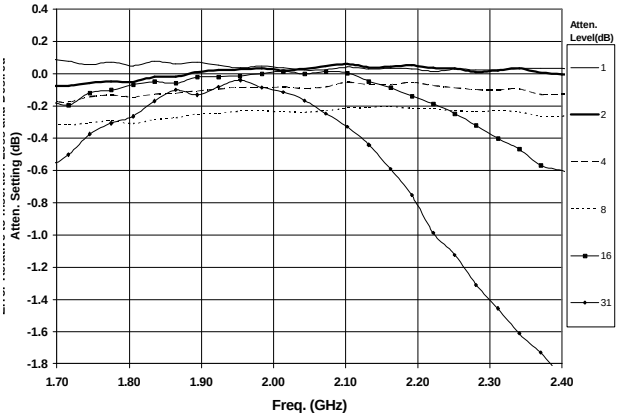
S21 vs. Frequency, T= +85c



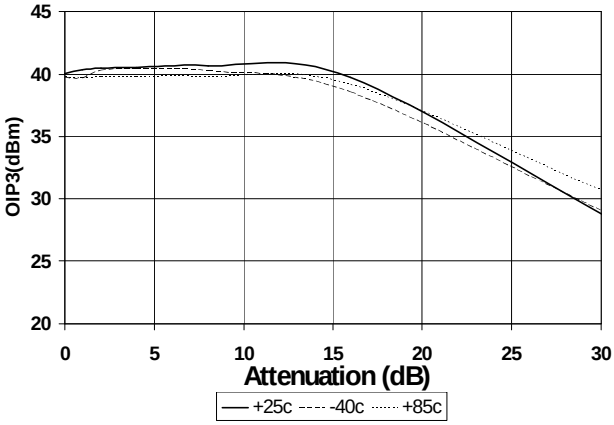
S22 vs. Frequency, T= +85c



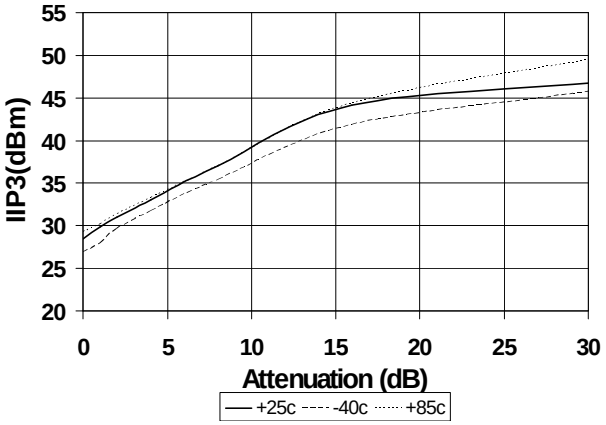
T=+85c Attenuation Error vs. Frequency



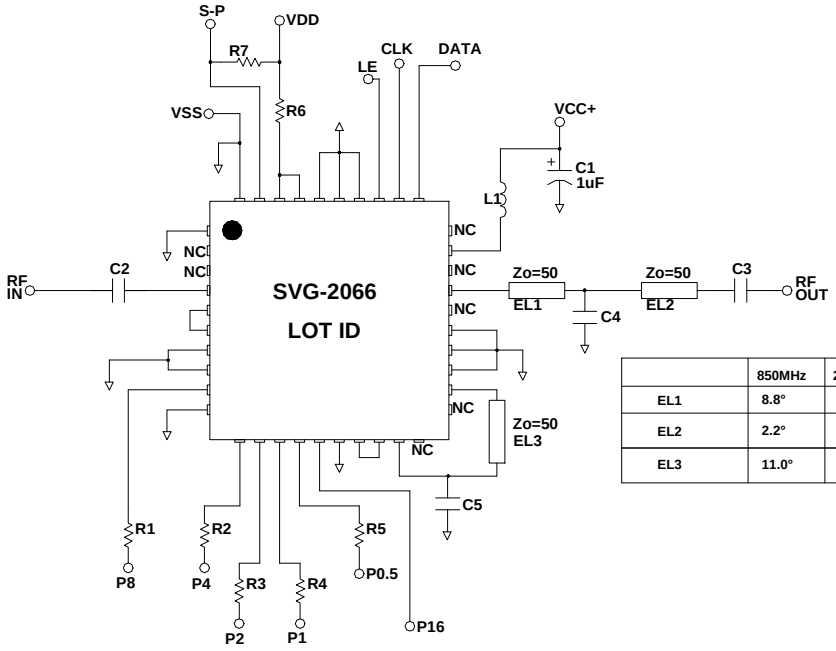
Output IP3 vs Atten.



Input IP3 vs Atten.



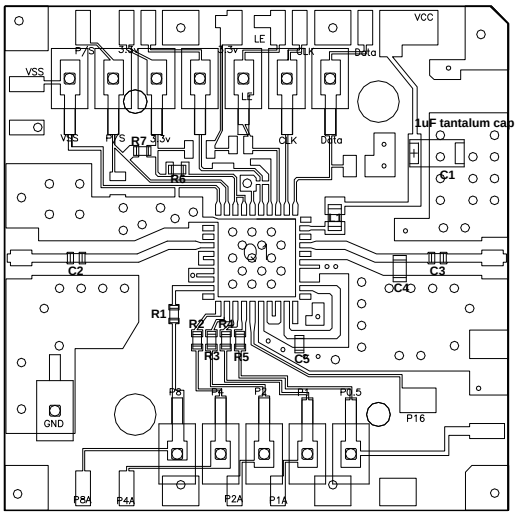
850MHz, 2140MHz Evaluation Board Schematic For Vcc = 5.0V, Vdd = 3.0V, Iq = 115mA



	850MHz	2140MHz
EL1	8.8°	22.1°
EL2	2.2°	5.5°
EL3	11.0°	N/A

850MHz, 2140MHz Evaluation Board Layout For Vcc = 5.0V, Vdd = 3.0V, Iq = 115mA

Board material GETEK, 10mil thick, Dk=3.9, 2 oz. copper



DESG	850MHz	2140MHz
Q1	SVG-2066	SVG-2066
R1,R2,R3 R4,R5,R7	0 ohm 0402 5%	0 ohm 0402 5%
C1	1uF Tantalum cap	1uF Tantalum cap
L1	33nH inductor 0603	18nH inductor 0603
C2,C3	47pF 0402 cap	22pF 0402 cap
R6	100 ohm 0402 5%	100 ohm 0402 5%
C4	2.7pF 0402 cap	1pF 0402 cap
C5	1.8pF 0402 cap	N/A

Note: Parallel interface controls should be held high or low for proper serial mode operation. Logic on these pins determine power up state for serial mode.

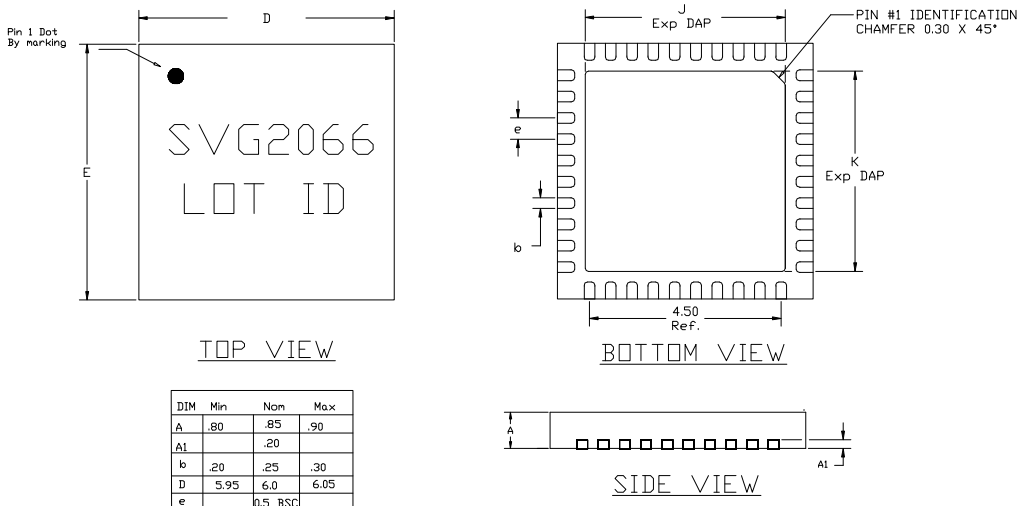
Part Number Ordering Information

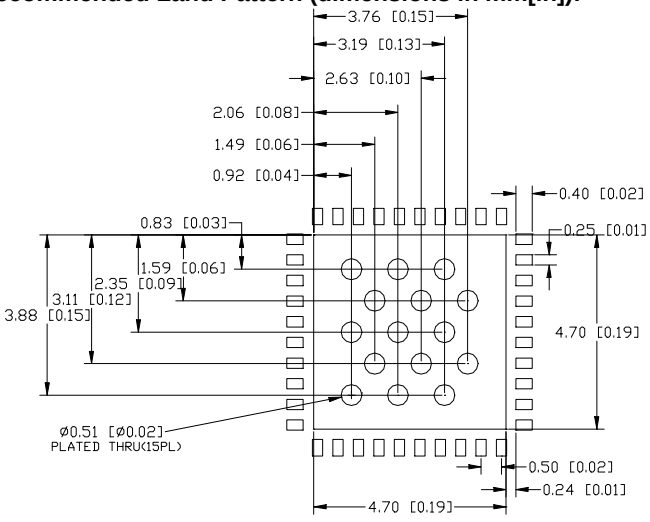
Part Number	Reel Size	Devices/Reel
SVG-2066 or SVG-2066Z	7”	1000

Part Symbolization

The part will be symbolized with an “SVG-2066” marking designator on the top surface of the package.

Package Outline Drawing (dimensions in mm):



DIM	Min	Nom	Max
A	.80	.85	.90
A1		.20	
b	.20	.25	.30
D	5.95	6.0	6.05
e		0.5 BSC	
E	5.95	6.0	6.05
J	4.65	4.70	4.75
K	4.65	4.70	4.75

Recommended Land Pattern (dimensions in mm[in]):