

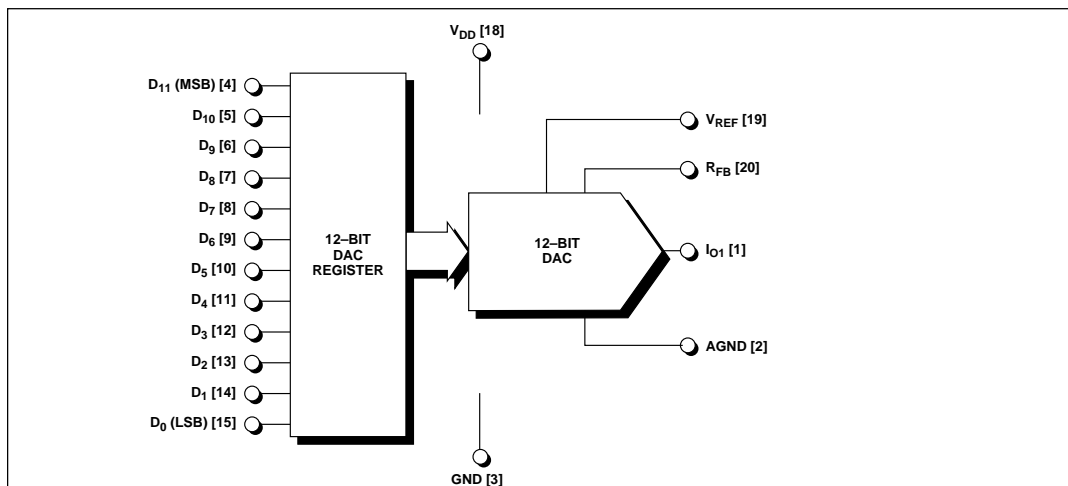
## 12–Bit, Buffered Multiplying DAC

- $\pm 1.0$  LSB Relative Accuracy Over Temperature
- Monotonic to 12–Bits Over Temperature
- High Stability, Segmented Architecture
- Proprietary, Low TCR Thin–Film Resistor Technology
- Operates With +5V to +15V Power Supplies
- On–Board, Level–Triggered Latches
- 2kVESD Protection on all Digital Inputs



### DESCRIPTION...

The **SP7545** is a low–cost, high stability 12–bit CMOS multiplying DAC with on–board data latches. The **SP7545** is constructed using a proprietary low–TCR thin–film process that requires no laser–trimming to achieve 12–bit performance. With no laser–trimming, inherent high stability, and a segmented (decoded) DAC architecture, the **SP7545** retains its performance over time and temperature. The **SP7545** is available for use in commercial and industrial temperature ranges. It is available in 20–pin plastic DIP and PLCC packages.



## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted.)

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{DD}$ to GND .....	-0.3V, +17V
Digital Input Voltage to GND .....	-0.3V, $V_{DD} + 0.3\text{V}$
$V_{REF}$ or $V_{REF}$ to GND .....	$\pm 25\text{V}$
Output Voltage (Pin 1, Pin 2) .....	-0.3V, $V_{DD} + 0.3\text{V}$
Power Dissipation (Any Package to $+75^\circ\text{C}$ ) .....	450mW
Derates above $75^\circ\text{C}$ by .....	6mW/ $^\circ\text{C}$
Dice Junction Temperature .....	$+150^\circ\text{C}$
Storage Temperature .....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 seconds) .....	$+300^\circ\text{C}$



**CAUTION:**  
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

## SPECIFICATIONS

( $T_A = 25^\circ\text{C}$ ;  $V_{DD} = +5\text{V}$  or  $+15\text{V}$  as noted;  $V_{REF} = +10\text{V}$ ;  $I_{O1} = \text{AGND} = \text{GND} = 0\text{V}$ ; unipolar unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
<b>STATIC PERFORMANCE</b>					
Resolution	12			Bits	
Integral Non-Linearity					Note 6
-J			$\pm 2.0$	LSB	Note 5; 11-bit relative accuracy
-K			$\pm 1.0$	LSB	Note 5; 12-bit relative accuracy
Differential Non-Linearity					Note 7
-J			$\pm 4.0$	LSB	Note 5; monotonic to 12-bits
-K			$\pm 1.0$	LSB	Note 5; monotonic to 12-bits
Gain Error					Note 16
-J			$\pm 20$	LSB	$V_{DD} = +5\text{V}$ ; Note 5
			$\pm 25$	LSB	$V_{DD} = +15\text{V}$
-K			$\pm 10$	LSB	$V_{DD} = +5\text{V}$
			$\pm 15$	LSB	$V_{DD} = +15\text{V}$
Output Leakage Current			$\pm 10$	nA	At $I_{O1}$ (Pin 1); Note 5 and 17
<b>AC PERFORMANCE CHARACTERISTICS</b>					
Propagation Delay			300	ns	Output Amplifier HOS-050; Note 10
			250	ns	$V_{DD} = +5\text{V}$ ; Note 11
Current Settling Time			2.0	$\mu\text{s}$	$V_{DD} = +15\text{V}$ ; Note 11
Output Capacitance		50	200	pF	Full scale transition; Note 12
			200	pF	WR, CS = 0V; data inputs $V_{DD}$
		25	70	pF	Note 5; data inputs $V_{DD}$
			70	pF	Data inputs 0V
Glitch Energy		250		nV-s	Note 5; data inputs 0V
Multiplying Feedthrough Error		2.0		$\text{mV}_{\text{p-p}}$	Note 13
		0.2		$\text{mV}_{\text{p-p}}$	Measured at output $I_{O1}$ ; Note 14
					Measured at output $I_{O1}$ ; Note 15
<b>STABILITY</b>					
Gain Error TC		$\pm 1.0$	$\pm 2.0$	ppm/ $^\circ\text{C}$	
			$\pm 2.0$	ppm/ $^\circ\text{C}$	Note 5
Integral Non-Linearity TC		$\pm 0.1$	$\pm 1.0$	ppm/ $^\circ\text{C}$	
			$\pm 1.0$	ppm/ $^\circ\text{C}$	Note 5
Differential Non-Linearity TC		$\pm 0.1$	$\pm 1.0$	ppm/ $^\circ\text{C}$	
			$\pm 1.0$	ppm/ $^\circ\text{C}$	Note 5
Power Supply Rejection		$\pm 0.002$	$\pm 0.01$	%/%	%/0.005% change in power supply voltage
			$\pm 0.02$	%/%	Note 5
<b>REFERENCE INPUT</b>					
Input Resistance	7	10	15	K $\Omega$	Pin 19 to GND
Input Resistance TC		$\pm 150$		ppm/ $^\circ\text{C}$	
Voltage Range			$\pm 25$	Volts	Note 5 and 8

## SPECIFICATIONS (continued)

( $T_A = 25^\circ\text{C}$ ;  $V_{DD} = +5\text{V}$ ;  $V_{REF} = +10\text{V}$ ;  $I_{O1} = \text{AGND} = \text{GND} = 0\text{V}$ ; unipolar unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
<b>DIGITAL INPUTS</b>					
Logic Levels					
$V_{IH}$	2.4		$V_{DD}$ 2.4	Volts Volts	$V_{DD} = +5\text{V}$ $V_{DD} = +5\text{V}$ ; Note 5
	13.5		$V_{DD}$ 13.5	Volts Volts	$V_{DD} = +15\text{V}$ $V_{DD} = +15\text{V}$ ; Note 5
$V_{IL}$	-0.3		0.8	Volts	$V_{DD} = +5\text{V}$
	-0.3		0.8	Volts	$V_{DD} = +5\text{V}$ ; Note 5
			1.5	Volts	$V_{DD} = +15\text{V}$
			1.5	Volts	$V_{DD} = +15\text{V}$ ; Note 5
Input Current			$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 0\text{V}$ or $V_{DD}$
			$\pm 10$	$\mu\text{A}$	Note 5 and 9
Input Capacitance					$V_{IN} = 0$ ; Note 5 and 8
Bits 1—12			5	pF	
WR, CS			20	pF	
Coding					
Unipolar		Binary			
Bipolar		Offset Binary			
<b>POWER REQUIREMENTS</b>					
Supply Current			2.0	mA	All digital inputs $V_{IL}$ or $V_{IH}$
			2.0	mA	Note 5; all digital inputs
			0.5	mA	$V_{IL}$ or $V_{IH}$
				mA	Note 18
					Note 5 and 18
<b>ENVIRONMENTAL AND MECHANICAL</b>					
Operating Temperature					
Commercial	0		+70	$^\circ\text{C}$	
Industrial	-40		+85	$^\circ\text{C}$	
Storage Temperature	-65		+150	$^\circ\text{C}$	
Package					20-pin Plastic DIP 20-pin Plastic LCC

### Notes and Cautions:

- Do not apply voltages higher than  $V_{DD}$  or less than GND potential on any terminal other than  $V_{REF}$  or  $V_{RFB}$ .
- The digital inputs are diode-clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Use proper anti-static handling procedures.
- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above these specifications is not implied. Exposure to the above maximum rated conditions for extended periods may affect device reliability.
- From  $T_{MIN}$  to  $T_{MAX}$ .
- End-point linearity.
- Differential Non-linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
- Guaranteed by design, but not production tested.
- Logic inputs are MOS gates.  $I_{IN}$  typically is less than 1nA @ 25 $^\circ\text{C}$ .
- AC performance characteristics are included for design guidance only and are subject to sample testing only.
- $R_L = 100\Omega$ ,  $C_{EXT} = 13\text{pF}$ ; all data inputs 0V to  $V_{DD}$  or  $V_{DD}$  to 0V; from 50% digital input change to 90% of final analog output.
- Settling to  $\pm 0.01\%$  FSR (strobed); all data inputs 0V to  $V_{DD}$  or  $V_{DD}$  to 0V.
- $V_{REF} = 0\text{V}$ , DAC register alternatively loaded with all 0's and all 1's.
- $V_{REF} = 20V_{P-P}$ ;  $F = 10\text{kHz}$  sinewave.
- $V_{REF} = 20V_{P-P}$ ;  $F = 1\text{kHz}$  sinewave.
- Measured using internal feedback resistor with DAC loaded with all 1's.
- All digital inputs = 0V.
- All digital inputs 0V or  $V_{DD}$ .

## ORDERING INFORMATION

Model	Integral Linearity	Package
0°C to +70°C Operating Temperature		
SP7545JCN .....	±2LSB .....	20-pin, 0.3" Plastic DIP
SP7545JCL .....	±2LSB .....	20-pin PLCC
SP7545KCN .....	±1LSB .....	20-pin, 0.3" Plastic DIP
SP7545KCL .....	±1LSB .....	20-pin PLCC
-40°C to +85°C Operating Temperature		
SP7545JIN .....	±2LSB .....	20-pin, 0.3" Plastic DIP
SP7545JIL .....	±2LSB .....	20-pin PLCC
SP7545KIN .....	±1LSB .....	20-pin, 0.3" Plastic DIP
SP7545KIL .....	±1LSB .....	20-pin PLCC