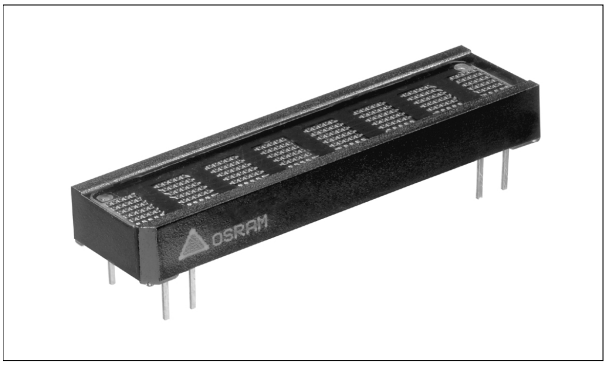
Infineon technologies

OSRAM

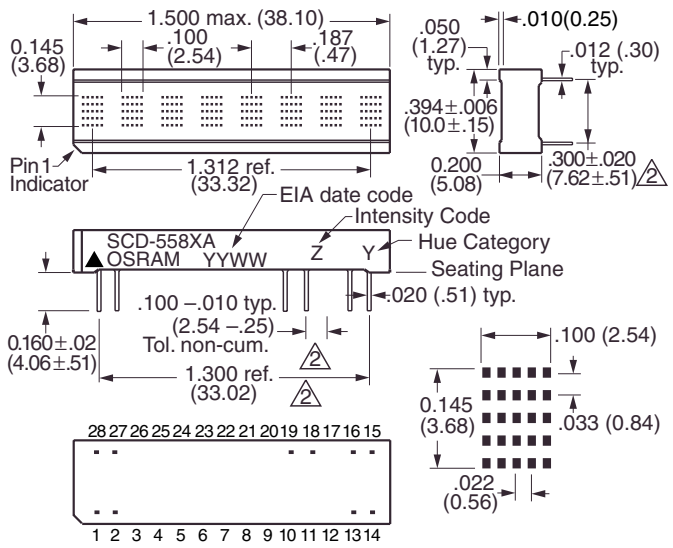
STANDARD RED SCD5580A
YELLOW SCD5581A
HIGH EFFICIENCY RED SCD5582A
GREEN SCD5583A
HIGH EFFICIENCY GREEN SCD5584A

Slimline

0.145" 8-Character 5 x 5 Dot Matrix Serial Input Dot Addressable Intelligent Display® Devices



Dimensions in inches (mm)



Notes: Unless otherwise specified
1. Tolerances .XXX ±.010(0.254)
2. Dimension at seating plane
3. Lead Dim. 0.018 wide x 0.012 thk.

FEATURES

- **Low Profile Package: 60% Smaller than Industry Standard 8-Digit Display**
- **Eight 0.145" (3.68 mm) 5 x 5 Dot Matrix Characters in Red, Yellow, High Efficiency Red, Green, or High Efficiency Green**
- **Optimum Display Surface Efficiency (display area to package ratio)**
- **Low Power—30% Less Power Dissipation than 5 x 7 Format**
- **High Speed Data Input Rate: 5.0 MHz**
- **ROMless Serial Input, Dot Addressable Display—Ideal for User Defined Characters**
- **Built-in Decoders, Multiplexers and LED Drivers**
- **Readable from 6.0 feet (1.8 meters)**
- **Wide Viewing Angle, X Axis ±55°, Y Axis ±65°**
- **Attributes:**
  - **200 Bit RAM for User Defined Characters**
  - **Eight Dimming Levels**
  - **Power Down Mode (<250 μW)**
  - **Hardware/Software Clear Function**
  - **Lamp Test**
- **Internal or External Clock**
- **End-Stackable Dual-In-Line Plastic Package**
- **3.3 V Capability**

DESCRIPTION

The SCD5580A (Red), SCD5581A (Yellow), SCD5582A (HER), SCD5583A (Green) and SCD5584A (HEG) are eight digit dot addressable 5 x 5 matrix, Serial Input, Intelligent Display devices. The eight 0.145" (3.68 mm) high digits are packaged in a transparent, 0.3" pin spacing plastic DIP.

The on-board CMOS has a 200 bit RAM, (one bit associated with one LED), to generate User Defined Characters. Due to the reduced LED count, power requirement and heat dissipation are reduced by 30%. Additionally in Power Down Mode quiescent current is <50 μA.

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OSRAM Opto Semiconductors GmbH & Co. OHG • Regensburg, Germany
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DESCRIPTION (continued)

The SCD558XA is designed to work with the Serial port of most common microprocessors. The Clock I/O (CLK I/O) and Clock Select ($\overline{\text{CLKSEL}}$) pins offer the user the capability to supply a high speed external clock. This feature can minimize audio band interference for portable communication equipment or eliminate the visual synchronization effects found in high vibration environments such as avionics equipment.

Maximum Ratings

DC Supply Voltage ..... –0.5 to +7.0 Vdc
Input Voltage Levels Relative
to Ground ..... –0.5 to V_{CC} +0.5 Vdc
Operating Temperature ..... –40°C to +85°C
Storage Temperature ..... –40°C to +100°C
Maximum Solder Temperature
0.063" below Seating Plane, t<5 s ..... 260°C
Relative Humidity at 85°C 85%
Maximum Number of LEDs on at 100% Brightness 128
IC Junction Temperature ..... 125°C
ESD (100 pF, 1.5 kΩ) ..... 2.0 kV
Max SDCLK frequency ..... 5.0 MHz

Figure 1. Data Write Cycle

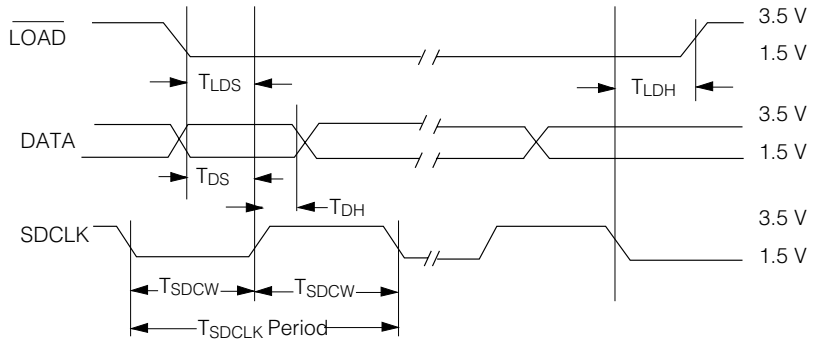

Figure 2. Instruction Cycle

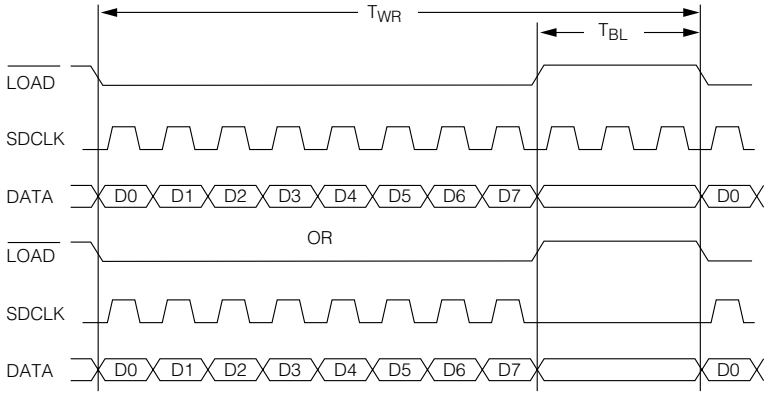

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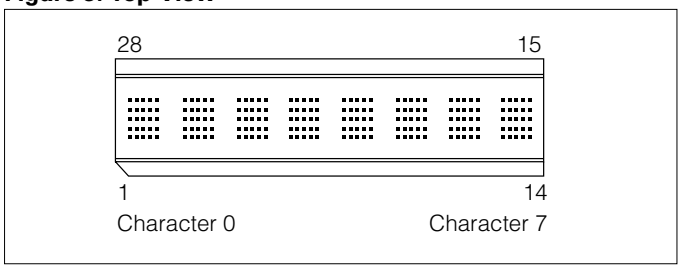
Figure 3. Top View



Electrical Characteristics at 25°C

Parameter	Min.	Typ.	Max.	Units	Conditions
V_{CC}	4.5	5.0	5.5	V	—
I_{CC} (Pwr Dwn Mode)[1][2]	—	5.0	—	µA	V_{CC}=5.0 V, all inputs=0 V or V_{CC}
I_{CC} 8 digits[3] 16 dots/character	—	200	240	mA	V_{CC}=5.0 V, "#" displayed in all 8 digits at 100% brightness at 25°C
I_{IL} Input current	—	—	–10	µA	V_{CC}=5.0 V, V_{IN}=0 (all inputs)
I_{IH} Input current	—	—	10	µA	V_{CC}=V_{IN}=5.0 V (all inputs)
V_{IH}	3.5	—	—	V	V_{CC}=4.5 V to 5.5 V
V_{IL}	—	—	1.5	V	V_{CC}=4.5 V to 5.5 V
I_{OH} (CLK I/O)	—	–8.9	—	mA	V_{CC}=4.5 V, V_{OH}=2.4 V
I_{OL} (CLK I/O)	—	1.6	—	mA	V_{CC}=4.5 V, V_{OL}=0.4 V
$\theta_{J\text{-pin}}$	—	35	—	°C/W	—
F_{ext} External Clock Input Frequency	120	—	347	kHz	V_{CC}=5.0 V, $\overline{CLKSEL}$=0
F_{osc} Internal Clock Input Frequency	120	—	347	kHz	V_{CC}=5.0 V, $\overline{CLKSEL}$=1.0
Clock I/O Bus Loading	—	—	240	pF	—
Clock Out Rise Time	—	—	500	ns	V_{CC}=4.5 V, V_{OH}=2.4 V
Clock Out Fall Time	—	—	500	ns	V_{CC}=4.5 V, V_{OH}=0.4 V
Digit Multiplex Frequency	375	768	1086	Hz	—

Notes:

1) When an external clock is used it must be stopped.
2) Unused inputs must be tied high.
3) Peak current $^5/_3$ xI_{CC}.

Input/Output Circuits

Figures 5 and 6 show the input and output resistor/diode networks used for ESD protection and to eliminate substrate latch-up caused by input voltage over/under shoot.

Figure 4. Inputs

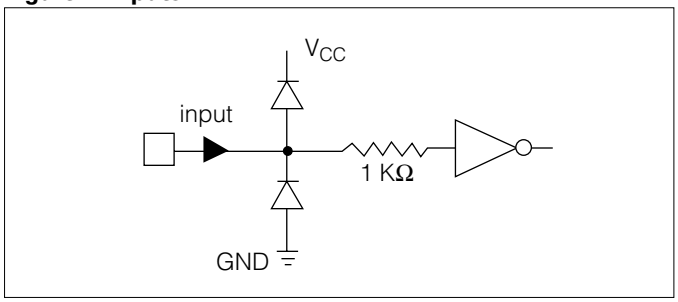
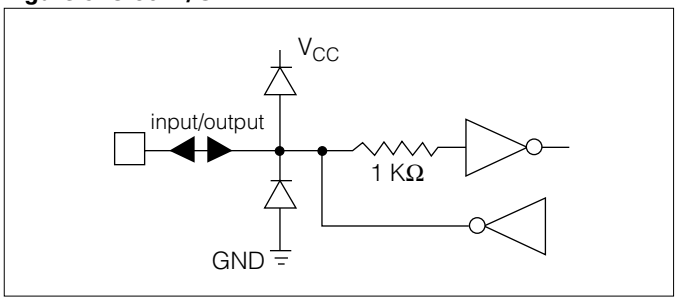


Figure 5. Clock I/O



Optical Characteristics at 25°C
(V_{CC}=5.0 V at 100% brightness level, viewing angle: X axis ±55°, Y axis ±65°)

Red SCD5580A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	36	90	µcd/dot
Peak Wavelength	λ_{peak}	—	660	nm
Dominant Wavelength	λ_{dom}	—	639	nm

Yellow SCD5581A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	124	213	µcd/dot
Peak Wavelength	λ_{peak}	—	583	nm
Dominant Wavelength	λ_{dom}	—	585	nm

High Efficiency Red SCD5582A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	124	265	µcd/dot
Peak Wavelength	λ_{peak}	—	630	nm
Dominant Wavelength	λ_{dom}	—	626	nm

Green SCD5583A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	124	221	µcd/dot
Peak Wavelength	λ_{peak}	—	565	nm
Dominant Wavelength	λ_{dom}	—	570	nm

High Efficiency Green SCD5584A

Description	Symbol	Min.	Typ.	Units
Luminous Intensity	I_V	124	505	µcd/dot
Peak Wavelength	λ_{peak}	—	568	nm
Dominant Wavelength	λ_{dom}	—	574	nm

Notes:

1. Dot to dot intensity matching at 100% brightness is 1.8:1.
2. Displays are binned for hue at 2.0 nm intervals.
3. Displays within a given intensity category have an intensity matching of 1.5:1 (max.).

Pin Assignment

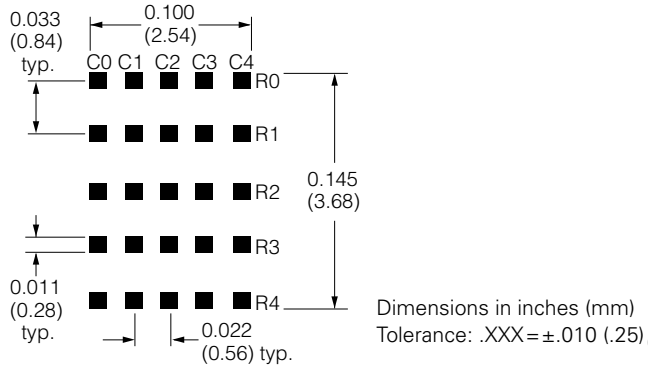
Pin	Function	Pin	Function
1	SDCLK	28	GND
2	$\overline{\text{LOAD}}$	27	DATA
3	NP	26	NP
4	NP	25	NP
5	NP	24	NP
6	NP	23	NP
7	NP	22	NP
8	NP	21	NP
9	NP	20	NP
10	NP	19	V_{CC}
11	NP	18	NC
12	NP	17	NP
13	$\overline{\text{RST}}$	16	$\overline{\text{CLKSEL}}$
14	GND	15	CLK I/O

Switching Specifications
(T_A=25°C and V_{CC}=4.5 V to 5.5 V)

Symbol	Description	Min.	Units
T_{RC}	Reset Active Time	600	ns
T_{LDS}	Load Setup Time	40	ns
T_{DS}	Data Setup Time	40	ns
T_{SDCLK}	Clock Period	200	ns
T_{SDCW}	Clock Width	70	ns
T_{LDH}	Load Hold Time	0	ns
T_{DH}	Data Hold Time	20	ns
T_{WR}	Total Write Time	2.2	µs
T_{BL}	Time Between Loads	600	ns

Note:
SDCLK duty cycle=30% Min. and 50% Max.

Figure 6. Dot Matrix Format



Pin Definitions

Pin	Function	Definitions
1	SDCLK	Loads data into the 8-bit serial data register on a low to high transition.
2	$\overline{\text{LOAD}}$	Low input enables data clocking into 8-bit serial shift register. When LOAD goes high, the contents of 8-bit serial Shift Register will be decoded.
3	NP	No pin
4	NP	No pin
5	NP	No pin
6	NP	No pin
7	NP	No pin
8	NP	No pin
9	NP	No pin
10	NP	No pin
11	NP	No pin
12	NP	No pin
13	$\overline{\text{RST}}$	Asynchronous input, when low will clear the Multiplex Counter, User RAM and Data Register. Control Word Register is set to 100% brightness and the Address Register is set to select Digit 0. The display is blanked.
14	GND	Power supply ground
15	CLK I/O	Outputs master clock or inputs external clock.
16	$\overline{\text{CLKSEL}}$	H=internal clock, L=external clock
17	NP	No pin
18	NC	No connection
19	V_{CC}	Power supply
20	NP	No pin
21	NP	No pin
22	NP	No pin
23	NP	No pin
24	NP	No pin
25	NP	No pin
26	NP	No pin
27	DATA	Serial data input
28	GND	Power supply ground

Display Column and Row Format

	C0	C1	C2	C3	C4
Row 0	1	1	1	1	1
Row 1	0	0	1	0	0
Row 2	0	0	1	0	0
Row 3	0	0	1	0	0
Row 4	0	0	1	0	0

1=Display dot "On"
0=Display dot "Off'

Column Data Ranges

Row 0	00H to 1FH
Row 1	20H to 3FH
Row 2	40H to 5FH
Row 3	60H to 7FH
Row 4	80H to 9FH

Operation of the SCD558XA

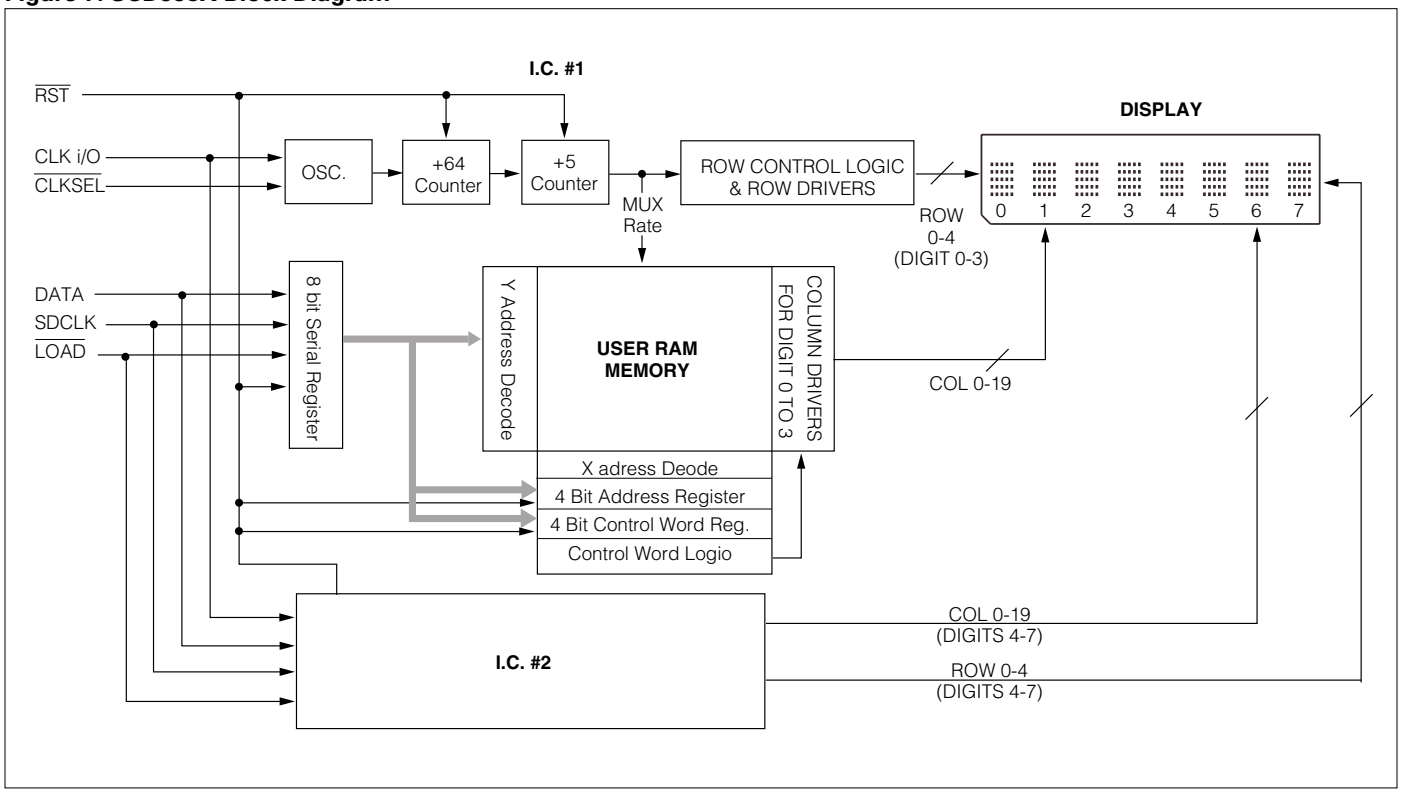
The display consists of 2 CMOS ICs containing control logic and drivers for eight 5 x 5 characters. These components are assembled in a compact (38 mm x 10 mm) plastic package.

Individual LED dot addressablity allows the user great freedom in creating special characters or mini-icons. The User Definable Character Set Examples illustrate 200 different character and symbol possibilities.

The use of a serial data interface provides a highly efficient interconnection between the display and the mother board. The SCD558XA requires only 4 lines as compared to 15 for an equivalent 8 character parallel input part.

The on-board CMOS ICs are the electronic heart of the display. The IC accepts decoded serial data, which is stored in the internal RAM. Asynchronously the RAM is read by the character multiplexer at a strobe rate that results in a flicker free display. Figure 7 shows the three functional areas of the ICs. These include: the input serial data register and control logic, a 200 bits two port RAM, and an internal multiplexer/display driver.

Figure 7. SCD558X Block Diagram



The following explains how to format the serial data to be loaded into the display. The user supplies a string of bit mapped decoded characters. The contents of this string is shown in Figure 8a. Figure 8b shows that each character consist of six 8 bit words. The first word encodes the display character location and the succeeding five bytes are row data. The row data represents the status (On, Off) of individual column LEDs. Figure 9c shows that each that each 8 bit word is formatted to include a three bit Operational Code (OPCODE) defined by bits D7–D5 and five bits (D4–D0) representing Column Data, Character Address, or Control Word Data.

Figure 8d shows the sequence for loading the bytes of data. Bringing the $\overline{\text{LOAD}}$ line low enables the serial register to accept data. The shift action occurs on the low to high transition of the serial data clock (SDCLK). The least significant bit (D0) is loaded first. After eight clock pulses the $\overline{\text{LOAD}}$ line is brought high. With this transition the OPCODE is decoded. The decoded OPCODE directs D4–D0 to be latched in the Character Address register, stored in the RAM as Column data, or latched in the Control Word register. The control IC requires a minimum 600 ns delay between successive byte loads. As indicated in Figure 8a, a total of 528 bits of data are required to load all eight characters into the display.

The Character Address Register bits, D4–D0 (Table 2), and Row Address Register bits, D7–D5 (Table 3), direct the Column Data bits, D4–D0 (Table 3) to specific RAM location. Table 1 shows the Row Address for the example character "D." Column data is written and read asynchronously from the 200 bit RAM. Once loaded the internal oscillator and character multiplexer reads the data from the RAM. These characters are row strobed with column data as shown in Figures 10 and 11. The character strobe rate is determined by the internal or user supplied external MUX Clock and the IC's ÷320 counter.

Table 1. Character "D"

	Op code D7	D6	D5	Column Data D4 C0	D3 C1	D2 C2	D1 C3	D0 C4	Hex
Row 0	0	0	0	1	1	1	1	0	1E
Row 1	0	0	1	1	0	0	0	1	31
Row 2	0	1	0	1	0	0	0	1	51
Row 3	0	1	1	1	0	0	0	1	71
Row 4	1	0	0	1	1	1	1	0	9E

Figure 8. Loading Serial Character Data

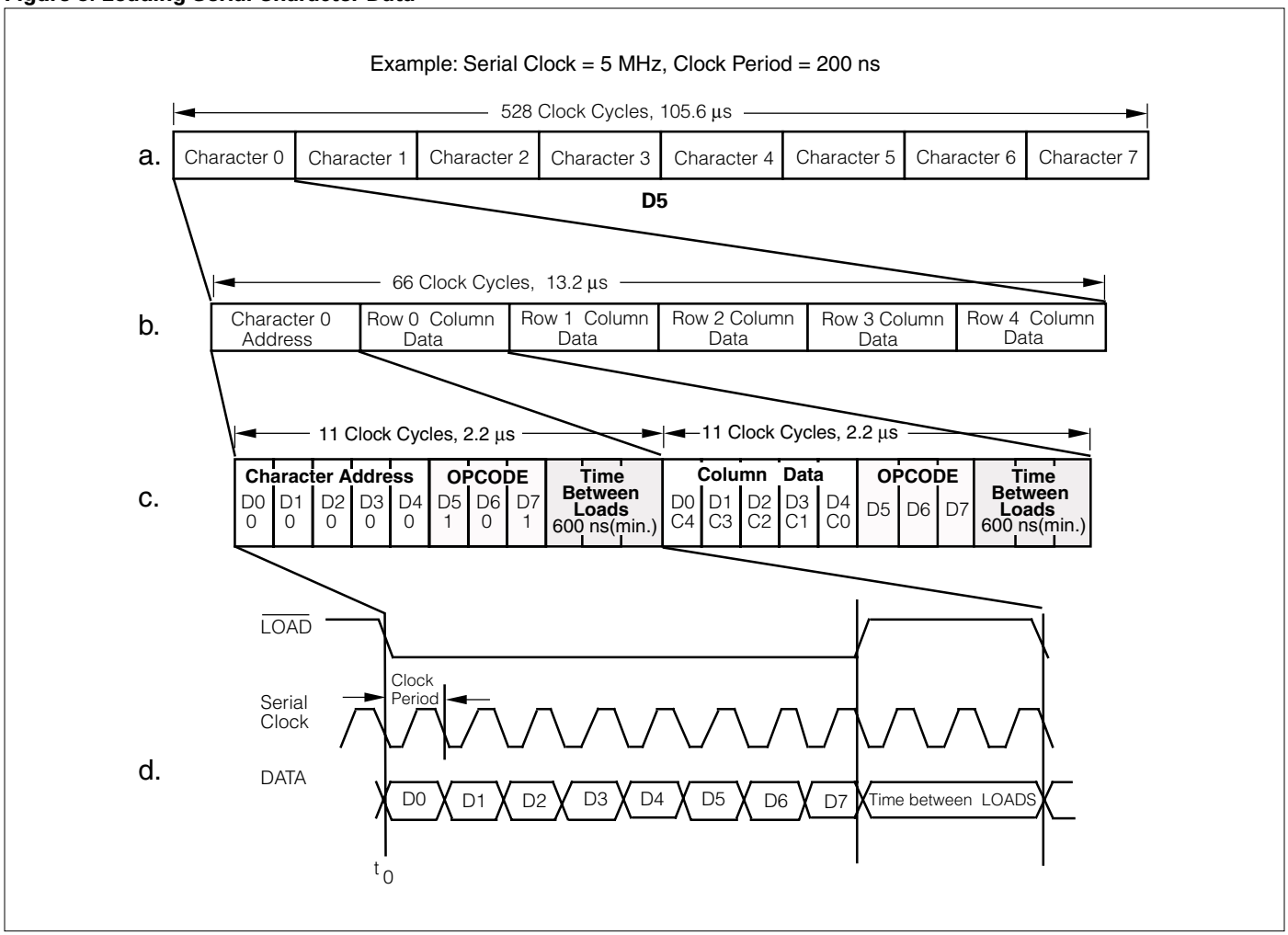


Table 2. Load Character Address

Op code D7	D6	D5	Character Address D4	D3	D2	D1	D0	Hex	Operation Load
1	0	1	0	0	0	0	0	A0	Character 0
1	0	1	0	0	0	0	1	A1	Character 1
1	0	1	0	0	0	1	0	A2	Character 2
1	0	1	0	0	0	1	1	A3	Character 3
1	0	1	0	0	1	0	0	A4	Character 4
1	0	1	0	0	1	0	1	A5	Character 5
1	0	1	0	0	1	1	0	A6	Character 6
1	0	1	0	0	1	1	1	A7	Character 7

Table 3. Load Column Data

Op code D7	D6	D5	Column Data D4	D3	D2	D1	D0	Operation Load
0	0	0	C0	C1	C2	C3	C4	Row 0
0	0	1	C0	C1	C2	C3	C4	Row 1
0	1	0	C0	C1	C2	C3	C4	Row 2
0	1	1	C0	C1	C2	C3	C4	Row 3
1	0	0	C0	C1	C2	C3	C4	Row 4

The user can activate four Control functions. These include: LED Brightness Level, Lamp Test, IC Power Down, or Display Clear. OPCODEs and five bit words are used to initiate these functions. The OPCODEs and Control Words for the Character Address and Loading Column Data are shown in Tables 2 and 3.

The user can select seven specific LED brightness levels, Table 4. These brightness levels (in percentages of full brightness of the display) include: 100% ($F0_{HEX}$), 53% ($F1_{HEX}$), 40% ($F2_{HEX}$), 27% ($F3_{HEX}$), 20% ($F4_{HEX}$), 13% ($F5_{HEX}$), and 6.6% ($F6_{HEX}$). The brightness levels are controlled by changing the duty factor of the row strobe pulse.

The SCD558XA offers a unique Display Power Down feature which reduces I_{CC} to less than 50 µA. When FF_{HEX} is loaded, as shown in Table 5, the display is set to 0% brightness and the internal multiplex clock is stopped. When in the Power Down mode data may still be written into the RAM. The display is reactivated by loading a new Brightness Level Control Word into the display.

Figure 9. Row and Column Location

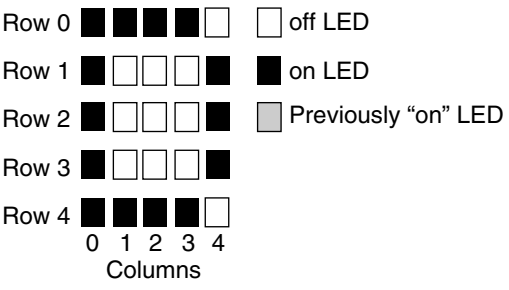


Table 4. Display Brightness

Op code D7	D6	D5	Control Word D4	D3	D2	D1	D0	Hex	Operation Level
1	1	1	1	0	0	0	0	F0	100%
1	1	1	1	0	0	0	1	F1	53%
1	1	1	1	0	0	1	0	F2	40%
1	1	1	1	0	0	1	1	F3	27%
1	1	1	1	0	1	0	0	F4	20%
1	1	1	1	0	1	0	1	F5	13%
1	1	1	1	0	1	1	0	F6	6.6%

Table 5. Power Down

Op code D7	D6	D5	Control Word D4	D3	D2	D1	D0	Hex	Operation Level
1	1	1	1	1	1	1	1	FF	0% brightness

The Lamp Test is enabled by loading $F8_{HEX}$, Table 6, into the serial shift register. This Control Word sets all of the LEDs to a 53% brightness level. Operation of the Lamp Test has no affect on the RAM and is cleared by loading a Brightness Control Word.

Table 6. Lamp Test

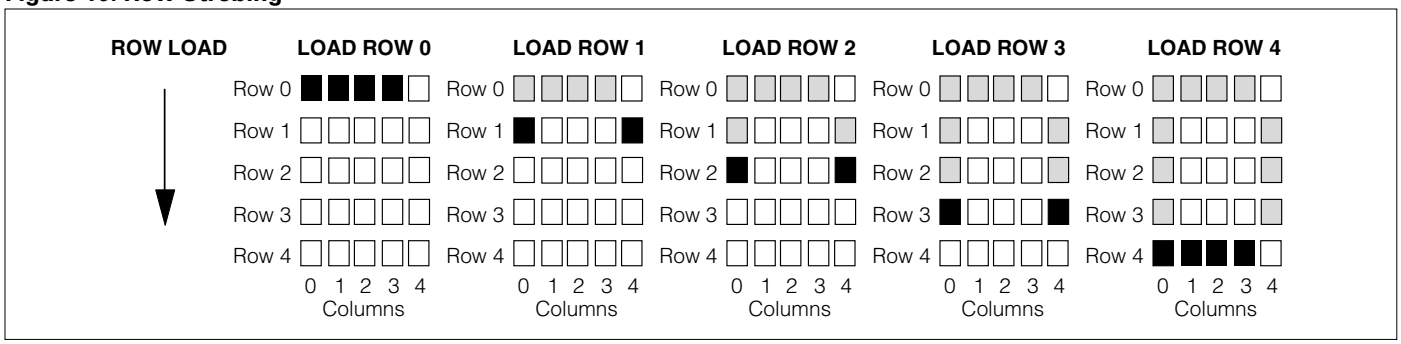
Op code D7	D6	D5	Control Word D4	D3	D2	D1	D0	Hex	Operation Level
1	1	1	1	0	B	B	B		Lamp Test (OFF)
1	1	1	1	1	0	0	0	F8	Lamp Test (ON)

The Software Clear ($C0_{HEX}$), given in Table 7, clears the Address Register and the RAM. The display is blanked and the Character Address Register will be set to Character 0. The internal counter and the Control Word Register are unaffected. The Software Clear will remain active until the next data input cycle is initiated.

Table 7. Software Clear

Op code D7	D6	D5	Control Word D4	D3	D2	D1	D0	Hex	Operation Level
1	1	0	0	0	0	0	0	C0	CLEAR

Figure 10. Row Strobing



Multiplexer and Display Driver

The eight characters are row multiplexed with RAM resident column data. The strobe rate is established by the internal or external MUX Clock rate. The MUX Clock frequency is divided by a 320 counter chain. This results in a typical strobe rate of 750 Hz. By pulling the Clock SEL line low, the display can be operated from an external MUX Clock. The external clock is attached to the CLK I/O connection (pin 15). The maximum external MUX Clock frequency should be limited to 1.0 MHz.

An asynchronous hardware Reset (pin 13) is also provided. Bringing this pin low will clear the Character Address Register, Control Word Register, RAM, and blanks the display. This action leaves the display set at Character Address 0, and the Brightness Level set at 100%.

Thermal Considerations

The SCD558XA has been designed to provide lowest thermal resistance from the CMOS to the ground pin.

The heat is then conducted through the traces on the users circuit board to free air. The max. IC operating temperature is 125°C. Maximum. IC junction temperature is calculated using the following equation:

T_J (IC) Max.=T_A+(P_D Max.) ($R\theta_{J\text{-}PIN}$+$R\theta_{PIN\text{-}A}$)

where $R\theta_{J\text{-}PIN}$=35°C/W.

P_D Max.=V_{CC} Max.x I_{CC} Max

=5.5 Vx0.240=1.32 W.

$R\theta_{PIN\text{-}A}$ will depend on ground trace thickness, whether parts are soldered to the pcb or socketed and on air circulation.

Electrical & Mechanical Considerations

Interconnect Considerations

Optimum product performance can be had when the following electrical and mechanical recommendations are adopted. The SCD558XA's ICs are constructed in a high speed CMOS process, consequently high speed noise on the SERIAL DATA, SERIAL DATA CLOCK, $\overline{\text{LOAD}}$ and $\overline{\text{RESET}}$ lines may cause incorrect data to be written into the serial shift register. Adhere to transmission line termination procedures when using fast line drivers and long cables (>10 cm).

Good digital grounds (pins 14, 28) and power supply decoupling (pins 6, 9, 20, 23) will insure that I_{CC} (<400 mA peak) switching currents do not generate localized ground bounce. Therefore it is recommended that each display package use a 0.1 µF and 20 µF capacitor between V_{CC} and ground.

When the internal MUX Clock is being used, connect the $\overline{\text{CLKSEL}}$ pin to V_{CC} and leave CLK I/O floating. In those applications where $\overline{\text{RESET}}$ will not be connected to the system's reset control, it is recommended that this pin be connected to the center node of a series 0.1, µF and 100 kΩ RC network. Thus upon initial power up the $\overline{\text{RESET}}$ will be held low for 10 ms allowing adequate time for the system power supply to stabilize.

ESD Protection

The input protection structure of the SCD558XA provides significant protection against ESD damage. It is capable of withstanding discharges greater than 2.0 kV. Take all the standard precautions, normal for CMOS components. These include properly grounding personnel, tools, tables, and transport carriers that come in contact with unshielded parts. If these conditions are not, or cannot be met, keep the leads of the device shorted together or the parts in anti-static packaging.

Soldering Considerations

The SCD558XA can be hand soldered with SN63 solder using a grounded iron set to 260°C.

Wave soldering is also possible following these conditions: Preheat that does not exceed 93°C on the solder side of the PC board or a package surface temperature of 85°C. Water soluble organic acid flux (except carboxylic acid) or rosin-based RMA flux without alcohol can be used.

Wave temperature of 245°C ±5°C with a dwell between 1.5 sec. to 3.0 sec. Exposure to the wave should not exceed temperatures above 260°C for five seconds at 0.063" below the seating plane. The packages should not be immersed in the wave.

Post Solder Cleaning Procedures

The least offensive cleaning solution is hot D.I. water (60°C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

For faster cleaning, solvents may be used. Exercise care in choosing solvents as some may chemically attack the nylon package. Maximum exposure should not exceed two minutes at elevated temperatures. Acceptable solvents are TF (trichlorotrifluorethane), TA, 111 Trichloroethane, and unheated acetone. [1]

Note:

1) Acceptable commercial solvents are: Basic TF, Arklone, P. Genesolv, D. Genesolv DA, Blaco-Tron TF, Blaco-Tron TA, and Freon TA.

Unacceptable solvents contain alcohol, methanol, methylene chloride, ethanol, TP35, TCM, TMC, TMS+, TE, or TES. Since many commercial mixtures exist, contact a solvent vendor for chemical composition information. Some major solvent manufacturers are: Allied Chemical Corporation, Specialty Chemical

Division, Morristown, NJ; Baron-Blakeslee, Chicago, IL; Dow Chemical, Midland, MI; E.I. DuPont de Nemours & Co., Wilmington, DE.

For further information refer to Appnotes 18 and 19 at www.infineon.com/opto.

An alternative to soldering and cleaning the display modules is to use sockets. Naturally, 28 pin DIP sockets .300" wide with .100" centers work well for single displays. Multiple display assemblies are best handled by longer SIP sockets or DIP sockets when available for uniform package alignment. Socket manufacturers are Aries Electronics, Inc., Frenchtown, NJ; Garry Manufacturing, New Brunswick, NJ; Robinson-Nugent, New Albany, IN; and Samtec Electronic Hardward, New Albany, IN.

For further information refer to Appnote 22 at www.infineon.com/opto.

Optical Considerations

The 0.145" high character of the SCD558XA gives readability up to eight feet. Proper filter selection enhances readability over this distance.

Using filters emphasizes the contrast ratio between a lit LED and the character background. This will increase the discrimination of different characters. The only limitation is cost. Take into consideration the ambient lighting environment for the best cost/benefit ratio for filters.

Incandescent (with almost no green) or fluorescent (with almost no red) lights do not have the flat spectral response of sunlight. Plastic band-pass filters are an inexpensive and effective way to strengthen contrast ratios. The SCD5580/2A are red/high efficiency red displays and should be matched with long wavelength pass filter in the 570 nm to 590 nm range. The SCD5583/4A should be matched with a yellow-green band-pass filter that peaks at 565 nm. For displays of multiple colors, neutral density grey filters offer the best compromise.

Additional contrast enhancement is gained by shading the displays. Plastic band-pass filters with built-in louvers offer the next step up in contrast improvement. Plastic filters can be improved further with anti-reflective coatings to reduce glare. The trade-off is fuzzy characters. Mounting the filters close to the display reduces this effect. Take care not to overheat the plastic filter by allowing for proper air flow.

Optimal filter enhancements are gained by using circular polarized, anti-reflective, band-pass filters. The circular polarizing further enhances contrast by reducing the light that travels through the filter and reflects back off the display to less than 1%.

Several filter manufacturers supply quality filter materials. Some of them are: Panelgraphic Corporation, W. Caldwell, NJ; SGL Homalite, Wilmington, DE; 3M Company, Visual Products Division, St. Paul, MN; Polaroid Corporation, Polarizer Division, Cambridge, MA; Marks Polarized Corporation, Deer Park, NY, Hoya Optics, Inc., Fremont, CA.

One last note on mounting filters: recessing displays and bezel assemblies is an inexpensive way to provide a shading effect in overhead lighting situations. Several Bezel manufacturers are: R.M.F. Products, Batavia, IL; Nobex Components, Griffith Plastic Corp., Burlingame, CA; Photo Chemical Products of California, Santa Monica, CA; I.E.E.–Atlas, Van Nuys, CA.

Microprocessor Interface

The microprocessor interface is through the serial port, SPI port or one out of eight data bits on the eight bit parallel port and also control lines $\overline{\text{SDCLK}}$ and $\overline{\text{LOAD}}$.

Power Up Sequence

Upon power up display will come on at random. Thus the display should be reset at power-up. The reset will set the Address Register to Digit 0, User RAM is set to 0 (display blank) the Control Word is set to 0 (100% brightness with Lamp Test off) and the internal counters are reset.

Figure 11. Interface with Siemens/Intel 8031 Microprocessor
(using serial port in mode 0)

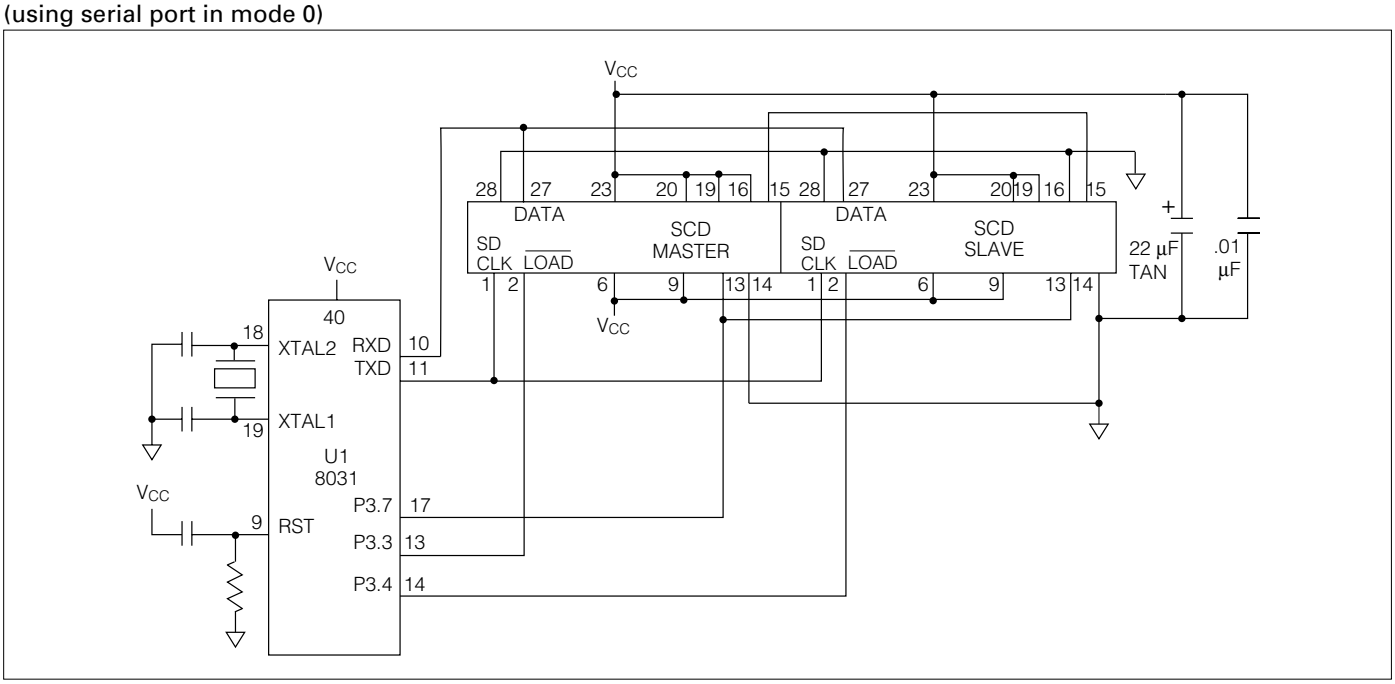


Figure 12. Interface with Siemens/Intel 8031 Microprocessor
(using one bit of parallel port as serial input)

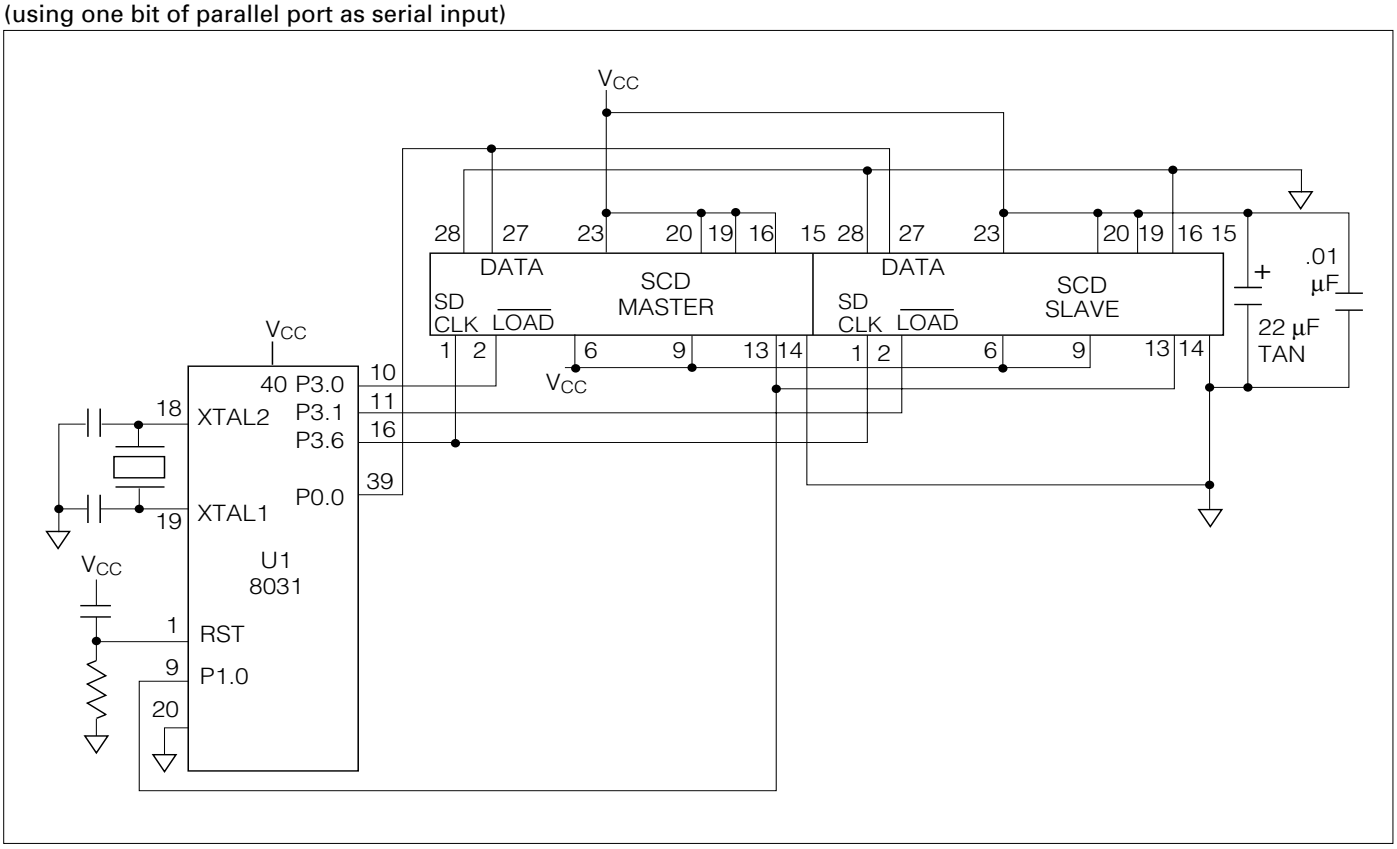
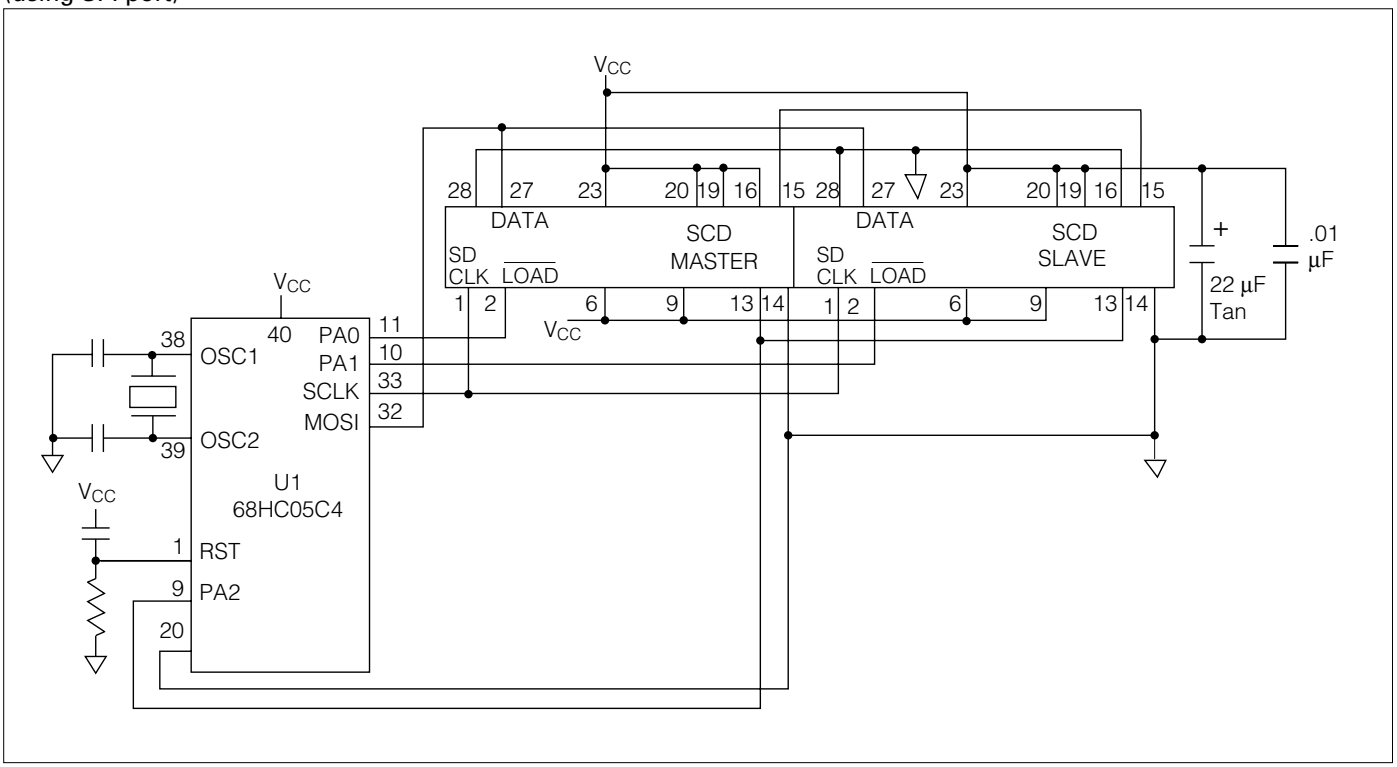


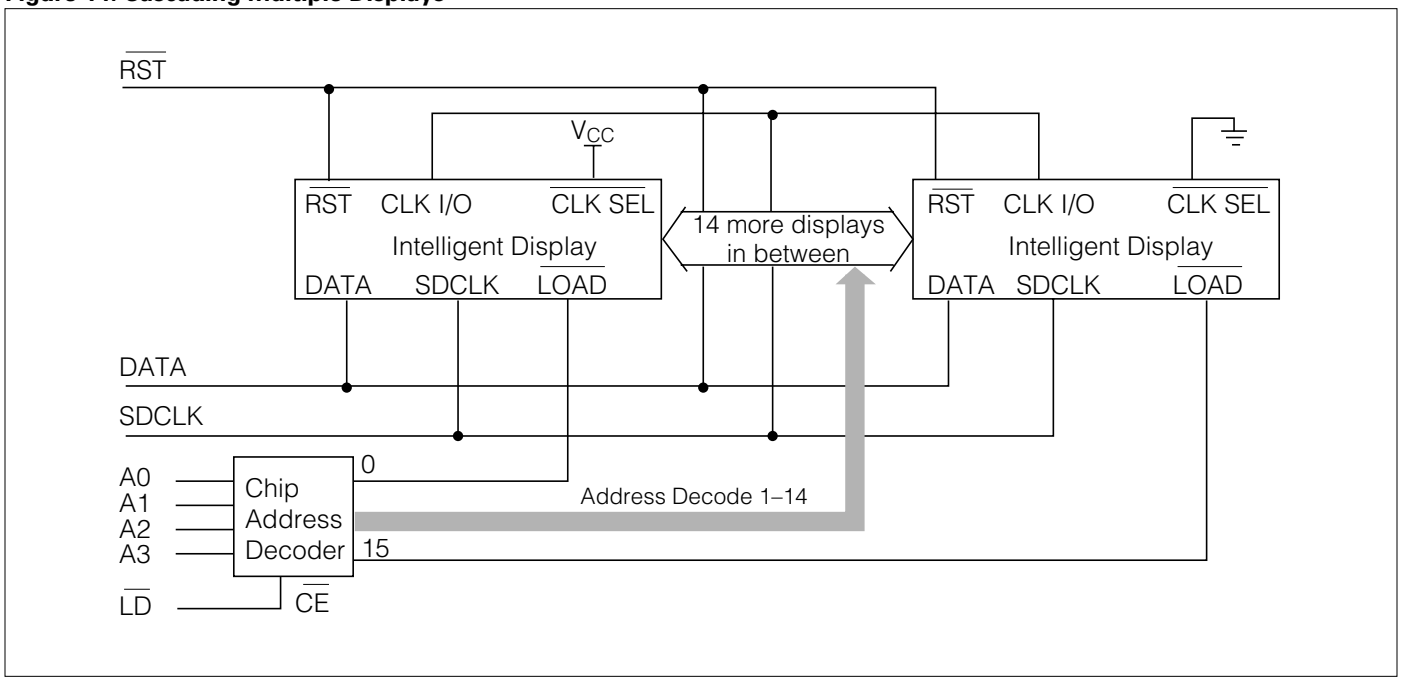
Figure 13. Interface with Motorola 68HC05C4 Microprocessor
(using SPI port)



Cascading Multiple Displays

Multiple displays can be cascaded using the $\overline{\text{CLK SEL}}$ and CLK I/O pins as shown below. The display designated as the Master Clock source should have its $\overline{\text{CLK SEL}}$ pin tied high and the slaves should have their $\overline{\text{CLK SEL}}$ pins tied low. All CLK I/O pins should be tied together. One display CLK I/O can drive 15 slave CLK I/Os. Use $\overline{\text{RST}}$ to synchronize all display counters.

Figure 14. Cascading Multiple Displays



Loading Data Into the Display

Use following procedure to load data into the display:

1. Power up the display.
2. Bring $\overline{\text{RST}}$ low (600 ns duration minimum) to clear the Multiplex Counter, Address Register, Control Word Register, User RAM and Data Register. The display will be blank. Display brightness is set to 100%.
3. If a different brightness is desired, load the proper brightness opcode into the Control Word Register.
4. Load the Digit Address into the display.
5. Load display row and column data for the selected digit.
6. Repeat steps 4 and 5 for all digits.

Data Contents for the Word "Displays"

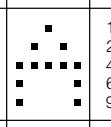
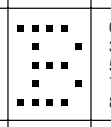
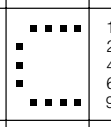
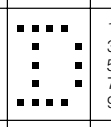
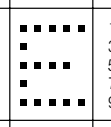
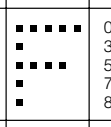
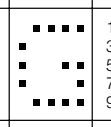
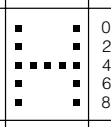
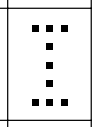
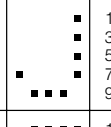
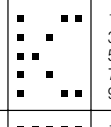
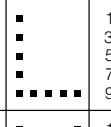
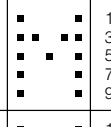
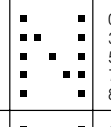
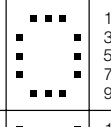
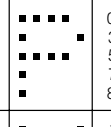
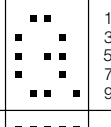
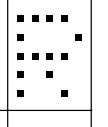
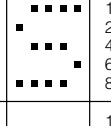
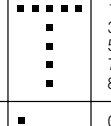
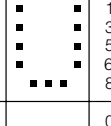
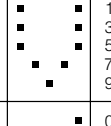
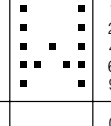
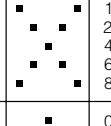
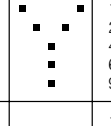
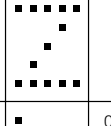
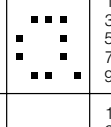
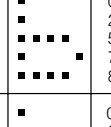
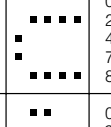
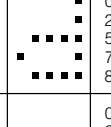
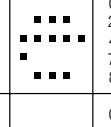
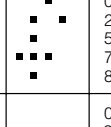
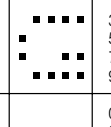
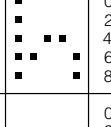
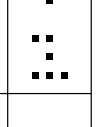
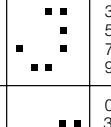
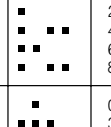
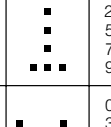
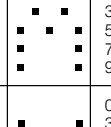
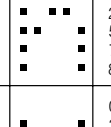
Step	D7	D6	D5	D4	D3	D2	D1	D0	Function
A	1	1	0	0	0	0	0	0	CLEAR
B (optional)	1	1	1	1	0	B	B	B	BRIGHTNESS SELECT
1	1	0	1	0	0	0	0	0	DIGIT D0 SELECT
2	0	0	0	1	1	1	1	0	ROW 0 D0 (D)
3	0	0	1	1	0	0	0	1	ROW 1 D0 (D)
4	0	1	0	1	0	0	0	1	ROW 2 D0 (D)
5	0	1	1	1	0	0	0	1	ROW 3 D0 (D)
6	1	0	0	1	1	1	1	0	ROW 4 D0 (D)
7	1	0	1	0	0	0	0	1	DIGIT D1 SELECT
8	0	0	0	0	1	1	1	0	ROW 0 D1 (I)
9	0	0	1	0	0	1	0	0	ROW 1 D1 (I)
10	0	1	0	0	0	1	0	0	ROW 2 D1 (I)
11	0	1	1	0	0	1	0	0	ROW 3 D1 (I)
12	1	0	0	0	1	1	1	0	ROW 4 D1 (I)
13	1	0	1	0	0	0	1	0	DIGIT D2 SELECT
14	0	0	0	0	1	1	1	1	ROW 0 D2 (S)
15	0	0	1	1	0	0	0	0	ROW 1 D2 (S)
16	0	1	0	0	1	1	1	0	ROW 2 D2 (S)
17	0	1	1	0	0	0	0	1	ROW 3 D2 (S)
18	1	0	0	1	1	1	1	0	ROW 4 D2 (S)
19	1	0	1	0	0	0	1	1	DIGIT D3 SELECT
20	0	0	0	1	1	1	1	0	ROW 0 D3 (P)
21	0	0	1	1	0	0	0	1	ROW 1 D3 (P)
22	0	1	0	1	1	1	1	0	ROW 2 D3 (P)
23	0	1	1	1	0	0	0	0	ROW 3 D3 (P)
24	1	0	0	1	0	0	0	0	ROW 4 D3 (P)
25	1	0	1	0	0	1	0	0	DIGIT D4 SELECT
26	0	0	0	1	0	0	0	0	ROW 0 D4 (L)
27	0	0	1	1	0	0	0	0	ROW 1 D4 (L)
28	0	1	0	1	0	0	0	0	ROW 2 D4 (L)
29	0	1	1	1	0	0	0	0	ROW 3 D4 (L)
30	1	0	0	1	1	1	1	1	ROW 4 D4 (L)
31	1	0	1	0	0	1	0	1	DIGIT D5 SELECT
32	0	0	0	0	0	1	0	0	ROW 0 D5 (A)
33	0	0	1	0	1	0	1	0	ROW 1 D5 (A)
34	0	1	0	1	1	1	1	1	ROW 2 D5 (A)
35	0	1	1	1	0	0	0	1	ROW 3 D5 (A)
36	1	0	0	1	0	0	0	1	ROW 4 D5 (A)
37	1	0	1	0	0	1	1	0	DIGIT D6 SELECT
38	0	0	0	1	0	0	0	1	ROW 0 D6 (Y)
39	0	0	1	0	1	0	1	0	ROW 1 D6 (Y)
40	0	1	0	0	0	1	0	0	ROW 2 D6 (Y)
41	0	1	1	0	0	1	0	0	ROW 3 D6 (Y)
42	1	0	0	0	0	1	0	0	ROW 4 D6 (Y)
43	1	0	1	0	0	1	1	1	DIGIT D7 SELECT
44	0	0	0	0	1	1	1	1	ROW 0 D7 (S)
45	0	0	1	1	0	0	0	0	ROW 1 D7 (S)
46	0	1	0	0	1	1	1	0	ROW 2 D7 (S)
47	0	1	1	0	0	0	0	1	ROW 3 D7 (S)
48	1	0	0	1	1	1	1	0	ROW 4 D7 (S)

Note:

If the display is already reset at Power Up, there is no need for Software Clear.

User Definable Character Set Examples*

Upper and Lower Case Alphabets

HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE	
04 2A 5F 71 91		1E 29 4E 69 9E		0F 30 50 70 8F		1E 29 49 69 9E		1F 30 5E 70 9F		1F 30 5E 70 90		0F 30 53 71 8F		11 31 5F 71 91		0E 24 44 64 8E	
01 21 41 71 8E		13 34 58 74 93		10 30 50 70 9F		11 3B 55 71 91		11 39 55 73 91		0E 31 51 71 8E		1E 31 5E 70 90		0C 32 56 72 8D		1E 31 5E 74 92	
0F 30 4E 61 9E		1F 24 44 64 84		11 31 51 71 8E		11 31 51 6A 84		11 31 55 7B 91		11 2A 44 6A 91		11 2A 44 64 84		1F 22 44 68 9F			
00 2E 52 72 8D		10 30 5E 71 9E		00 2F 50 70 8F		01 21 4F 71 8F		00 2E 5F 70 8E		04 2A 48 7C 88		00 2F 50 73 8F		10 30 56 79 91		04 20 4C 64 8E	
00 26 42 72 8C		10 30 56 78 96		0C 24 44 64 8E		00 2A 55 71 91		00 36 59 71 91		00 2E 51 71 8E		00 3E 51 7E 90		00 2F 51 6F 81		00 33 54 78 90	
00 23 44 62 8C		08 3C 48 6A 84		00 32 52 72 8D		00 31 51 6A 84		00 31 55 7B 91		00 32 4C 6C 92		00 31 4A 64 98		00 3E 44 68 9E			

DOT ON = 1
DOT OFF = 0

Numerals and Punctuation

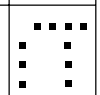
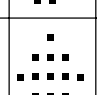
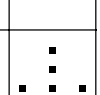
HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE	
0E 33 55 79 8E		04 2C 44 64 8E		1E 21 46 68 9F		1E 21 4E 61 9E		06 2A 5F 62 82		1F 30 5E 61 9E		06 28 5E 71 8E		1F 22 44 68 88		0E 31 4E 71 8E	
0E 31 4F 62 8C		0A 3F 4A 7F 8A		0F 34 4E 65 9E		06 29 5C 68 9F		19 3A 44 6B 93		08 34 4D 72 8D		0C 2C 44 68 80		02 24 44 64 82		08 24 44 64 88	
0C 2C 48 64 80		04 24 5F 64 84		00 2C 4C 64 88		00 20 5F 60 80		00 20 40 6C 8C		01 22 44 68 90		04 24 44 60 84		0A 2A 40 60 80		07 24 44 64 87	
10 28 44 62 81		1C 24 44 64 9C		0E 35 57 70 8E		00 20 40 60 9F		0C 2C 40 6C 8C		0C 20 4C 64 88		02 24 48 64 82		00 3F 40 7F 80		08 24 42 64 88	
0E 31 42 64 88		06 24 48 64 86		0C 24 42 64 8C		04 24 40 64 84		11 2A 44 6E 84		15 2E 5F 6E 95		04 2A 51 60 80		08 35 42 60 80			

DOT ON = 1
DOT OFF = 0

*CAUTION: No more than 128 LEDs "on" at one time at 100% brightness.

User Definable Character Set Examples* (continued)

Scientific Notations, etc.

HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE	
06 2E 5E 6E 86		04 24 48 71 8E		1F 20 59 75 93		1F 20 56 79 91		0E 20 4A 64 8A		0D 32 52 72 8D		0C 32 56 71 96		0E 24 4E 71 8E		00 24 4A 71 9F	
10 3C 52 72 81		0E 31 5F 71 8E		10 28 44 6A 91		09 29 49 6E 90		01 2E 54 64 84		04 2E 55 6E 84		0E 31 51 6A 9B		01 2E 5A 6A 8A		0F 32 52 72 8C	
1F 28 44 68 9F		18 24 48 7C 80		1C 28 44 78 80		12 36 5A 67 80		06 21 5A 67 80		07 22 59 66 80		1C 34 5C 60 80		0F 28 48 78 88		04 2E 5F 6E 80	
00 24 4E 7F 8E		00 2E 5F 6E 84		0E 3F 4E 64 80		04 3E 5F 7E 84		04 2F 5F 6F 84		0E 2E 4E 6E 8E		00 3F 5F 7F 80		04 2E 55 64 84		04 24 55 6E 84	
04 22 5F 62 84		04 28 5F 68 84		1F 31 51 71 9F		08 2C 4A 78 98		0A 35 4A 75 8A		15 2A 55 6A 95		1F 35 5F 75 9F		00 3F 5F 7C 80		0E 3F 5B 7F 8E	
00 27 4F 78 9C		00 3C 5F 63 87		00 20 40 60 83		00 20 40 67 9F		00 23 5F 7F 9F		0C 3C 5C 7C 9C		15 2E 44 64 84					

DOT ON = 1
DOT OFF = 0

Foreign Characters

HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE		HEX CODE	
1F 21 5F 62 84		1F 21 46 64 88		01 22 46 6A 82		04 3F 51 61 86		00 3F 44 64 9F		02 3F 46 6A 92		08 3F 49 6A 88		1F 21 45 67 8C		02 3F 51 62 8C	
08 3F 49 69 92		04 3F 44 7F 84		0F 29 51 62 8C		08 2F 52 62 82		0F 21 41 61 9F		0A 3F 4A 62 8C		19 21 59 62 9C		0F 29 55 63 8C		01 3E 42 7F 86	
15 35 55 62 8C		0E 20 5F 64 98		08 28 4C 6A 88		04 3F 44 64 98		0E 20 40 60 9F		1F 21 4A 64 9A		04 3E 44 6E 95		04 24 44 68 90		04 22 51 71 91	
10 3F 50 70 8F		1F 21 41 62 8C		0E 20 4E 60 8F		04 28 51 7F 81		01 21 4A 64 8A		1F 28 5F 68 87		1E 22 42 62 9F		1F 21 5F 61 9F		0E 20 5F 61 8E	
12 32 52 64 88		04 34 54 75 96		1E 25 4F 74 8F		0F 34 5F 74 97		0F 30 4F 64 98		0F 33 55 79 9E		0F 34 57 74 8F		00 2A 5F 74 8B		08 24 4E 72 8F	
0A 2E 51 7F 91		02 24 4C 64 8E		04 2A 4E 71 8E		0A 34 52 7A 96		08 24 51 71 8E		02 24 51 71 8E		04 2A 51 71 8E					

DOT ON = 1
DOT OFF = 0

*CAUTION: No more than 128 LEDs "on" at one time at 100% brightness.