NCP3520/NCP3521

LDO Regulator Controller

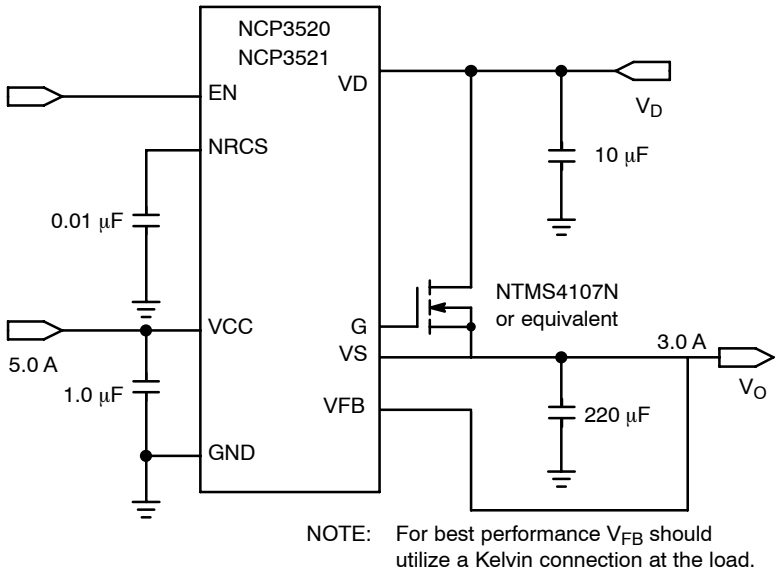
The NCP3520 / NCP3521 parts are Low Drop Out (LDO) regulator controllers for applications requiring high−currents and ultra low dropout voltages. The use of an external NMOS driver allows the user to adapt the device to a multitude of applications depending on system requirements for current and dropout voltage.

Features

- Fixed Voltage Options
  - NCP3520 (1.2 V)
  - NCP3521 (1.5 V)
- Low Operating Current
- Low Standby Current (sleep mode < 1 μA)
- Non Rush Current on Startup
- Short Circuit Protection
- 1% Output Voltage Tolerance
- Drop−In Replacement for Rohm BD3520FVM and BD3521FVM
- Functionally Equivalent to the Rohm BD3501FVM and BD3502FVM
- These are Pb−Free Devices

Typical Applications

- Computer based gaming consoles



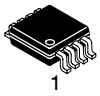
NOTE: For best performance V_{FB} should utilize a Kelvin connection at the load.

Figure 1. Application Diagram

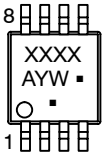
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



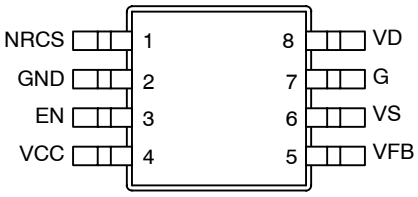
Micro8
DM SUFFIX
CASE 846A
STYLE 2



XXXX = 3520 for Fixed 1.2 V or
= 3521 for Fixed 1.5 V
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



Micro8
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

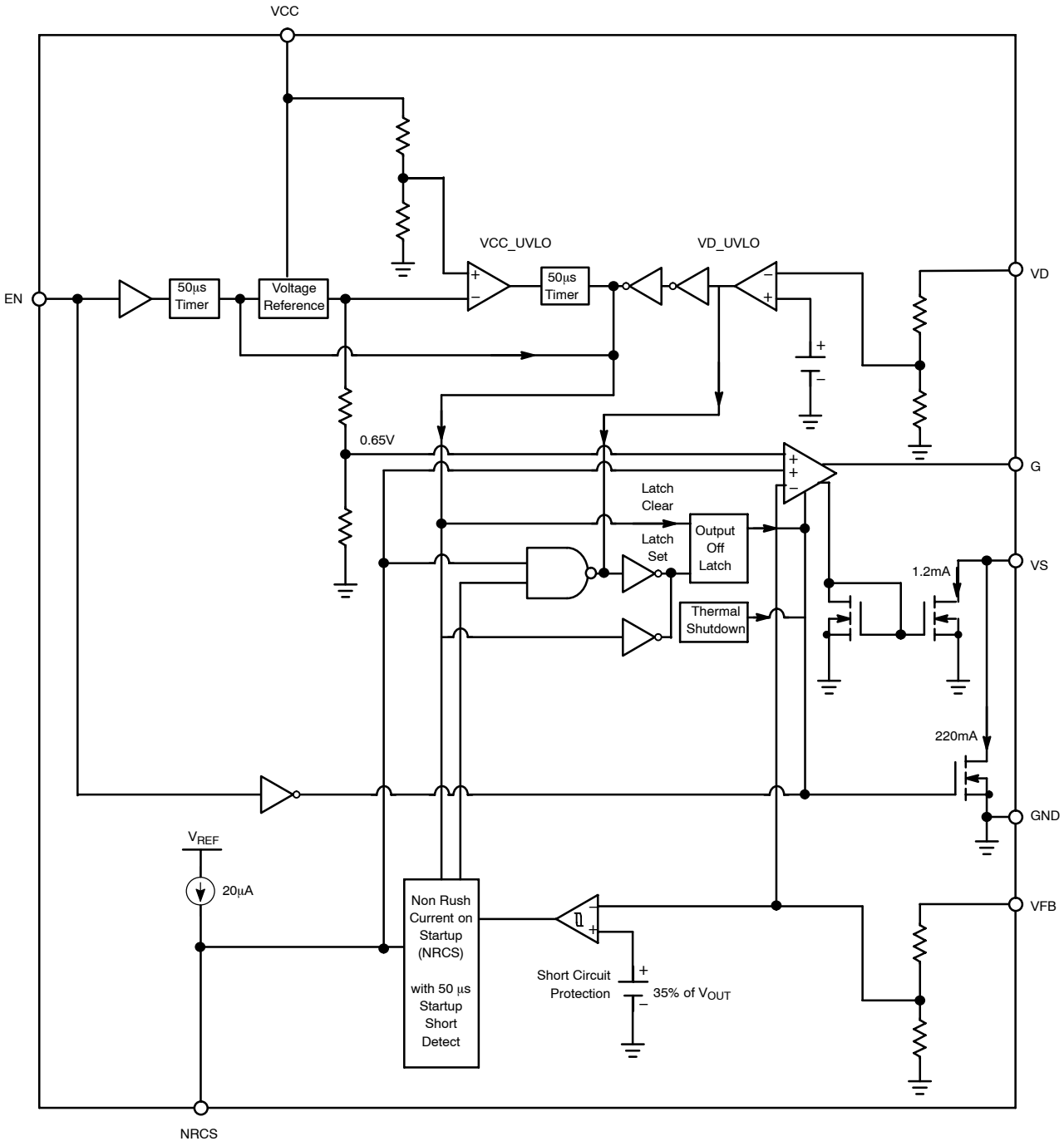


Figure 2. Block Diagram

PACKAGE PIN DESCRIPTION Micro8

Pin #	Symbol	Description
1	NRCS	Non Rush current on Startup. Capacitor to ground controls output voltage slew rate and short circuit delay time.
2	GND	Ground.
3	EN	Enable input control.
4	VCC	Power Supply Voltage Input.
5	VFB	Voltage Feedback pin into the error amplifier for maintaining the output voltage.
6	VS	Source input. Provides pulldown capability (1.2 mA operating & 220 mA turnoff) for fast output voltage response time.
7	G	Gate Drive for the external NFET.
8	VD	NFET Drain input for voltage sensing.

MAXIMUM RATINGS

Rating	Value	Unit
All Pins	−0.3 to 7	V
IG (DC) IG (AC) IVS (DC)	10 10 300	mA
Electrostatic Discharge, Human Body Model	1.5	kV
Electrostatic Discharge, Machine Model	100	V
Package Thermal Resistance Micro8	 238	 °C/W
Operating Junction Temperature	−10 to 150	°C
Storage Temperature Range	−55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 5 V, V_D = 2.0 V, EN = 3 V, External FET = NTMS4107N (Note 3), unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
REGULATOR OUTPUT					
Feedback Voltage (NCP3520)	I_O (NTMS4107N) = 50 mA 4.5 V < V_{CC} < 5.5 V, 0°C < T_J < 100°C (Note 1)	1.188 1.176	1.200 1.200	1.212 1.224	V V
Feedback Voltage (NCP3521)	I_O (NTMS4107N) = 50 mA 4.5 V < V_{CC} < 5.5V, 0°C < T_J < 100°C (Note 1)	1.485 1.470	1.500 1.500	1.515 1.530	V V
Supply Current Sleep Mode Run Mode Short Circuit Latch Condition	 EN = 0 V EN = 3 V EN = 3 V	 – – –	 0 1.25 0.5	 10 1.7 1.7	 μA mA mA
Line Regulation (NCP3520)	4.5 V < V_{CC} < 5.5 V, I_{OUT} = 0 4.5 V < V_{CC} < 5.5 V, I_{OUT} = 3 A (Note 1)	–	1.2 1.2	6.0 6.0	mV mV
Line Regulation (NCP3521)	4.5 V < V_{CC} < 5.5 V, I_{OUT} = 0 4.5 V < V_{CC} < 5.5 V, I_{OUT} = 3 A (Note 1)	–	1.5 1.5	7.5 7.5	mV mV
Load Regulation (Note 2)	I_O = 0 A to 3 A	–	0.50	10	mV

1. Guaranteed by Design
2. Load regulation may vary with the selection of an external FET other than the NTMS4107N.
3. See “External Components” section on Page 8.

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 5 V, V_D = 2.0 V, EN = 3 V, External FET = NTMS4107N (Note 3), unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
OUTPUT DRIVER					
Source Current	V_{FB} = V_{OUT} − 0.1 V, V_{GATE} = 2.5 V	−4	−3	−2	mA
Sink Current	V_{FB} = V_{OUT} + 0.1 V, V_{GATE} = 2.5 V	2	3	4	mA
GENERAL					
V_{FB} Input Impedance NCP3520 (1.2 V) NCP3521 (1.5 V)		 – –	 21 26	 – –	kΩ
V_S Input Bias Current		–	1.2	2.4	mA
V_S Standby Current	V_S = 1 V, EN = 0 V	150	220	–	mA
V_{CC} Undervoltage Lockout	V_{CC} Rising	4.20	4.35	4.50	V
V_{CC} Undervoltage Lockout Hysteresis		100	160	250	mV
V_D Undervoltage Lockout (NCP3520)		0.72	0.84	0.96	V
V_D Undervoltage Lockout (NCP3521)		0.90	1.05	1.20	V
V_D Input Impedance NCP3520 (1.2 V) NCP3521 (1.5 V)		 – –	 228 284	 – –	kΩ
Thermal Shutdown (Note 1)		150	180	210	°C
Thermal Hysteresis (Note 1)		–	15	–	°C
NON RUSH CURRENT ON STARTUP (NRCS) SHORT CIRCUIT PROTECTION (SCP)					
NRCS Charge Current	NRCS = 0.5 V	14	20	26	μA
SCP Charge Current	NRCS = 0.5 V	14	20	26	μA
SCP Discharge Current	NRCS = 0.5 V	300	400	–	μA
SCP Threshold Voltage		1.15	1.3	1.4	V
Short Detect Voltage	V_{FB} Decreasing	V_{FB} * 0.30	V_{FB} * 0.35	V_{FB} * 0.40	V
Power On Reset V_{CC}		–	50	–	μS
EN to G Turn on Delay		–	50	–	μS
Short Circuit Powerup Decision Timer		–	50	–	μS
NRCS Standby Voltage		–	25	50	mV
ENABLE					
Input Threshold Low High		 – 2.0	 1.34 1.40	 0.8 –	 V V
Input Hysteresis		–	60	–	mV
Input Current	EN = 3 V	–	7	10	μA

1. Guaranteed by Design
2. Load regulation may vary with the selection of an external FET other than the NTMS4107N.
3. See “External Components” section on Page 8.

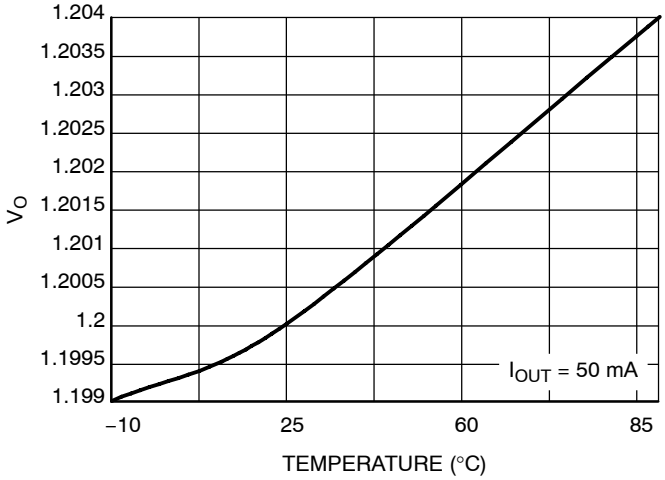


Figure 3. 1.2 V Output Voltage versus Temperature (NCP3520)

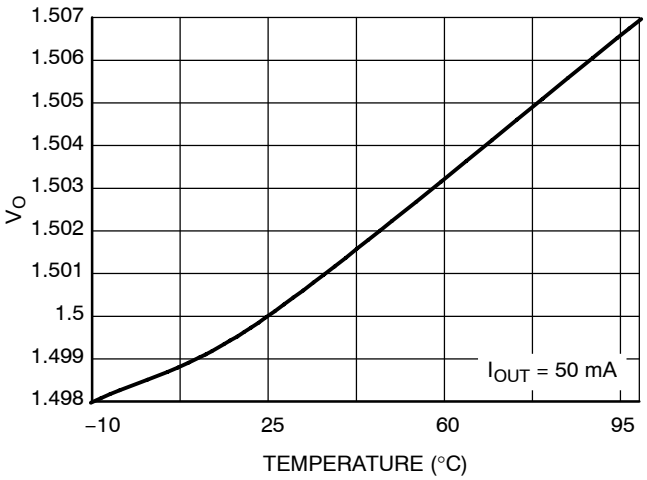


Figure 4. 1.5 V Output Voltage versus Temperature (NCP3521)

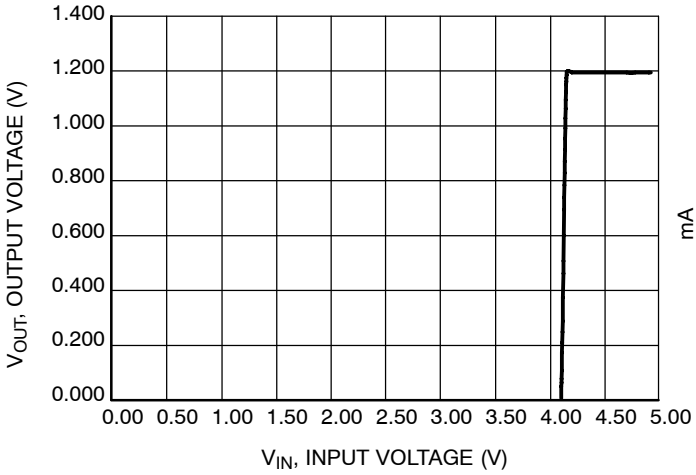


Figure 5. Output Voltage versus Input Voltage (NCP3520)

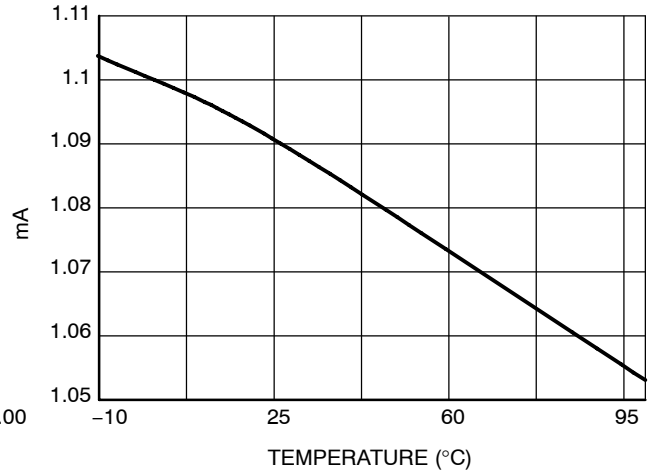


Figure 6. Run Mode Supply Current versus Temperature

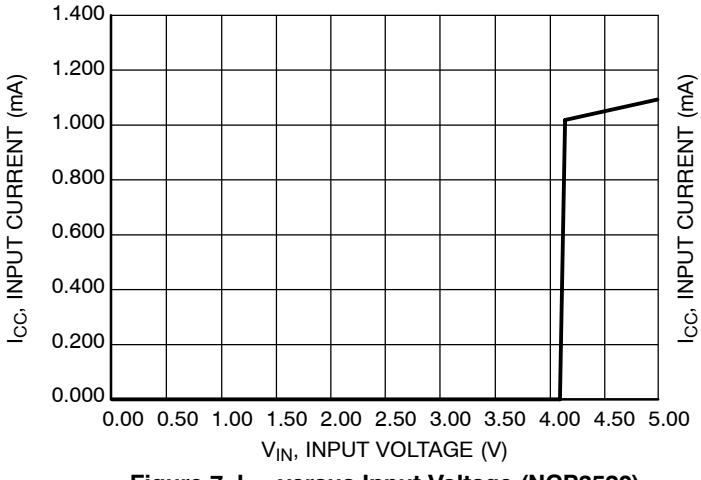


Figure 7. I_{CC} versus Input Voltage (NCP3520)

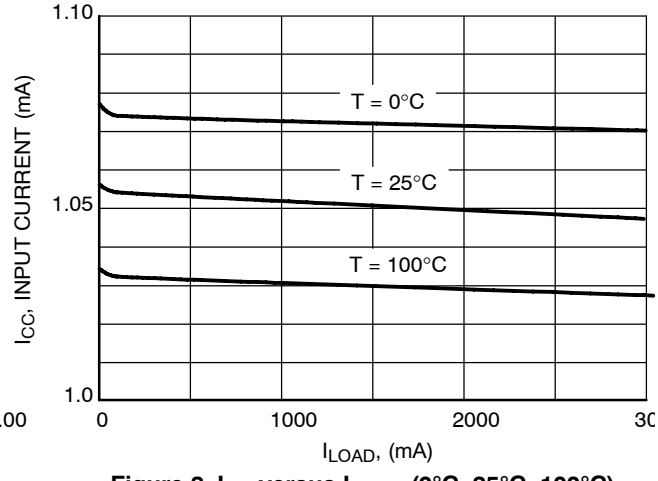


Figure 8. I_{CC} versus I_{LOAD} (0°C, 25°C, 100°C)

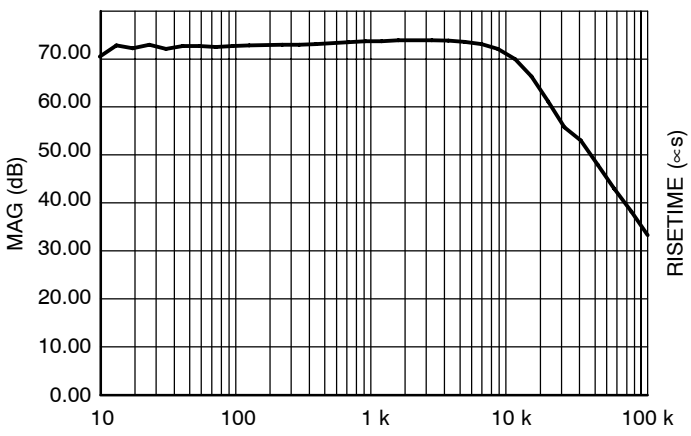


Figure 9. Ripple Rejection versus Frequency (V_{CC} = 5.0 V, I_{LOAD} = 3.0 A)

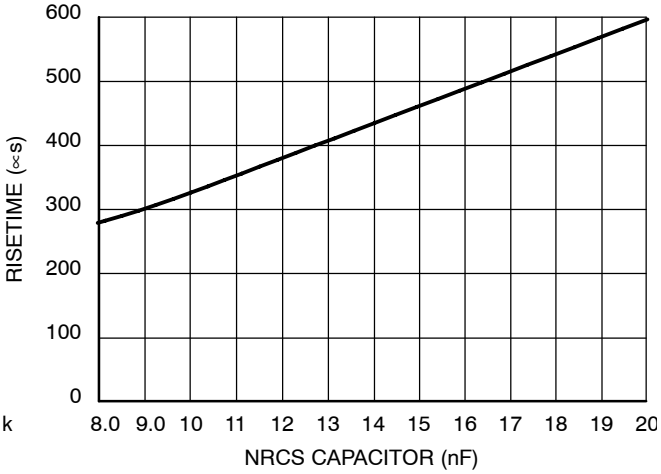


Figure 10. NRCS Time versus NRCS Capacitor (NCP3520)

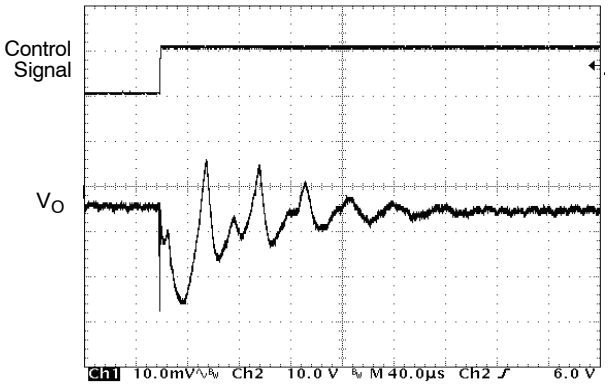


Figure 11. Load Transient Response (10 mA to 1.3 A) Channel 1 (V_O), Channel 2 (Switch Control)

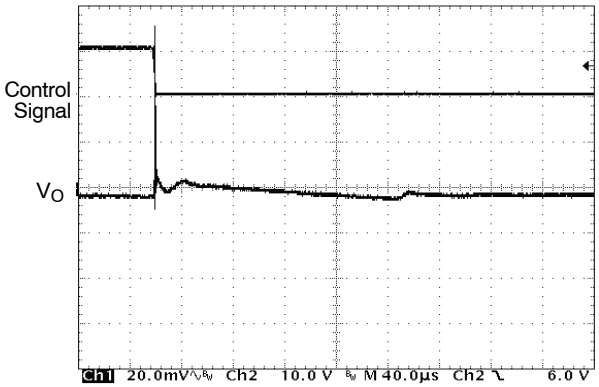


Figure 12. Load Transient Response (1.3 A to 10 mA) Channel 1 (V_O), Channel 2 (Switch Control)

DETAILED OPERATING DESCRIPTION

General

The NCP3520/NCP3521 are LDO Regulator Controllers. An external NFET device sets the current capability allowing for designer selection.

Features include an undervoltage lockout for both the integrated circuit supply Pin VCC, and the supply pin for the external FET connection to the drain of the FET.

The NRCS (Non Rush Current on Startup) feature prevents high currents through the external FET (drain−source). The external capacitor setting component used in NRCS is also used for short circuit protection (SCP).

The device also has an enable feature allowing it to go into a low supply current sleep mode demanded by most modern day feature rich systems when not in use.

Thermal shutdown functionality protects the IC from damage caused from excessively high temperatures appearing on the IC.

Output Driver

Output current drive capability is determined by the designer's choice of external MOSFET (NFET). Power dissipated in the driver can be controlled by the voltage applied to V_D. V_D should be kept low to minimize power dissipation and high enough to support regulated operation at the desired output current. It should also be noted the output capacitor (V_O to GND) value supports regulation during high speed transient events until the system loop can respond to any voltage dips to drive the external FET.

High Speed Control

Unlike most linear regulators whose reaction to overvoltage events is to turn off the upper driver and let the external load and resistor feedback network quench the incident, the NCP3520/21 include a 1.2 mA pulldown through the VS Pin. This keeps overshoot to a minimum during powerup. During turn−off and thermal overload, the pulldown current is increased from 1.2 mA to 220 mA to provide an even faster turn−off time.

Power On Reset

A 50 μs power on reset circuit is built into the IC acting as a digital filter and performing housekeeping activity during a short circuit event.

The timer effects three areas of operation.

1. EN turn on delay. Upon detection of an EN high, there is a 50 μs delay to when the internal circuitry turns on and the gate pin (G) goes high. A low on EN resets the timer.
2. V_{CC} startup delay. If V_{CC} drops out below the undervoltage lockout voltage and restored above its hysteresis value, a 50 μs time is also observed from reinitiation of V_{CC} and G going high. This is recognized to be different from the EN turn on delay by the active circuitry of the voltage reference, NRCS circuitry, and V_S high current pulldown.
3. Device startup into a short circuit. Further details are available on this subject under the heading "Starting Up Into A Short Circuit".

Normal Powerup/Down

The NRCS (Non Rush Current on Startup) timer controls the output driver during powerup. The output driver voltage (V_G) is controlled during powerup. The voltage on NRCS is mimicked to provide a duplicate voltage on VFB. When 1.2 V is reached normal operation of the error amplifier and feedback network take over. Regulation is maintained in the loop around 1.2 V. The NRCS pin rises up to 1 V. At 1 V, the NRCS capacitor is discharged fully at a 300 μA (min) rate. The IC enters a standby mode capable of short circuit detection.

A 20 μA pullup current source is used to charge the external NRCS capacitor linearly and maintain a predictable powerup. A recommended 0.01 μF will provide a 325 μs powerup time. Alternative times can be programmed with this equation:

$$T = C(NRCS) * V_{FB} / INRCS \qquad \text{(eq. 1)}$$

Rush current during startup can be calculated by $I = C_{OUT} * V_O / T$.

The NRCS circuit is not active during powerdown. Normal circuit operation will be maintained unless VCC_UVLO or VD_UVLO cause the gate drive output to turn off.

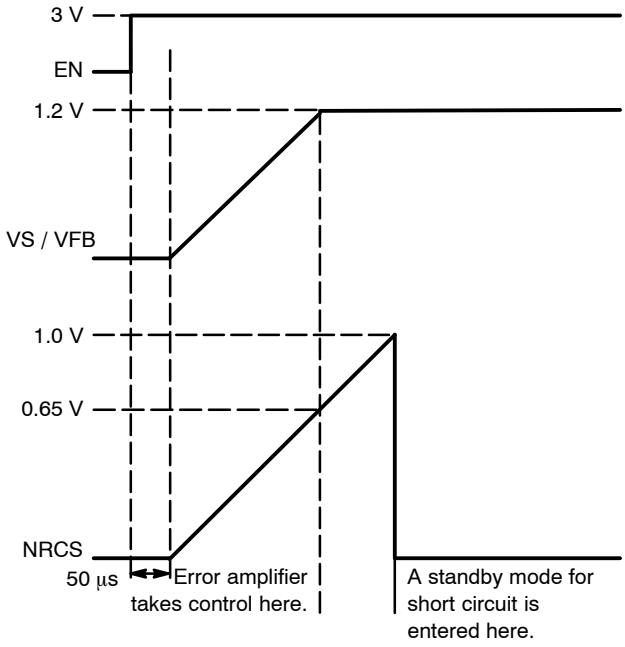


Figure 13. Powerup (NCP3520 (1.2 V) Version Shown)

Short Circuit Protection (SCP)

The IC enters normal mode after the NRCS has gone through powerup. The NRCS capacitor has reached a 1 V (typ) threshold and fully discharged (50 mV (max)).

When a short circuit event occurs it is detected when the voltage on V_{FB} goes below (35% of V_{OUT}). This triggers the NRCS current source to start charging the NRCS capacitor at the same 20 μA rate as during powerup. When the voltage on the capacitor reaches 1.3 V a short circuit event is confirmed, V_G goes low turning off the external FET. V_S Standby Current pulldown is enabled.

Clearing a Short Circuit Latch Condition

A short circuit latch condition can be cleared by toggling the EN from its high condition to a low condition, and then back to a high condition.

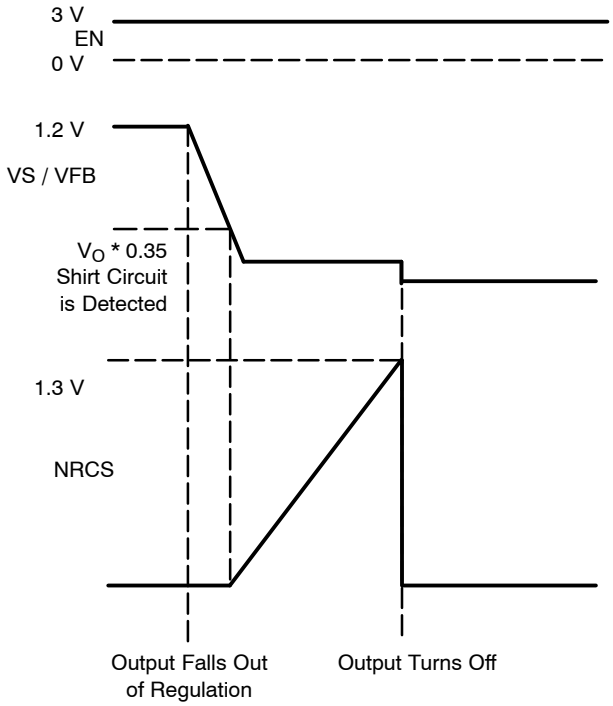


Figure 14. Short Circuit (NCP3520 (1.2 V) Version Shown)

Starting Up Into a Short Circuit

If the NCP3520/NCP3521 turns on and has not gone into a normal mode of operation, additional time has been added to the NRCS to ignore potential false short circuit confirmation during in−rush current events. This time is independent of the external capacitor value and is typically 50 μs. The voltage on NRCS operates as a normal condition until it reaches 1 V. The current source charging NRCS turns off for 50 μs disallowing the voltage to rise on NRCS. After 50 μs the current source turns back on and continues to charge the NRCS capacitor. Once 1.3 V is reached, the circuit operates as during a typical short circuit event.

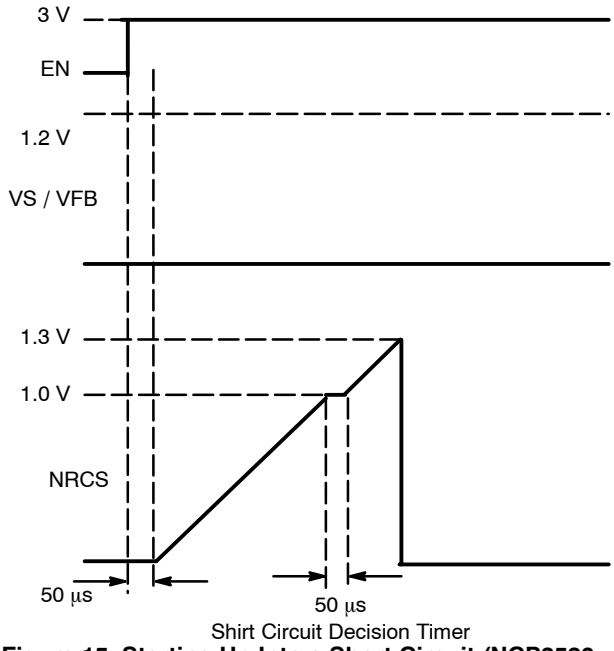


Figure 15. Starting Up Into a Short Circuit (NCP3520 (1.2 V) Version Shown)

Undervoltage Lockout

V_{CC} and V_D detection is provided in conjunction with the EN input pin. When all three conditions are met (V_{CC} is up, V_D is up, and EN is high), the Non Rush Current on Startup (NRCS) circuitry is allowed to start. Any one of the three conditions failing will not allow the device to turn on.

The V_{CC} undervoltage threshold is 4.35 V and the V_D threshold is V_O * 0.7.

Enable

The Enable function is controlled by the logic pin EN. The threshold of this pin is set to TTL logic levels. TTL logic levels are 0.8 V (low) and 2.0 V (high). A low on the EN pin puts the device is a low current sleep mode consuming less than 10 μA (I_{VCC}). A device going from normal operation to sleep will 1st go through a discharge mode maintaining a discharge current of 220 mA on V_S (measured @ V_S = 1 V). This pin has 60 mV (typ) of hysteresis to guarantee a clean switching threshold.

External Components

A capacitor between V_O and ground is required for stability. A 220 μF value capacitor such as the SANYO 2R5TPE220MF is recommended. The SANYO 2R5TPE220MF capacitor has a 15 mΩ maximum specification. Contact resistance and board trace resistance are the significant contributors to output capacitor ESR below 10 mΩ.

As ON Semiconductor's NCP352X family of LDO controllers may be considered as an alternative to Rohm's family of LDO controllers, alternative FETs such as industry compatible parts like the Si4866DY may also be used in conjunction with ON Semiconductor's controller.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold, a Thermal Shutdown (TSD) event is detected and V_G is turned off. The IC will remain in this state until the die temperature moves below the shutdown threshold (180°C typical) minus the hysteresis factor (15°C typical). The output will then go through a soft startup using the NRCS circuitry.

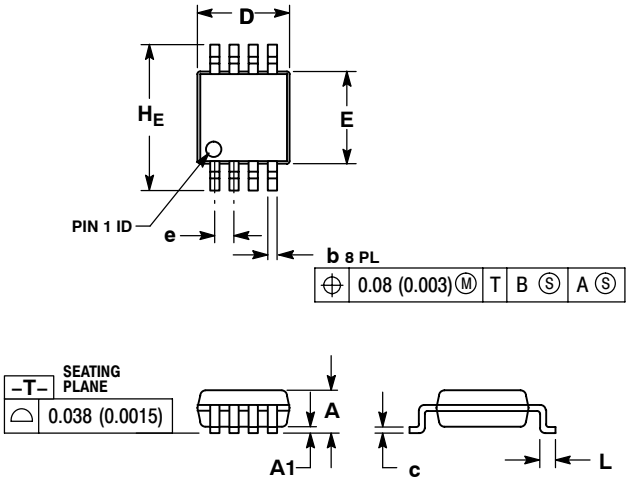
ORDERING INFORMATION

Device	Package	Shipping†
NCP3520DMR2G	Micro8 (Pb−Free)	4000 / Tape & Reel
NCP3521DMR2G	Micro8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

Micro8™
CASE 846A–02
ISSUE G

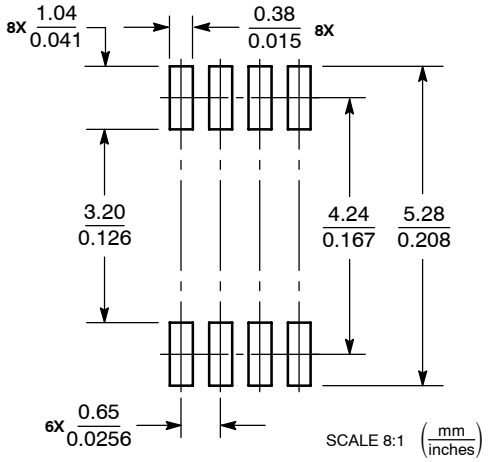


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A–01 OBSOLETE, NEW STANDARD 846A–02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	––	––	1.10	––	––	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5773–3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative