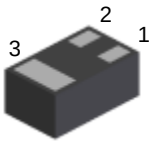
DDTA144ELP

PRE-BIASED (R1=R2) SMALL SIGNALSURFACE MOUNT 100mA PNP TRANSISTOR

NEW PRODUCT

Features

- Epitaxial Planar Die Construction
- Ultra-Small Leadless Surface Mount Package
- Ideally Suited for Automated Assembly Processes
- **Lead Free By Design/RoHS Compliant (Note 1)**
- **"Green" Device (Note 2)**



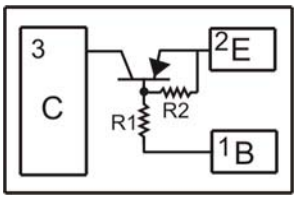
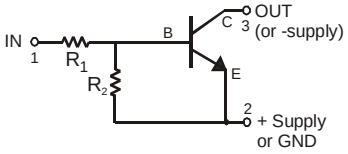


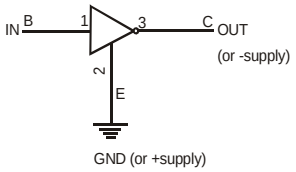
Fig. 1

Mechanical Data

- Case: DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminal Connections: Collector Dot (See Diagram)
- Terminals: Finish — NiPdAu annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Marking Code P2, Dot denotes Collector Side
- Ordering Information: See Page 4
- Weight: 0.001 grams (approximate)



Schematic and Pin Configuration



Equivalent Inverter Circuit

Fig. 2

Component P/N	R1(NOM)	R2(NOM)	Figure
DDTA144ELP	47K	47K	2

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	-50	V
Input Voltage	V_{IN}	+10 to -40	V
Output Current (I_o)	$I_{C(max)}$	-100	mA
Power Dissipation (Note 3)	P_d	250	mW
Power Deration above 25°C	P_{der}	2	mW/°C

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Junction Operation and Storage Temperature Range	T_j, T_{stg}	-55 to +150	°C
Thermal Resistance, Junction to Ambient Air (Note 3) (Equivalent to one heated junction of NPN)	$R_{\theta JA}$	400	°C/W

Notes:
1. No purposefully added lead.
2. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
3. Device mounted on FR-4 PCB, 1" x 0.85" x 0.062"; pad layout as shown on page 5 or Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

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Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Off Characteristics (Note 4)						
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	-50	—	—	V	I_C = -10μA, I_E = 0
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	-50	—	—	V	I_C = -1.0mA, I_B = 0
Emitter-Base Breakdown Voltage*	$V_{(BR)EBO}$	-4.5	—	—	V	I_E = -50μA, I_C = 0
Collector Cutoff Current*	I_{CEX}	—	—	-0.5	μA	V_{CE} = -50V, $V_{EB(OFF)}$ = 3.0V
Base Cutoff Current (I_{BEX})	I_{BL}	—	—	-0.5	μA	V_{CE} = -50V, $V_{EB(OFF)}$ = 3.0V
Collector-Base Cut Off Current	I_{CBO}	—	—	-0.5	μA	V_{CB} = -50V, I_E = 0
Collector-Emitter Cut Off Current, $I_{O(OFF)}$	I_{CEO}	—	—	-0.5	μA	V_{CE} = -50V, I_B = 0
Emitter-Base Cut Off Current	I_{EBO}	—	—	-0.5	mA	V_{EB} = 4V, I_C = 0
Input Off Voltage	$V_{I(OFF)}$	—	—	-0.3	V	V_{CC} = -5V, I_O = -100uA
On Characteristics (Note 4)						
Base-Emitter Turn-On Voltage*	$V_{BE(ON)}$	—	—	-0.69	V	V_{CE} = -5V, I_C = -2mA
		—	—	-0.78	V	V_{CE} = -5V, I_C = -10mA
Base-Emitter Saturation Voltage*	$V_{BE(SAT)}$	—	—	-0.88	V	I_C = -10mA, I_B = -1mA, V_{CE} = -5V
		—	—	-0.98	V	I_C = -50mA, I_B = -5mA, V_{CE} = -5V
Input-On Voltage	$V_{I(ON)}$	-3	—	—	V	V_O = -0.3V, I_O = -20mA
Input Current	I_I	—	—	-7.2	mA	V_I = -5V
DC Current Gain	h_{FE}	90	—	—	—	V_{CE} =-5V, I_C = -2mA
		120	—	—	—	V_{CE} = -5V, I_C = -5mA
		150	—	—	—	V_{CE} = -5V, I_C = -10mA
		100	—	—	—	V_{CE} = -5V, I_C = -100mA
		180	—	—	—	V_{CE} = -5V, I_C = -200mA
		250	—	—	—	V_{CE} = -5V, I_C = -300mA
Collector-Emitter Saturation Voltage*	$V_{CE(SAT)}$	—	—	-0.15	V	I_B = -1mA, I_C = -10mA
		—	—	-0.85	V	I_B = -5mA, I_C = -50mA
Output On Voltage (Same as $V_{CE(SAT)}$)	$V_{O(ON)}$	—	—	-0.3	V	I_I = -0.5mA, I_O = -50mA
Input Resistance	R1	1.54	2.2	2.86	KΩ	—
Resistance Ratio	(R2/R1)	17	21	26	—	—
Small Signal Characteristics						
Current Gain-Bandwidth Product	f_T	—	250	—	MHz	V_{CE} = -10V, I_E = -5mA, f = 100 MHz

* Guaranteed by design.

Notes: 4. Short duration test pulse used to minimize self-heating effect.
Pulse Test: Pulse width tp<300 uS, Duty Cycle, d<=2%.

Typical Characteristics

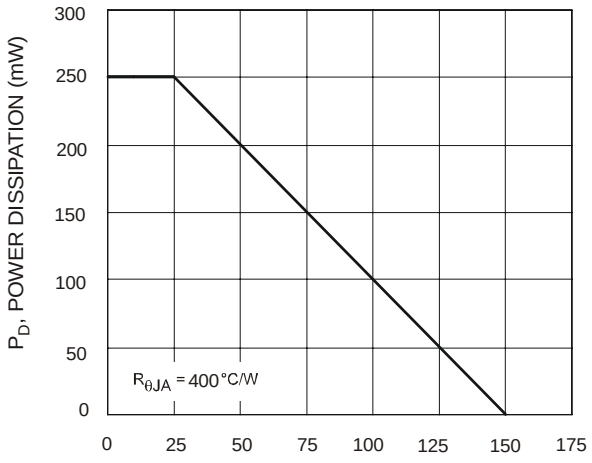

Fig. 3 Power Derating Curve

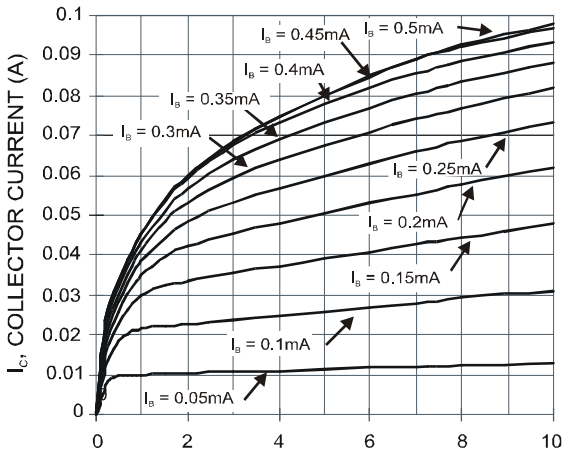

Fig. 4 V_{CE} vs. I_C

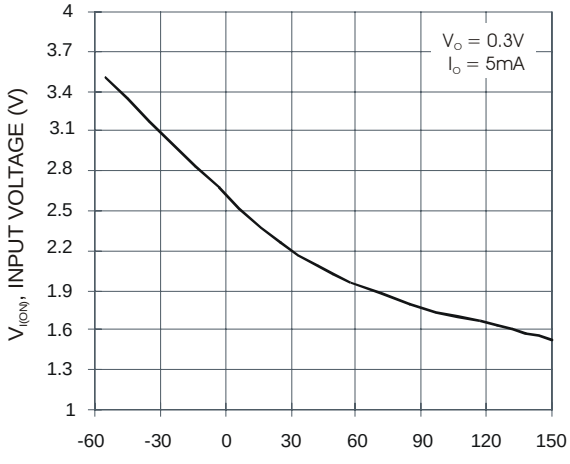

Fig. 5 Input Voltage vs. T_A

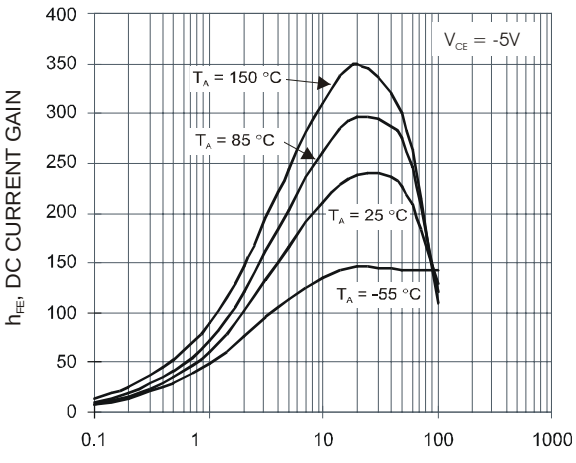

Fig. 6 DC Current Gain vs I_C

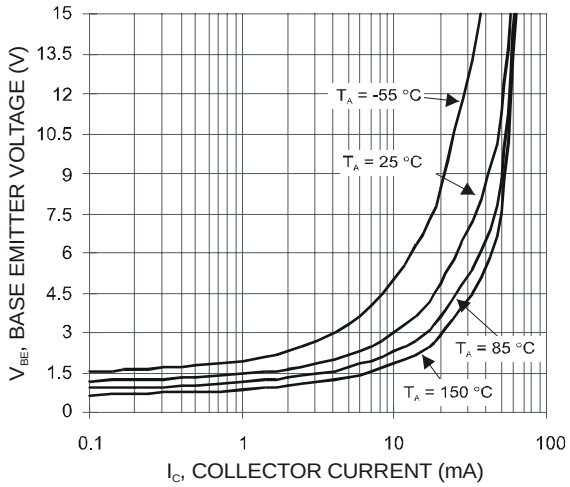

Fig. 7 I_C vs. $V_{BE(ON)}$

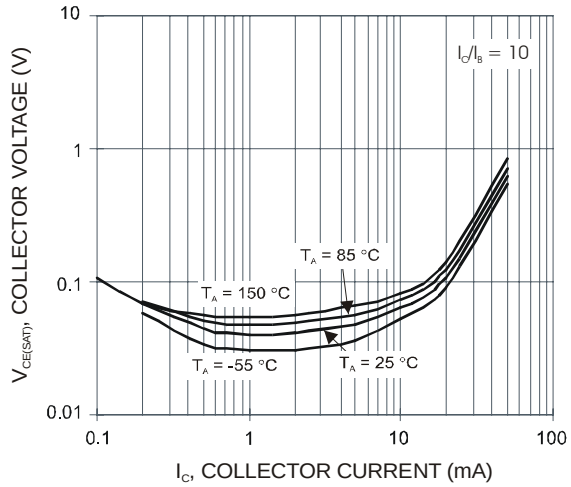

Fig. 8 I_C vs. $V_{CE(SAT)}$

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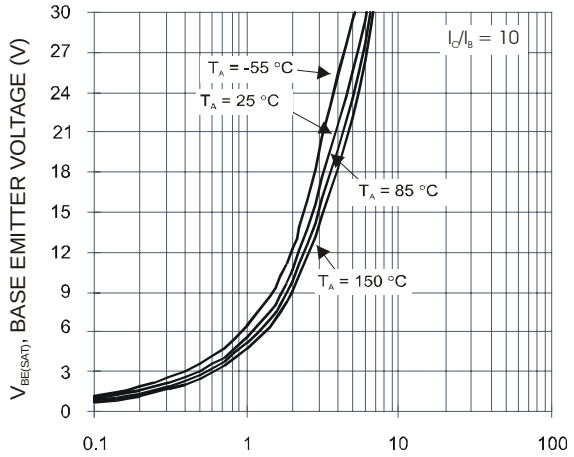


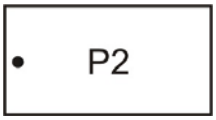
Fig. 9 I_C vs. $V_{BE(SAT)}$

Ordering Information (Note 6)

Device	Marking Code	Packaging	Shipping
DDTA144ELP-7	P2	DFN1006-3	3000/Tape & Reel

Notes: 6. For packaging details, please see page 5 or go to our website at http://www.diodes.com/ap2007.pdf.

Marking Information



P2 = Product Type Marking Code
YM = Date Code Marking
Y = Year ex: T = 2007
M = Month e.g. 9 = September

Fig. 10

Date Code Key

Year	2007	2008	2009	2010	2011	2012
Code	U	V	W	X	Y	Z

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

NEW PRODUCT

Mechanical Details

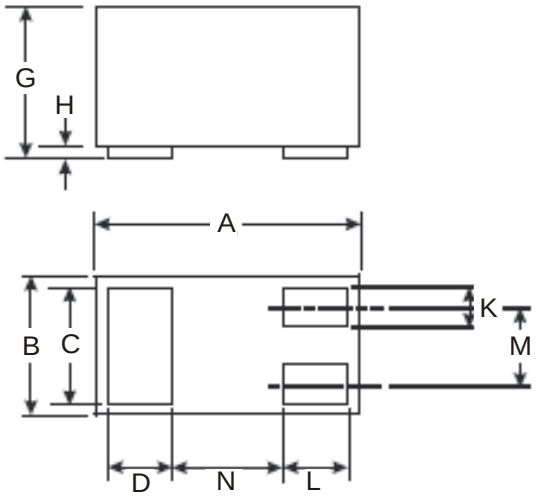


Fig. 11

DFN1006-3			
Dim	**Min**	**Max**	**Typ**
A	0.95	1.05	1.00
B	0.55	0.65	0.60
C	0.45	0.55	0.50
D	0.20	0.30	0.25
G	0.47	0.53	0.50
H	0	0.05	0.03
K	0.10	0.20	0.15
L	0.20	0.30	0.25
M	—	—	0.35
N	—	—	0.40
All Dimensions in mm			

Suggested Pad Layout: (Based on IPC-SM-782)

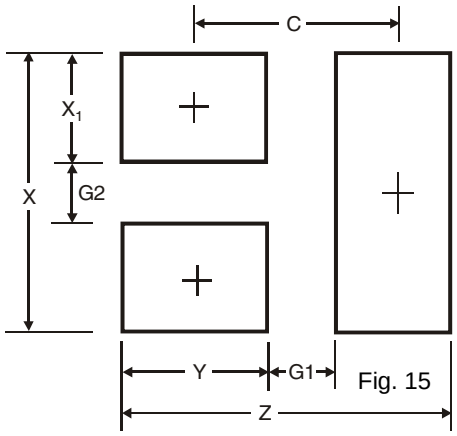


Fig. 15

Fig. 12

DFN1006-3	
Z	1.1
G1	0.3
G2	0.2
X	0.7
X1	0.25
Y	0.4
C	0.7
All Dimensions in mm	