GENERAL DESCRIPTION

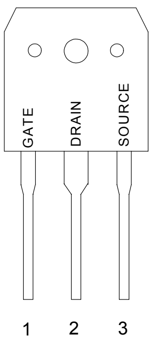
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

FEATURES

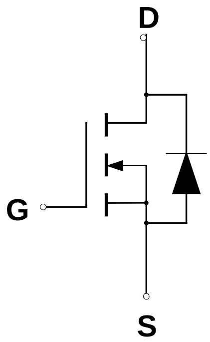
- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and V_{DS}(on) Specified at Elevated Temperature

PIN CONFIGURATION

TO-3P
Top View



SYMBOL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current — Continuous	I_D	14	A
— Pulsed	I_{DM}	56	
Gate-to-Source Voltage — Continue	V_{GS}	±20	V
— Non-repetitive	V_{GSM}	±40	V
Total Power Dissipation	P_D	190	W
Derate above 25℃		1.5	W/℃
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	℃
Single Pulse Drain-to-Source Avalanche Energy — T_J = 25℃ (V_{DD} = 100V, V_{GS} = 10V, I_L = 14A, L = 6mH, R_G = 25Ω)	E_{AS}	588	mJ
Thermal Resistance — Junction to Case	θ_{JC}	0.65	℃/W
— Junction to Ambient	θ_{JA}	40	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	℃

ORDERING INFORMATION

Part Number	Package
CMT14N50N3P	TO-3P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 25℃.

Characteristic		Symbol	CMT14N50 Min	Typ	Max	Units
Drain-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μA)		$V_{(BR)DSS}$	500			V
Drain-Source Leakage Current (V_{DS} = 500 V, V_{GS} = 0 V) (V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125℃)		I_{DSS}			 25 250	μA
Gate-Source Leakage Current-Forward (V_{gsf} = 20 V, V_{DS} = 0 V)		I_{GSSF}			100	nA
Gate-Source Leakage Current-Reverse (V_{gsr} = 20 V, V_{DS} = 0 V)		I_{GSSR}			100	nA
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0		4.0	V
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 8.4A) *		$R_{DS(on)}$			0.4	Ω
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 14 A)		$V_{DS(on)}$			7.5	V
Forward Transconductance (V_{DS} = 50 V, I_D = 8.4A) *		g_{FS}	9.3			mhos
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}		2038		pF
Output Capacitance		C_{oss}		307		pF
Reverse Transfer Capacitance		C_{rss}		10		pF
Turn-On Delay Time	(V_{DD} = 250 V, I_D = 14 A, R_D = 17Ω, R_G = 6.2Ω) *	$t_{d(on)}$		15		ns
Rise Time		t_r		36		ns
Turn-Off Delay Time		$t_{d(off)}$		35		ns
Fall Time		t_f		29		ns
Total Gate Charge	(V_{DS} = 400 V, I_D = 14 A, V_{GS} = 10 V)*	Q_g			64	nC
Gate-Source Charge		Q_{gs}			16	nC
Gate-Drain Charge		Q_{gd}			26	nC
Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)		L_D		5.0		nH
Internal Drain Inductance (Measured from the source lead 0.25" from package to source bond pad)		L_S		13		nH
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage(1)	(I_S = 14 A, V_{GS} = 0 V, d_{IS}/d_t = 100A/μs)	V_{SD}			1.5	V
Forward Turn-On Time		t_{on}		**		ns
Reverse Recovery Time		t_{rr}		487	731	ns

* Pulse Test: Pulse Width ≦300μs, Duty Cycle ≦2%

** Negligible, Dominated by circuit inductance

TYPICAL ELECTRICAL CHARACTERISTICS

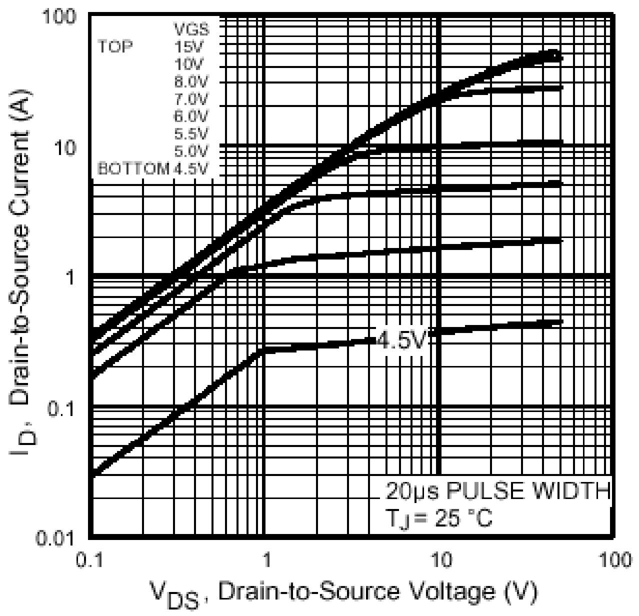


Fig 1. Typical Output Characteristics

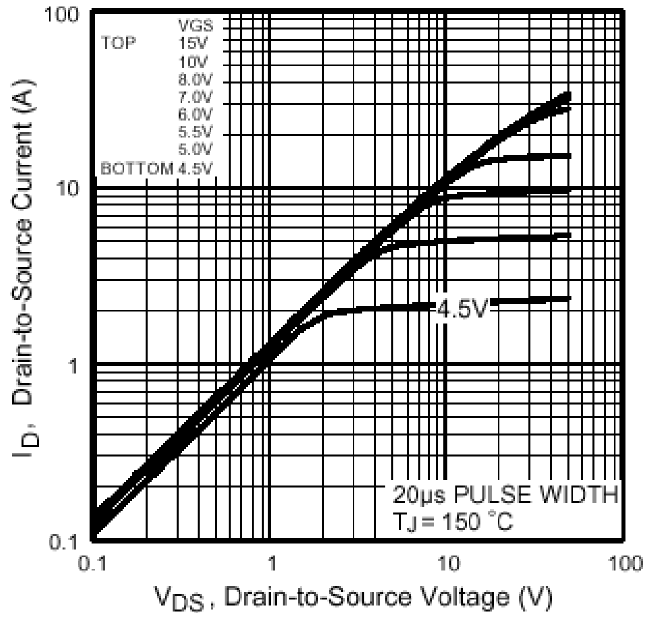


Fig 2. Typical Output Characteristics

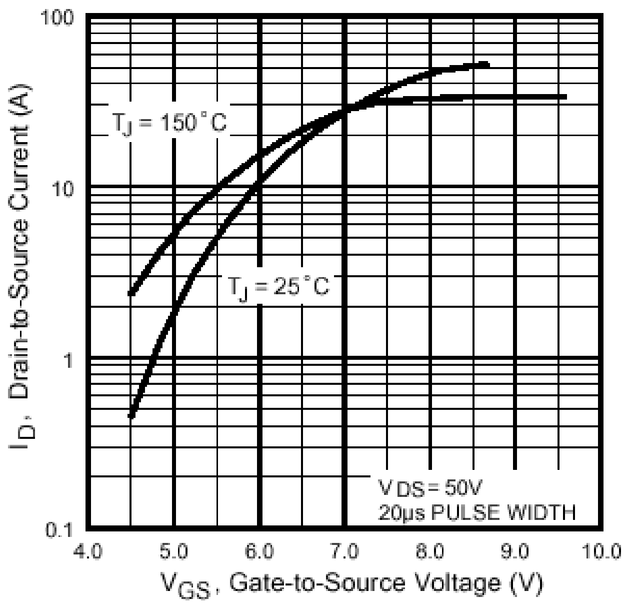


Fig 3. Typical Transfer Characteristics

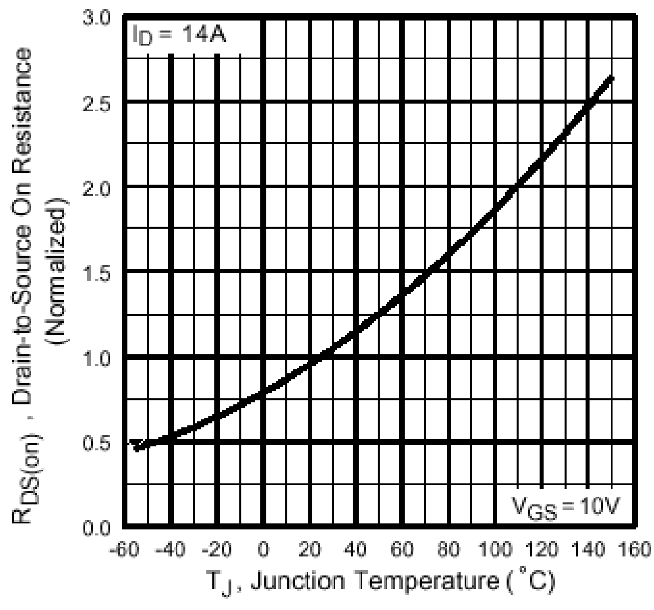


Fig 4. Normalized On-Resistance Vs. Temperature

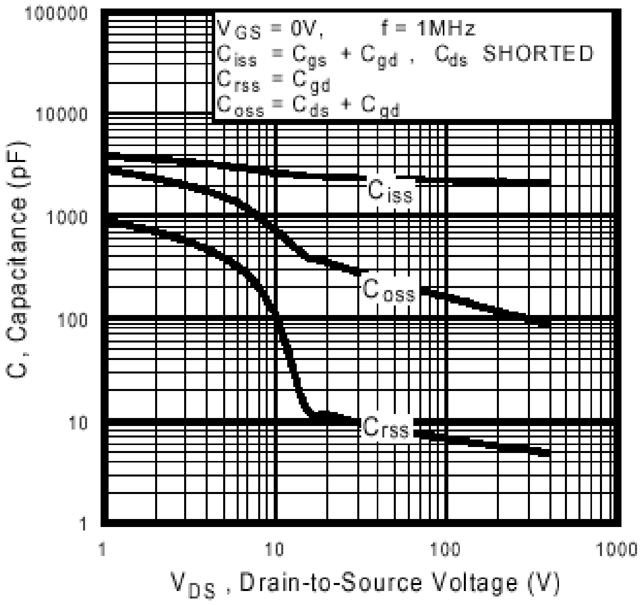


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

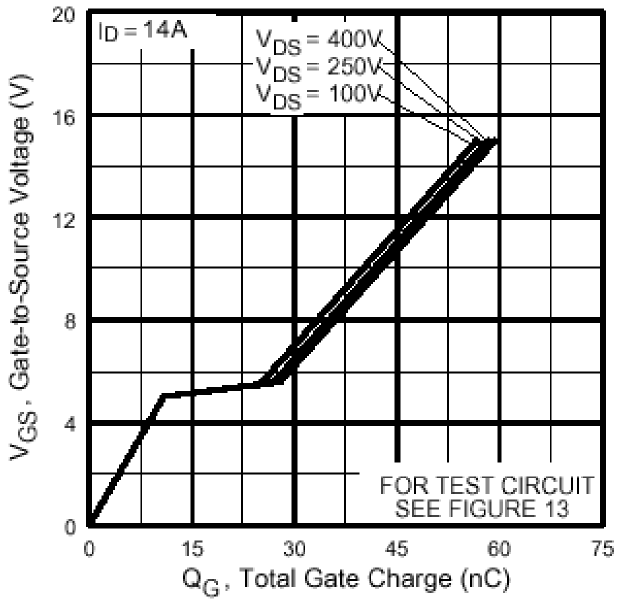


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

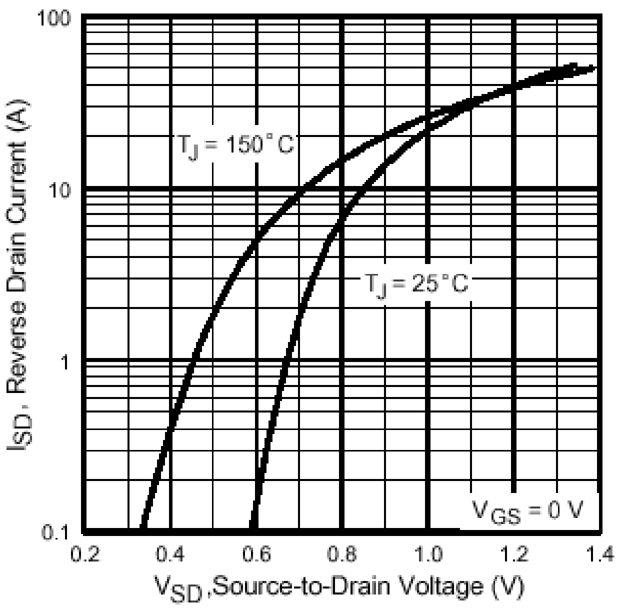


Fig 7. Typical Source-Drain Diode Forward Voltage

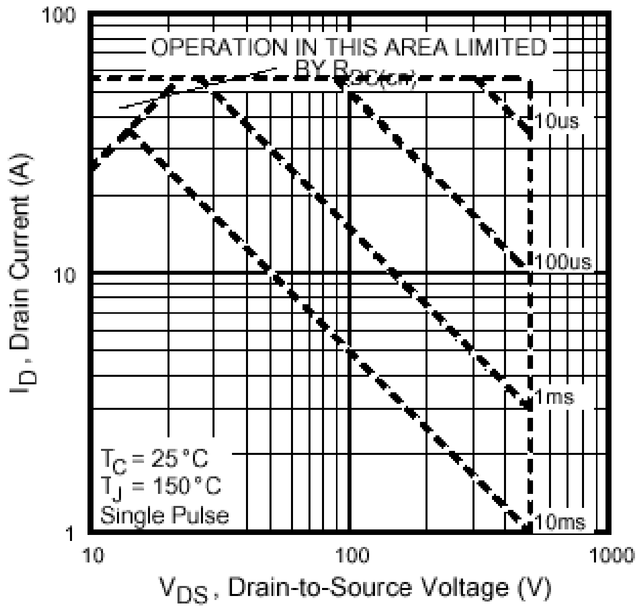


Fig 8. Maximum Safe Operating Area

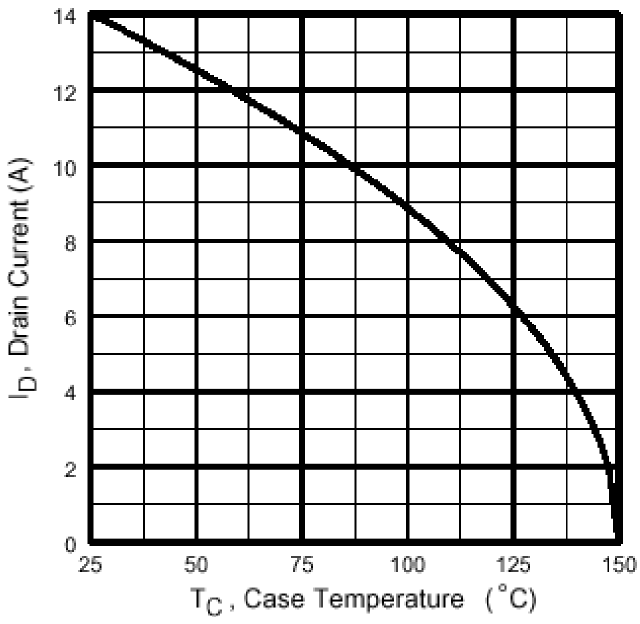


Fig 9. Maximum Drain Current Vs. Case Temperature

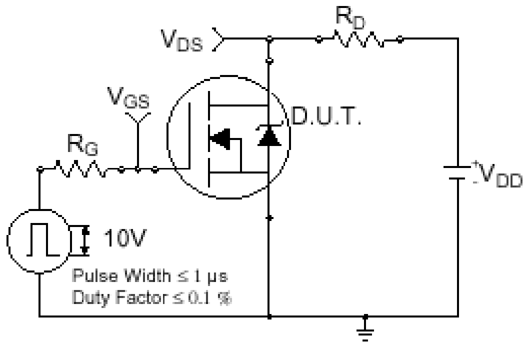


Fig 10a. Switching Time Test Circuit

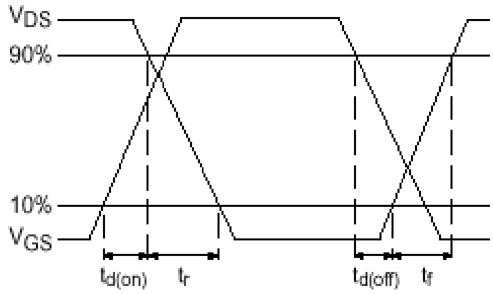


Fig 10b. Switching Time Waveforms

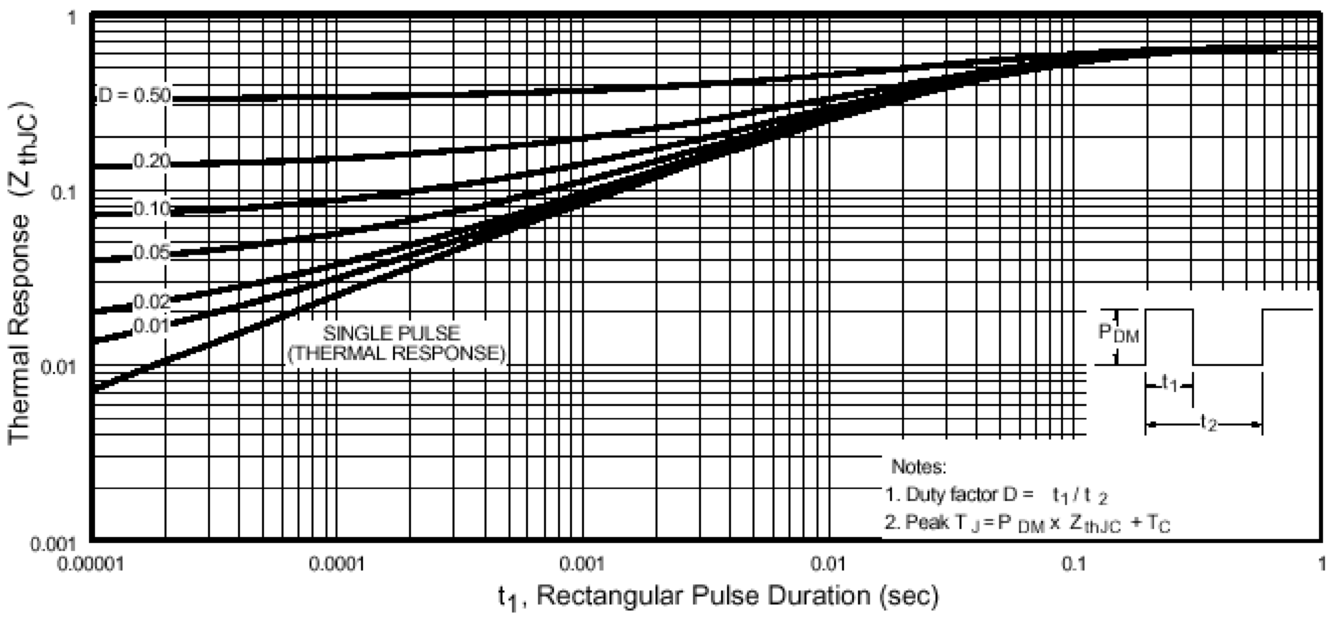


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

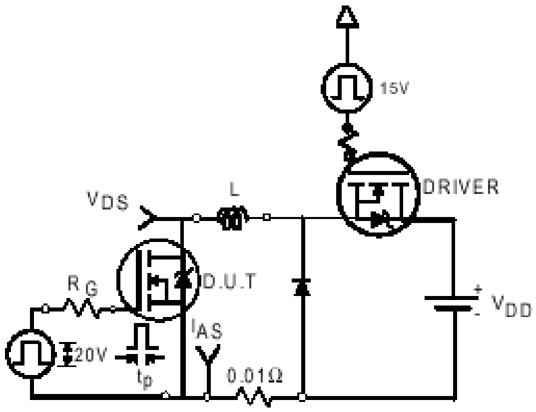


Fig 12a. Unclamped Inductive Test Circuit

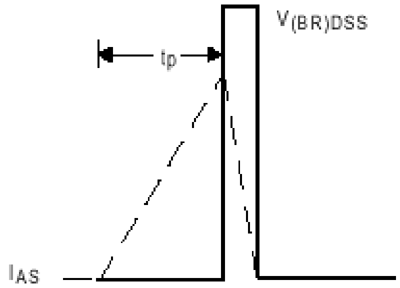


Fig 12b. Unclamped Inductive Waveforms

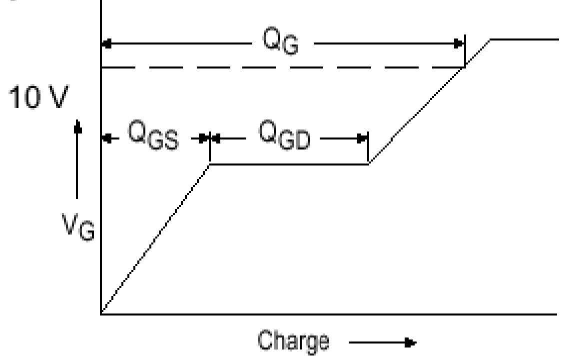


Fig 13a. Basic Gate Charge Waveform

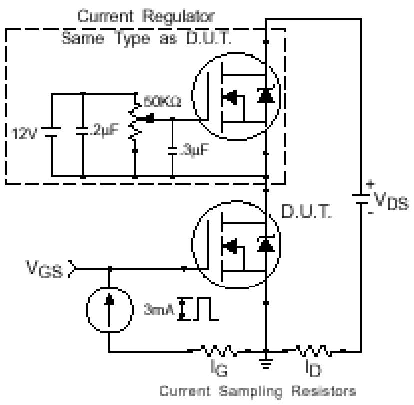


Fig 13b. Gate Charge Test Circuit

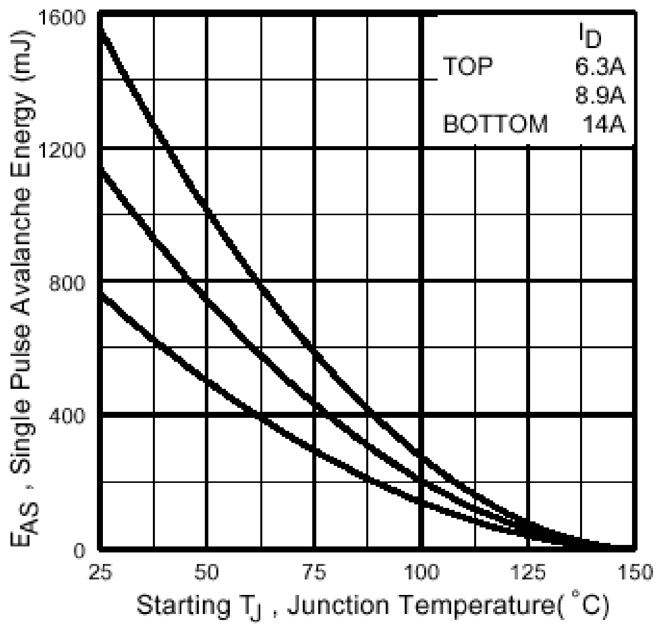


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

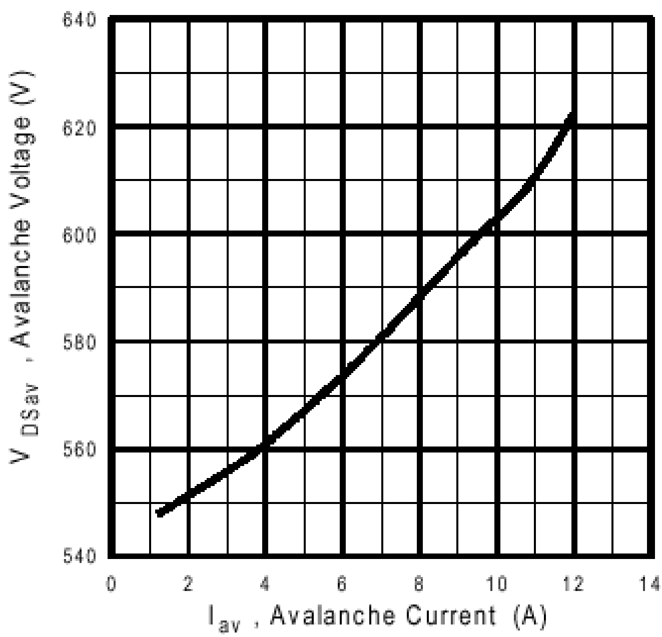
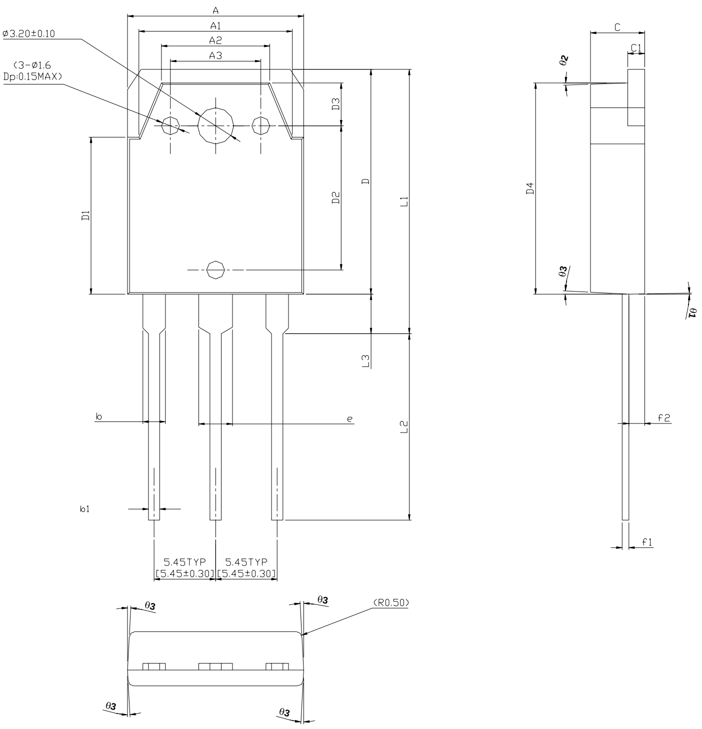


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

PACKAGE DIMENSION

TO-3P



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	15.40	---	15.80	0.606	---	0.622
A1	13.40	---	13.80	0.527	---	0.543
A2	9.40	---	9.80	0.370	---	0.386
A3	---	8.00	---	---	0.315	---
b	1.80	---	2.20	0.071	---	0.087
b1	0.80	---	1.20	0.031	---	0.047
C	4.60	---	5.00	0.181	---	0.197
C1	1.45	---	1.65	0.057	---	0.065
D	19.70	---	20.10	0.775	---	0.791
D1	13.70	---	14.10	0.539	---	0.555
D2	12.56	---	12.96	0.494	---	0.510
D3	3.60	---	4.00	0.142	---	0.157
D4	18.50	---	18.90	0.728	---	0.744
e	2.80	---	3.20	0.110	---	0.126
f1	0.55	---	0.75	0.021	---	0.029
f2	1.20	---	1.60	0.047	---	0.063
L1	23.20	---	23.60	0.913	---	0.929
L2	16.20	---	16.80	0.638	---	0.661
L3	3.30	---	3.70	0.130	---	0.146
θ1	---	1°	---	---	1°	---
θ2	---	2°	---	---	2°	---
θ3	---	3°	---		3°	---

IMPORTANT NOTICE

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