74LVT16646A

3.3 V 16-bit bus transceiver; 3-state

Rev. 03 — 12 January 2005 Product data sheet

1. General description

The 74LVT16646A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V. This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable ($\overline{OE}$) input for easy cascading and a direction (DIR) input for direction control.

Data on bus A or bus B is clocked into the registers on the LOW-to-HIGH transition of the appropriate clock (CPAB or CPBA). The select control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode data).

2. Features

- 16-bit universal bus interface
- 3-state buffers
- Output capability: from +64 mA to –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus-current loading when output is tied to 5 V bus
- Power-up reset
- Power-up 3-state
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
  - MIL STD 883 Method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

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3. Quick reference data

Table 1: Quick reference data

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}, t_{PHL}	propagation delay nAx to nBx or nBx to nAx	C_L = 50 pF; V_{CC} = 3.3 V	-	1.9	-	ns
C_I	input capacitance	V_I = 0 V or 3.0 V	-	3	-	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0 V or 3.0 V; outputs disabled	-	9	-	pF
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; outputs disabled	-	70	-	µA

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT16646ADGG	–40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
74LVT16646ADL	–40 °C to +85 °C	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1

5. Functional diagram

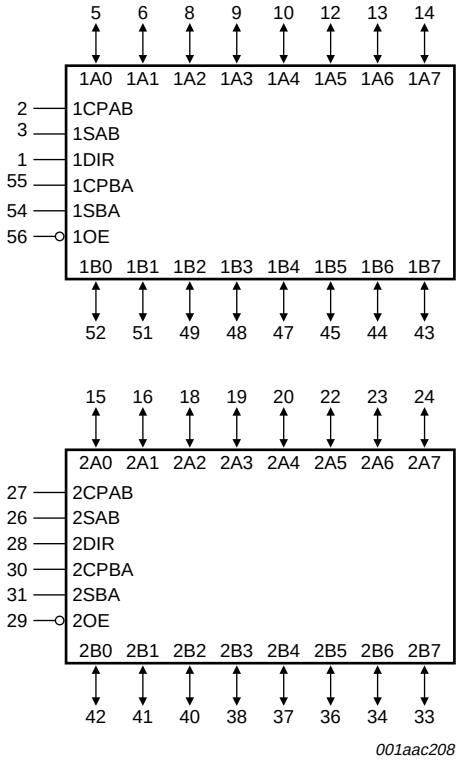


Fig 1. Logic symbol

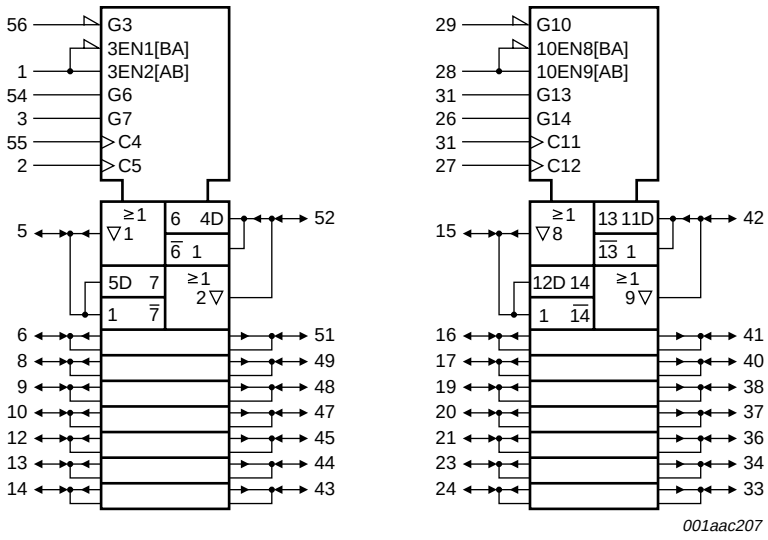


Fig 2. IEC logic symbol

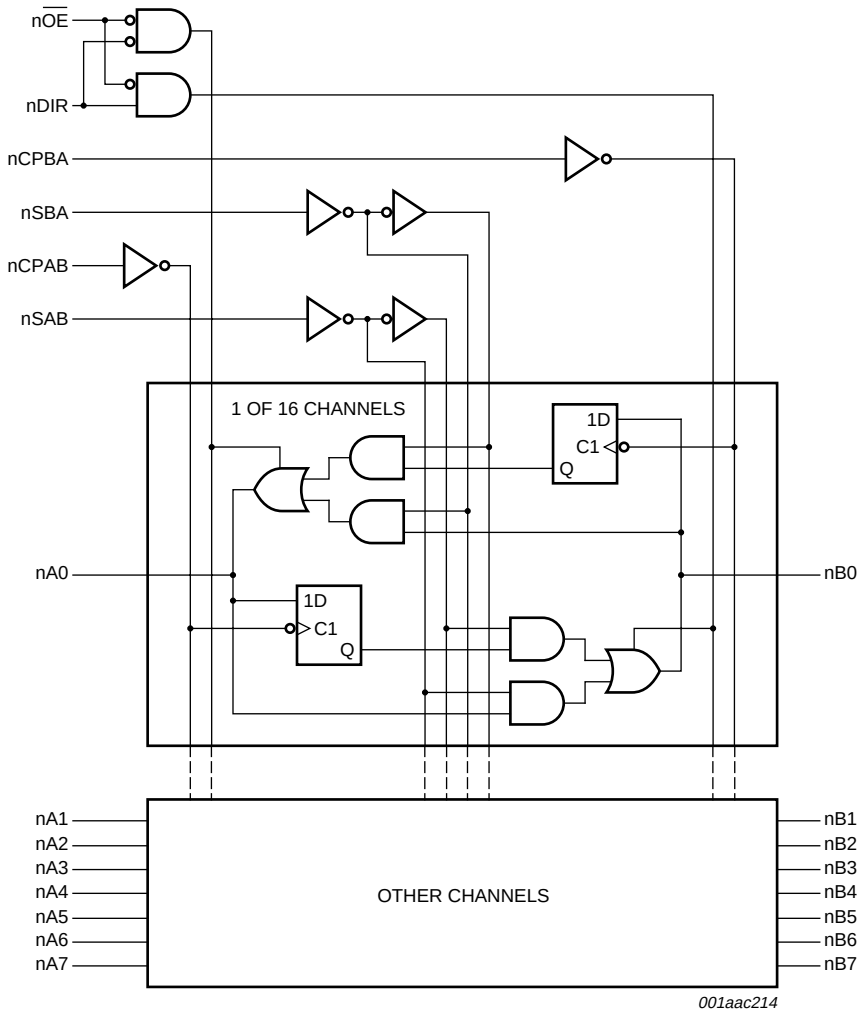


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

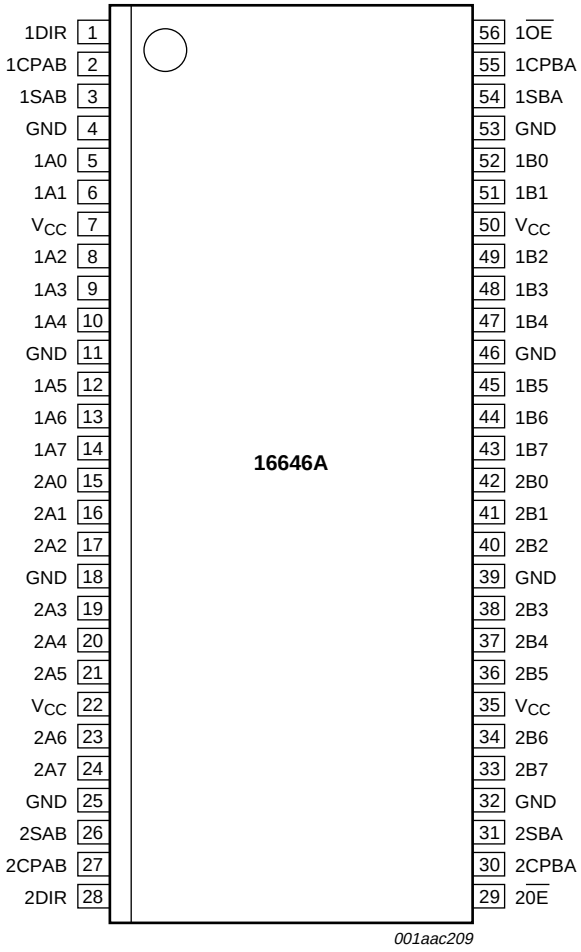


Fig 4. Pinning configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1DIR	1	direction control inputs 0 to 7
1CPAB	2	clock inputs 0 to 7; A to B side
1SAB	3	select inputs 0 to 7; A to B side
GND	4	ground (0V)
1A0	5	data input or output 0; A side
1A1	6	data input or output 1; A side
V_{CC}	7	positive supply voltage
1A2	8	data input or output 2; A side

Table 3: Pin description *...continued*

Symbol	Pin	Description
1A3	9	data input or output 3; A side
1A4	10	data input or output 4; A side
GND	11	ground (0V)
1A5	12	data input or output 5; A side
1A6	13	data input or output 6; A side
1A7	14	data input or output 7; A side
2A0	15	data input or output 8; A side
2A1	16	data input or output 9; A side
2A2	17	data input or output 10; A side
GND	18	ground (0V)
2A3	19	data input or output 11; A side
2A4	20	data input or output 12; A side
2A5	21	data input or output 13; A side
V_{CC}	22	positive supply voltage
2A6	23	data input or output 14; A side
2A7	24	data input or output 15; A side
GND	25	ground (0V)
2SAB	26	select inputs 8 to 15; A to B side
2CPAB	27	clock inputs 8 to 15; A to B side
2DIR	28	direction control inputs 8 to 15
$2\overline{OE}$	29	output enable inputs 8 to 15
2CPBA	30	clock inputs 8 to 15; B to A side
2SBA	31	select inputs 8 to 15; B to A side
GND	32	ground (0V)
2B7	33	data input or output 15; B side
2B6	34	data input or output 14; B side
V_{CC}	35	positive supply voltage
2B5	36	data input or output 13; B side
2B4	37	data input or output 12; B side
2B3	38	data input or output 11; B side
GND	39	ground (0V)
2B2	40	data input or output 10; B side
2B1	41	data input or output 9; B side
2B0	42	data input or output 8; B side
1B7	43	data input or output 7; B side
1B6	44	data input or output 6; B side
1B5	45	data input or output 5; B side
GND	46	ground (0V)
1B4	47	data input or output 4; B side
1B3	48	data input or output 3; B side
1B2	49	data input or output 2; B side

Table 3: Pin description *...continued*

Symbol	Pin	Description
V_{CC}	50	positive supply voltage
1B1	51	data input or output 1; B side
1B0	52	data input or output 0; B side
GND	53	ground (0V)
1SBA	54	select inputs 0 to 7; B to A side
1CPBA	55	clock inputs 0 to 7; B to A side
$1\overline{OE}$	56	output enable inputs 0 to 7

7. Functional description

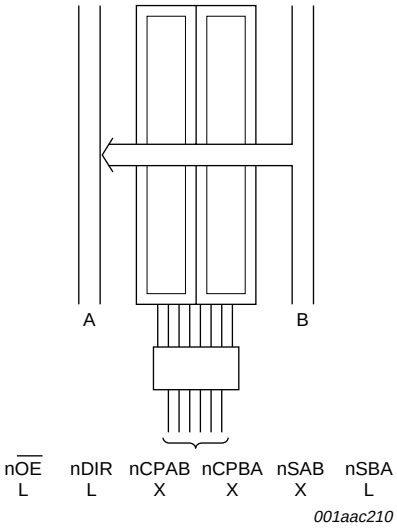
7.1 Function table

Table 4: Function table [1]

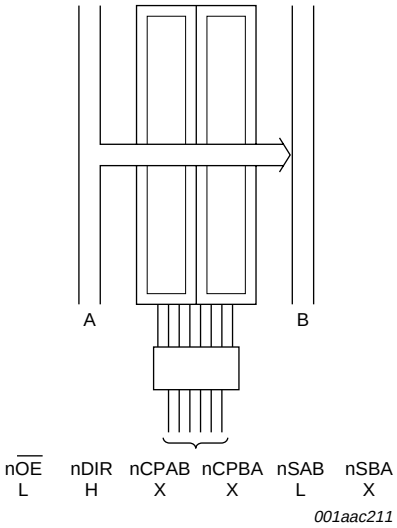
Operating mode	Inputs						Data I/O		reference
	$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
Store A (B unspecified)	X	X	↑	X	X	X	input	unspecified output [2]	Figure 5c
Store B (A unspecified)	X	X	X	↑	X	X	unspecified output [2]	input	Figure 5c
Store A and B data	H	X	↑	↑	X	X	input	input	Figure 5c
Isolation, hold storage	H	X	H or L	H or L	X	X	input	input	-
Real time B data to A bus	L	L	X	X	X	L	output	input	Figure 5a
Stored B data to A bus	L	L	X	H or L	X	H	output	input	Figure 5d
Real time A data to B bus	L	H	X	X	L	X	input	output	Figure 5b
Stored A data to B bus	L	H	H or L	X	H	X	input	output	Figure 5d

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH clock transition.

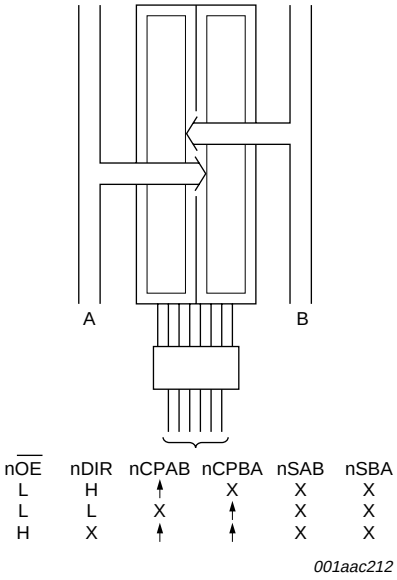
[2] The data output function may be enabled or disabled by various signals at the $n\overline{OE}$ input. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.



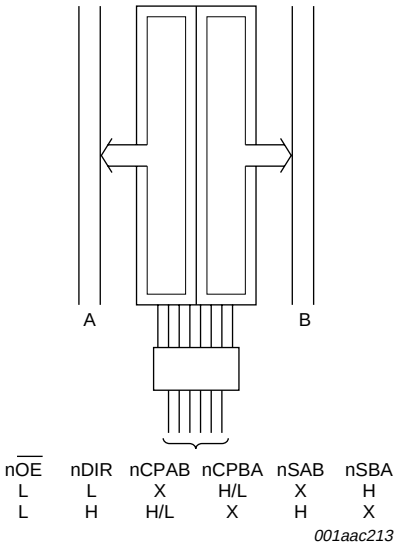
a. Real time bus transfer bus B to bus A



b. Real time bus transfer bus A to bus B



c. Storage from bus A, bus B or bus A and bus B



d. Transfer stored data to bus A or bus B

Fig 5. Examples of bus-management functions

8. Limiting values

Table 5: Limiting values

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage		[1]	–0.5	+7.0	V
V_O	output voltage	output in off-state or HIGH state	[1]	–0.5	+7.0	V
I_{IK}	input diode current	$V_I < 0$ V		–50	-	mA
I_{OK}	output diode current	$V_O < 0$ V		–50	-	mA
I_O	output source current	output in LOW state		-	128	mA
		output in HIGH state		–64	-	mA
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature		[2]	-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	–32	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		duty cycle ≤ 50 %; $f \geq 1$ kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature		–40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
V_{IK}	input clamp voltage	V_{CC} = 2.7 V; I_{IK} = −18 mA		-	−0.85	−1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = 100 µA		V_{CC} − 0.2	V_{CC}	-	V
		V_{CC} = 2.7 V; I_{OH} = −8 mA		2.4	2.5	-	V
		V_{CC} = 3.0 V; I_{OH} = −32 mA		2.0	2.3	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V					
		I_{OL} = 100 µA		-	0.07	0.2	V
		I_{OL} = 24 mA		-	0.03	0.5	V
		V_{CC} = 3.0 V					
		I_{OL} = 16 mA		-	0.25	0.4	V
		I_{OL} = 32 mA		-	0.3	0.5	V
		I_{OL} = 64 mA		-	0.4	0.55	V
V_{RST}	power-up LOW output voltage	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC}	[2]	-	-	0.55	V
I_{LI}	input leakage current of control pins	V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	0.1	±1	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	0.1	10	µA
	input leakage current of I/O data pins	V_{CC} = 3.6 V; V_I = 5.5 V	[3]	-	0.1	20	µA
		V_{CC} = 3.6 V; V_I = V_{CC}	[3]	-	0.5	10	µA
		V_{CC} = 3.6 V; V_I = 0 V	[3]	-	+0.1	−5	µA
I_{OFF}	output off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	0.1	±100	µA
I_{HOLD}	bus hold current A or B outputs	V_{CC} = 3 V; V_I = 0.8 V	[4]	75	130	-	µA
		V_{CC} = 3 V; V_I = 2.0 V	[4]	−75	−140	-	µA
		V_{CC} = 0 V to 3.6 V; V_I = 3.6 V	[4]	±500	-	-	µA
I_{EX}	current into an output in HIGH state when V_O > V_{CC}	V_O = 5.5 V; V_{CC} = 3.0 V		-	50	125	µA
I_{PU}, I_{PD}	power-up and power-down 3-state output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; pin nDIR and $\overline{nOE}$ are don't care	[5]	-	35	±100	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; I_O = 0 A; V_I = GND or V_{CC}					
		outputs HIGH		-	0.07	0.12	mA
		outputs LOW		-	4.9	6	mA
		outputs disabled	[6]	-	0.07	0.12	mA

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔI_{CC}	additional supply current per input pin	V_{CC} = 3 V to 3.6 V; one input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND	[7]	-	0.1	0.2	mA
C_I	input capacitance	V_I = 0 V or 3.0 V		-	3	-	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0 V or 3.0 V; outputs disabled		-	9	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for V_{CC} = 0 V to 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to 3.3 V ± 0.3 V. A transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; for input definitions see Figure 13; for test circuit see Figure 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
f_{max}	maximum clock frequency	V_{CC} = 3.3 V ± 0.3 V; see Figure 6	150	-	-	MHz
t_{PLH}	propagation delay nAx to nBx or nBx to nAx	see Figure 8				
		V_{CC} = 3.3 V ± 0.3 V	0.5	1.9	3.7	ns
		V_{CC} = 2.7 V	-	-	4.3	ns
	propagation delay nCPAB to nBx or nCPBA to nAx	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	1.5	2.7	4.5	ns
		V_{CC} = 2.7 V	-	-	5.3	ns
	propagation delay nSAB to nBx or nSBA to nAx	see Figure 7				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.5	4.6	ns
		V_{CC} = 2.7 V	-	-	5.4	ns
t_{PHL}	propagation delay nAx to nBx or nBx to nAx	see Figure 8				
		V_{CC} = 3.3 V ± 0.3 V	0.5	1.9	3.7	ns
		V_{CC} = 2.7 V	-	-	4.4	ns
	propagation delay nCPAB to nBx or nCPBA to nAx	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	1.5	2.4	4.5	ns
		V_{CC} = 2.7 V	-	-	5.2	ns
	propagation delay nSAB to nBx or nSBA to nAx	see Figure 7				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.8	4.8	ns
		V_{CC} = 2.7 V	-	-	5.6	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; for input definitions see Figure 13; for test circuit see Figure 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZH}	output enable time $n\overline{OE}$ to nAx or nBx	see Figure 11				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.7	4.7	ns
		V_{CC} = 2.7 V	-	-	5.4	ns
	output enable time nDIR to nAx or nBx	see Figure 11				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.9	4.8	ns
		V_{CC} = 2.7 V	-	-	5.4	ns
t_{PZL}	output enable time $n\overline{OE}$ to nAx or nBx	see Figure 12				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.5	4.9	ns
		V_{CC} = 2.7 V	-	-	5.7	ns
	output enable time nDIR to nAx or nBx	see Figure 12				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.8	4.9	ns
		V_{CC} = 2.7 V	-	-	5.6	ns
t_{PHZ}	output disable time $n\overline{OE}$ to nAx or nBx	see Figure 11				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.2	5.2	ns
		V_{CC} = 2.7 V	-	-	5.5	ns
	output disable time nDIR to nAx or nBx	see Figure 11				
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.1	5.7	ns
		V_{CC} = 2.7 V	-	-	6.6	ns
t_{PLZ}	output disable time $n\overline{OE}$ to nAx or nBx	see Figure 12				
		V_{CC} = 3.3 V ± 0.3 V	1.5	2.9	4.6	ns
		V_{CC} = 2.7 V	-	-	4.7	ns
	output disable time nDIR to nAx or nBx	see Figure 12				
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.9	5.2	ns
		V_{CC} = 2.7 V	-	-	5.7	ns

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

Table 9: Dynamic characteristics setup requirements

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω.

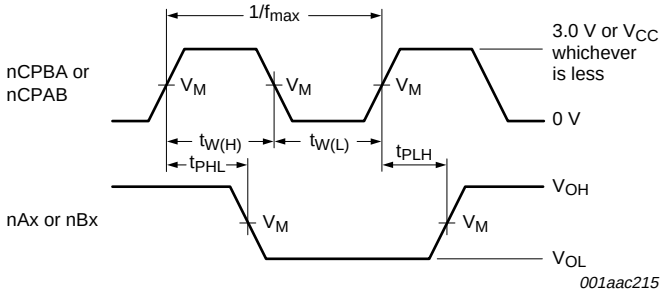
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
$t_{su(H)}$	set-up time HIGH nAx to nCPAB or nBx to nCPBA	see Figure 10				
		V_{CC} = 3.3 V ± 0.3 V	1.0	0.6	-	ns
		V_{CC} = 2.7 V	1.1	-	-	ns
$t_{su(L)}$	set-up time LOW nAx to nCPAB or nBx to nCPBA	see Figure 10				
		V_{CC} = 3.3 V ± 0.3 V	1.9	0.4	-	ns
		V_{CC} = 2.7 V	2.4	-	-	ns
$t_{h(H)}$	hold time HIGH nAx to nCPAB or nBx to nCPBA	see Figure 10				
		V_{CC} = 3.3 V ± 0.3 V	1.0	0.4	-	ns
		V_{CC} = 2.7 V	1.0	-	-	ns

Table 9: Dynamic characteristics setup requirements *…continued*

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(L)}$	hold time LOW nAx to nCPAB or nBx to nCPBA	see Figure 10				
		V_{CC} = 3.3 V ± 0.3 V	1.0	0.5	-	ns
		V_{CC} = 2.7 V	1.0	-	-	ns
$t_{W(H)}$	pulse width HIGH nCPAB or nCPBA	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	2.6	2.2	-	ns
		V_{CC} = 2.7 V	2.6	-	-	ns
$t_{W(L)}$	pulse width HIGH nCPAB or nCPBA	see Figure 6				
		V_{CC} = 3.3 V ± 0.3 V	2.8	2.4	-	ns
		V_{CC} = 2.7 V	2.8	-	-	ns

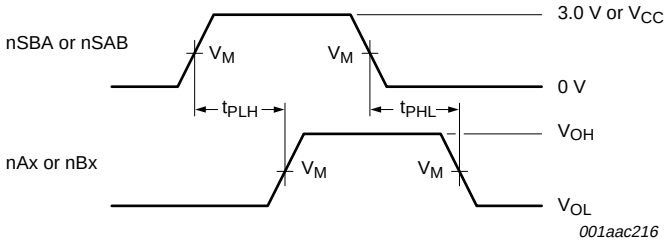
12. Waveforms



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

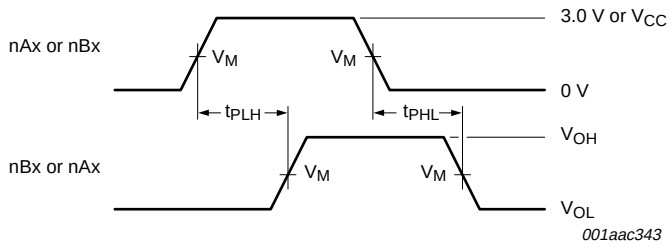
Fig 6. Propagation delay clock input to output, clock pulse width and maximum clock frequency



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

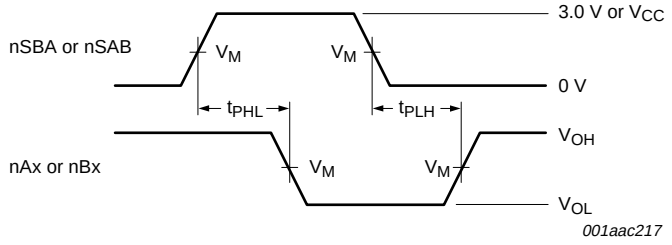
Fig 7. Propagation delay nSAB to nBx or nSBA to nAx



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

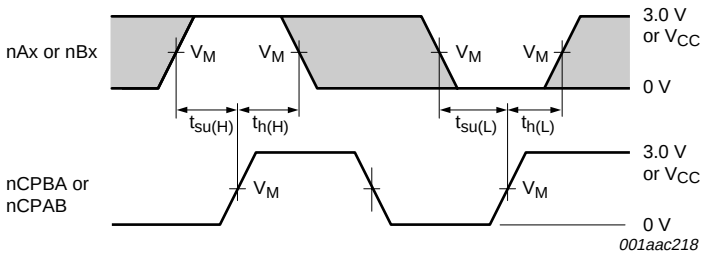
Fig 8. Propagation delay nAx to nBx or nBx to nAx



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

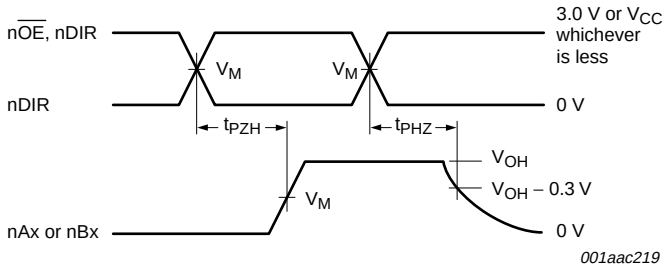
Fig 9. Propagation delay nSBA to nAx or nSAB to nBx



V_M = 1.5 V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

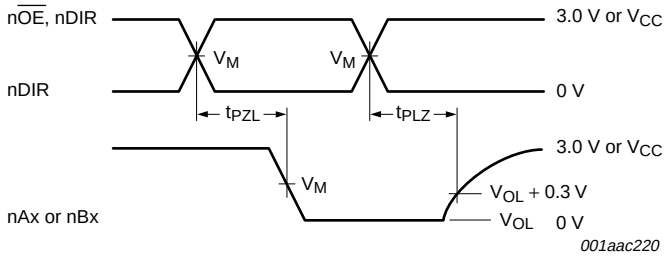
Fig 10. Data setup and hold times



V_M = 1.5 V.

V_{OH} is typical voltage output drop that occur with the output load.

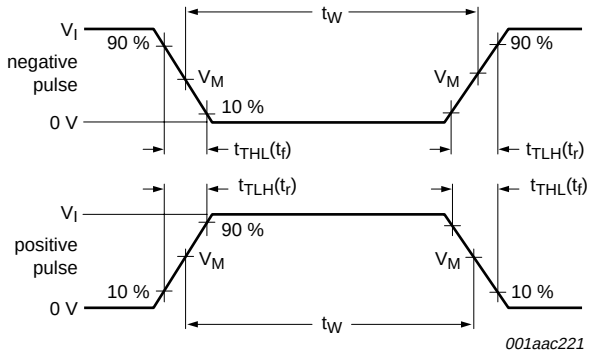
Fig 11. 3-state output enable and disable time nOE, nDIR to nAx or nBx



V_M = 1.5 V.

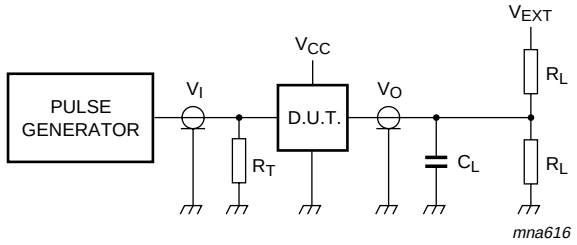
V_{OL} is typical voltage output drop that occur with the output load.

Fig 12. 3-state output enable and disable time nOE, nDIR to nAx or nBx



V_M = 1.5 V.

Fig 13. Input pulse definition



Test data is given in Table 10.

R_L = Load resistor; see Section 11 for value.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

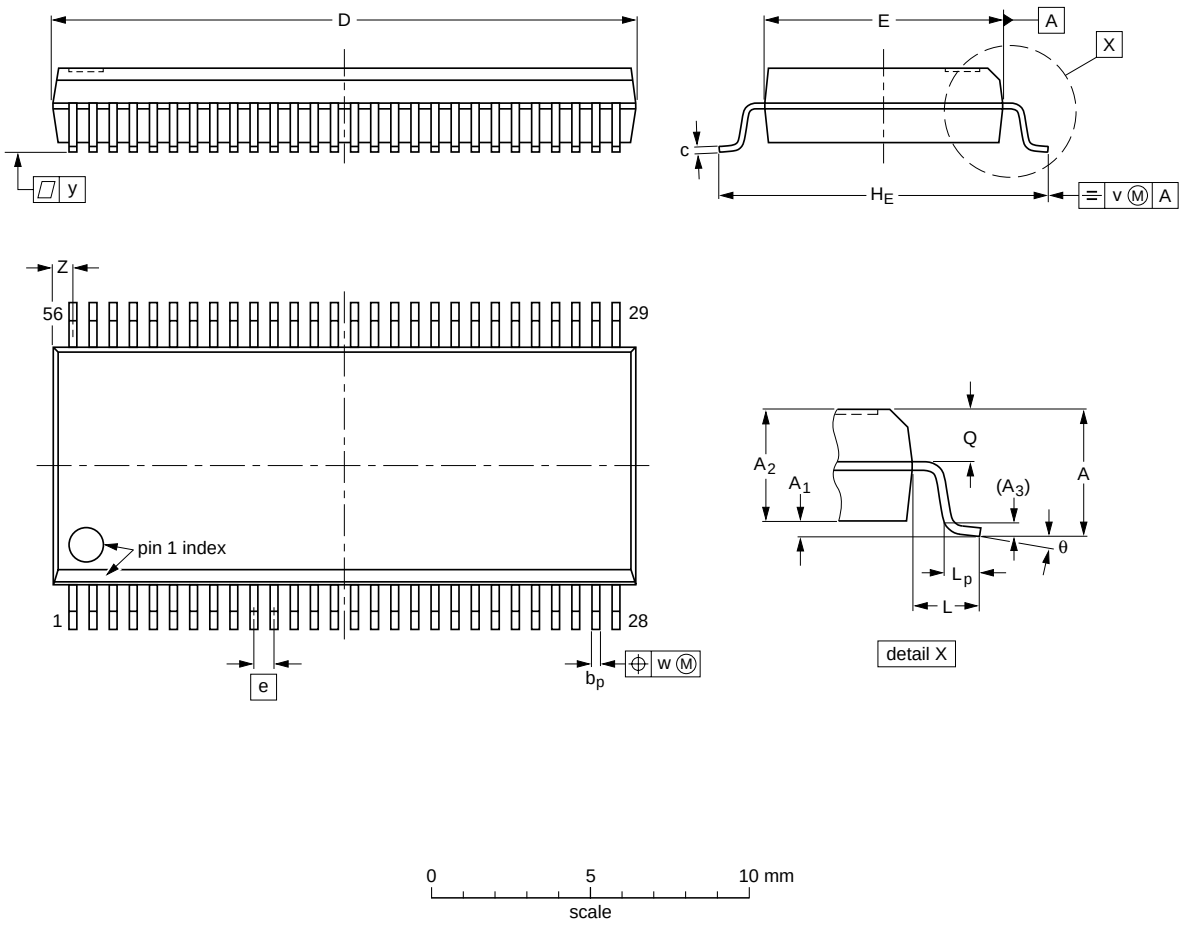
Fig 14. Load circuitry for switching times

Table 10: Test data

V_I	Repetition rate	t_W	t_r	t_f	C_L	R_L	V_{EXT}		
							t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

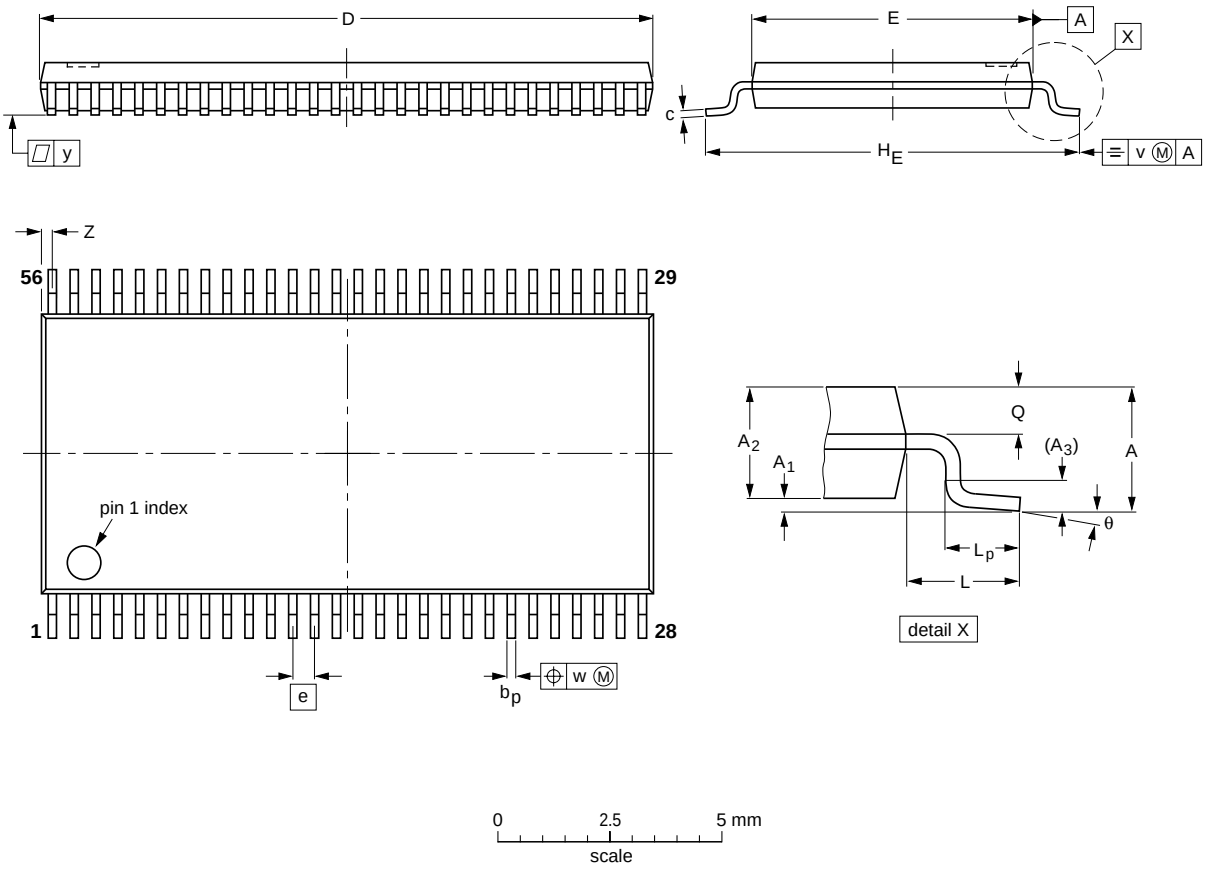
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT371-1		MO-118				~~99-12-27~~ 03-02-18

Fig 15. Package outline SOT371-1 (SSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT364-1 (TSSOP56)

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVT16646A_3	20050112	Product data sheet	-	9397 750 14326	74LVT16646A_2
Modifications:	• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Data sheet title changed from “3.3 V ABT 16-bit bus transceiver (3-state)” to “3.3 V 16-bit bus transceiver; 3-state” • Table 8: updated parameter descriptions and values.				
74LVT16646A_2	19980219	Product specification	-	9397 750 03559	74LVT16646A_1
74LVT16646A_1	19940725	-	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contents

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