CURRENT MODE PWM CONTROL CIRCUITS—YD3842

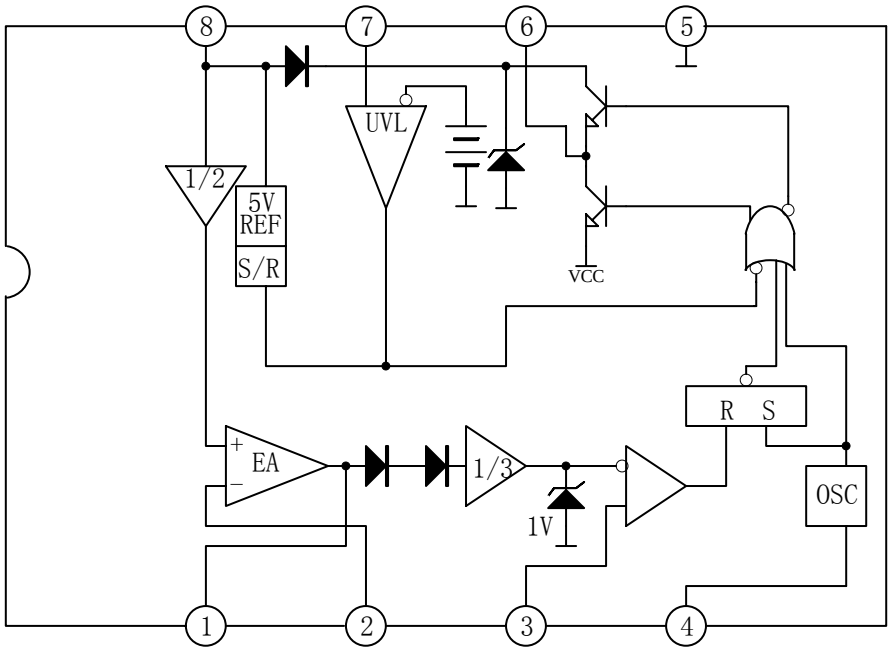
DESCRIPTION

The YD3842 provides the necessary features to implement off-line or DC fixed frequency current mode control schemes with a minimal external parts count.

FEATURES

*Optimized For Off-line and DC to DC Converts
*Low Start up Current
*Automatic Feed Forward Compensation
*Pulse-by-Pulse Current Limiting
*Under-voltage Lookout with Hysteresis
*Double Pulse Suppression
*High Current Totem Pole Output
*Internally Trimmed Band-gap Reference
*500kHz Operation

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(Tamb=25℃)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (Low impedance Source)	V_{CC}	30	V
Output Current	Io	±1	A
Analog Inputs(pin 2, 3)	$V_{I(ANA)}$	-0.3 to +6.3	V
Error Amplifier Output Sink Current	$I_{SINK(EA)}$	10	mA
Power Dissipation	P_D	1.0	W

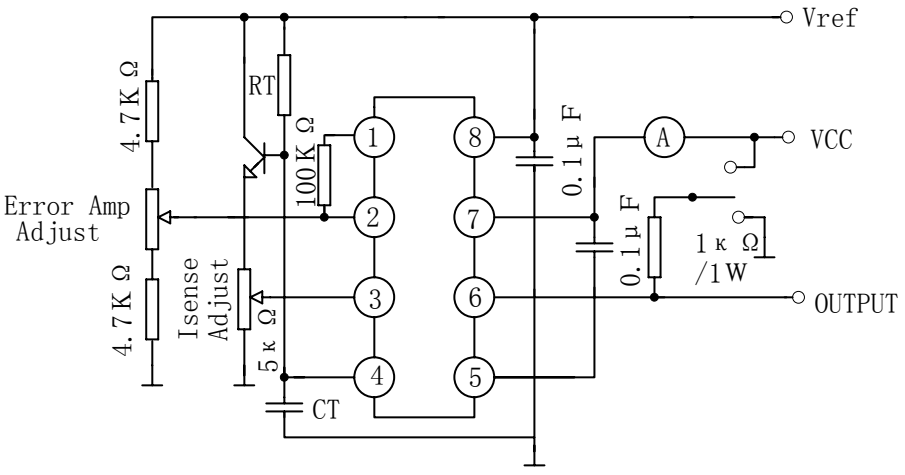
ELECTRICAL CHARACTERISTICS

(Tamb=25℃, V_{CC1}=10V, Vcc2=9.5V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section						
Output Voltage	V_{REF}	Tj=25℃, Io=1mA	4.90	5.00	5.10	V
Line Regulation	$\triangle V_{REF}$	12≤V_{IN}≤25V		6	20	mV
Load Regulation	$\triangle V_{REF}$	1≤lo=20mA		6	25	MV
Output Noise Voltage	Vose	10Hz≤f≤10kHz, Tj=25℃(note 2)		50	6	mV
Long Term Stability		Ta=25℃, 1000Hrs (note 2)		5	25	mV
Output Short Circuit	lsc		-30	-100	-180	mA
Oscillator Section						
Initial Accuracy	f	Tj=25℃	47	52	57	kHz
Voltage Stability	△f/△Vcc	12≤Vcc≤25V		0.2	1	%
Temp Stability		Tmin≤T_A≤Tmax (note 2)		5		%
Amplitude	Vosc	Vpin 4 peak to peak		1.7		V
Error Amplifier Section						
Input Voltage	$V_{I(EA)}$	Vpin 1=2.5V	2.42	2.50	2.58	V
Input Bias Current	I_{BIAS}			-0.3	-2	μA
A_{VOL}		2≤Vo≤4V	60	90		dB
Unity Gain Bandwidth		Tj=25℃(note 2)	0.7	1	6.0	mHz
PSRR		12≤Vcc≤25V	60	70		dB
Output Sink Current	lsink	Vpin2=2.7V, Vpin 1=1.1V	2	6		mA
Output Source Current	lsource	Vpin 2=2.3V, Vpin 1=5V	-0.5	-0.8		mA
Vout High	V_{OH}	Vpin 2=2.3V, R_L=15kΩ to GND	5	6		V
Vout Low	V_{OL}	Vpin 2=2.7V, Vpin 1=1.1V		0.7	1.1	V

Current Sense Section						
Gain	Gv	(note 3, 4)	2.85	3	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	Vpin 1=5V(note 3)	0.9	1	1.1	V
PSRR		12≤Vcc≤25V		70		dB
Input Bias Current	I_{BIAS}			-2	-10	μA
Delay to Output		Vpin 3=0 to 2V		150	300	ns
Output Section						
Output Low Level	V_{OL}	lsink=20mA		0.1	0.4	V
		lsink=200mA		1.5	2.2	V
Output High Level	V_{OH}	lsource=20mA	13	13.5		V
		lsource=200mA	12	13.5		V
Rise Time	t_R	Tj=25℃, C_L=1nF (note 2)		50	150	ns
Fall Time	t_F	Tj=25℃, C_L=1nF(note 2)		50	150	ns
UVLO Saturation		Vcc=5V, lsink=10mA		0.7	1.2	V
Under-Voltage lockout Output Section						
Start Threshold	$V_{TH(ST)}$		14.5	16	17.5	V
Min. Operating Voltage After Turn On	V_{OPR}(min)		8.5	10	11.5	V
PWM Section						
Maximum Duty Cycle	D(MAX)		95	07	100	%
Minimum Duty Cycle	D(MIN)				0	%
Total Standby Current						
Start-up Current	I_{ST}			0.5	1	mA
Operating Supply Current	Icc(OPR)	Vpin 2=Vpin 3=0V		11	17	mA
Vcc Zener Voltage	Vz	Icc=25mA		34		V

APPLICATION CIRCUIT



OUTLINE DRAWING