Document Title

4Mx16 bit Page Mode Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft - Design Target	November 3, 2004	Preliminary
1.0	Finalize	April 06, 2005	Final

4M x 16 bit Page Mode Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 4M x16 bit
- Power Supply Voltage: 1.7~2.0V
- Three State Outputs
- Compatible with Low Power SRAM
- Support 4 page read mode
- Package Type: TBD

GENERAL DESCRIPTION

The K1S6416BCC is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports 4 page read operation and Industrial temperature range. The device supports dual chip selection for user interface. The device also supports internal Temperature Compensated Self Refresh mode for the standby power saving at room temperature range.

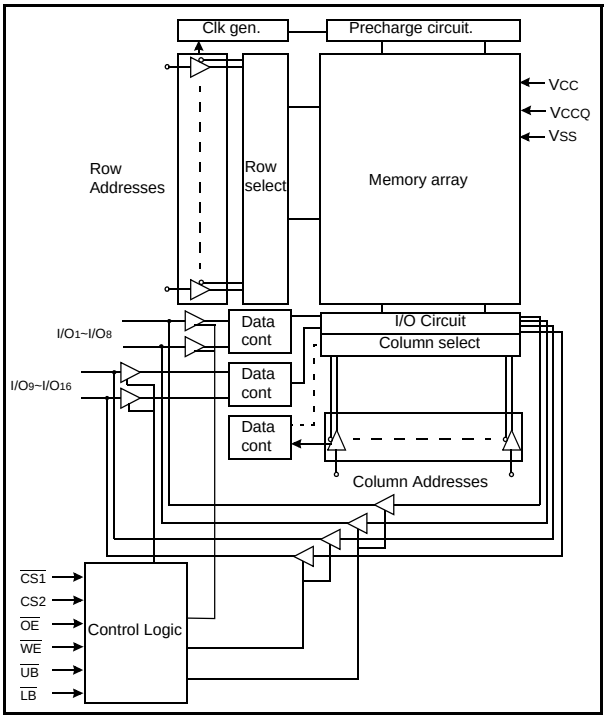
PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Speed (t_{RC})	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max.)	Operating (I_{CC2}, Max.)	
K1S6416BCC-I	Industrial(-40~85°C)	1.7~2.0V	70ns	120μA(< 40°C)	40mA	TBD
				180μA(< 85°C)		

PIN DESCRIPTION

TBD

FUNCTIONAL BLOCK DIAGRAM



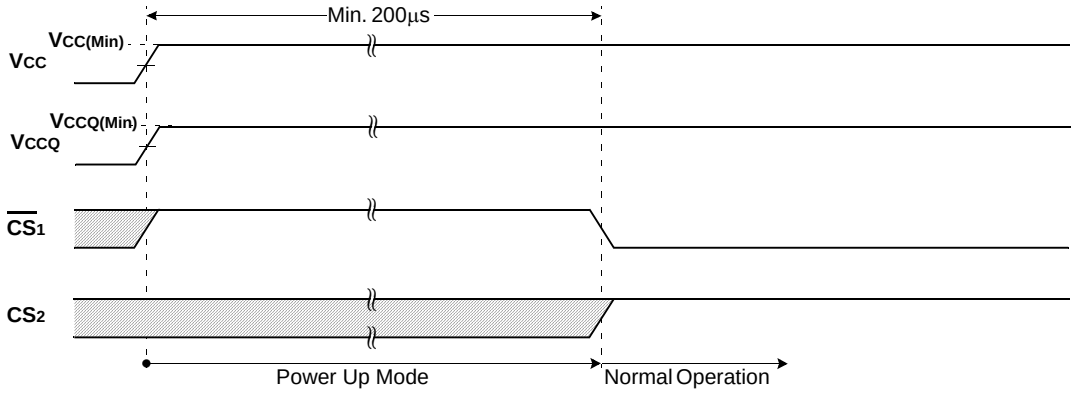
Name	Function	Name	Function
$\overline{CS}$1,CS2	Chip Select Inputs	Vcc/V_{CCQ}[2]	Power Supply(core / I/O)
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
A0~A21	Address Inputs	$\overline{LB}$	Lower Byte(I/O1~8)
I/O1~I/O16	Data Inputs/Outputs	NC	No Connection[1]

1) Reserved for future use
2) Vcc and V_{CCQ} should be the same level

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min. and V_{CCQ} min.=1.7V) for a minimum 200μs with $\overline{CS}1$=high.or CS2=low.

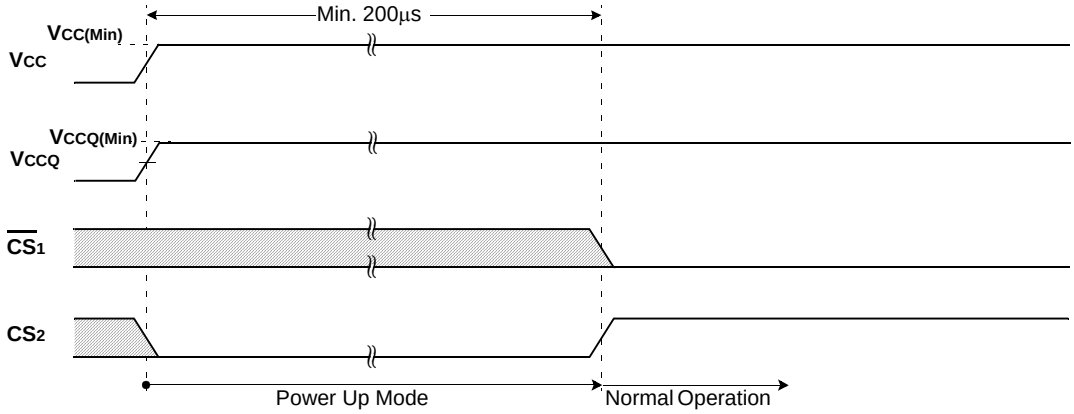
TIMING WAVEFORM OF POWER UP(1) ($\overline{CS}_1$ controlled)



POWER UP(1)

1. After V_{CC} reaches V_{CC}(Min.) and V_{CCQ}(Min.), wait 200μs with $\overline{CS}1$ high. Then the device gets into the normal operation.

TIMING WAVEFORM OF POWER UP(2) (CS_2 controlled)



POWER UP(2)

1. After V_{CC} reaches V_{CC}(Min.) and V_{CCQ}(Min.), wait 200μs with CS_2 low. Then the device gets into the normal operation.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	X[1]	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CCQ}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

PRODUCT LIST

Industrial Temperature Product(-40~85°C)	
Part Name	**Function**
K1S6416BCC	70ns, 1.85V

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	1.7	1.85	2.0	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	0.8 x V_{CCQ}	-	V_{CCQ}+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CCQ}+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to V_{CCQ}		-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS}_1$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{LB}$=$\overline{UB}$=V_{IH}, V_{IO}=Vss to V_{CCQ}		-1	-	1	μA
Average operating current	I_{CC2}	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, $\overline{CS}_1$=V_{IL}, CS_2=V_{IH}, $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	-	40	mA
Output low voltage	V_{OL}	I_{OL}=0.1mA		-	-	0.2	V
Output high voltage	V_{OH}	I_{OH}=-0.1mA		1.4	-	-	V
Standby Current(CMOS)	I_{SB1}[1)]	Other inputs=0~V_{CCQ} 1) $\overline{CS}_1$≥V_{CCQ}-0.2V, CS_2≥V_{CCQ}-0.2V($\overline{CS}_1$ controlled) or 2) 0V ≤ CS_2 ≤ 0.2V(CS_2 controlled)	< 40°C	-	-	120	μA
			< 85°C	-	-	180	μA

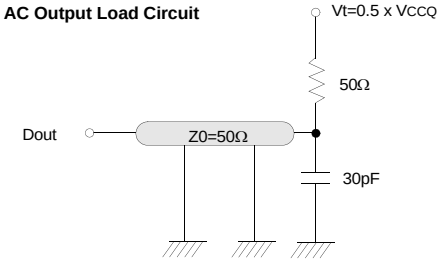
1. Standby mode is supposed to be set up after at least one active operation.after power up.
   I_{SB1} is measured after 60ms from the time when standby mode is set up.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{CCQ}-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x V_{CCQ}
Output load (See right): C_L=30pF

AC Output Load Circuit



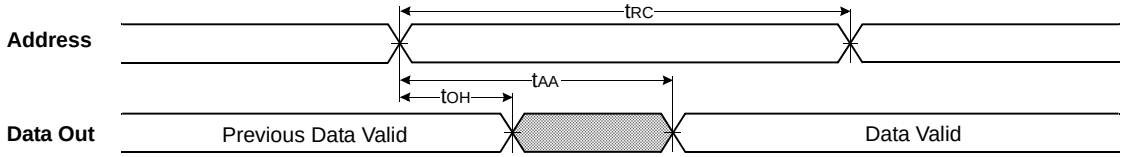
AC CHARACTERISTICS (V_{CC}=V_{CCQ}=1.7~2.0V, T_A=-40 to 85°C)

Parameter List		Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Common	$\overline{CS}$ High Pulse Width	t_{CSHP}	10	-	ns
Read	Address Access Time	t_{AA}	-	70	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	35	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	ns
	Output Hold from Address Change	t_{OH}	3	-	ns
	Page Cycle	t_{PC}	25	-	ns
	Page Access Time	t_{PA}	-	20	ns
Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Set-up Time	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55[1)]	-	ns
	$\overline{WE}$ High Pulse Width	t_{WHP}	5	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	25	ns
	Data to Write Time Overlap	t_{DW}	30	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	ns

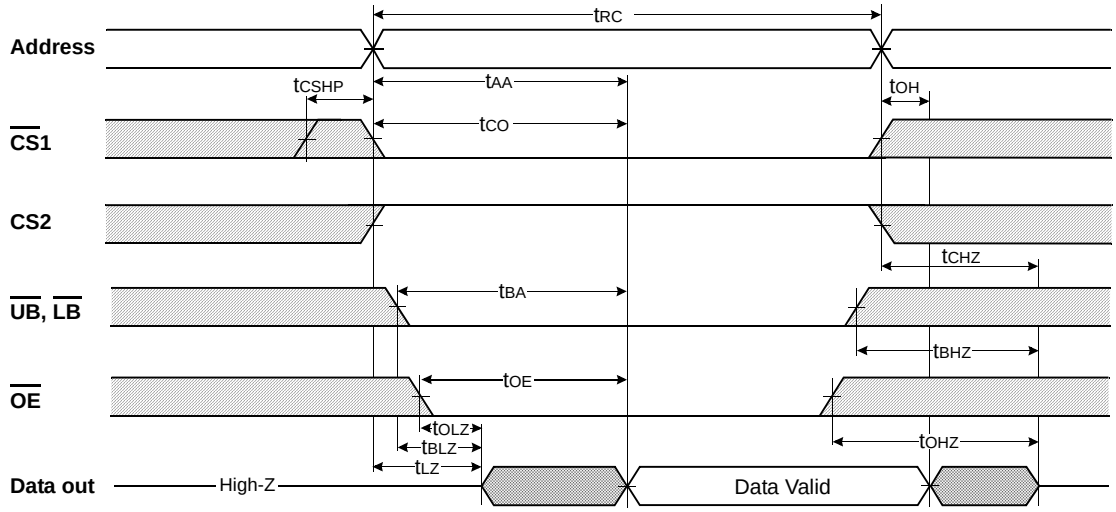
1. t_{WP}(min)=70ns for continuous write operation over 50 times.

TIMING DIAGRAMS

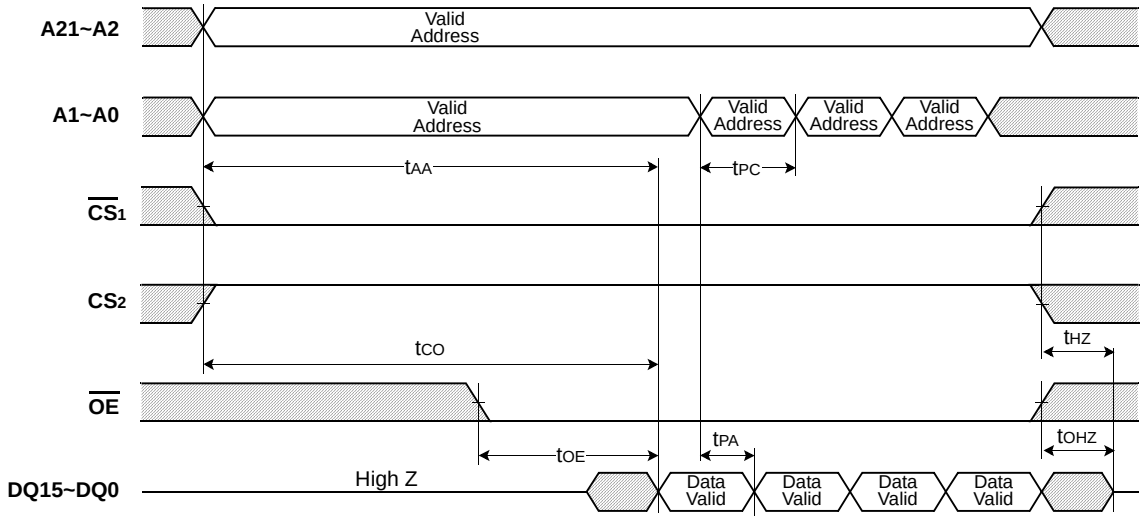
TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



TIMING WAVEFORM OF READ CYCLE(2)($\overline{WE}$=V_{IH})



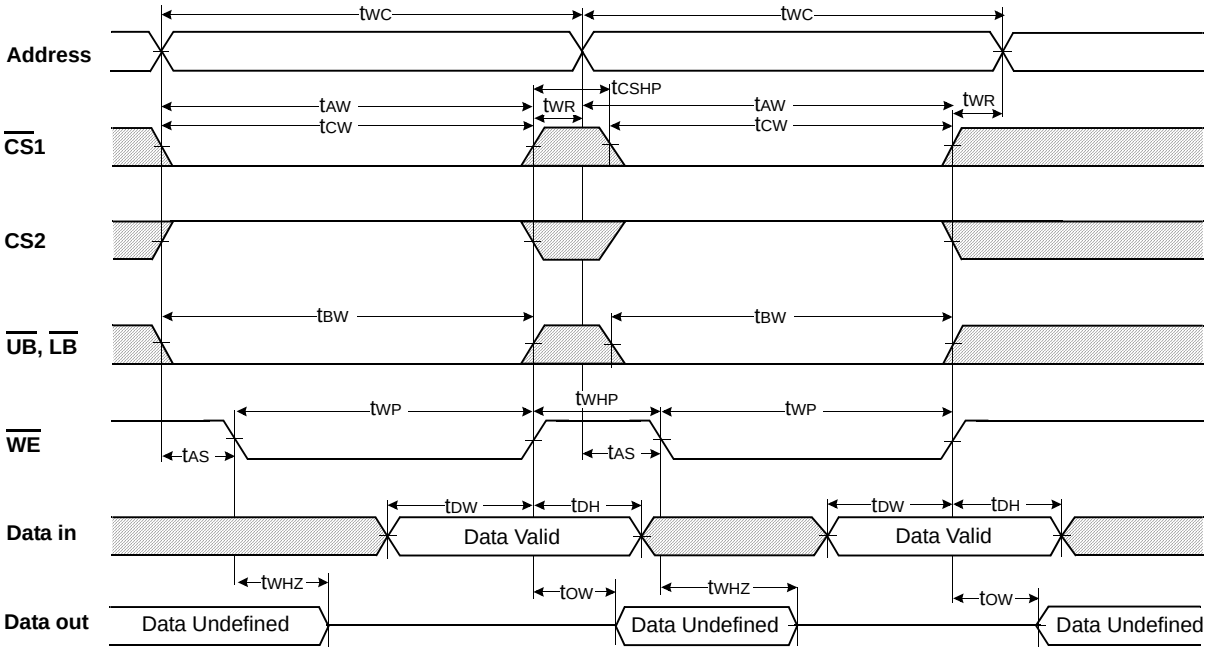
TIMING WAVEFORM OF PAGE CYCLE(READ ONLY)



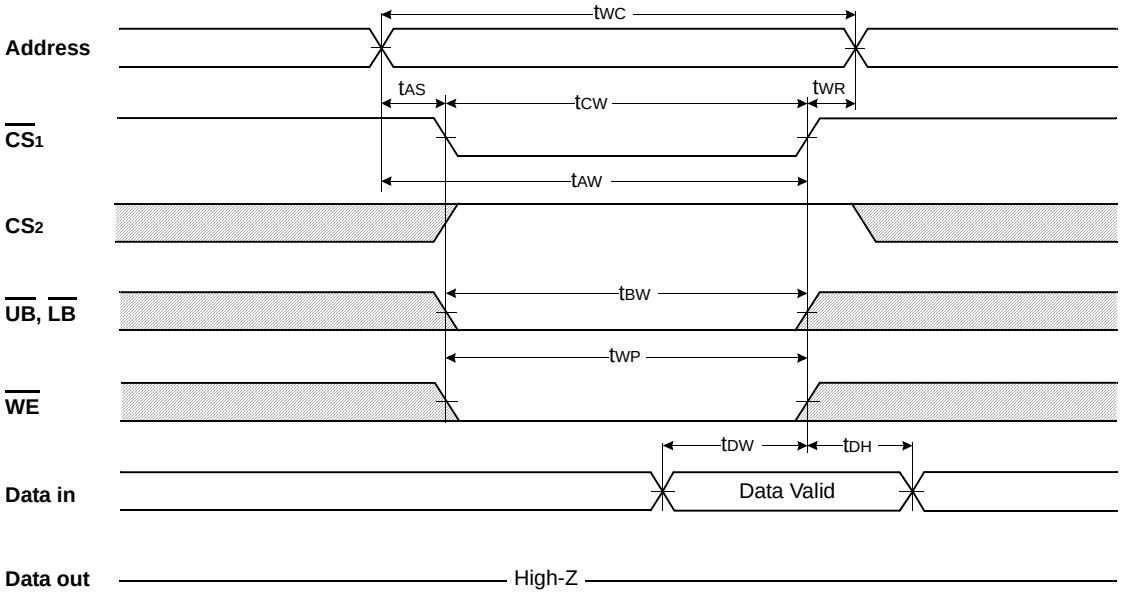
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).
4. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4us.

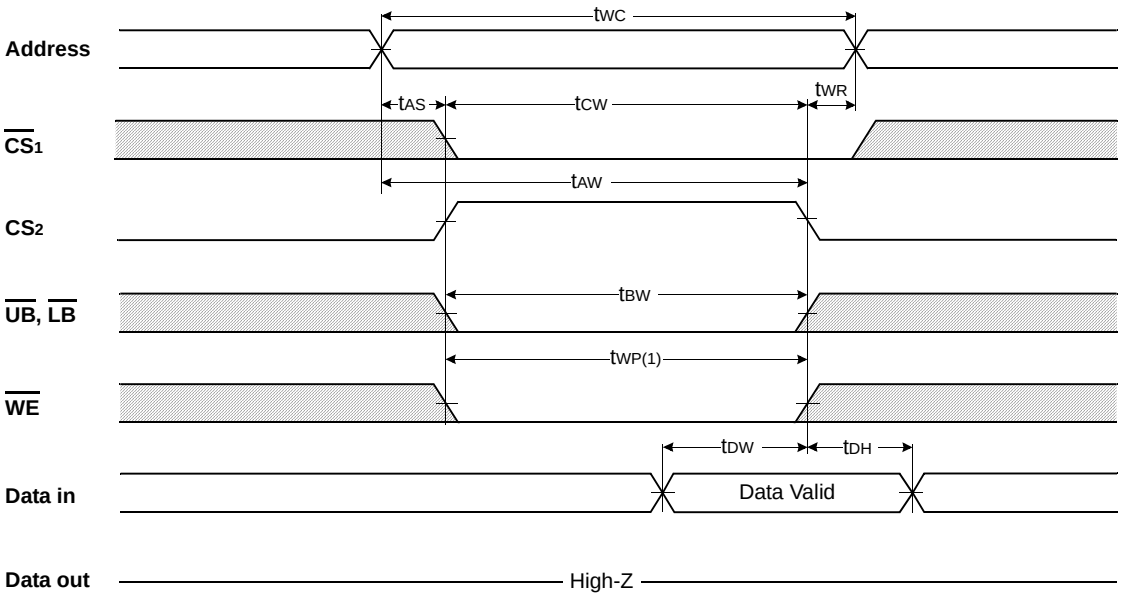
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



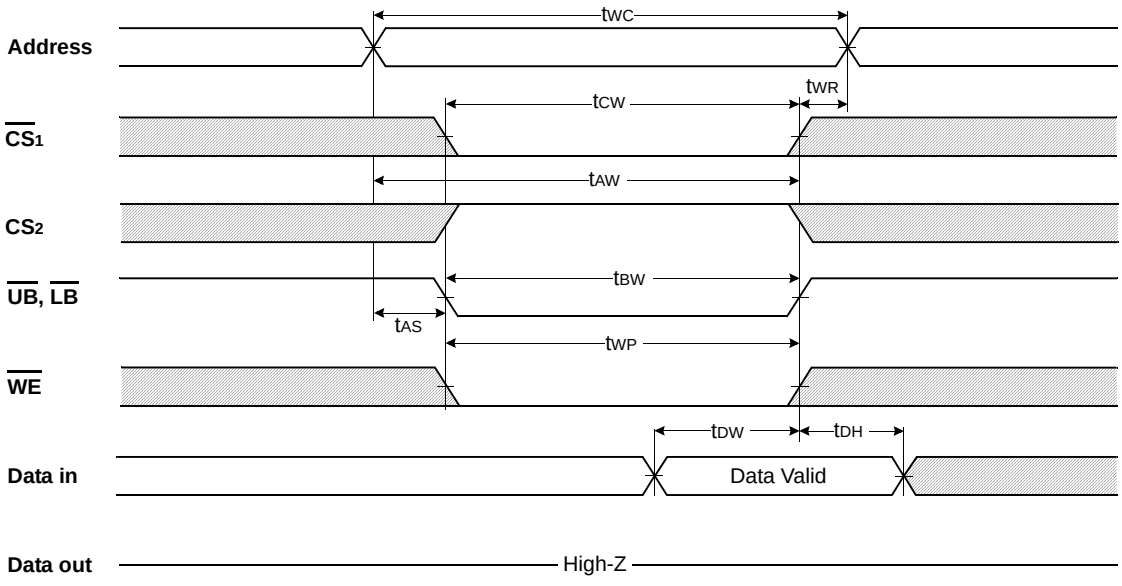
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$ and low $\overline{WE}$. A write begins when $\overline{CS_1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS_1}$ or $\overline{WE}$ going high.

PACKAGE DIMENSION

TBD