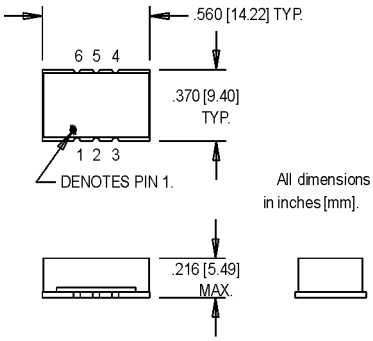
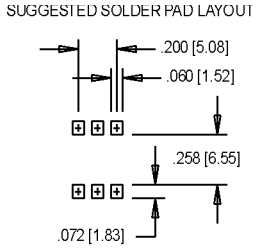
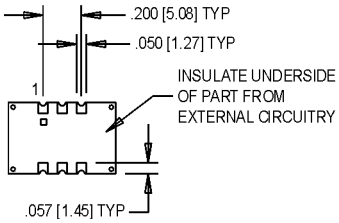
F17250B/F17350B & F17255B/F17355B Series

9x14 mm FR-4, 5.0 or 3.3 Volt, PECL, VCXO

- Former Champion Technologies, Inc. Product
- Clock Recovery, PLL, Optic Transmission Equipment, Digital Cross Connect Equipment







Ordering Information

F 1 7 X 5 X B D X -R 00.0000 MHz

- **Product Series**
  - 2: 5.0 Volt
  - 3: 3.3 Volt
- **Logic**
  - 0: PECL - 100E Logic
  - 5: PECL - 10E Logic
- **Temperature Range**
  - Blank: 0°C to +70°C
  - M: -40°C to +85°C
- **RoHS Compliance**
  - Blank: non-RoHS compliant part
  - -R: RoHS compliant part
- **Frequency (customer specified)**

Enable/Disable Control

Pin 1	Outputs	
	Pin 4	Pin 5
"0" Enables	Active	Active
"1" Disables	Low	High

Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Enable/Disable
3	Vss/Ground
4	Output
5	Output
6	+Vcc

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	75		180	MHz	
Operating Temperature	T_A	(See Ordering Information)				
Storage Temperature	Ts	-45		+125	°C	
Frequency Stability	ΔF/F					
Overall		Inclusive of Calibration, Temperature, Voltage, Load, and Aging				
0°C to +70°C				±30	ppm	
-40°C to +85°C				±50	ppm	
Aging						
1st Year		-4		+4	ppm	
10 Year		-10		+10	ppm	
Pullability/APR		±80		±140	ppm	75 to 156 MHz
		±60		±140	ppm	156.1 to 180 MHz
Control Voltage	Vc	0.5	2.5	4.5	V	F17250B & F17255B
		0.3	1.65	3.0	V	F17350B & F17355B
Linearity				10	%	Positive Monotonic Slope
Modulation Bandwidth	fm	10			kHz	±3dB
Input Impedance	Zin	50k			Ohms	@ 10 kHz
Input Voltage	Vcc	4.75	5.0	5.25	V	F17250B & F17255B
		3.135	3.3	3.465	V	F17350B & F17355B
Input Current	Icc			70	mA	
Output Type						PECL
Load						See Note 1
Symmetry (Duty Cycle)		45		55	%	Vcc -1.3 VDC
Output Skew				50	ps	
Logic "1" Level	Voh	Vcc -1.1		Vcc -0.88	V	50Ω into Vcc-2
Logic "0" Level	Vol	Vcc -1.95		Vcc -1.55	V	50Ω into Vcc-2
Rise Time	Tr			450	ps	50Ω into 20% to 80%
Fall Time	Tf			450	ps	50Ω into 80% to 20%
Enable Function		PECL low: output active PECL high: output disables				
Start up Time				10	ms	
Phase Jitter	ϕJ					
@ 155.52 MHz				1	ps RMS	Integrated 12 kHz - 20 MHz
Phase Noise (Typical)	**10 Hz**	**100 Hz**	**1 kHz**	**10 kHz**	**100 kHz**	**Offset from carrier**
@ 155.52 MHz	-40	-70	-100	-120	-140	dBc/Hz

1. PECL load - see load circuit diagram #5