CDB5378

Single-channel Seismic Evaluation System

Features

- Single-channel Seismic Acquisition Node
  - CS3301 geophone amplifier
  - CS5373A ΔΣ modulator + test DAC
  - CS5378 digital filter + PLL
  - Precision voltage reference
- On-board Microcontroller
  - SPI™ interface to digital filter
  - USB communication with PC
- PC Evaluation Software
  - Register setup & control
  - FFT frequency analysis
  - Time domain analysis
  - Noise histogram analysis

General Description

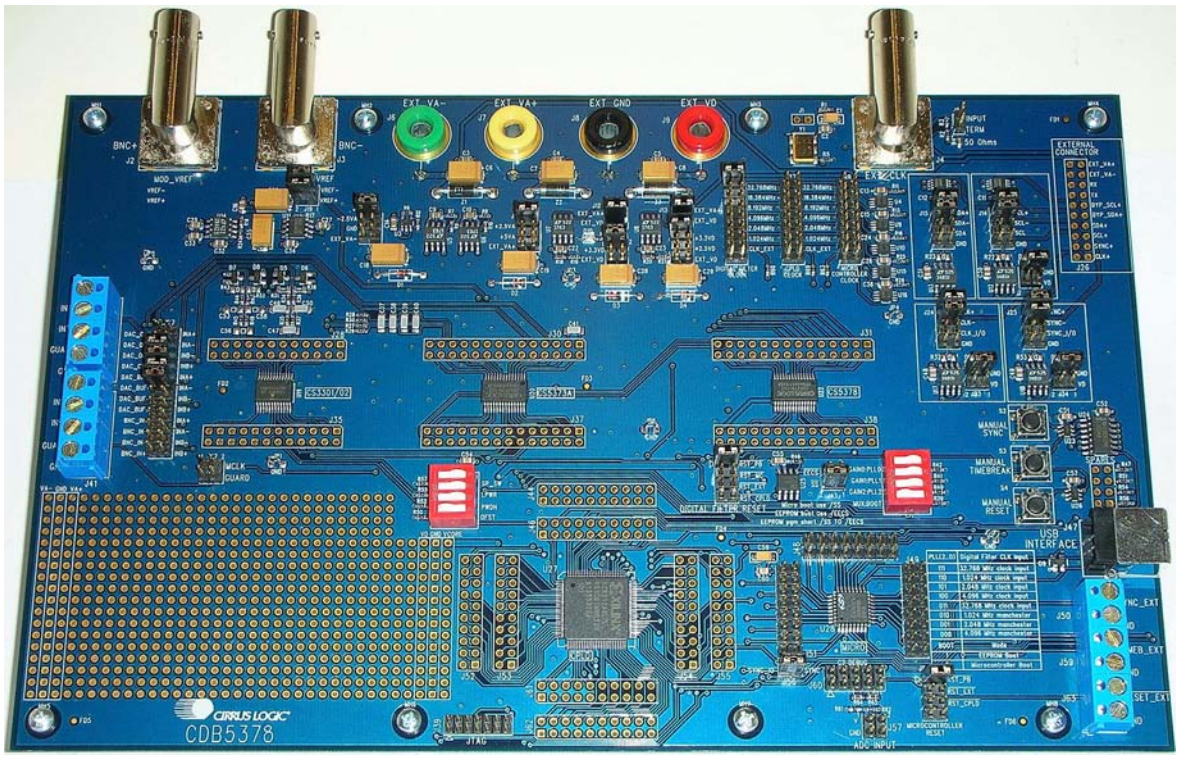
The CDB5378 board is used to evaluate the functionality and performance of the Cirrus Logic single-channel seismic chip set. Data sheets for the CS3301, CS5373A, and CS5378 devices should be consulted when using the CDB5378 evaluation board.

Screw terminals connect an external differential geophone or hydrophone sensor to the analog inputs of the measurement channel. An on-board test DAC creates precision differential analog signals for in-circuit performance testing without an external signal source.

The evaluation board includes an 8051-type microcontroller with hardware SPI™ and USB serial interfaces. The microcontroller communicates with the digital filter via SPI and with the PC evaluation software via USB. The PC software controls register and coefficient initialization and performs time domain, histogram, and FFT frequency analysis on captured data.

ORDERING INFORMATION

CDB5378	Evaluation Board



Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

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1. INITIAL SETUP

1.1 Kit Contents

The CDB5378 evaluation kit includes:

- CDB5378 Evaluation Board
- USB Cable (A to B)
- Software Download Information Card

The following are required to operate CDB5378, and are not included:

- Bipolar Power Supply with Banana Jack Outputs (+/-12 V @ 100 mA)
- Banana Jack Cables (4x)
- PC Running Windows 2000 or XP with an Available USB Port
- Internet Access to Download the Evaluation Software

1.2 Hardware Setup

To set up the CDB5378 evaluation board:

- Set all jumpers and DIP switches to their default settings (see next sections).
- With power off, connect the CDB5378 power inputs to the power supply outputs.
  VA- = -12 V
  VA+ = +12 V
  GND = 0 V
  VD = +12 V
- Connect the USB cable between the CDB5378 USB connector and the PC USB port.
- Proceed to the Software Setup section to install the evaluation software and USB driver.

1.2.1 Default Jumper Settings

J27					
Analog Input Selections					
DAC_OUT+	1	*	*	2	INA+
DAC_OUT-	3	*	*	4	INA-
DAC_OUT-	5	----------		6	INB-
DAC_OUT+	7	----------		8	INB+
DAC_BUF+	9	----------		10	INA+
DAC_BUF-	11	----------		12	INA-
DAC_BUF-	13	*	*	14	INB-
DAC_BUF+	15	*	*	16	INB+
BNC_IN+	17	*	*	18	INA+
BNC_IN-	19	*	*	20	INA-
BNC_IN-	21	*	*	22	INB-
BNC_IN+	23	*	*	24	INB+

Table 1. Analog Input Default Jumper Settings

J40				
Digital Filter RESET Selection				
RST_PB	1	----------		2
RST_MC	3	*	*	4
RST_EXT	5	*	*	6
RST_CPLD	7	*	*	8

J58				
Microcontroller RESET Selection				
RST_PB	1	----------		2
RST_EXT	3	*	*	4
RST_CPLD	5	*	*	6
	7	*	*	8

J43				
SPI Chip Select Input				
EECS	4	*	*	3	SS
SS	2	----------		1	SS

J56				
SYNC Source Selection				
SYNC_IO	2	----------	1	SYNC

Table 2. RESET, SPI, SYNC Default Jumper Settings

J19				
Voltage Reference Jumpers				
VREF-	4	----------		3
VREF+	2	----------		1

J10				
VA- Voltage Selection				
-2.5VA	1	----------		2
GND	3	*	*	4
EXT_VA-	5	*	*	6

J11				
VA+ Voltage Selection				
+2.5VA	1	----------		2
+5VA	3	*	*	4
EXT_VA+	5	*	*	6

J12				
VD Input Voltage Source				
EXT_VA+	1	*	*	2
EXT_VD	3	----------		4

J13				
VCORE Input Voltage Source				
EXT_VA+	1	*	*	2
EXT_VD	3	----------		4

J22				
VD Voltage Selection				
+3.3VD	1	----------		2
EXT_VD	3	*	*	4

J21				
VCORE Voltage Selection				
+3.3VD	1	----------		2
+2.5VD	3	*	*	4
EXT_VD	5	*	*	6

Table 3. VREF, Power Supplies Default Jumper Settings

J16, J17, J18				
Digital Filter, CPLD, Microcontroller Input Clock Selections				
32.768 MHz	1	----------		2
16.384 MHz	3	*	*	4
8.192 MHz	5	*	*	6
4.096 MHz	7	*	*	8
2.048 MHz	9	*	*	10
1.024 MHz	11	*	*	12
CLK_EXT	13	*	*	14
	15	*	*	16

J5				
Clock Input TERM				
50 Ohms	2	*	*	1

Table 4. Clock Default Jumper Settings

J15				
I2C Data				
SDA+	1	----------		2
SDA-	3	----------		4
SDA	5	*	*	6
GND	7	*	*	8

J14				
I2C Clock				
SCL+	1	----------		2
SCL-	3	----------		4
SCL	5	*	*	6
GND	7	*	*	8

J23				
I2C Clock Driver Enable				
GND	1	----------		2
VD	3	*	*	4

J24				
Clock Source				
CLK+	1	----------		2
CLK-	3	----------		4
CLK_I/O	5	*	*	6
GND	7	*	*	8

J25				
Sync Source				
SYNC+	1	----------		2
SYNC-	3	----------		4
SYNC_I/O	5	*	*	6
GND	7	*	*	8

J33				
Clock Driver Enable				
GND	1	----------		2
VD	3	*	*	4

J34				
Sync Driver Enable				
GND	1	----------		2
VD	3	*	*	4

Table 5. RS-485 Default Jumper Settings

1.2.2 Default DIP Switch Settings

S5				
* = down, - = up				
SP_SW	1	*	-	2
LPWR	3	*	-	4
PWDN	5	*	-	6
	7	*	-	8

S1				
* = down, - = up				
GAIN0:PLL0	1	*	-	2
GAIN1:PLL1	3	*	-	4
GAIN2:PLL2	5	*	-	6
MUX:BOOT	7	-	*	8

Table 6. DIP Switch Default Settings

1.3 Software Setup

1.3.1 PC Requirements

The PC hardware requirements for the Cirrus Seismic Evaluation system are:

- *Windows XP, Windows 2000, Windows NT*
- *Intel Pentium 600MHz or higher microprocessor*
- *VGA resolution or higher video card*
- *Minimum 64MB RAM*
- *Minimum 40MB free hard drive space*

1.3.2 Seismic Evaluation Software Installation

Important: For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

To install the Cirrus Logic Seismic Evaluation Software:

- Go to the Cirrus Logic Industrial Software web page (http://www.cirrus.com/industrialsoftware). Click the link for *"Cirrus Seismic Evaluation GUI"* to get to the download page and then click the link for *"Cirrus Seismic Evaluation GUI Release Vxx"* (*xx* indicates the version number).
- Read the software license terms and click *"Accept"* to download the *"SeismicEvalGUI_vxx.zip"* file to any directory on the PC.
- Unzip the downloaded file to any directory and a *"distribution"* sub-folder containing the installation application will automatically be created.
- Open the *"distribution"* sub-folder and run *"setup.exe"*. If the Seismic Evaluation Software has been previously installed, the uninstall wizard will automatically remove the previous version and you will need to run *"setup.exe"* again.
- Follow the instructions presented by the Cirrus Seismic Evaluation Installation Wizard. The default installation location is *"C:\Program Files\Cirrus Seismic Evaluation"*.

An application note, AN271 - *Cirrus Seismic Evaluation GUI Installation Guide*, is available from the Cirrus Logic web site with step-by-step instructions on installing the Seismic Evaluation Software.

1.3.3 USBXpress Driver Installation

Important: For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

The Cirrus Logic Seismic Evaluation Software communicates with CDB5378 via USB using the USBXpress driver from Silicon Laboratories (http://www.silabs.com). For convenience, the USBXpress driver files are included as part of the installation package.

To install the USBXpress driver (after installing the Seismic Evaluation Software):

- Connect CDB5378 to the PC through an available USB port and apply power. The PC will detect

CDB5378 as an unknown USB device.

- If prompted for a USB driver, skip to the next step. If not, using Windows Hardware Device Manager go to the properties of the unknown USB API device and select *"Update Driver"*.
- Select *"Install from a list or specific location"*, then select *"Include this location in the search"* and then browse to *"C:\Program Files\Cirrus Seismic Evaluation\Driver\"*. The PC will recognize and install the USBXpress device driver.
- After driver installation, cycle power to CDB5378. The PC will automatically detect it and add it as a USBXpress device in the Windows Hardware Device Manager.

An application note, AN271 - *Cirrus Seismic Evaluation GUI Installation Guide*, is available from the Cirrus Logic web site with step-by-step instructions on installing the USBXpress driver.

1.3.4 Launching the Seismic Evaluation Software

Important: For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

To launch the Cirrus Seismic Evaluation Software, go to:

- *Start ⇨ Programs ⇨ Cirrus Seismic Evaluation ⇨ Cirrus Seismic Evaluation*

or:

- *C:\Program Files\Cirrus Seismic Evaluation\SeismicGUI.exe*

For the most up-to-date information about the software, please refer to its help file:

- Within the software: *Help ⇨ Contents*

or:

- Start ⇨ Programs ⇨ *Cirrus Seismic Evaluation ⇨ SEISMICGUI*

or:

- *C:\Program Files\Cirrus Seismic Evaluation\SEISMICGUI.HLP*

1.4 Self-testing CDB5378

Noise and distortion self-tests can be performed once hardware and software setup are complete.

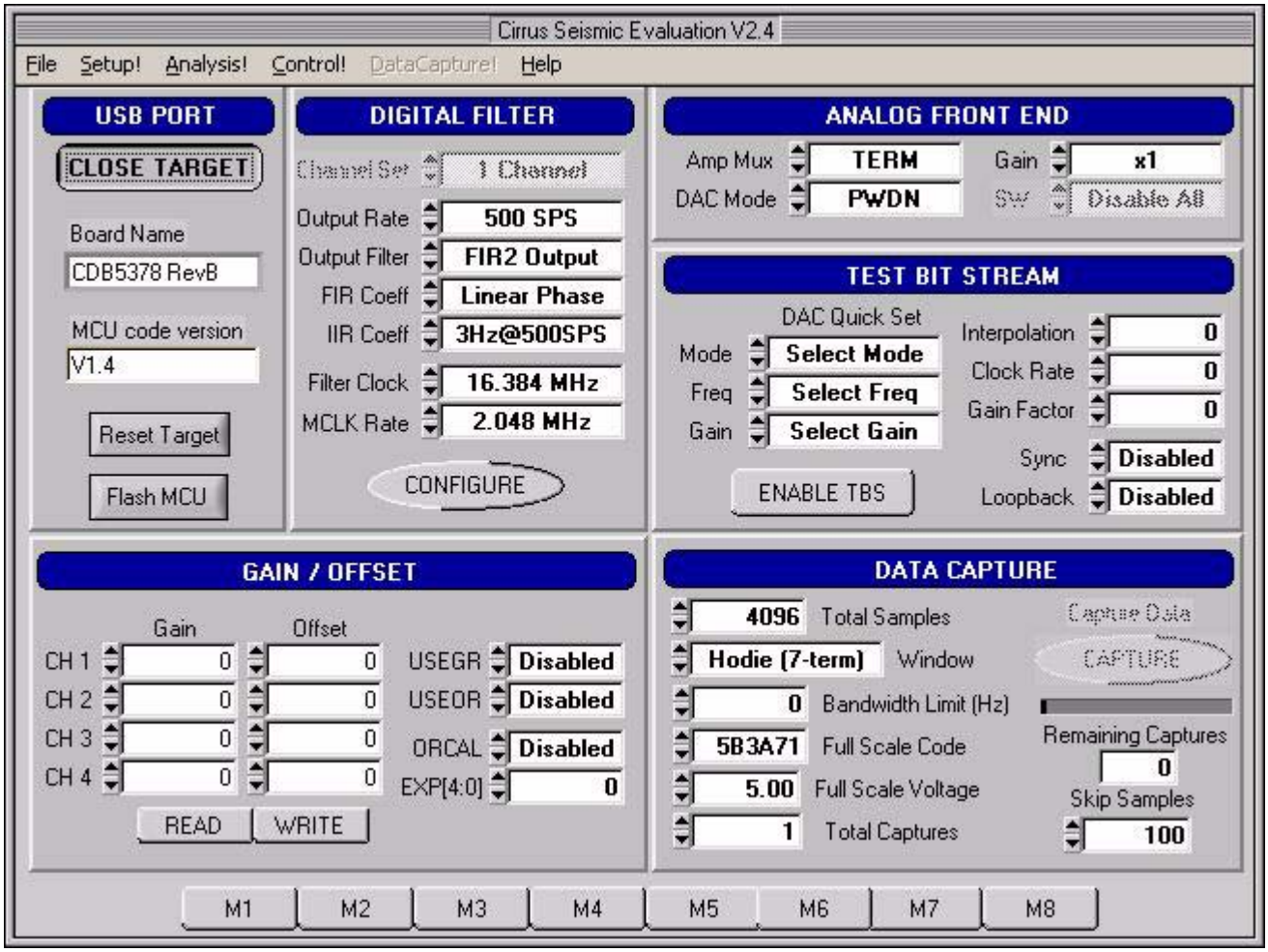
First, initialize the CDB5378 evaluation system:

- Launch the evaluation software and apply power to CDB5378.
- Click ‘OK’ on the **About** panel to get to the **Setup** panel.
- On the **Setup** panel, select *Open Target* on the **USB Port** sub-panel.
- When connected, the *Board Name* and *MCU code version* will be displayed.

1.4.1 Noise test

Noise performance of the measurement channel can be tested as follows:

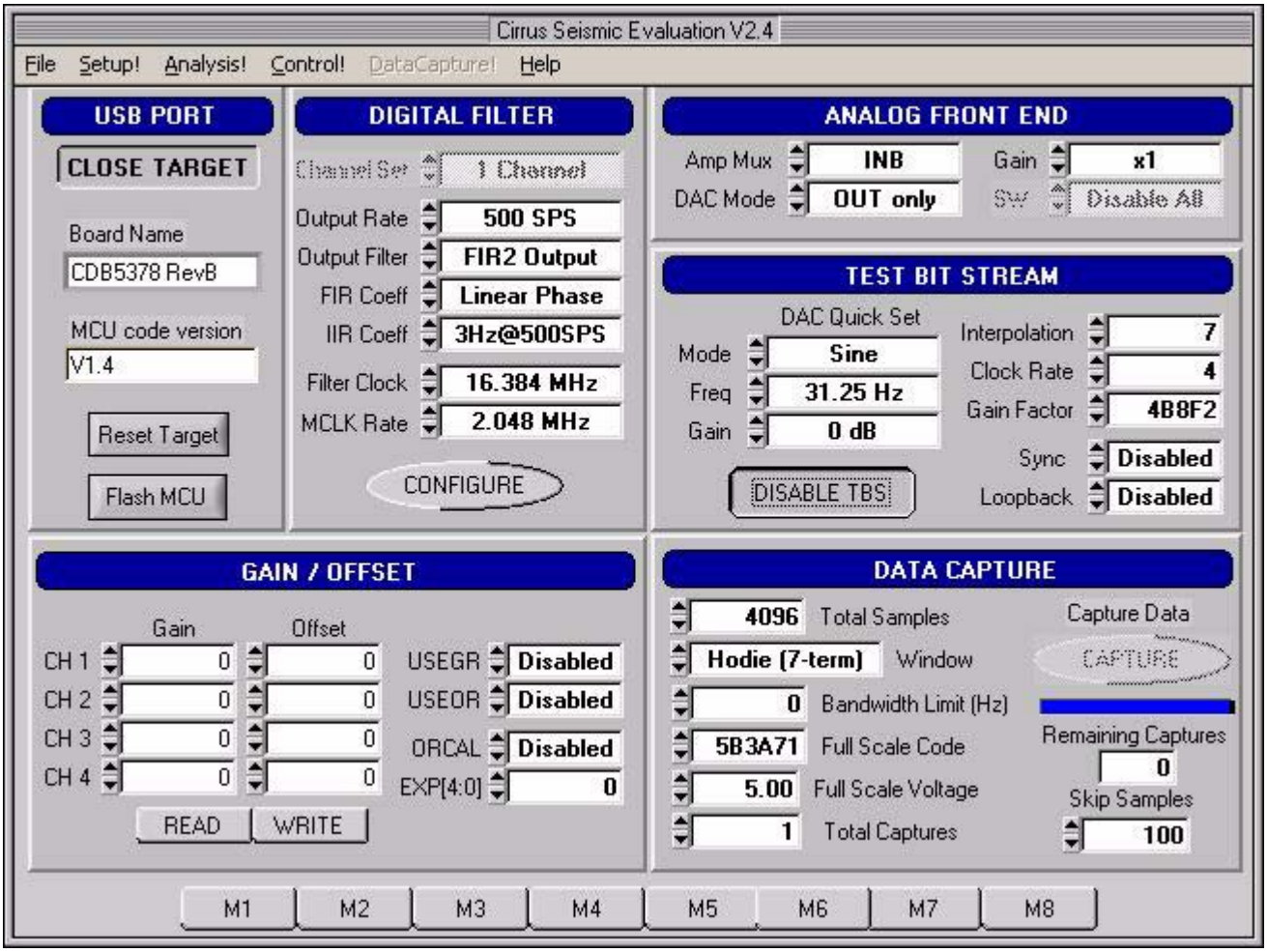
- Set the controls on the **Setup** panel to match the picture:



- Once the **Setup** panel is set, select *Configure* on the **Digital Filter** sub-panel.
- After digital filter configuration is complete, click *Capture* to collect a data record.
- Once the data record is collected, the **Analysis** panel is automatically displayed.
- Select *Noise FFT* from the *Test Select* control to display the calculated noise statistics.
- Verify the noise performance (S/N) is 124 dB or better.

1.4.2 Distortion Test

- Set the controls on the **Setup** panel to match the picture:



- Once the **Setup** panel is set, select *Configure* on the **Digital Filter** sub-panel.
- After digital filter configuration is complete, click *Capture* to collect a data record.
- Once the data record is collected, the **Analysis** panel is automatically displayed.
- Select *Signal FFT* from the *Test Select* control to display the calculated signal statistics.
- Verify the distortion performance (S/D) is 112 dB or better.

2. HARDWARE DESCRIPTION

2.1 Block Diagram

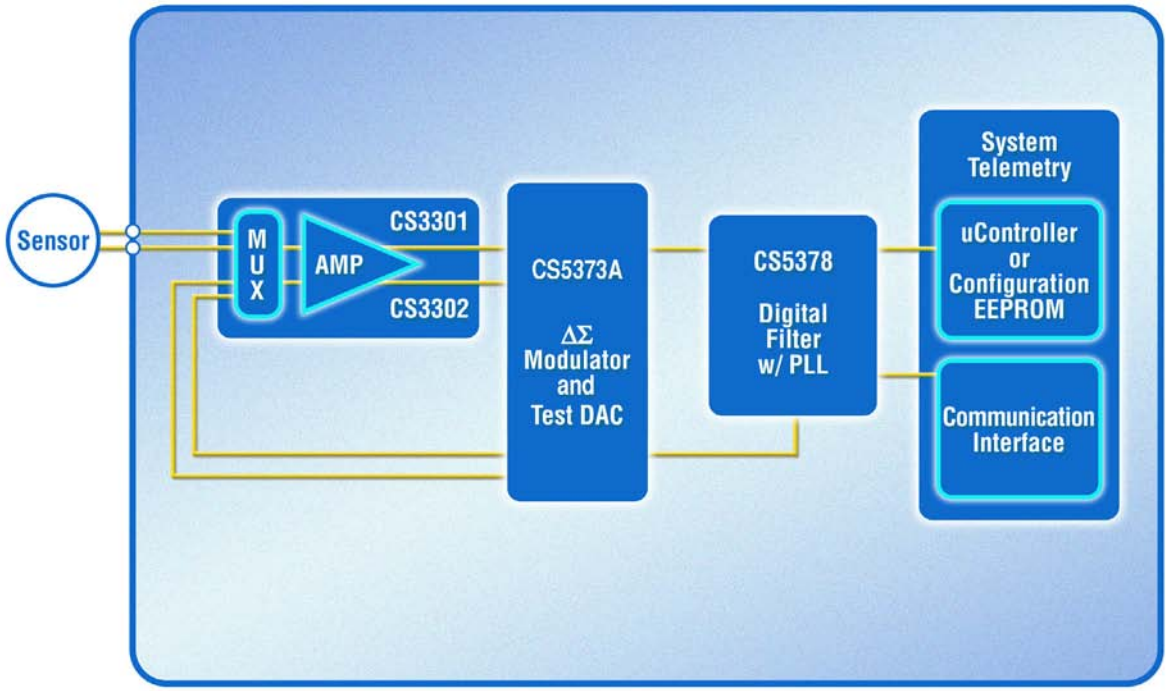


Figure 1. CDB5378 Block Diagram

Major blocks of the CDB5378 evaluation board include:

- **CS3301 Geophone Amplifier**
- **CS5373A ΔΣ Modulator + Test DAC**
- **CS5378 Digital Filter + PLL**
- **Precision Voltage Reference**
- **Interface CPLD**
- **Microcontroller with USB**
- **RS-485 Transceivers**
- **Voltage Regulators**

2.2 Analog Hardware

2.2.1 Analog Inputs

2.2.1.1 External Inputs - INA, INB, BNC

External signals into CDB5378 are from two major classes of sensors, moving coil geophones and piezo-electric hydrophones. Geophones are low-impedance sensors optimized to measure vibrations in land applications. Hydrophones are high-impedance sensors optimized to measure pressure in marine applications. Other sensors for earthquake monitoring and military applications are considered as geophones for this datasheet.

External signals connect to CDB5378 through screw terminals on the left side of the PCB. These screw terminals make connections to two external differential inputs, INA and INB. In addition, GND and GUARD connections are provided for connecting sensor cable shields, if present.

Signal Input	Screw Terminal
INA	J32
INB	J41

Table 7. Screw Terminal Input Connectors

BNC inputs for connecting external signals are not populated during board manufacture, but the empty PCB footprints exist and can be installed. The inner conductors of the BNC inputs make connections to the + and - differential signal traces, with the outer shields connected to ground. The BNC inputs can be connected to the INA or INB inputs through the input selection jumpers.

2.2.1.2 GUARD Output, GND Connection

By default, CDB5378 uses the CS3301 differential geophone amplifier. By replacing the amplifier and changing the pin 13 signal assignment (J42) it is possible to use the CS3302 hydrophone amplifier instead. The CS3301 amplifier expects an MCLK clock input to pin 13 while the CS3302 amplifier produces an analog GUARD signal output to pin 13.

The CS3302 hydrophone amplifier analog GUARD signal output is designed to actively drive the cable shield of a high impedance sensor with the common mode voltage of the sensor differential signal. This GUARD output on the cable shield minimizes leakage by minimizing the voltage differential between the sensor signal and the cable shield.

When using the CS3301 amplifier, which does not have a GUARD output, a separate GND screw terminal is provided for the sensor cable shield. When jumper J42 is set for the CS3301 amplifier the GUARD output screw terminal is left floating.

2.2.1.3 Internal Inputs - DAC_OUT, DAC_BUF

The CS5373A test DAC has two high-performance differential test outputs, a precision output (DAC_OUT) and a buffered output (DAC_BUF). These test outputs can be connected to the INA or INB inputs through the input selection jumpers.

By default, CDB5378 is populated with passive RC filter components on the INA inputs, and no filter components on the INB inputs (though the component footprints are present on the INB inputs). Because the CS5373A precision output will not tolerate significant loading, on CDB5378 the DAC_OUT signal should only jumper to the INB inputs. The CS5373A buffered outputs are less sensitive to the RC filter load and DAC_BUF can be jumpered to either the INA or INB inputs.

2.2.1.4 Input Protection

Sensor inputs must have circuitry to protect the analog electronics from voltage spikes. Geophone coils are susceptible to magnetic fields (especially from lightning) and hydrophones can produce large voltage spikes if located near an air gun source.

Discrete switching diodes quickly clamp the analog inputs to the power supply rails when the input voltage spikes. These diodes are reverse biased in normal operation and have low reverse bias leakage and capacitance characteristics to maintain high linearity on the analog inputs.

Specification	Value
Dual Series Switching Diode - ON Semiconductor	BAV99LT1
Surface Mount Package Type	SOT-23
Non-Repetitive Peak Forward Current (1 µs, 1 ms, 1 s)	2.0 A, 1.0 A, 500 mA
Reverse Bias Leakage (25 C to 85 C)	0.004 µA - 0.4 µA
Reverse Bias Capacitance (0 V to 5 V)	1.5 pF - 0.54 pF

2.2.1.5 Input RC Filters

Following the diode clamps is an RC filter network that bandwidth limits the sensor inputs into the amplifier to “chop the tops off” residual voltage spikes not clamped by the discrete diodes. In addition, all Cirrus Logic component ICs have built in ESD protection diodes guaranteed to 2000 V HBM / 200 V MM (JEDEC standard). The small physical size of these ESD diodes restricts their current capacity to 10 mA.

For land applications using the CS3301 amplifier, the INA input has a common mode and differential RC filter. The common mode filter sets a low-pass corner to shunt very-high-frequency components to ground with minimal noise contribution. The differential filter sets a low-pass corner high enough not to affect the magnitude response of the measurement bandwidth.

For marine applications that use the CS3302 amplifier, the inherent capacitance of the piezoelectric sensor is combined with large resistors connected to the input signal common mode to create an analog high-pass RC filter to eliminate the low-frequency components of ocean noise. Following the high-pass common mode filter is a differential low-pass filter to reject high-frequency signals into the amplifier. The cutoff frequency for the low-pass filter is high enough not to affect the magnitude response of the measurement bandwidth.

By default, CDB5378 uses the CS3301 differential geophone amplifier and so the input RC filter on the INA inputs are set for land applications. Marine applications using the CS3302 amplifier will need to modify the input RC filter components.

Land Common Mode Filter Specification	Value
Common Mode Capacitance	10 nF ± 10%
Common Mode Resistance	200 Ω
Common Mode -3 dB Corner @ 6 dB/octave	80 kHz ± 10%

Land Differential Filter Specification	Value
Differential Capacitance	10 nF ± 10%
Differential Resistance	200 Ω + 200 Ω = 400 Ω
Differential -3 dB Corner @ 6 dB/octave	40 kHz ± 10%

Marine Common Mode Filter Specification	Value
Hydrophone Group Capacitance	128 nF ± 10%
Common Mode Resistance	825 kΩ || 825 kΩ = 412 kΩ
-3 dB Corner @ 6 dB/octave	3 Hz ± 10%

Marine Differential Filter Specification	Value
Differential Capacitance	10 nF ± 10%
Differential Resistance	200 Ω + 200 Ω = 400 Ω
-3 dB Corner @ 6 dB/octave	40 kHz ± 10%

2.2.1.6 Common Mode Bias

Differential analog signals into the CS3301/02 amplifiers are required to be biased to the center of the power supply voltage range, which for bipolar supplies is near ground potential. This common mode bias voltage is created by buffering the voltage reference, which is nominally +2.5 V relative to the VA- power supply.

By default, CDB5378 uses the CS3301 differential geophone amplifier and so the common mode bias resistors on the INA inputs are set for land applications. Marine applications using the CS3302 amplifier will need to modify the default common mode bias resistors.

Resistors to create the common mode bias are normally selected based on the sensor impedance and may need to be modified from the CDB5378 defaults depending on the sensor used. Refer to the recommended operating bias conditions for the selected sensor, which are available from the sensor manufacturer.

Specification	Value
Geophone Sensor Bias Resistance	20 kΩ || 20 kΩ = 10 kΩ
Hydrophone Sensor Bias Resistance	18 MΩ || 18 MΩ = 9 MΩ

2.2.2 Differential Amplifiers

The CS3301/02 amplifiers act as a low-noise gain stage for internal or external differential analog signals.

Analog Signals	Description
INA	Sensor analog input
INB	Test DAC analog input
OUTR, OUTF	Analog rough / fine outputs
GUARD	CS3302 guard output (jumper selection)

Digital Signals	Description
MUX[0..1]	Input mux selection
GAIN[0..2]	Gain range selection
PWDN	Power down mode enable
CLK	CS3301 clock input (jumper selection)

2.2.2.1 MCLK Input vs. GUARD Output

By default, CDB5378 uses the CS3301 geophone amplifier which is chopper stabilized. The CS3301 connects pin 13 to a clock source (MCLK) to run the chopper circuitry synchronous to the modulator analog sampling clock. The CS3302 hydrophone amplifier is not chopper stabilized (with 1/f noise typically buried below the low-frequency ocean noise) to achieve very high input impedance. To minimize leakage from high-impedance sensors connected to the CS3302 amplifier, pin 13 produces a GUARD signal output to actively drive a sensor cable shield with the common mode voltage of the sensor signal.

Comparing the CS3301 and CS3302 amplifiers, the functionality of pin 13 (MCLK input vs. GUARD output) is the only external difference. CDB5378 can be converted to use either the CS3301 or CS3302 by replacing the amplifier device and properly setting the pin 13 jumper (J42). By default this jumper is not populated and has a shorting trace between pins on the back side of the PCB. Converting between amplifier types requires ***carefully*** cutting the default short and installing a jumper. A replacement amplifier can be requested as a sample from your local Cirrus Logic sales representative.

2.2.2.2 Rough-Fine Outputs - OUTR, OUTF

The analog outputs of the CS3301/02 differential amplifiers are split into rough-charge and fine-charge signals for input to the CS5373A ΔΣ modulator. The amplifier outputs include integrated series resistors to create the anti-alias RC filters required to limit the modulator input signal bandwidth.

Analog signal traces out of the CS3301/02 amplifiers and into the CS5373A modulator are 4-wire INR+ / INF+ / INF- / INR- quad groups, and are routed with INF+ and INF- as a traditional differential pair and INR+ and INR- as guard traces outside the respective INF+ and INF- traces.

2.2.2.3 Anti-alias RC Filters

The CS5373A ΔΣ modulator is 4th order and high-frequency input signals can cause instability. Simple single-pole anti-alias RC filters are required between the CS3301/02 amplifier outputs and the CS5373A modulator inputs to bandwidth limit analog signals into the modulator.

The CS3301/02 amplifier outputs include internal series resistors, so a differential anti-alias RC filter is created by connecting 20 nF of high-linearity differential capacitance (2x 10 nF C0G) between each half of the rough and fine signals. External 0-ohm resistors are included in series with the amplifier internal anti-alias resistors to support testing of other anti-alias RC filter configurations.

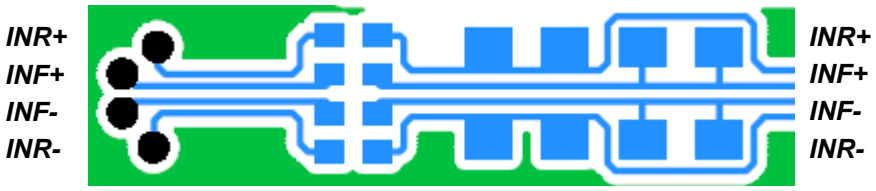


Figure 2. Quad Group Routing of RC Filter Components

2.2.3 Delta-Sigma Modulator

The CS5373A ΔΣ modulator performs the A/D function for the differential analog signal from the CS3301/02 amplifier. The digital output from the modulator is an oversampled ΔΣ bit stream.

Analog Signals	Description
INR, INF	Modulator analog rough / fine inputs
VREF	Voltage reference analog inputs

Digital Signals	Description
MDATA	Modulator delta-sigma data output
MFLAG	Modulator over-range flag output
MCLK	Clock input
MSYNC	Synchronization input

2.2.3.1 Rough-Fine Inputs - INR, INF

The modulator analog inputs are separated into rough and fine signals, each of which has a differential anti-alias RC filter to limit the input signal bandwidth.

2.2.4 Delta-Sigma Test DAC

The CS5373A ΔΣ DAC creates differential analog signals for system tests. Multiple test modes are available and their use is described in the CS5373A data sheet.

Analog Signals	Description
OUT	Precision differential analog output
BUF	Buffered differential analog output
CAP	Capacitor connection for internal anti-alias filter
VREF	Voltage reference analog inputs

Digital Signals	Description
TDATA	Delta-sigma test data input
MCLK	Clock input
MSYNC	Synchronization input
MODE[0..2]	Test mode selection
ATT[0..2]	Attenuation range selection

2.2.4.1 Precision Output - DAC_OUT

The CS5373A test DAC has a precision output (DAC_OUT) that is routed to the input selection jumper. This output is sensitive to loading, and on CDB5378 should only be jumpered into the INB input which does not have passive RC filter components installed. The input impedance of the CS3301/02 amplifiers are high enough that the DAC precision output can be connected to the INB input directly.

2.2.4.2 Buffered Output - DAC_BUF

The CS5373A test DAC has a buffered output (DAC_BUF) that is also routed to the input selection jumper. This output is less sensitive to loading than the precision output, and can be jumpered into either the INA or INB input without affecting performance. The buffered output can also drive a sensor attached to the input screw terminals, provided the sensor meets the impedance requirements specified in the CS5373A data sheet.

2.2.5 Voltage Reference

A voltage reference on CDB5378 creates a precision voltage from the regulated analog supplies for the CS5373A VREF input. Because the voltage reference output is generated relative to the negative analog power supply, VREF+ is near GND potential for bipolar power supplies.

Specification	Value
Precision Reference - Linear Tech	LT1019AIS8-2.5
Surface Mount Package Type	SO-8
Output Voltage Tolerance	+/- 0.05%
Temperature Drift	10 ppm / degC
Quiescent Current	0.65 mA
Output Voltage Noise, 10 Hz - 1 kHz	4 ppm_{RMS}
Ripple Rejection, 10 Hz - 200 Hz	> 100 dB

2.2.5.1 VREF_MOD

The voltage reference output is provided to the CS5373A modulator and test DAC through a low-pass RC filter. By filtering the voltage reference input to the device, high-frequency noise is eliminated and any signal-dependent sampling of VREF is isolated. The voltage reference signal is routed as a differential pair from the large RC filter capacitor to control the sensitive VREF source-return currents and keep them out of the ground plane. In addition to the RC filter function, the 100 uF filter capacitor provides a large charge-well to help settle voltage reference sampling transients.

2.2.5.2 Common Mode Bias

A buffered version of the voltage reference is created as a low-impedance common mode bias source for the analog signal inputs. The bias resistors connected between the buffered voltage reference and each analog signal input half depends on the sensor type and should be modified to match the sensor manufacturer recommendations.

2.3 Digital Hardware

2.3.1 Digital Filter

The CS5378 digital filter performs filtering and decimation of the ΔΣ bit stream from the CS5373A modulator. It also creates a ΔΣ test bit stream output to create analog test signals in the CS5373A DAC.

The CS5378 requires several control signal inputs from the external system.

Control Signals	Description
CLK	Master clock input.
RESETz	Reset input, active low
SYNC	Master synchronization input, rising edge triggered
TIMEB	Time Break input, rising edge triggered

Configuration and data collection are through the SPI port.

SPI1 Signals	Description
DRDYz	Data ready output, active low
SCK	Serial clock
MISO	Master in / slave out serial data
MOSI	Master out / slave in serial data
SS:EECSz	Serial chip select, active low

Modulator ΔΣ data is input through the modulator interface, and test DAC ΔΣ data is generated by the test bit stream generator.

Modulator Signals	Description
MCLK	Modulator clock output
MSYNC	Modulator synchronization output
MDATA	Modulator delta-sigma data inputs
MFLAG	Modulator over-range flag inputs
TBSDATA	Test DAC delta-sigma data output

Amplifier, modulator and test DAC pin settings are controlled through the GPIO port.

GPIO Signals	Description
GPIO[0]:MUX[0]	Amplifier input mux selection
GPIO[1..3]:MODE[0..2]	Test DAC mode selection
GPIO[4..6]:GAIN[0..2]	Amplifier gain / test DAC attenuation
GPIO[7]:MUX[1]	Amplifier input mux selection

2.3.1.1 Reset Options - BOOT, PLL

Immediately following the reset signal rising edge, the CS5378 digital filter latches the states of the GPIO[4..6]:PLL[0..2] and GPIO7:BOOT pins. The reset states of the GPIO[4..6]:PLL[0..2] pins select the master clock input frequency and type, while the reset state of the GPIO7:BOOT pin selects how the CS5378 digital filter receives configuration data.

At reset the CS5378 digital filter GPIO pins default as inputs with weak pull-up resistors enabled. If left floating, the GPIO state reads high at reset because of the internal pull-up resistor. A four-position DIP switch on CDB5378 (S5) can connect 10kΩ pull-down resistors to the GPIO[4..6]:PLL[0..2] or GPIO7:BOOT pins so they will read low at reset. Because the pin states are latched at reset, GPIO pins can be programmed and used normally after reset without affecting the PLL and BOOT selections.

Detailed information about the PLL input clock and BOOT mode selections at reset can be found in the CS5378 data sheet.

2.3.1.2 Configuration - SPI Port

On CDB5378, configuration of the digital filter is through the SPI port by the on-board 8051 microcontroller, which receives commands from the PC evaluation software via the USB interface. Evaluation software commands can write/read digital filter registers, specify digital filter coefficients and start/stop digital filter operation. Alternately, the digital filter can automatically load configuration information from an on-board serial EEPROM.

The configuration method for the digital filter is selected by the BOOT signal from a dip switch (S1, #4). By default the BOOT signal is set low (S1, #4 - LO) to indicate configuration information is written by the microcontroller. If BOOT is instead set high (S1, #4 - HI), the digital filter attempts to automatically read configuration information from the serial EEPROM after reset. Configuration information is initially written into the serial EEPROM by jumpering its chip select input (EECS) to the microcontroller chip select output (SS) and sending EEPROM programming commands and data from the PC evaluation software.

2.3.1.3 Phase Locked Loop

To make synchronous analog measurements throughout a distributed system, a synchronous system clock is required to be provided to each measurement node. For evaluation testing purposes, a BNC clock input on CDB5378 can receive an external system clock and create a synchronous local clock using the CS5378 PLL.

The system clock into the BNC clock input is applied to the CS5378 CLK input by selecting CLK_EXT on the DIGITAL FILTER CLOCK jumper (J16). The CS5378 PLL input frequency is specified at reset by the state of the GPIO[4..6]:PLL[0..2] pins, as detailed in the CS5378 data sheet.

Specification	Value
Input Clock Frequency	1.024, 2.048, 4.096 MHz
Distributed Clock Synchronization	± 240 ns
Maximum Input Clock Jitter, RMS	1 ns

Specification	Value
PLL Internal Clock Frequency	32.768 MHz
Maximum Jitter, RMS	300 ps
Loop Filter Architecture	Internal

If no system clock is supplied to CDB5378, the DIGITAL FILTER CLOCK jumper (J16) can select a PLL input clock from a local oscillator. Using a clock divider, the on-board oscillator produces 1.024 MHz, 2.048 MHz, 4.096 MHz and 32.768 MHz clock outputs that can be applied to the CS5378 CLK input.

Specification	Value
Oscillator - Citizen 32.768 MHz VCXO	CSX750VBEL32.768MTR
Surface Mount Package Type	Leadless 6-Pin, 5x7 mm
Supply Voltage, Current	3.3 V, 11 mA
Frequency Stability, Pullability	± 50 ppm, ± 90 ppm
Startup Time	4 ms

Specification	Value
Clock Divider - TI LittleLogic D-Flop	SN74LVC2G74DCTR
Surface Mount Package Type	SSOP8-199
Supply Voltage, Current	3.3 V, 10 µA

2.3.2 Interface CPLD

A Xilinx CPLD is included on CDB5378 (XCR3128XL-10VQ100I) as an interface between the CS5378 digital filter and the microcontroller. By default the CPLD only passes through the interface signals, but can be reprogrammed to disconnect the on-board 8051 microcontroller and connect to another external microcontroller through the spare dual-row headers. Control signals taken off the CDB5378 board to an external microcontroller should pair with a ground return wire to maintain signal integrity.

Free software tools and an inexpensive hardware programmer for the Xilinx CPLD are available from the internet (http://www.xilinx.com). The hardware programmer interfaces with the Xilinx JTAG programming port (J39) on CDB5378. Note that early versions of the Xilinx WebPack tools (7.1i SP1 and earlier) have a bug in the JEDEC programming file for the CPLD included on CDB5378, and WebPack version 7.1i SP2 or later is required.

Included below is the default Verilog HDL file used by CDB5378 inside the interface CPLD. Comparing the input and output definitions of this file with the CPLD schematic pinout should demonstrate how signals are selected and passed through from the microcontroller to the CS5378 digital filter. Several signal connections to the CPLD are not defined in the default HDL file, but are routed to the CPLD on CDB5378 for convenience during custom reprogramming.

```
//////////////////////////////////////////////////////////////////////
// MODULE:       CDB5378 top module
//
// FILE NAME:    Top module for connecting CS5378 to C8051F320
// VERSION:      1.0
// DATE:         February 1, 2006
// COPYRIGHT:    Cirrus Logic, Inc.
//
// CODE TYPE:    Register Transfer Level
//
// DESCRIPTION:  This module includes assignments for signals between
//               the serial port of CS5378 and the SLAB micro.
//
//////////////////////////////////////////////////////////////////////


module cdb5378(
      sck_mc,         // 5  I serial clock from printer port
      miso_mc,        // 6  O serial output
      mosi_mc,        // 7  I serial input
      ssz_mc,         // 8  I slave select (active low)
      drdyz_mc,       // 9  O data ready (active low)

      sck,            // 61 O serial clock
      miso,           // 60 I serial output
      mosi,           // 58 O serial input
      ssz,            // 57 O slave select (active low)
      drdyz,          // 56 I data ready (active low)

      sync_pb,        // 94 I pushbutton sync
      sync_mc,        // 13 I sync from micro
      sync,           // 53 O sync to CS5378

      timeb_pb,       // 93 I pushbutton timebreak
      timeb_mc,       // 14 I timebreak from micro
      timeb,          // 52 O timebreak to CS5378

      cpld0_mc,       // 16 I reset from micro
      reset_cpld      // 1  O reset to CS5378
);

      ////////////////////
      // input signals
      ////////////////////

      input sck_mc, mosi_mc, ssz_mc;
      input miso, drdyz;
      input sync_pb, sync_mc;
      input timeb_pb, timeb_mc;
      input cpld0_mc;


      ////////////////////
      //output signals
      ////////////////////

      output miso_mc, drdyz_mc;
      output sck, mosi, ssz;
      output sync, timeb;
      output reset_cpld;


      ////////////////////////
      // signal assignments
      ////////////////////////

      assign sck = sck_mc;
      assign miso_mc = miso;
      assign mosi = mosi_mc;
      assign ssz = ssz_mc;
      assign drdyz_mc = drdyz;
      assign reset_cpld = cpld0_mc;
      assign sync = sync_pb | sync_mc;
      assign timeb = timeb_pb | timeb_mc;

      endmodule
```

Figure 3. CPLD Default Signal Assignments

2.3.3 Digital Control Signals

The reset, synchronization and timebreak signals to the CS5378 digital filter can be generated by push buttons, received from external inputs or generated by the on-board microcontroller. By default, the microcontroller reset (CPLD0_MC), push button SYNC_PB and push button TIMEB_PB signals are connected through the interface CPLD to the CS5378 digital filter RESETz, SYNC and TIMEB inputs.

A four-position DIP switch on CDB5378 (S5) sets static digital control signals not normally changed during operation. The LPWR signal (S5, #2) reduces the power consumption of the analog components at the expense of analog performance. The PWDN signal (S5, #3) disables the analog components by placing them in a micropower sleep state.

2.3.4 Microcontroller

Included on CDB5378 is an 8051-type microcontroller with integrated hardware SPI and USB interfaces. This C8051F320 microcontroller is a product of Silicon Laboratories (http://www.silabs.com). Key features of the C8051F320 microcontroller are:

8051 compatibility - uses industry-standard 8051 software development tools

In-circuit debugger - software development on the target hardware

Internal memory - 16k flash ROM and 2k static RAM included on-chip

Multiple serial connections - SPI, USB, I2C, and UART

High performance - 25 MIPS maximum

Low power - 0.6 mA @ 1 MHz w/o USB, 9 mA @ 12 MHz with USB

Small size - 32 pin LQFP package, 9mm x 9mm

Industrial temperature - full performance (including USB) from -40 C to +85 C

Internal temperature sensor - with range violation interrupt capability

Internal timers - four general purpose plus one extended capability

Power on reset - can supply a reset signal to external devices

Analog ADC - 10 bit, 200 ksps SAR with internal voltage reference

Analog comparators - arbitrary high/low voltage compare with interrupt capability

The exact use of these features is controlled by embedded firmware.

C8051F320 has dedicated pins for power and the USB connection, plus 25 general-purpose I/O pins that connect to the various internal resources through a programmable crossbar. Hardware connections on CDB5378 limit how the blocks can operate, so the port mapping of microcontroller resources is detailed below.

Pin #	Pin Name	Assignment	Description
1	P0.1	SYNC_IO	SYNC signal input from RS-485
2	P0.0	SYNC_MC	SYNC signal output
3	GND		Ground
4	D+		USB differential data transceiver
5	D-		USB differential data transceiver
6	VDD		+3.3 V power supply input
7	REGIN		+5 V power supply input (unused on CDB5378)
8	VBUS		USB voltage sense input

Pin #	Pin Name	Assignment	Description
9	/RST C2CK	RESETz	Power on reset output, active low Clock input for debug interface
10	P3.0 C2D	GPIO	General purpose I/O Data in/out for debug interface
11	P2.7	AIN-	ADC input
12	P2.6	AIN+	ADC input
13	P2.5	CPLD5_MC	General Purpose I/O
14	P2.4	CPLD4_MC	General Purpose I/O
15	P2.3	CPLD3_MC	General Purpose I/O
16	P2.2	CPLD2_MC	General Purpose I/O

Pin #	Pin Name	Assignment	Description
17	P2.1	CPLD1_MC	General Purpose I/O
18	P2.0	CPLD0_MC	General Purpose I/O (CS5378 RESETz)
19	P1.7	BYP_EN	I2C bypass switch control
20	P1.6	SDA_DE	I2C data driver enable
21	P1.5	SCL	I2C clock in/out
22	P1.4	SDA	I2C data in/out
23	P1.3	SS_MCz	SPI chip select output, active low
24	P1.2	MOSI_MC	SPI master out / slave in

Pin #	Pin Name	Assignment	Assignment
25	P1.1	MISO_MC	SPI master in / slave out
26	P1.0	SCK_MC	SPI serial clock
27	P0.7		Internal VREF bypass capacitors
28	P0.6	DRDY_MCz	Data ready input, active low
29	P0.5	RX	UART receiver
30	P0.4	TX	UART transmitter
31	P0.3	CLOCK_MC	External clock input
32	P0.2	TIMEB_MC	Time Break output

Many connections to the C8051F320 microcontroller are inactive by default, but are provided for convenience during custom reprogramming. Listed below are the default active connections to the microcontroller and how they are used.

2.3.4.1 SPI Interface

The microcontroller SPI interface communicates with the CS5378 digital filter to write/read configuration information and collect conversion data from the SPI port. Detailed information about interfacing to the digital filter SPI port can be found in the CS5378 data sheet.

2.3.4.2 USB Interface

The microcontroller USB interface communicates with the PC evaluation software to receive configuration commands and return collected conversion data. The USB interface uses the Silicon Laboratories API and Windows drivers, which are available free from the internet (http://www.silabs.com).

2.3.4.3 Reset Source

By default, the C8051F320 microcontroller receives its reset signal from the RESET_PBz push button.

2.3.4.4 Clock Source

By default, the C8051F320 microcontroller uses an internally generated 12 MHz clock for compatibility with USB standards.

2.3.4.5 Timebreak Signal

By default, the C8051F320 microcontroller sends the TIMEB_MC signal to the digital filter for the first collected sample of a data record. By default, 100 initial samples are skipped during data collection to ensure the CS5378 digital filters are fully settled, and the timebreak signal is automatically set for the first “real” collected sample.

2.3.4.6 C2 Debug Interface

Through the PC evaluation software, the microcontroller default firmware can be automatically flashed to the latest version without connecting an external programmer. To flash custom firmware, software tools and an inexpensive hardware programmer (DEBUGADPTR1-USB) that connects to the C2 Debug Interface on CDB5378 are available from Silicon Laboratories.

2.3.5 RS-485 Telemetry

By default, CDB5378 communicates with the PC evaluation software through the microcontroller USB port. Additional hardware is designed onto CDB5378 to use the microcontroller I2C port as a low-level local telemetry, but it is provided for custom programming convenience only and is not directly supported by the CDB5378 PC evaluation software or microcontroller firmware.

Telemetry signals enter CDB5378 through RS-485 transceivers, which are differential current mode transceivers that can reliably drive long distance communication. Data passes through the RS-485 transceivers to the microcontroller I2C interface and the clock and synchronization inputs.

Specification	Value
RS-485 Transceiver - Linear Tech	LTC1480IS8
Surface Mount Package Type	SOIC-8, 5mm x 6mm
Supply Voltage, Quiescent Current	3.3V, 600 µA
Maximum Data Rate	2.5 Mbps
Transmitter Delay, Receiver Delay	25 - 80 ns, 30 - 200 ns
Transmitter Current, Full Termination (60 Ω)	25 mA
Transmitter Current, Half Termination (120 Ω)	13 mA

2.3.5.1 CLK, SYNC

Clock and synchronization telemetry signals into CDB5378 are received through RS-485 twisted pairs. These signals are required to be distributed through the external system with minimal jitter and timing skew, and so are normally driven through high-speed bus connections.

Specification	Value
Synchronous Inputs, 2 wires each	CLK±, SYNC±

Specification	Value
Distributed SYNC Signal Synchronization	± 240 ns
Distributed Clock Synchronization	± 240 ns
Analog Sampling Synchronization Accuracy	± 480 ns

Synchronization of the measurement channel is critical to ensure simultaneous analog sampling across a network. Several options are available for connecting a SYNC signal through the RS-485 telemetry to the digital filter.

A direct connection is made when the SYNC_IO signal is received over the dedicated RS-485 twisted pair and sent directly to the digital filter SYNC pin through jumper J56. The incoming SYNC_IO signal must be synchronized to the network at the transmitter since no local timing adjustment is available.

A microcontroller hardware connection is made when the SYNC_IO signal is received over the dedicated RS-485 twisted pair and detected by a microcontroller interrupt. The microcontroller can then use an internal counter to re-time the SYNC_MC signal output to the digital filter SYNC input as required.

A microcontroller software connection is made when the SYNC_MC signal output is created by the microcontroller on command from the system telemetry. The microcontroller can use an internal counter to re-time the SYNC_MC signal output to the digital filter SYNC input as required.

2.3.5.2 I2C - SCL, SDA, Bypass

The I2C telemetry connections to CDB5378 transmit and receive through RS-485 twisted pairs. Because signals passing through the transceivers are actively buffered, full I2C bus arbitration and error detection cannot be used (i.e. high-impedance NACK).

The I2C inputs and outputs can be externally wired to create either a daisy chain or a bus-type network, depending how the telemetry system is to be implemented. Analog switches included on CDB5378 can bypass the I2C signals to create a bus network from a daisy chain network following address assignment.

Specification	Value
I2C Inputs, 2 wires each	SCL±, SDA±
I2C Outputs, 2 wires each	BYP_SCL±, BYP_SDA±
I2C Bypass Switch Control	BYP_EN

When CDB5378 is used in a distributed measurement network, each node must have a unique address. This address is used to transmit individual configuration commands and tag the source of returned conversion data. Address assignment can be either dynamic or static, depending how the telemetry system is to be implemented.

Dynamic address assignment uses daisy-chained I2C connections to assign an address to each measurement node. Once a node receives an address, it enables the I2C bypass switches to the next node so it can be assigned an address.

Static address assignment has a serial number assigned to each node during manufacturing. When placed in the network, the location is recorded and a master list of serial numbers vs. location is maintained. Alternately, a location-dependent serial number can be assigned during installation.

2.3.6 UART Connection

A UART connection on CDB5378 provides a low-speed standardized connection for telemetry solutions not using I2C. UART connections are provided for custom programming convenience only and are not directly supported by the CDB5378 PC evaluation software or microcontroller firmware.

Specification	Value
UART Connections, 2 wires each	TX/GND, RX/GND

2.3.7 External Connector

Power supplies and telemetry signals route to a 20-pin double row connector with 0.1" spacing (J26). This header provides a compact standardized connection to the CDB5378 external signals.

Pins	Name	Signal
1, 2	CLK+, CLK-	Clock Input
3, 4	SYNC+, SYNC-	Synchronization Input
5, 6	SCL+, SCL-	I2C Clock
7, 8	SDA+, SDA-	I2C Data
9, 10	BYP_SDA+, BYP_SDA-	I2C Data Bypass
11, 12	BYP_SCL+, BYP_SCL-	I2C Clock Bypass
13, 14	TX, GND	UART transmit
15, 16	RX, GND	UART receive
17, 18	EXT_VA-, GND	Negative Power Supply
19, 20	EXT_VA+, GND	Positive Power Supply

2.4 Power Supplies

Power is supplied to CDB5378 through banana jacks (J6, J7, J8, J9) or through the external connector (J26). The banana jacks make separate connections to the EXT_VA-, EXT_VA+, GND, and EXT_VD power supply nets, which connect to the analog and digital linear voltage regulator inputs. The external connector makes separate connections only to the EXT_VA-, GND, and EXT_VA+ power supply inputs and it is required to jumper EXT_VA+ to EXT_VD when powering CDB5378 from the external connector.

The EXT_VA-, EXT_VA+ and EXT_VD power supply inputs have zener protection diodes that limit the maximum input voltages to +13 V or -13 V with respect to ground. Each input also has 100 uF bulk capacitance for bypassing and to help settle transients and another 0.01 uF capacitor to bypass high-frequency noise.

2.4.1 Analog Voltage Regulators

Linear voltage regulators create the positive and negative analog power supply voltages to the analog components on CDB5378. These regulate the EXT_VA+ and EXT_VA- power supply inputs to create the VA+ and VA- analog power supplies.

Specification	Value
Positive Analog Power Supply	+2.5 V, +5 V
Low Noise Micropower Regulator - Linear Tech	LT1763CS8
Surface Mount Package Type	SO-8
Load Regulation, -40 C to +85 C	+/- 25 mV
Quiescent Current, Current @ 100 mA Load	40 µA, 2 mA
Output Voltage Noise, 10 Hz - 100 kHz	20 μV_{RMS}
Ripple Rejection, DC - 200 Hz	> 50 dB

Specification	Value
Negative Analog Supply, -2.5VA	-2.5 V
Low Noise Micropower Regulator - Linear Tech	LT1964ES5-BYP
Surface Mount Package Type	SOT-23
Load Regulation, -40 C to +85 C	+/- 30 mV
Quiescent Current, Current @ 100 mA Load	30 µA, 1.3 mA
Output Voltage Noise, 10 Hz - 100 kHz	20 μV_{RMS}
Ripple Rejection, DC - 200 Hz	> 45 dB

The VA+ and VA- power supplies to the analog components on CDB5378 can be jumpered to use regulated bipolar power supplies (+2.5 V, -2.5 V), regulated unipolar power supplies (+5 V, GND), or unregulated direct connections (EXT_VA+, EXT_VA-). When using direct connections to EXT_VA+ and EXT_VA-, extreme care must be taken not to exceed the maximum specified power supply voltages of the analog components on CDB5378.

Characterization testing has shown the analog components on CDB5378 work best using bipolar analog power supplies (+2.5 V, -2.5 V) instead of unipolar analog power supplies (+5 V, GND). It is recommended to always use the regulated bipolar analog power supplies for optimal performance.

The VA+ and VA- power supply nets to the analog components on CDB5378 include reverse-biased Schottkey diodes to ground to protect against reverse voltages that could latch-up the CMOS analog components. Also included on VA+ and VA- are 100 uF bulk capacitors for bypassing and to help settle transients plus individual 0.1 uF bypass capacitors local to the analog power supply pins of each device.

2.4.2 Digital Voltage Regulators

Linear voltage regulators create the positive digital power supply voltages on CDB5378. Jumper options select which external power supply input voltage, EXT_VD or EXT_VA+, is supplied to the digital voltage regulators to create the VD and VCORE power supplies.

Specification	Value
Positive Digital Power Supply	+2.5 V, +3.3 V
Low Noise Micropower Regulator - Linear Tech	LT1763CS8
Surface Mount Package Type	SO-8
Load Regulation, -40 C to +85 C	+/- 25 mV
Quiescent Current, Current @ 100 mA Load	40 µA, 2 mA
Output Voltage Noise, 10 Hz - 100 kHz	20 μV_{RMS}
Ripple Rejection, DC - 200 Hz	> 50 dB

The VD and VCORE power supplies on CDB5378 can be jumpered to use regulated +3.3 V or +2.5 V power supplies or an unregulated direct connection to EXT_VD. Extreme care must be taken when using a direct connection to EXT_VD not to exceed the maximum specified power supply voltages of the digital components on CDB5378.

Even though the Cirrus Logic components on CDB5378 will tolerate up to 5 V from the VD power supply, other components are specified for +3.3 V operation only and so it is recommended to use only the regulated +3.3 V jumper setting for VD.

The VD and VCORE power supplies on CDB5378 include reverse-biased Schottkey diodes to ground to protect against reverse voltages that could latch-up the CMOS components. Also included on VD and VCORE are 100 uF bulk capacitors for bypassing and to help settle transients plus individual 0.1 uF bypass capacitors local to the digital power supply pins of each device.

2.5 PCB Layout

2.5.1 Layer Stack

CDB5378 layer 1 is dedicated as an analog routing layer. All critical analog signal routes are on this layer. Some CPLD and microcontroller digital routes are also included on this layer away from the analog signal routes.

CDB5378 layer 2 is a solid ground plane without splits or routing. A solid ground plane provides the best return path for bypassed noise to leave the system. No separate analog ground is required since analog signals on CDB5378 are differentially routed.

CDB5378 layer 3 is dedicated for power supply routing. Each power supply net includes at least 100 µF bulk capacitance as a charge well for settling transient current loads.

CDB5378 layer 4 is dedicated as a digital routing layer.

2.5.2 Differential Pairs

Analog signal routes on CDB5378 are differential with dedicated + and - traces. All source and return analog signal currents are constrained to the differential pair route and do not return through the ground plane. Differential traces are routed together with a minimal gap between them so that noise events affect them equally and are rejected as common mode noise.

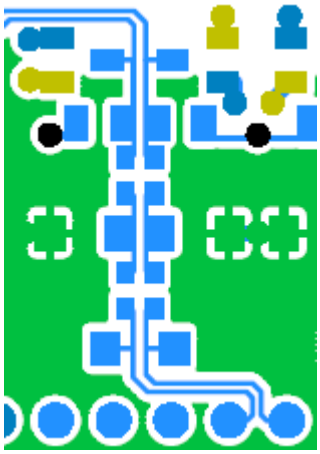


Figure 4. Differential Pair Routing

Analog signal connections into the CS3301/02 amplifiers are 2-wire IN+ and IN- differential pairs, and are routed as such. Analog signal connections out of the CS3301/02 amplifiers and into the CS5373A modulator is a 4-wire INR+, INF+, INF-, INR- quad group, and is routed with INF+ and INF- as a traditional differential pair and INR+ and INR- as guard traces outside the respective INF+ and INF- traces.

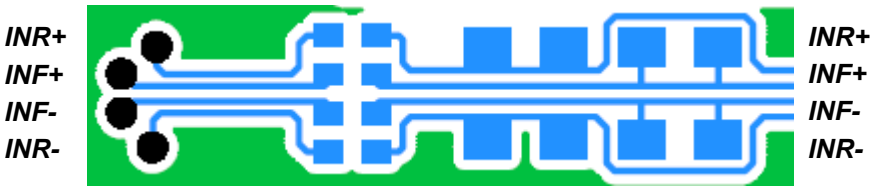


Figure 5. Quad Group Routing

2.5.3 Bypass Capacitors

Each device power supply pin includes 0.1 µF bypass capacitors placed as close as possible to the pin on the back side of the PCB. Each power supply net includes at least 100 µF bulk capacitance as a charge well for transient current loads.

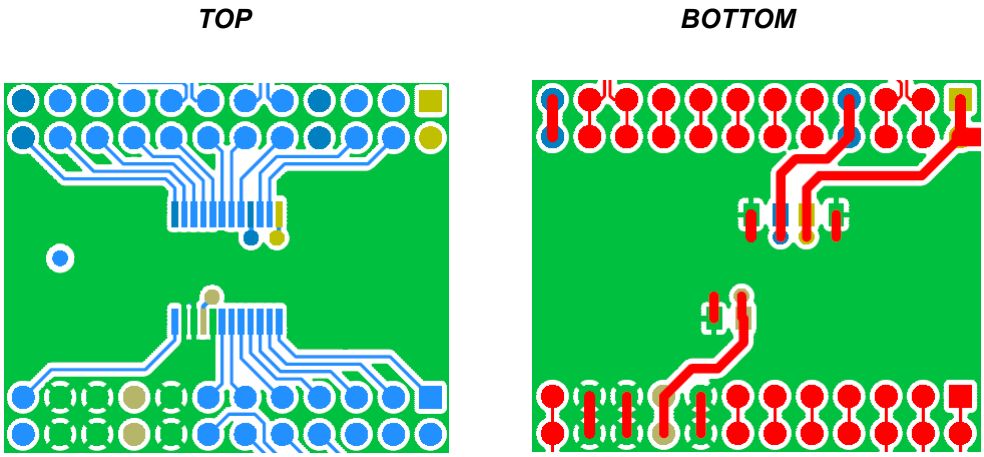


Figure 6. Bypass Capacitor Placement

2.5.4 Dual-row Headers

To simplify signal tracing on CDB5378, all device pins connect to dual-row headers. These dual-row headers are not populated during board manufacture, but the empty PCB footprint exists on the boards and can be used as test points.

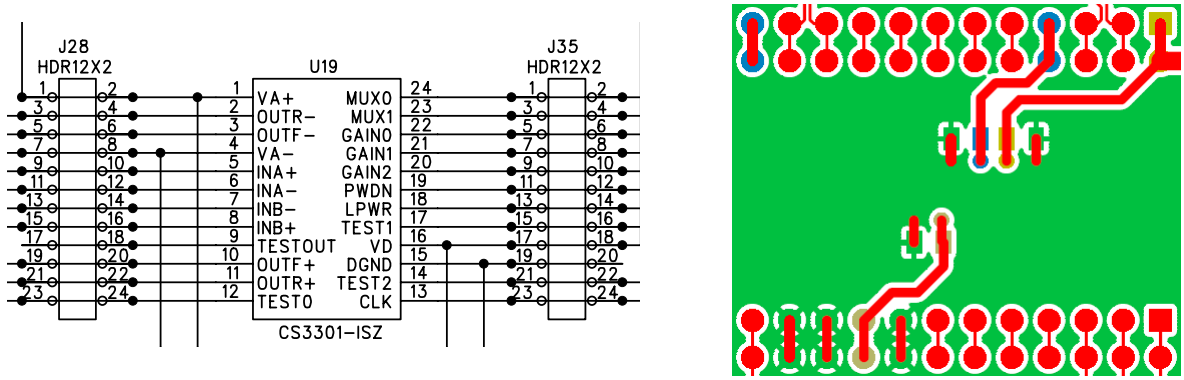


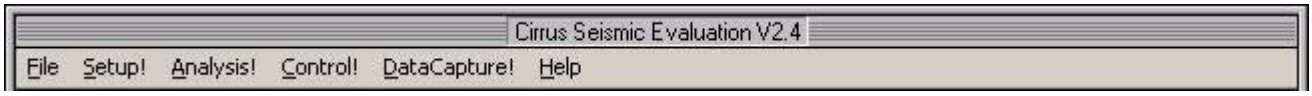
Figure 7. Dual-row Headers with Shorts

The dual-row header pins are shorted on the bottom side of the PCB to pass signals through to the rest of the board. These shorted traces between the dual-row pins can be *carefully* cut to isolate the device signals from the rest of the PCB to permit wiring changes to the existing route. To restore the previous connection, install a jumper to short across the dual-row pins.

Signals taken off the PCB should not be wired directly from the dual-row header pins, as there is no clean path for the signal return current. Instead, install a connector into the prototying area and wire the signal and a ground connection to it. Pairing the signal with a ground return before taking it off the PCB will improve signal integrity.

3. SOFTWARE DESCRIPTION

3.1 Menu Bar



The menu bar is always present at the top of the software panels and provides typical *File* and *Help* pull-down menus. The menu bar also selects the currently displayed panel.

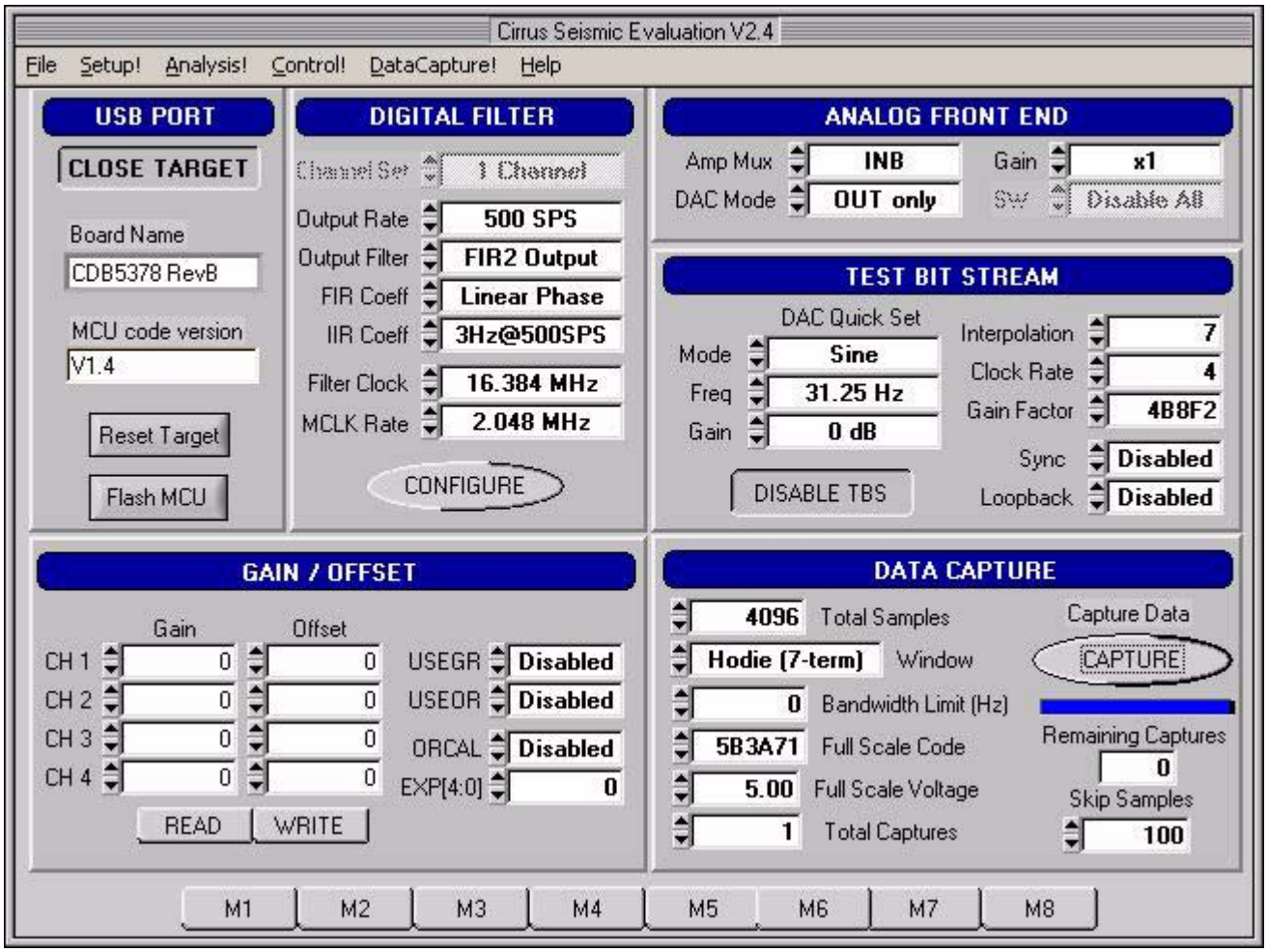
Control	Description
File	
Load Data Set	Loads a data set from disk.
Save Data Set	Saves the current data set to disk.
Copy Panel to Clipboard	Copies a bitmap of the current panel to the clipboard.
Print Analysis Screen	Prints the full Analysis panel, including statistics fields.
Print Analysis Graph	Prints only the graph from the Analysis panel.
High Resolution Printing	Prints using the higher resolution of the printer.
Low Resolution Printing	Prints using the standard resolution of the screen.
Quit	Exits the application software.
Setup!	Displays the Setup Panel.
Analysis!	Displays the Analysis Panel.
Control!	Displays the Control Panel.
DataCapture!	Displays the Setup Panel and starts Data Capture.
Help	
Contents	Find help by topic.
Search for help on	Find help by keywords.
About	Displays the About Panel.

3.2 *About* Panel

The ***About*** panel displays copyright information for the Cirrus Seismic Evaluation software.

Click *OK* to exit this panel. Select *Help* ⇨ *About* from the menu bar to display this panel.

3.3 *Setup* Panel



The ***Setup*** panel initializes the evaluation system to perform data acquisition. It consists of the following sub-panels and controls.

- ***USB Port***
- ***Digital Filter***
- ***Analog Front End***
- ***Test Bit Stream***
- ***Gain/Offset***
- ***Data Capture***
- ***External Macros***

3.3.1 USB Port

The ***USB Port*** sub-panel sets up the USB communication interface between the PC and the target board.

Control	Description
Open Target	Open USB communication to the target board and read the board name and microcontroller firmware version. When communication is established, the name of this control changes to *'Close Target'* and ***Setup***, ***Analysis*** and ***Control*** panel access becomes available in the menu bar.
Close Target	Disconnects the previously established USB connection. On disconnection, this control changes to *'Open Target'* and the ***Setup***, ***Analysis*** and ***Control*** panel access becomes unavailable in the menu bar. The evaluation software constantly monitors the USB connection status and automatically disconnects if the target board is turned off or the USB cable is unplugged.
Board Name	Displays the type of target board currently connected.
MCU code version	Displays the version number of the microcontroller code on the connected target board.
Reset Target	Sends a software reset command to the target board.
Flash MCU	Programs the microcontroller code on the target board using the *.thx* file found in the *"C:\Program Files\Cirrus Seismic Evaluation"* directory. This feature permits reprogramming of the microcontroller (without using a hardware programmer) when a new version of the MCU code becomes available.

3.3.2 Digital Filter

The ***Digital Filter*** sub-panel sets up the digital filter configuration options.

By default the ***Digital Filter*** sub-panel configures the system to use on-chip digital filter coefficients. The on-chip data can be overwritten by loading custom coefficients from the ***Customize*** sub-panel on the ***Control*** panel.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
Channel Set	Disabled for CDB5378. One channel operation only.
Output Rate	Selects the output word rate of the digital filter. Output word rates from 4000 SPS to 1 SPS (0.25 mS to 1 S) are available.
Output Filter	Selects the output filter stage from the digital filter. Sinc output, FIR1 output, FIR2 output, IIR 1st order output, IIR 2nd order output, or IIR 3rd order output can be selected. FIR2 output provides full decimation of the modulator data.
FIR Coeff	Selects the on-chip FIR coefficient set to use in the digital filter. Linear phase or minimum phase FIR coefficients can be selected.
IIR Coeff	Selects the on-chip IIR coefficient set to use in the digital filter. Coefficient sets producing a 3 Hz high-pass corner at 2000 SPS, 1000 SPS, 500 SPS, 333 SPS, and 250 SPS can be selected.
Filter Clock	Sets the digital filter internal clock rate. Lower internal clock rates can save power when using slow output word rates.
MCLK Rate	Sets the analog sample clock rate. The CS5373A modulator and test DAC typically runs with MCLK set to 2.048 MHz.
Configure	Writes all information from the ***Setup*** panel to the digital filter. The data *Capture* button becomes available once the configuration information is written to the target board.

3.3.3 Analog Front End

The ***Analog Front End*** sub-panel configures the amplifier, modulator and test DAC pin options. Pin options are controlled through the GPIO outputs of the digital filter.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
Amp Mux	Selects the input source for the CS3301/02 amplifiers. An internal termination, external INA inputs or external INB inputs can be selected.
DAC Mode	Selects the operational mode of the CS5373A test DAC. The test DAC operational modes are AC dual output (OUT&BUF), AC precision output (OUT only), AC buffered output (BUF only), DC common mode output (DC Common), DC differential output (DC Diff), or AC common mode output (AC Common). The test DAC can also be powered down (PWDN) when not in use to save power.
Gain	Sets the amplifier gain range and test DAC attenuation. Amplifier gain and DAC attenuation settings of 1x, 2x, 4x, 8x, 16x, 32x, or 64x can be selected and are controlled together.
Pwdn	Disabled for CDB5378. PWDN routes to DIP switch S5.

3.3.4 Test Bit Stream

The ***Test Bit Stream*** sub-panel configures test bit stream (TBS) generator parameters. The digitial filter data sheet describes TBS operation and options.

The *DAC Quick Set* controls automatically set the *Interpolation*, *Clock Rate*, and *Gain Factor* controls based on the selected *Mode*, *Freq*, and *Gain*. Additional configurations can be programmed by writing the *Interpolation*, *Clock Rate*, and *Gain Factor* controls manually.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
DAC Quick Set	Automatically sets test bit stream options. *Mode* selects sine or impulse output mode, *Freq* selects the test signal frequency for sine mode, and *Gain* selects the test signal amplitude in dB.
Interpolation	Manual control for the data interpolation factor of the test bit stream generator.
Clock Rate	Manual control for the output clock and data rate of the test bit stream generator.
Gain Factor	Manual control to set the test bit stream signal amplitude.
Sync	Enables test bit stream synchronization by the MSYNC signal.
Loopback	Enables digital loopback from the test bit stream generator output to the digital filter input.

3.3.5 Gain / Offset

The ***Gain / Offset*** sub-panel controls the digital filter GAIN and OFFSET registers.

The OFFSET and GAIN registers can be manually written with any 24-bit 2's complement value from 0x800000 to 0x7FFFFF. The USEGR, USEOR, ORCAL, and EXP[4:0] values enable gain correction, offset correction, and offset calibration in the digital filter.

The offset calibration routine built into the digital filter is enabled by writing the ORCAL and EXP[4:0] bits. The EXP[4:0] value can range from 0x00 to 0x18 and represents an exponential shift of the calibration feedback, as described in the digital filter data sheet. Offset calibration results are automatically written to the OFFSET registers and remain there, even after offset calibration is disabled.

Control	Description
Gain	Displays the digital filter GAIN register.
Offset	Displays the digital filter OFFSET register.
Read	Reads values from the GAIN and OFFSET registers.
Write	Writes values to the GAIN and OFFSET registers.
USEGR	Enables gain correction. When enabled, output samples are gained down by the value in the GAIN register.(Output = GAIN / 0x7FFFFF).
USEOR	Enables offset correction. When enabled, output samples are offset by the value in the OFFSET register. (Output = Sample - OFFSET).
ORCAL	Enables offset calibration using the exponent value from the EXP[4:0] control. Results are automatically written to the OFFSET registers as they are calculated.
EXP[4:0]	Sets the exponential value used by offset calibration.

3.3.6 Data Capture

The ***Data Capture*** sub-panel collects samples from the target board and sets analysis parameters.

When the *Capture* button is pressed, the requested number of samples are collected from the target board through the USB port. The maximum number of samples that can be collected is 1,048,576 (1M). The number of samples should be a power of two for the analysis FFT routines to work properly.

After data is collected, analysis is performed using the selected parameters and the results are displayed on the ***Analysis*** panel. The selected analysis *window*, *bandwidth limit*, *full scale code*, and *full scale voltage* parameters can be modified for the data set currently in memory and the analysis re-run by pressing the *REFRESH* button on the ***Analysis*** Panel.

Control	Description
Total Samples	Sets the total number of samples to be collected. A maximum of 1,048,576 (1M) samples can be collected.
Window	Selects the type of analysis windowing function to be applied to the collected data set. Used to ensure proper analysis of discontinuous data sets.
Bandwidth Limit (Hz)	Sets the frequency range over which to perform analysis, used to exclude higher-frequency components. Default value of zero performs analysis for the full Nyquist frequency range.
Full Scale Code	Defines the maximum positive full-scale 24-bit code from the digital filter. Used during FFT noise analysis to set the 0 dB reference level.
Full Scale Voltage	Defines the maximum peak-to-peak input voltage for the nV/rtHz Spot Noise analysis.
Total Captures	Sets the number of data sets to be collected and averaged together in the FFT magnitude domain. The maximum number of data sets that can be averaged is 100.
Capture	Starts data collection from the target board through the USB port. After data collection, analysis is run using parameters from this sub-panel.
Remaining Captures	Indicates how many more data captures are remaining to complete the requested number of *Total Captures*. A zero value means that the current data capture is the last one.
Skip Samples	Sets the total number of samples to be skipped prior to data collection. A maximum of 64K samples can be skipped

3.3.7 External Macros

Macros are generated within the ***Macros*** sub-panel on the ***Control*** panel. Once a macro has been built it can either be saved with a unique macro name to be run within the ***Macros*** sub-panel, or saved as an external macro and be associated with one of the *External Macro* buttons.

A macro is saved as an *External Macro* by saving it in the *. /macros/* subdirectory using the name *'m1.mac'*, *'m2.mac'*, etc. Depending on the selected name the macro will be associated with the corresponding *External Macro* button *M1*, *M2*, etc.

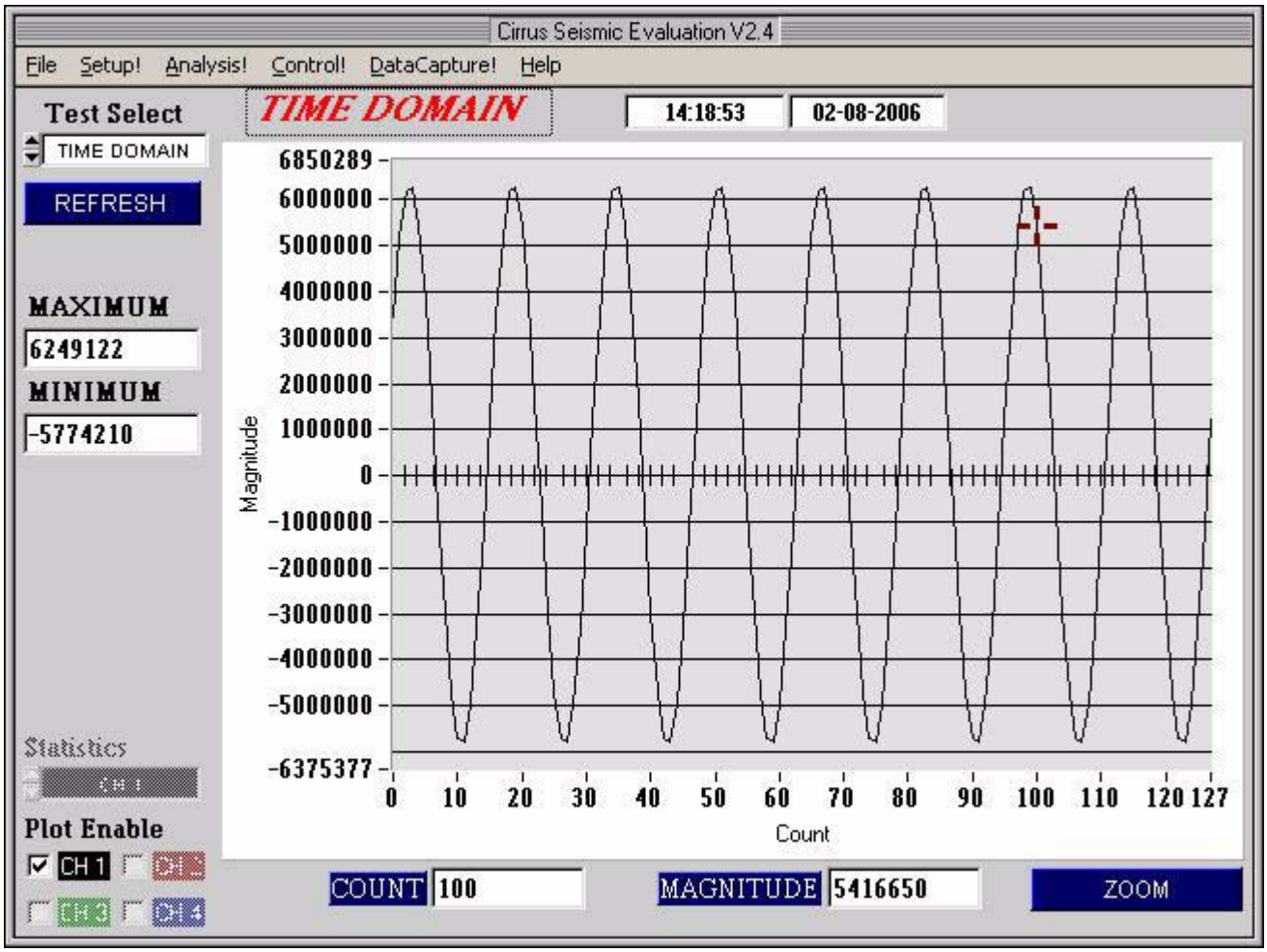
- M1 = . /macros/m1.mac
- M2 = . /macros/m2.mac
- etc.

External Macro buttons can be re-named on the panel by right clicking on them. The button name will change, but the macro associated with that button is always saved as '*m1.mac'*, *'m2.mac'*, etc., in the *. /macros/* subdirectory. The *External Macro* button names are stored in the file *'Mnames.txt'*, also in the *. /macros/* subdirectory.

*External Macro*s allow up to eight macros to be accessed quickly without having to load them into the ***Macros*** sub-panel on the ***Control*** panel. These *External Macro*s operate independently of the ***Macros*** sub-panel and are not affected by operations within it, except when a macro is saved to the *. /macros/* subdirectory to replace a currently existing *External Macro*.

Control	Description
M1 - M8	Runs the *External Macro* associated with that button.

3.4 *Analysis* Panel



The ***Analysis*** panel is used to display the analysis results on collected data. It consists of the following controls.

- ***Test Select***
- ***Statistics***
- ***Plot Enable***
- ***Cursor***
- ***Zoom***
- ***Refresh***
- ***Harmonics***
- ***Spot Noise***
- ***Plot Error***

3.4.1 Test Select

The *Test Select* control sets the type of analysis to be run on the collected data set.

Control	Description
Time Domain	Runs a min / max calculation on the collected data set and then plots sample data value vs. sample number.
Histogram	Runs a histogram calculation on the collected data set and then plots sample occurrence vs. sample value. Only valid for noise data since sine wave data varies over too many codes to plot as a histogram.
Signal FFT	Runs an FFT on the collected data set and then plots frequency magnitude vs. frequency. Statistics are calculated using the largest frequency magnitude bin as a full-scale signal reference.
Noise FFT	Runs an FFT on the collected data set and then plots frequency magnitude vs. frequency. Statistics are calculated using a simulated full-scale signal as a full-scale signal reference.
Phase	Runs an FFT on the collected data set and then plots phase vs. frequency. Limited usefulness for real collected data since noise has random phase.

3.4.2 Statistics

The *Statistics* control displays calculated statistics for the analysis. Errors that affect statistical calculations will cause the *Plot Error* control to appear. Information about errors can be accessed by accessing the *Plot Error* controls.

Control	Description
Time Domain	
Max	Maximum code of collected data set.
Min	Minimum code of collected data set.
Histogram	
Max	Maximum code of collected data set.
Min	Minimum code of collected data set.
Mean	Mean of collected data set.
Std Dev	Standard Deviation of collected data set.
Variance	Variance of collected data set.
Signal FFT	
S/N	Signal to Noise of calculated FFT.
S/PN	Signal to Peak Noise of calculated FFT.
S/D	Signal to Distortion of calculated FFT.
S/N+D	Signal to Noise plus Distortion of calculated FFT.
# of bins	Number of Bins covering the Nyquist frequency.
Noise FFT	
S/N	Signal to Noise of calculated FFT.
S/PN	Signal to Peak Noise of calculated FFT.
Spot Noise dB	Spot Noise in dB/Hz of calculated FFT.
Spot Noise nV	Spot Noise in nV/rtHz of calculated FFT.
# of bins	Number of Bins covering the Nyquist frequency.
Phase	
	No statistics are calculated.

3.4.3 Plot Enable

The *Plot Enable* control is disabled for CDB5378. One channel operation only.

3.4.4 Cursor

The *Cursor* control is used to identify a point on the graph using the mouse and then display its plot values. When any point within the plot area of the graph is clicked, the *Cursor* will snap to the closest plotted point and the plot values for that point display below the graph. When using the *Zoom* function, the *Cursor* is used to select the corners of the area to zoom.

3.4.5 Zoom

The *ZOOM* function allows an area on the graph to be expanded.

To use the zoom function, click the *ZOOM* button and select the box corners of the area on the graph to expand. The graph will then expand to show the details of this area, and the plot axes will be re-scaled. While zoomed, you can zoom in farther by repeating the process.

To restore the graph to its original scale, click the *RESTORE* button that appears while zoomed. If multiple zooms have been initiated, the *RESTORE* button will return to the previously viewed plot scale. Repeated *RESTORE* will eventually return to the original plot scale. From within multiple zooms the original scale can be directly restored by clicking the *REFRESH* button.

3.4.6 Refresh

The *REFRESH* button will clear and re-plot the current data set. *Refresh* can be used to apply new analysis parameters from the ***Data Capture*** sub-panel, or to restore a *ZOOM* graph to its default plot scale.

3.4.7 Harmonics

The *HARMONICS* control is only visible during a Signal FFT analysis and highlights the fundamental and harmonic bins used to calculate the Signal FFT statistics. *HARMONICS* highlighting helps to understand the source of any Signal FFT plot errors.

3.4.8 Spot Noise

The *Spot Noise* control (labeled *dB* or *nV*) is only visible during a Noise FFT analysis and selects the units used for plotting the graph, either dB/Hz or nV/rtHz. The dB/Hz plot applies the *Full Scale Code* value from the ***Data Capture*** sub-panel on the ***Setup*** panel to determine the 0 dB point of the dB axis. The nV/rtHz plot applies the *Full Scale Voltage* value from the ***Data Capture*** sub-panel on the ***Setup*** panel to determine the absolute scaling of the nV axis.

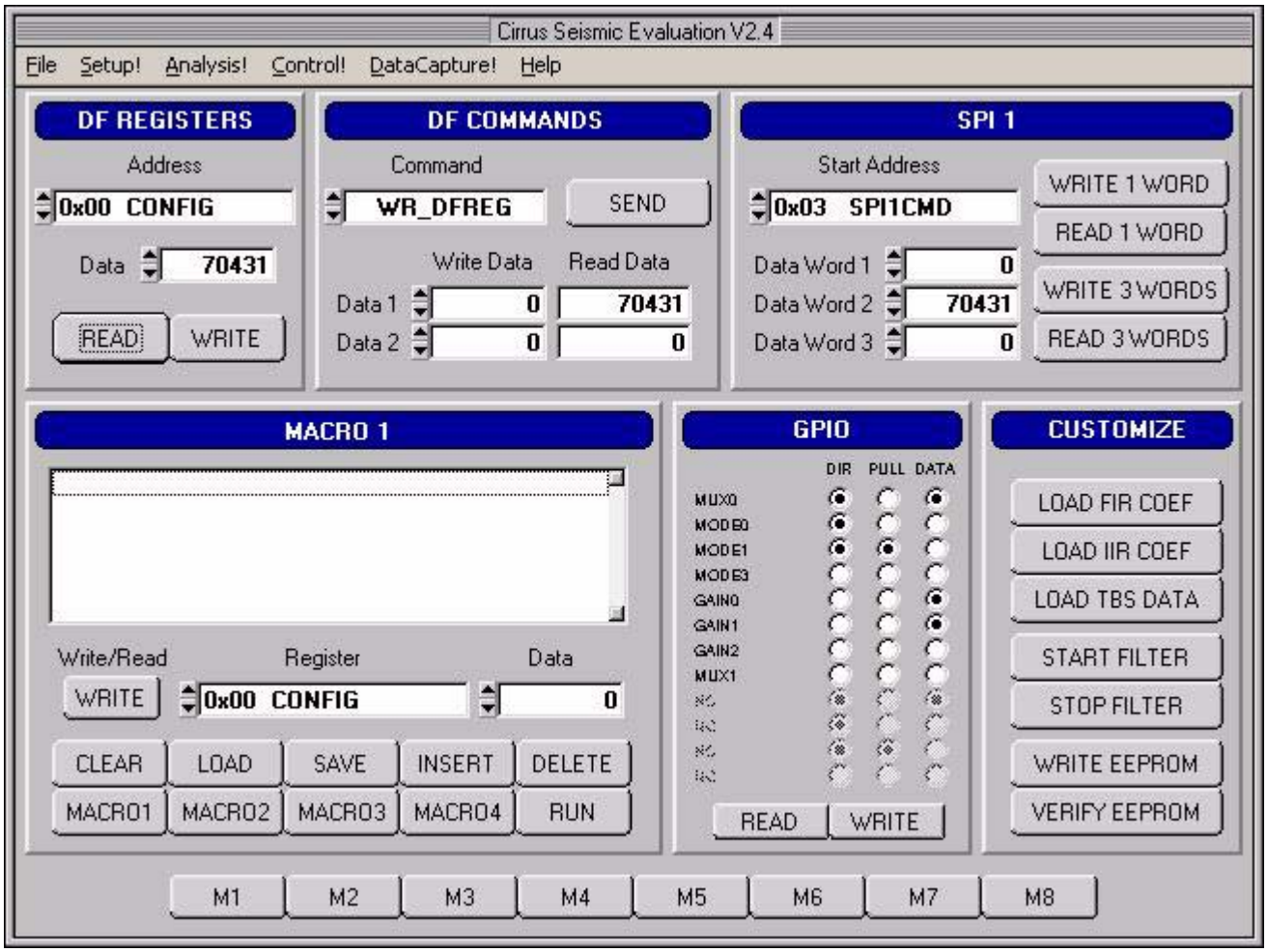
3.4.9 Plot Error

The *PLOT ERROR* control provides information about errors that occured during an analysis.

An analysis error stores an error code in the numerical display box of the *PLOT ERROR* control. If more than one error occurs, all error codes are stored and the last error code is displayed. Any of the accumulated error codes can be displayed by clicking on the numerical box and selecting it.

Once an error code is displayed in the numerical box, a description can be displayed by clicking the *PLOT ERROR* button. This causes a dialog box to display showing the error number and a text error message.

3.5 *Control* Panel



The ***Control*** panel is used to write and read register settings and to send commands to the digital filter. It consists of the following sub-panels and controls.

- ***DF Registers***
- ***DF Commands***
- ***SPI1***
- ***Macros***
- ***GPIO***
- ***Customize***
- ***External Macros***

3.5.1 DF Registers

The ***DF Registers*** sub-panel writes and reads registers within the digital filter. Digital filter registers control operation of the digital filter and the included hardware peripherals, as described in the digital filter data sheet.

Control	Description
Address	Selects a digital filter register.
Data	Contains the data written to or read from the register.
Read	Initiates a register read.
Write	Initiates a register write.

3.5.2 DF Commands

The ***DF Commands*** sub-panel sends commands to the digital filter. The digital filter commands and their required parameters are described in the digital filter data sheet.

Not all commands require write data values, and not all commands will return read data values. Some commands require formatted data files for uploading custom coefficients. Example formatted data files are included in the SPI sub-directory of the software installation.

Control	Description
Command	Selects the command to be written to the digital filter.
Write Data 1	Contains the SPI1DAT1 data to be written to the digital filter.
Write Data 2	Contains the SPI1DAT2 data to be written to the digital filter.
Read Data 1	Contains the SPI1DAT1 data read from the digital filter.
Read Data 2	Contains the SPI1DAT2 data read from the digital filter.
Send	Initiates the digital filter command.

3.5.3 SPI

The ***SPI*** sub-panel writes and reads registers in the digital filter SPI register space. They can be used to check the SPI serial port status bits or to manually write commands to the digital filter.

Control	Description
Start Address	Selects the address to begin the SPI transaction.
Data Word 1	Contains the first data word written to or read from the SPI registers.
Data Word 2	Contains the second data word written to or read from the SPI registers.
Data Word 3	Contains the third data word written to or read from the SPI registers.
Read 1 Word	Initiates a 1 word SPI read transaction.
Read 3 Words	Initiates a 3 word SPI read transaction.
Write 1 Word	Initiates a 1 word SPI write transaction.
Write 3 Words	Initiates a 3 word SPI write transaction.

3.5.4 Macros

The ***Macros*** sub-panel is designed to write a large number of registers with a single command. This allows the target evaluation system to be quickly set into a specific state for testing.

The *Register* control gives access to both digital filter registers and SPI registers. These registers can be written with data from the *Data* control, or data can be read and output to a text window. The *Register* control can also select special commands to be executed, with the *Data* control used to define a parameter value for the special command, if necessary.

Control	Description
Write / Read	Selects the type of operation to be performed by the inserted macro command.
Register	Selects the target register for the inserted macro command. Also selects special commands that can be performed.
Data	Sets the register data value for the inserted macro command. Also sets the parameter value for special commands.
Clear	Clears the currently displayed macro.
Load	Loads a previously saved macro.
Save	Saves the currently displayed macro. Macros can be saved with unique names or can be saved as *External Macros*.
Insert	Inserts a macro command at the selected macro line. The macro command is built from the *Write/Read*, *Register*, and *Data* controls.
Delete	Deletes the macro command at the selected macro line.
Macro1 - Macro4	Selects which of the four working macros is displayed.
Run	Runs the currently displayed working macro.

3.5.5 GPIO

The ***GPIO*** sub-panel controls the digital filter GPIO pin configurations. GPIO pins have dedicated functions on the target board, but can be used in any manner for custom designs.

Control	Description
Direction	Sets the selected GPIO pin as an output (*) or input ( ).
Pull Up	Turns the pull up resistor for the selected GPIO pin on (*) or off ( ).
Data	Sets the selected output GPIO pin to a high (*) or low ( ) level.
Write	Initiates a write to GPIO registers.The *Direction*, *Pull Up* and *Data* controls are read to determine the register values to be written.
Read	Initiates a read from GPIO registers.The *Direction*, *Pull Up* and *Data* controls are updated based on the register values that are read.

3.5.6 Customize

The ***Customize*** sub-panel sends commands to upload custom FIR and IIR filter coefficients, start the digital filter, stop the digital filter and write/read custom EEPROM configuration files to the on-board boot EEPROM. Example data files are included in a sub-directory of the software installation.

Control	Description
Load FIR Coef	Write a set of FIR coefficients into the digital filter from a file.
Load IIR Coef	Write a set of IIR coefficients into the digital filter from a file.
Start Filter	Enables the digital filter by sending the *Start Filter* command.
Stop Filter	Disables the digital filter by sending the *Stop Filter* command.
Write EEPROM	Writes an EEPROM boot configuration file to the EEPROM memory.
Verify EEPROM	Verifies EEPROM memory against an EEPROM boot configuration file.

3.5.7 External Macros

Macros are generated within the ***Macros*** sub-panel on the ***Control*** panel. Once a macro has been built it can either be saved with a unique macro name to be run within the ***Macros*** sub-panel, or saved as an external macro and be associated with one of the *External Macro* buttons.

A macro is saved as an *External Macro* by saving it in the *. /macros/* subdirectory using the name *'m1.mac'*, *'m2.mac'*, etc. Depending on the selected name the macro will be associated with the corresponding *External Macro* button *M1*, *M2*, etc.

- M1 = . /macros/m1.mac
- M2 = . /macros/m2.mac
- etc.

External Macro buttons can be re-named on the panel by right clicking on them. The button name will-change, but the macro associated with that button is always saved as *'m1.mac'*, *'m2.mac'*, etc., in the *. /macros/* subdirectory. The *External Macro* button names are stored in the file *'Mnames.txt'*, also in the *. /macros/* subdirectory.

*External Macro*s allow up to eight macros to be accessed quickly without having to load them into the ***Macros*** sub-panel on the ***Control*** panel. These *External Macro*s operate independently of the ***Macros*** sub-panel and are not affected by operations within it, except when a macro is saved to the *. /macros/* subdirectory to replace a currently existing *External Macro*.

Control	Description
M1 - M8	Runs the *External Macro* associated with that button.

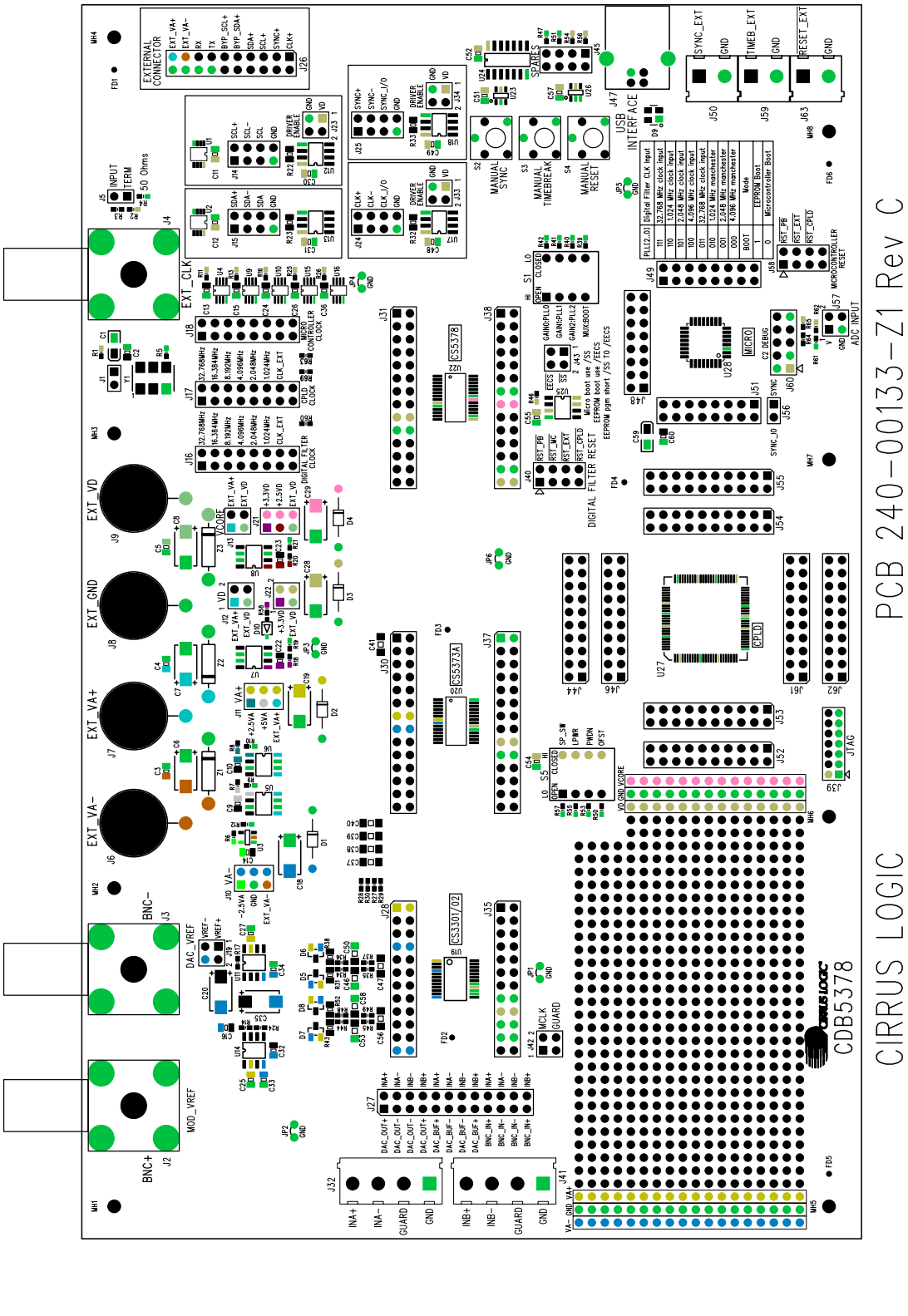
4. BILL OF MATERIALS

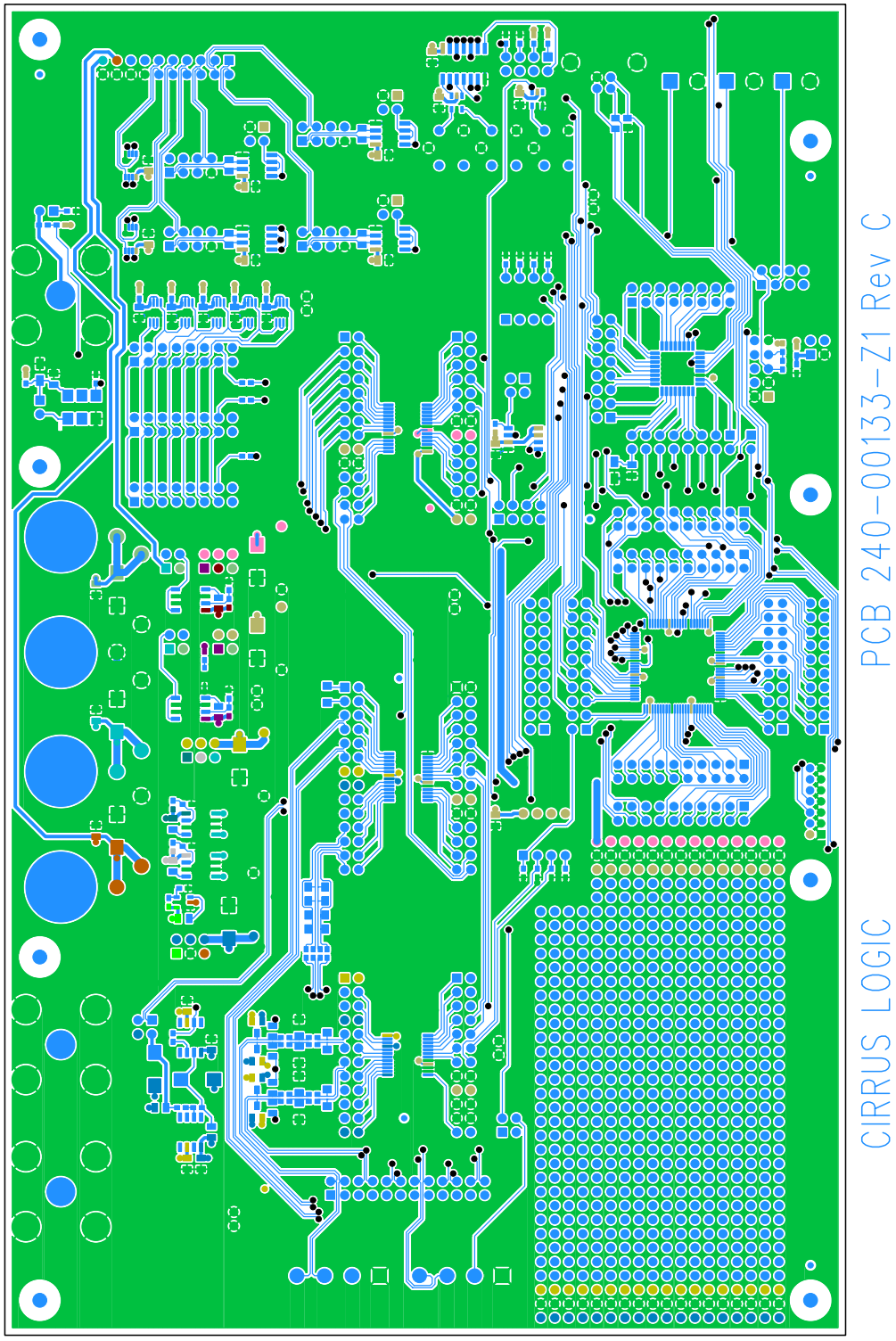
Item	Cirrus P/N	Rev	Description	Qty	Reference Designator	MFG	MFG P/N	Notes	Status
1	004-00068-Z1	A	CAP 4.7uF ±10% 10V NPb TANT CASE A	2	C1 C59	KEMET	T491A475K010AS		A
2	001-04345-Z1	A	CAP 0.1uF ±10% 50V X7R NPb 0805	44	C2 C11 C12 C13 C15 C16 C24 C25 C26 C27 C30 C31 C32 C33 C34 C36 C44 C45 C48 C49 C51 C52 C54 C55 C57 C60 C61 C62 C65 C66 C67 C68 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81	KEMET	C0805C104K5RAC		A
3	001-04076-Z1	A	CAP 0.01uF ±10% 50V NPb X7R 0805	8	C3 C4 C5 C9 C10 C14 C22 C23	KEMET	C0805C103K5RAC		A
4	004-00102-Z1	A	CAP 100uF ±10% 16V TANT NPb CASE D	9	C6 C7 C8 C18 C19 C20 C28 C29 C35	KEMET	T491D107K016AS		A
5	001-06603-Z1	A	CAP 0.01uF ±5% 25V C0G NPb 1206	8	C37 C38 C39 C40 C41 C46 C47 C50	KEMET	C1206C103J3GAC		A
6	000-00009-Z1	A	NO POP CAP NPb 1206	0	C53 C56 C58	NO POP	NP-CAP-1206	DO NOT POPULATE	A
7	070-00004-Z1	A	DIODE SCHTTKY BARR 30V 0.2A NPb AXL	4	D1 D2 D3 D4	PHILIPS	BAT85		A
8	070-00024-Z1	A	DIODE SWT 70V 215mA NPb SOT-23	4	D5 D6 D7 D8	ON SEMICONDUCTOR	BAV99LT1G		A
9	070-00055-Z1	A	DIODE ARRAY 5V (TVS) ESD NPb SOT143	1	D9	LITTELFUSE	SP0503BAHTL		A
10	165-00004-Z1	A	LED SUP RED 1.7V 1mA 1.6MCD NPb SMD	1	D10	CHICAGO MINIATURE	CMD28-21SRC/TR8/T1		A
11	115-00014-Z1	A	HDR 2x1 ML .1" 062BD ST GLD NPb TH	0	J1	SAMTEC	TSW-102-07-G-S	DO NOT POPULATE	A
12	110-00028-Z1	A	CON BNC-PCB RCPT NPb RA	1	J4	KINGS	KC-79-237 M06		A
13	115-00014-Z1	A	HDR 2x1 ML .1" 062BD ST GLD NPb TH	2	J5 J56	SAMTEC	TSW-102-07-G-S		A
14	130-00007-Z1	A	JACK BAN SOLDR TERM NYL INS GRN NPb	1	J6	JOHNSON COMPONENTS	108-0904-001	REQUIRES BINDING POST HOOK UP WIRE. L 1.500 X 0.250T X 0.250T TYPE E 24/19 BLU SQUIRES ELEC. INC.	A
15	130-00009-Z1	A	JACK BAN SOLDR TERM NYL INS YLW NPb	1	J7	JOHNSON COMPONENTS	108-0907-001	REQUIRES BINDING POST HOOK UP WIRE. L 1.500 X 0.250T X 0.250T TYPE E 24/19 BLU SQUIRES ELEC. INC.	A
16	130-00014-Z1	A	JACK BAN SOLDR TERM NYL INS BLK NPb	1	J8	JOHNSON COMPONENTS	108-0903-001	REQUIRES BINDING POST HOOK UP WIRE. L 1.500 X 0.250T X 0.250T TYPE E 24/19 BLU SQUIRES ELEC. INC.	A
17	130-00006-Z1	A	JACK BAN SOLDR TERM NYN INS RED NPb	1	J9	JOHNSON COMPONENTS	108-0902-001	REQUIRES BINDING POST HOOK UP WIRE. L 1.500 X 0.250T X 0.250T TYPE E 24/19 BLU SQUIRES ELEC. INC.	A
18	115-00016-Z1	A	HDR 3x2 ML .1"CTR 062 S GLD NPb	3	J10 J11 J21	SAMTEC	TSW-103-07-G-D		A
19	115-00013-Z1	A	HDR 2x2 MLE .1"CTR .062BD S GLD NPb	8	J12 J13 J19 J22 J23 J33 J34 J43	SAMTEC	TSW-102-07-G-D		A
20	115-00012-Z1	A	HDR 4x2 MLE .1"CTR S GLD NPb	6	J14 J15 J24 J25 J40 J58	SAMTEC	TSW-104-07-G-D		A
21	115-00029-Z1	A	HDR 8x2 ML .1" 062BD ST GLD NPB TH	3	J16 J17 J18	SAMTEC	TSW-108-07-G-D		A
22	115-00011-Z1	A	HDR 10x2 ML .1" 062BD ST GLD NPb TH	0	J26 J44 J46 J52 J53 J54 J55 J61 J62	SAMTEC	TSW-110-07-G-D	DO NOT POPULATE	A
23	115-00061-Z1	A	HDR 12x2 ML .1" CTR 062 S GLD NPb	1	J27	SAMTEC	TSW-112-07-G-D		A
24	115-00061-Z1	A	HDR 12x2 ML .1" CTR 062 S GLD NPb	0	J28 J35	SAMTEC	TSW-112-07-G-D	DO NOT POPULATE	A
25	115-00023-Z1	A	HDR 14x2 ML .1"CTR 062 S GLD NPb	0	J30 J31 J37 J38	SAMTEC	TSW-114-07-G-D	DO NOT POPULATE	A
26	110-00055-Z1	A	CON TERM BLCK 4 POS 5mm C/C NPb BLU	2	J32 J41	ON-SHORE TECHNOLOGY	ED 100/4DS		A
27	115-00176-Z1	A	HDR 7x2 ML 2MM CTR 062BD S GLDTHNPb	1	J39	MOLEX	87758-1416		A
28	115-00012-Z1	A	HDR 4x2 MLE .1"CTR S GLD NPb	0	J45	SAMTEC	TSW-104-07-G-D	DO NOT POPULATE	A
29	110-00041-Z1	A	CON RA USB BLK NPb	1	J47	AMP	292304-1		A
30	110-00056-Z1	A	CON TERM BLCK 2 POS 5mm C/C NPb BLU	3	J50 J59 J63	ON-SHORE TECHNOLOGY	ED 100/2DS		A
31	115-00003-Z1	A	HDR 5x2 MLE .1"CTR S GLD NPb	1	J60	SAMTEC	TSW-105-07-G-D		A
32	080-00004-Z1	A	WIRE JUMPER 2P 0.1" BRASS NPb	6	JP1 JP2 JP3 JP4 JP5 JP6	COMPONENTS CORPORATION	TP-101-10		A

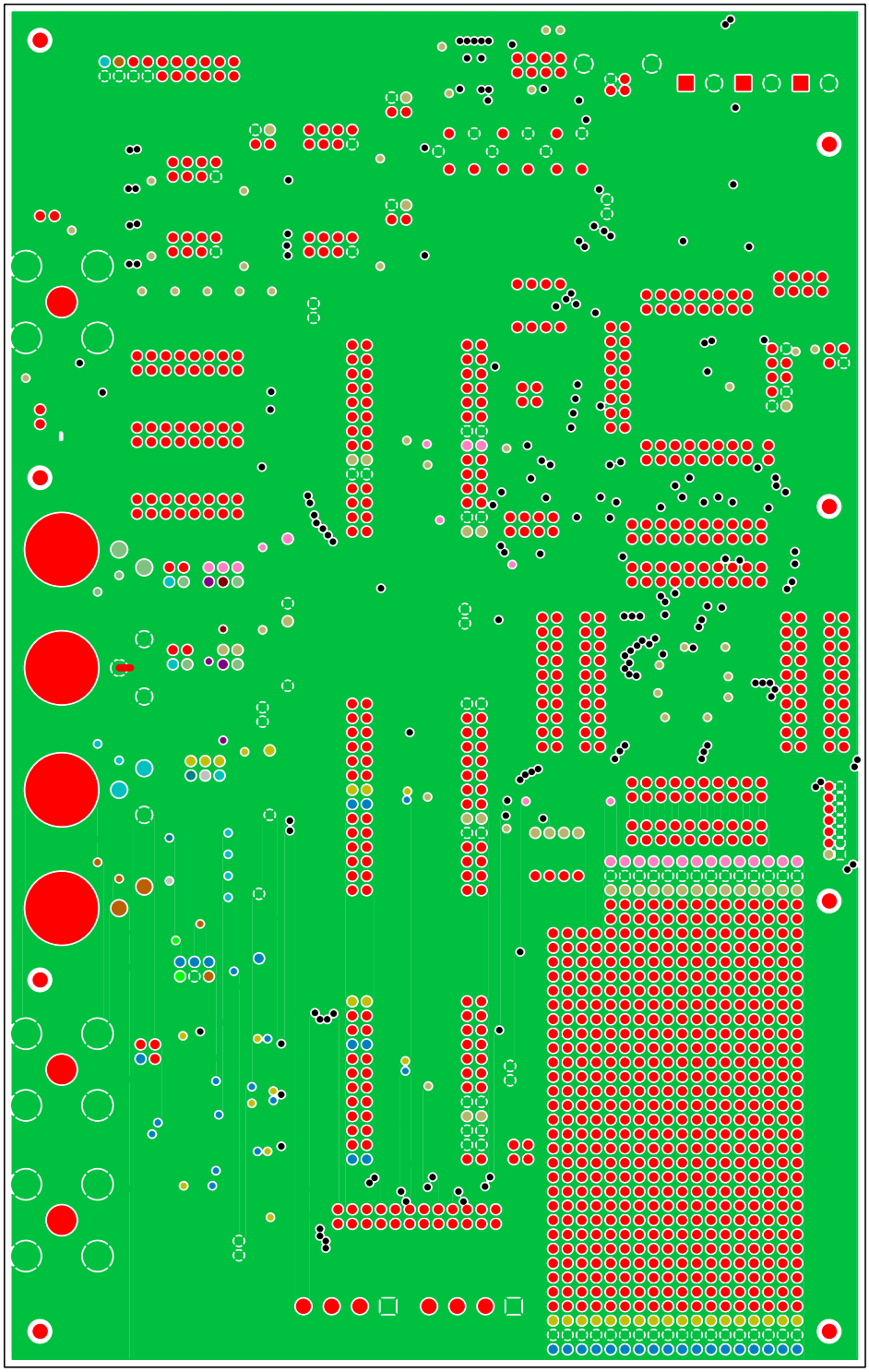
Item	Cirrus P/N	Rev	Description	Qty	Reference Designator	MFG	MFG P/N	Notes	Status
33	304-00001-Z1	A	SPCR STANDOFF 4-40 THR .875L AL NPb	8	MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8	KEYSTONE	1809	REQUIRES SCREW 4-40X5X16" PH STEEL, 300-00001-01	A
34	020-00788-Z1	A	RES 10 OHM 1/10W ±1% NPb 0603 FILM	10	R1 R11 R13 R14 R16 R17 R24 R25 R26 R68	DALE	CRCW060310R0FKEA		A
35	020-01130-Z1	A	RES 10k OHM 1/10W ±1% NPb 0603 FILM	19	R2 R6 R7 R8 R18 R20 R39 R40 R41 R42 R46 R47 R50 R51 R53 R54 R55 R56 R57	DALE	CRCW060310K0FKEA		A
36	020-00934-Z1	A	RES 200 OHM 1/10W ±1% NPb 0603 FILM	1	R3	DALE	CRCW0603200RFKEA		A
37	021-00211-Z1	A	RES 51 OHM 1/10W ±5% 0603 NPb FILM	1	R4	DALE	CRCW060351R0JNEA		A
38	020-01095-Z1	A	RES 4.99k OHM 1/10W ±1% NPb 0603	1	R5	DALE	CRCW06034K99FKEA		A
39	020-01074-Z1	A	RES 3.32k OHM 1/10W ±1% NPb 0603	2	R9 R58	DALE	CRCW06033K32FKEA		A
40	020-01128-Z1	A	RES 9.53k OHM 1/10W ±1% NPb 0603	3	R10 R12 R21	DALE	CRCW06039K53FKEA		A
41	020-01104-Z1	A	RES 5.9k OHM 1/10W ±1% NPb 0603 FLM	1	R19	DALE	CRCW06035K90FKEA		A
42	000-00001-Z1	A	NO POP RES NPb 0805	0	R22 R23 R32 R33 R43 R52	NO POP	NP-RES-0805	DO NOT POPULATE	A
43	020-00673-Z1	A	RES 0 OHM 1/10W ±5% NPb 0603 FILM	10	R27 R28 R29 R30 R44 R45 R48 R49 R59 R62	DALE	CRCW0603000Z0EA		A
44	020-01962-Z1	A	RES 20k OHM 1/8W ±1% NPb 0805 FILM	2	R31 R38	DALE	CRCW080520K0FKEA		A
45	020-00902-Z1	A	RES 100 OHM 1/10W ±1% NPb 0603 FILM	7	R34 R35 R36 R37 R60 R63 R69	DALE	CRCW0603100RFKEA		A
46	000-00002-Z1	A	NO POP RES NPb 0603	0	R61	NO POP	NP-RES-0603	DO NOT POPULATE	A
47	020-01016-Z1	A	RES 1k OHM 1/10W ±1% NPb 0603 FILM	4	R64 R65 R66 R67	DALE	CRCW06031K00FKEA		A
48	120-00011-Z1	A	SWT 4 POS DIP RAISED NPb SPST	2	S1 S5	GRAYHILL	76SB04T		A
49	120-00002-Z1	A	SWT SPST 130G 0/1 5mm TACT ESD NPb	3	S2 S3 S4	ITT INDUSTRIES	PTS645TL50	INSTALL AFTER WASH PROCESS	A
50	060-00195-Z1	A	IC LOW V DUL SPST ANA SWTCH NPbMSP8	2	U1 U2	VISHAY	DG2003DQ-E3		A
51	060-00063-Z1	A	IC LNR V REG200mA NEGADJ NPbSOT23-5	1	U3	LINEAR TECH	LT1964ES5-BYP#PBF		A
52	061-00062-Z1	A	IC LOG, LTTLE LG SNGL D-FF NPbSSOP8	5	U4 U9 U10 U15 U16	TEXAS INSTRUMENTS	SN74LVC2G74DCTRE4		A
53	060-00062-Z1	A	IC LN V REG LNOIS 500mA NPb SO8-150	4	U5 U6 U7 U8	LINEAR TECH	LT1763CS8#PBF		A
54	065-00178-Z1	E	IC CRUS LOW V AMP DC-1kHz NPb SOIC8	1	U11	CIRRUS LOGIC	CS3011-ISZ/E		A
55	060-00162-Z1	A	IC 3.3V U LW PWR RS485 XCVR NPSOIC8	4	U12 U13 U17 U18	LINEAR TECH	LTC1480IS8#PBF		A
56	060-00236-Z1	A	IC LNR PRC VRF 2.5V TC10 NPbSO8-150	1	U14	LINEAR TECH	LT1019AIS8-2.5#PBF		A
57	065-00051-Z1	C	IC CRUS DIDO AMP NPb SSOP24	1	U19	CIRRUS LOGIC	CS3301-ISZ/C		A
58	065-00196-Z1	A	IC CRUS TEST DAC NPb SSOP28	1	U20	CIRRUS LOGIC	CS5373A-ISZ/A		A
59	065-00130-Z1	A	IC CRUS 1CH DIG FLTR NPb SSOP28	1	U22	CIRRUS LOGIC	CS5378-ISZ/A		A
60	060-00067-Z1	A	IC LNR DUL CMOSSW DBNCR NPbSOT223-6	2	U23 U26	MAXIM	MAX6817EUT-T+		A
61	061-00064-Z1	A	IC LOG, HEX INVERTER NPb SO14-150	1	U24	TEXAS INSTRUMENTS	SN74LVC04ADE4		A
62	062-00022-Z1	A	IC PGM EEPROM 8kX8 SPI SRL NPbSOIC8	1	U25	ATMEL	AT25640N-10SI-2.7		A
63	062-00055-Z1	A	IC PGM 128 MCROCLL CPLD NPb VQFP100	1	U27	XILINX	XCR3128XL-10VQG100I		A
64	062-00079-Z1	A	IC PGM USB 16kB FLAS MCU NPb LQFP32	1	U28	SILICON LABORATORIES INC	C8051F320-GQ		A
65	102-00017-Z2	A	OSC 32.768MHz 90ppm 3.3V VCL NPb SM	1	Y1	CITIZEN	CSX750VBEL32.768M-UT		A
66	070-00005-Z1	A	DIODE TR 13V 600W NPb AXL	3	Z1 Z2 Z3	LITTELFUSE	P6KE13A		A
67	080-00003-Z1	A	WIRE BPOST 1.5X.25 24/19 GA BLU NPb	4	XJ6 XJ7 XJ8 XJ9	SQUIRES	L-1.5X.25TX.25T_TYPE_E_		A
68	110-00013-Z1	D	CON SHUNT 2P .1"CTR BLK NPb	28		MOLEX	15-29-1025		A
69	603-00133-Z1	C	ASSY DWG PWA CDB5378-Z NPb	REF		CIRRUS LOGIC	603-00133-Z1		
70	240-00133-Z1	C	PCB CDB5378-Z NPb	1		CIRRUS LOGIC	240-00133-Z1		A
71	600-00133-Z1	C	SCHEM CDB5378-Z NPb	REF		CIRRUS LOGIC	600-00133-Z1		A

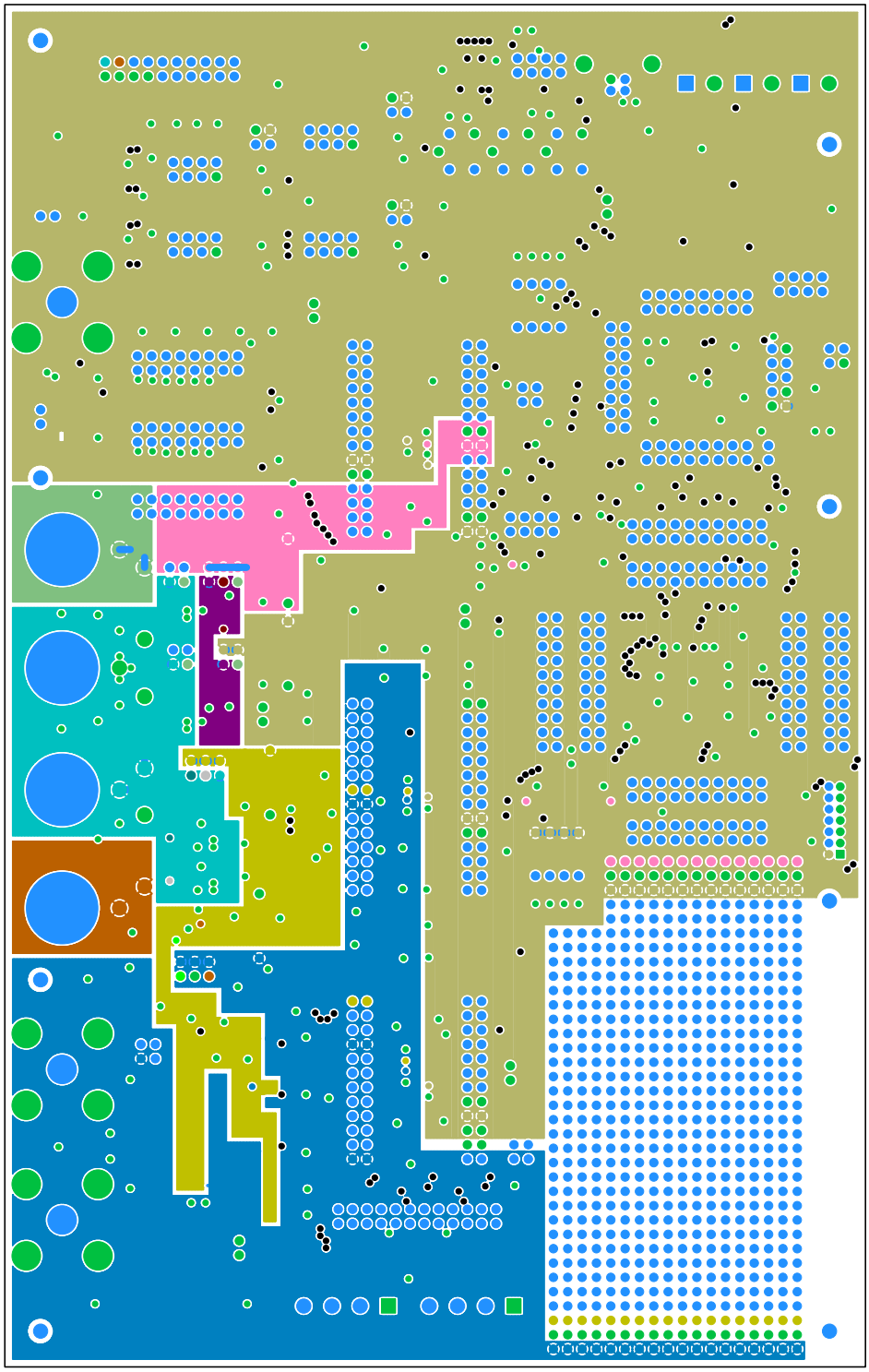
Item	Cirrus P/N	Rev	Description	Qty	Reference Designator	MFG	MFG P/N	Notes	Status
72	300-00025-Z1	A	SCREW 4-40X5/16" PH MACH SS NPb	8	XMH1 XMH2 XMH3 XMH4 XMH5 XMH6 XMH7 XMH8	BUILDING FASTENERS	PMSSS 440 0031 PH		A
73	110-00028-Z1	A	CON BNC-PCB RCPT NPb RA	0	J2 J3	KINGS	KC-79-237 M06	DO NOT POPULATE	A
74	115-00013-Z1	A	HDR 2x2 MLE .1"CTR .062BD S GLD NPb	0	J42 J57	SAMTEC	TSW-102-07-G-D	DO NOT POPULATE	A
75	115-00029-Z1	A	HDR 8x2 ML .1" 062BD ST GLD NPB TH	0	J48 J49 J51	SAMTEC	TSW-108-07-G-D	DO NOT POPULATE	A

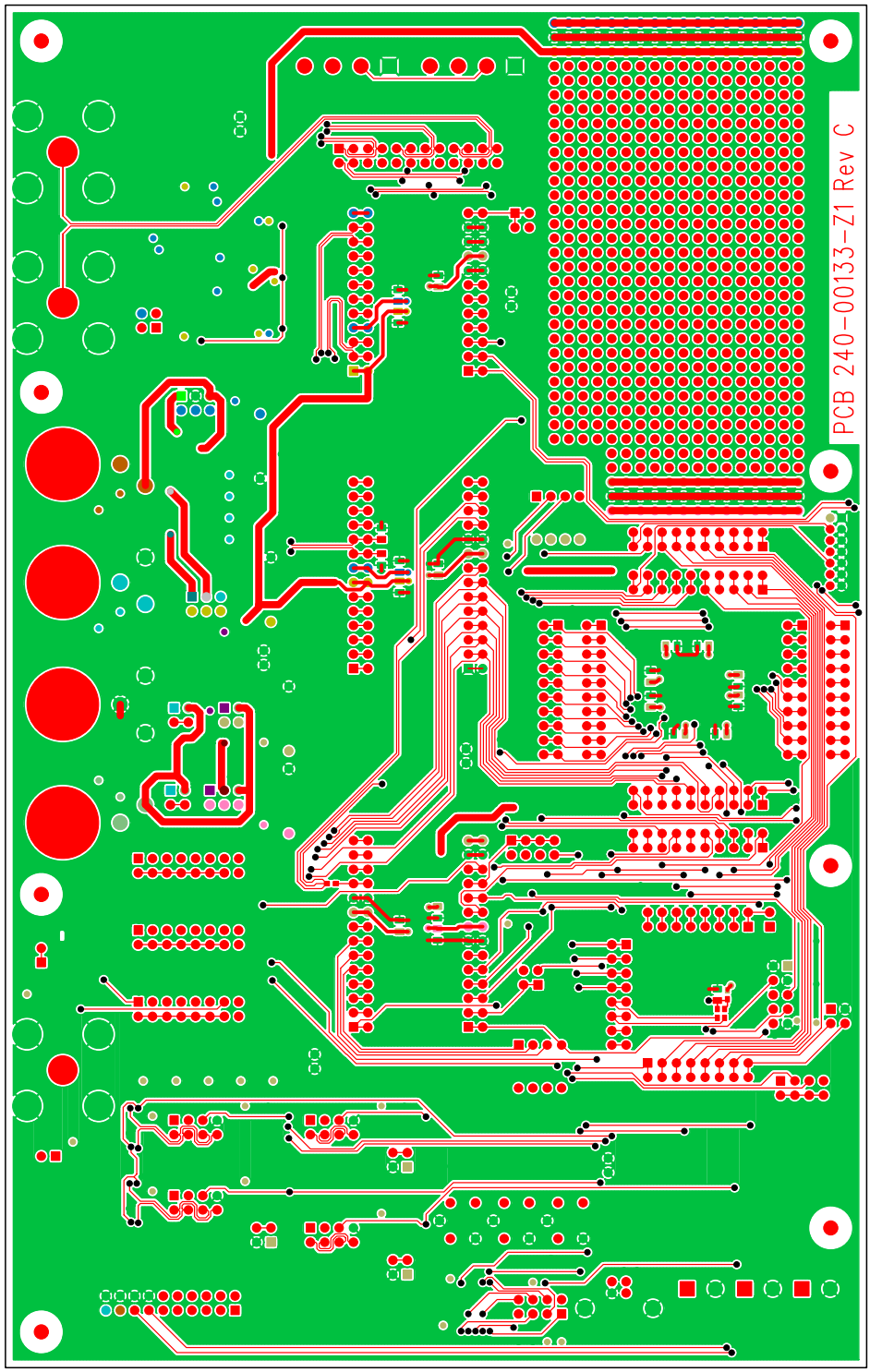
5. LAYER PLOTS

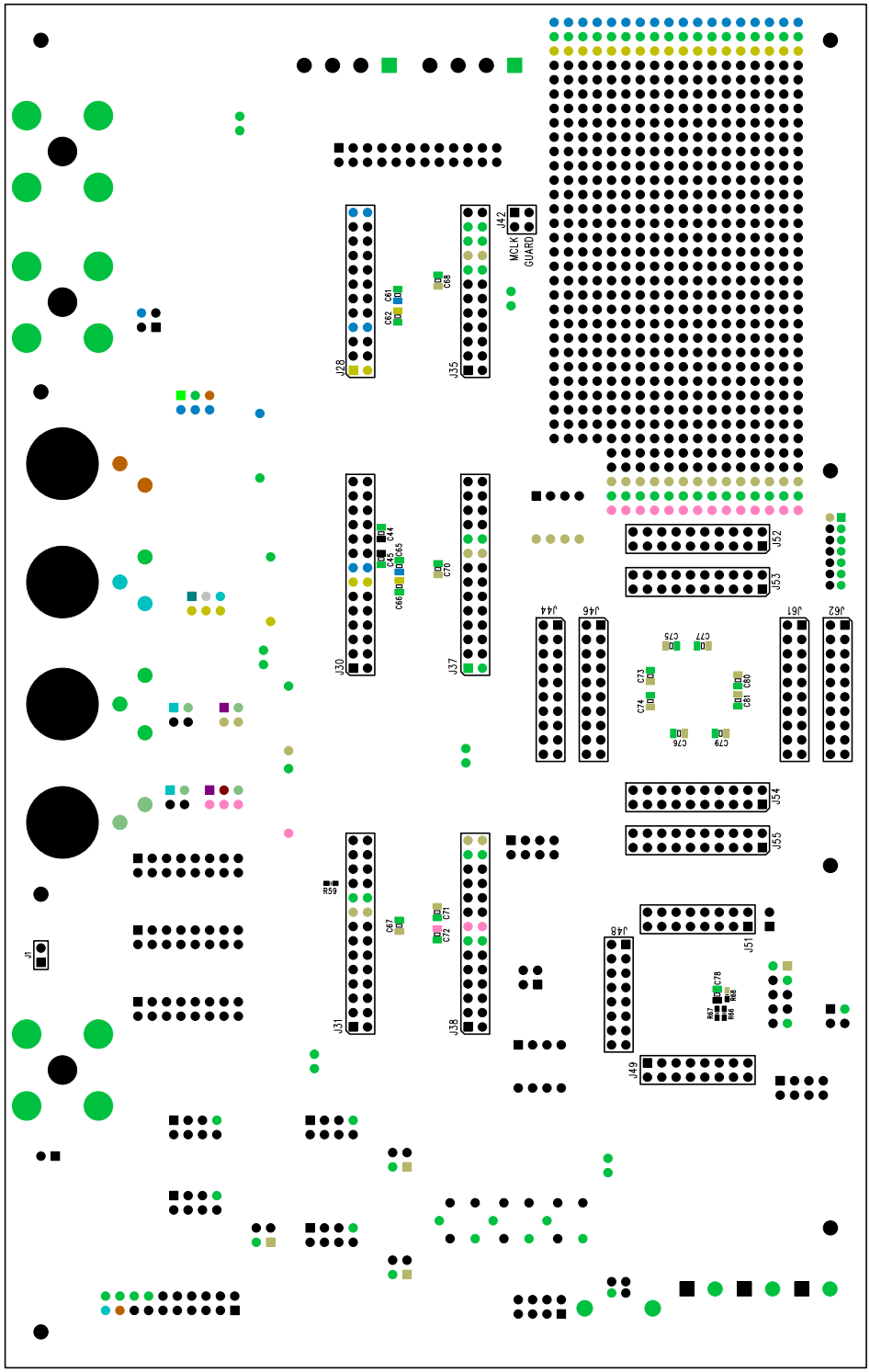



PCB 240-00133-Z1 Rev C
CIRRUS LOGIC
TOP SIDE

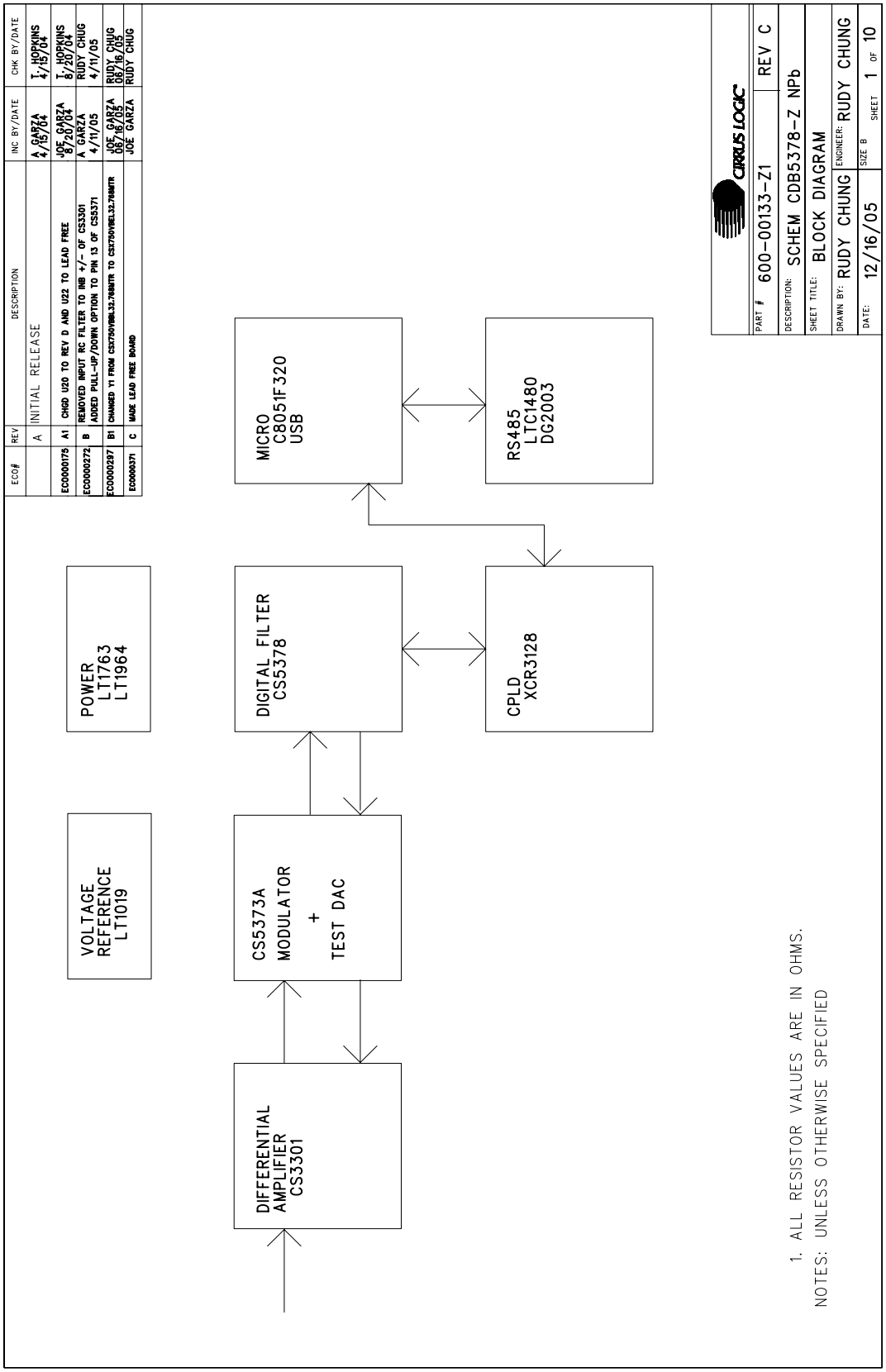

CIRRUS LOGIC
PCB 240-00133-Z1 Rev C
LAYER2 GND PLANE

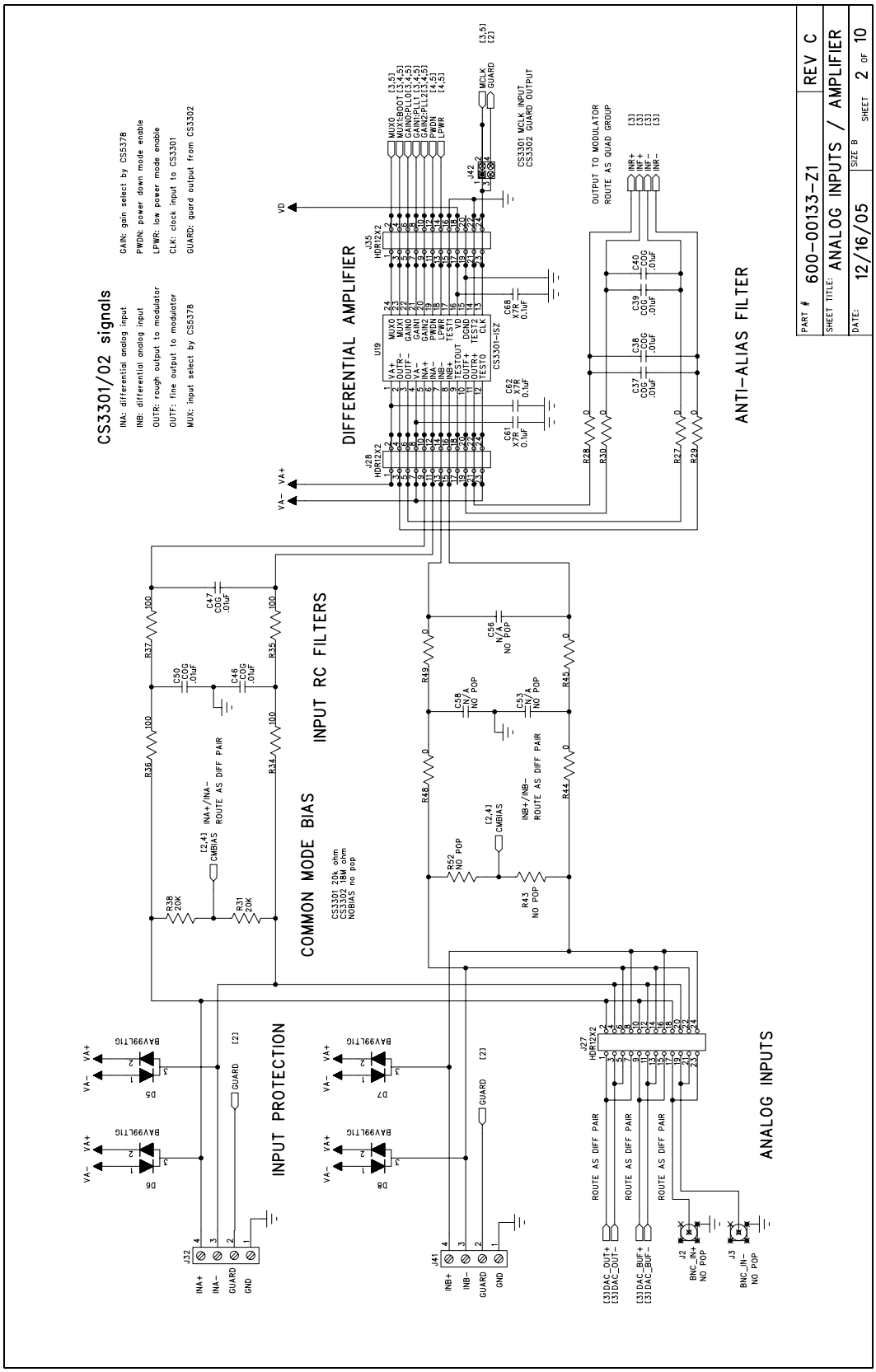

PCB 240-00133-Z1 Rev C
CIRRUS LOGIC
LAYER3 PWR PLANE

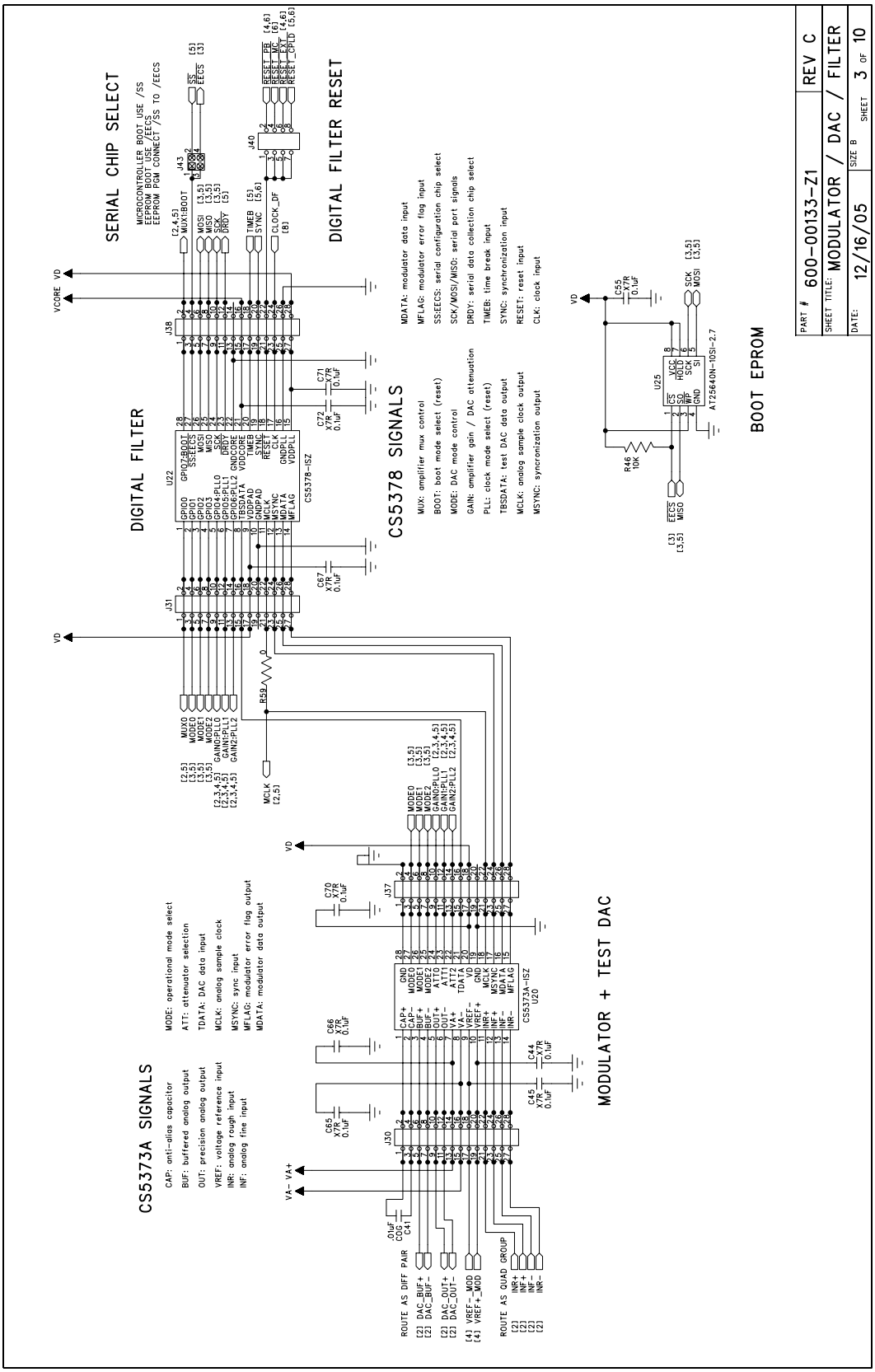

PCB 240-00133-Z1 Rev C
CIRRUS LOGIC
BOTTOM SIDE

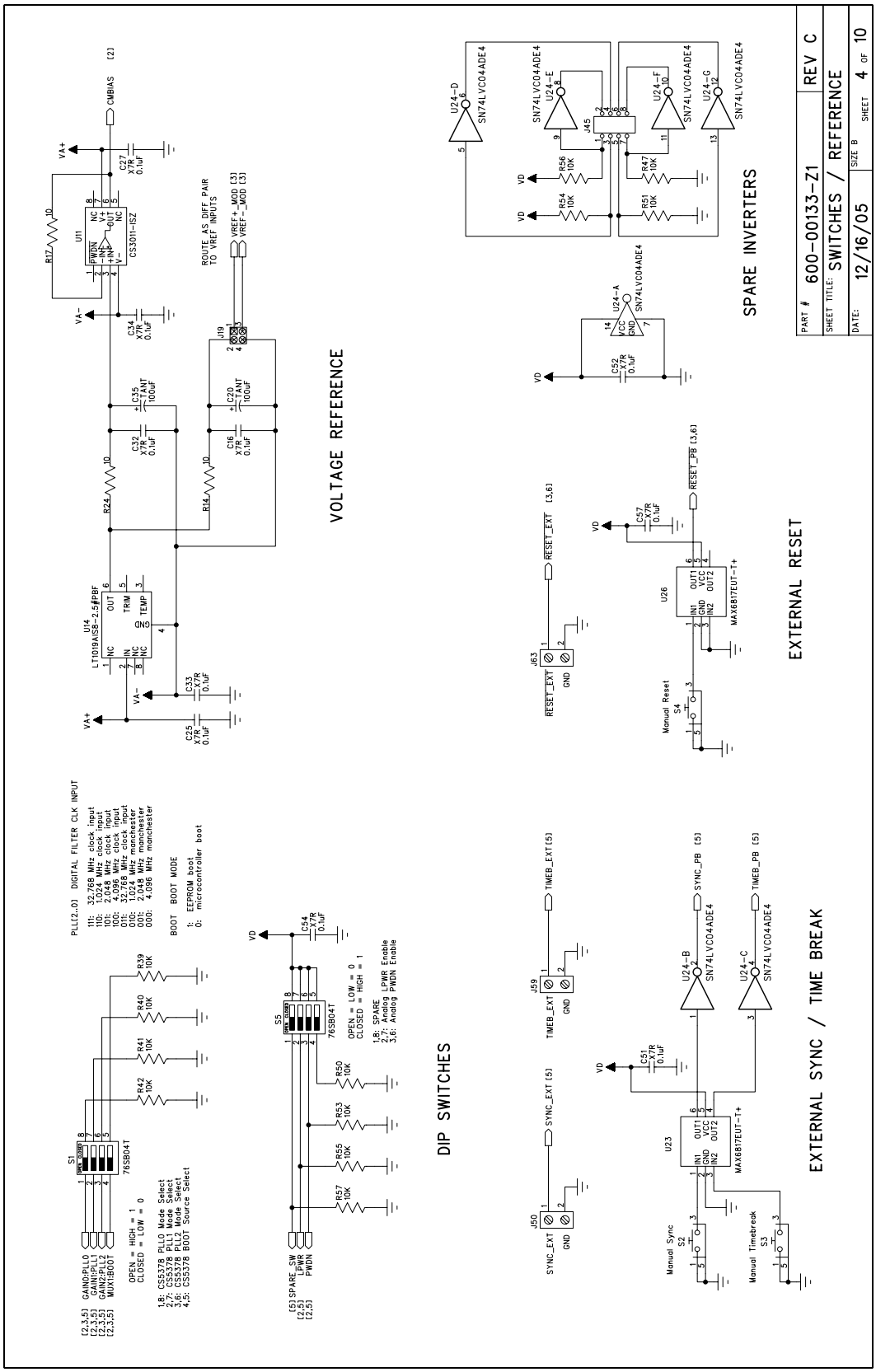

CIRRUS LOGIC
CDB5340-00132-F1 Rev C
SILKSCREEN BOTTOM

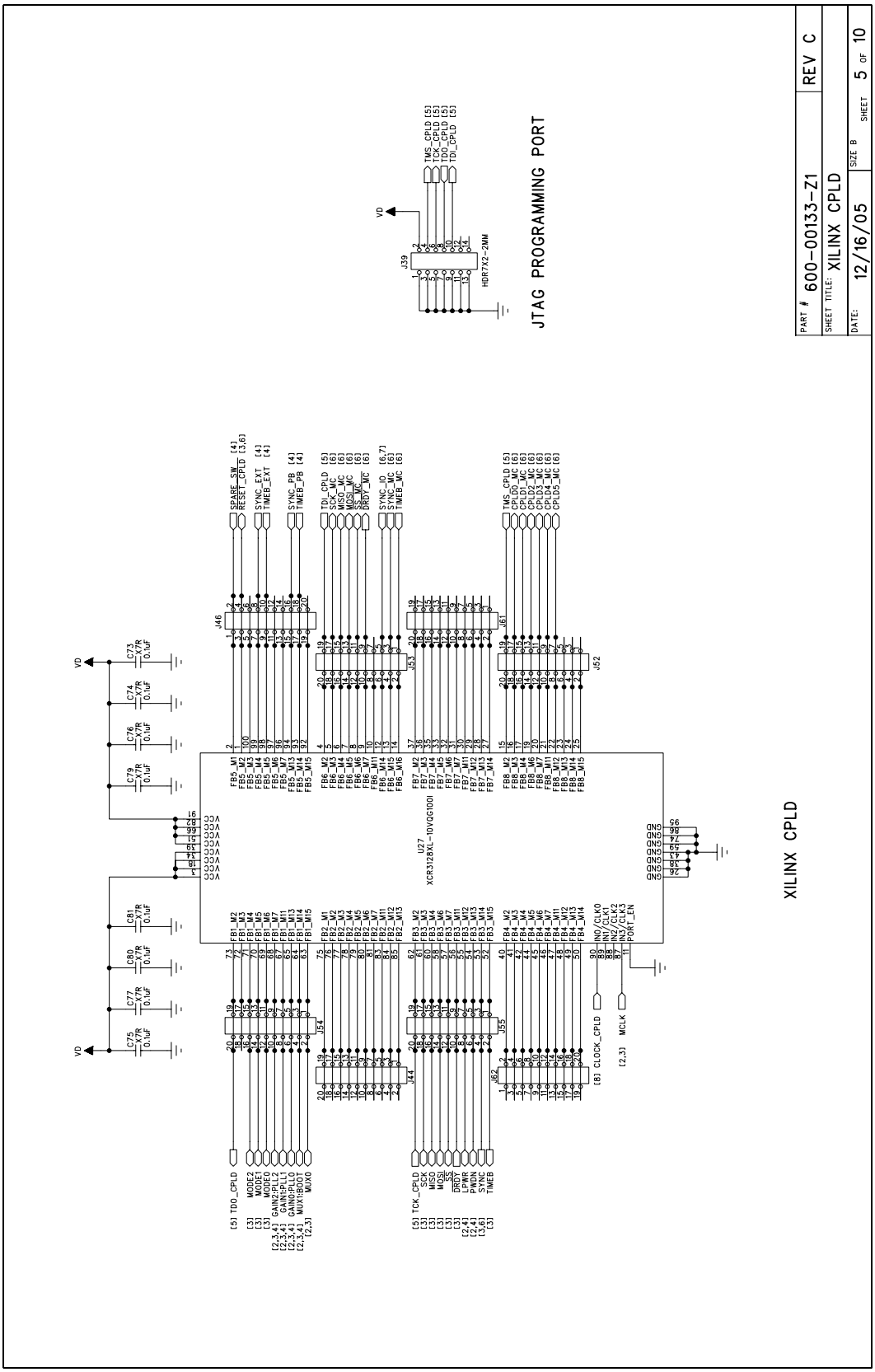
6. SCHEMATICS

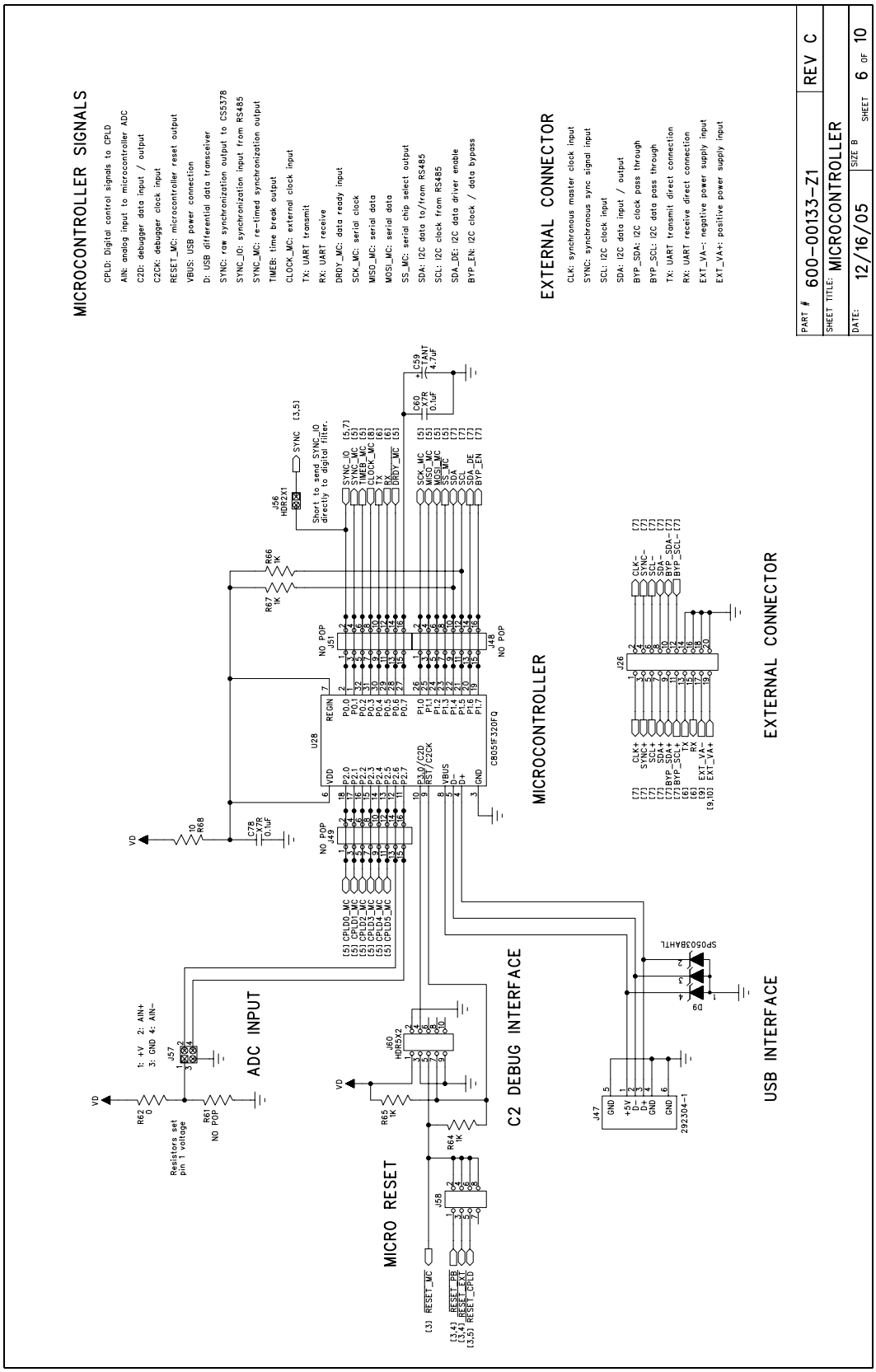


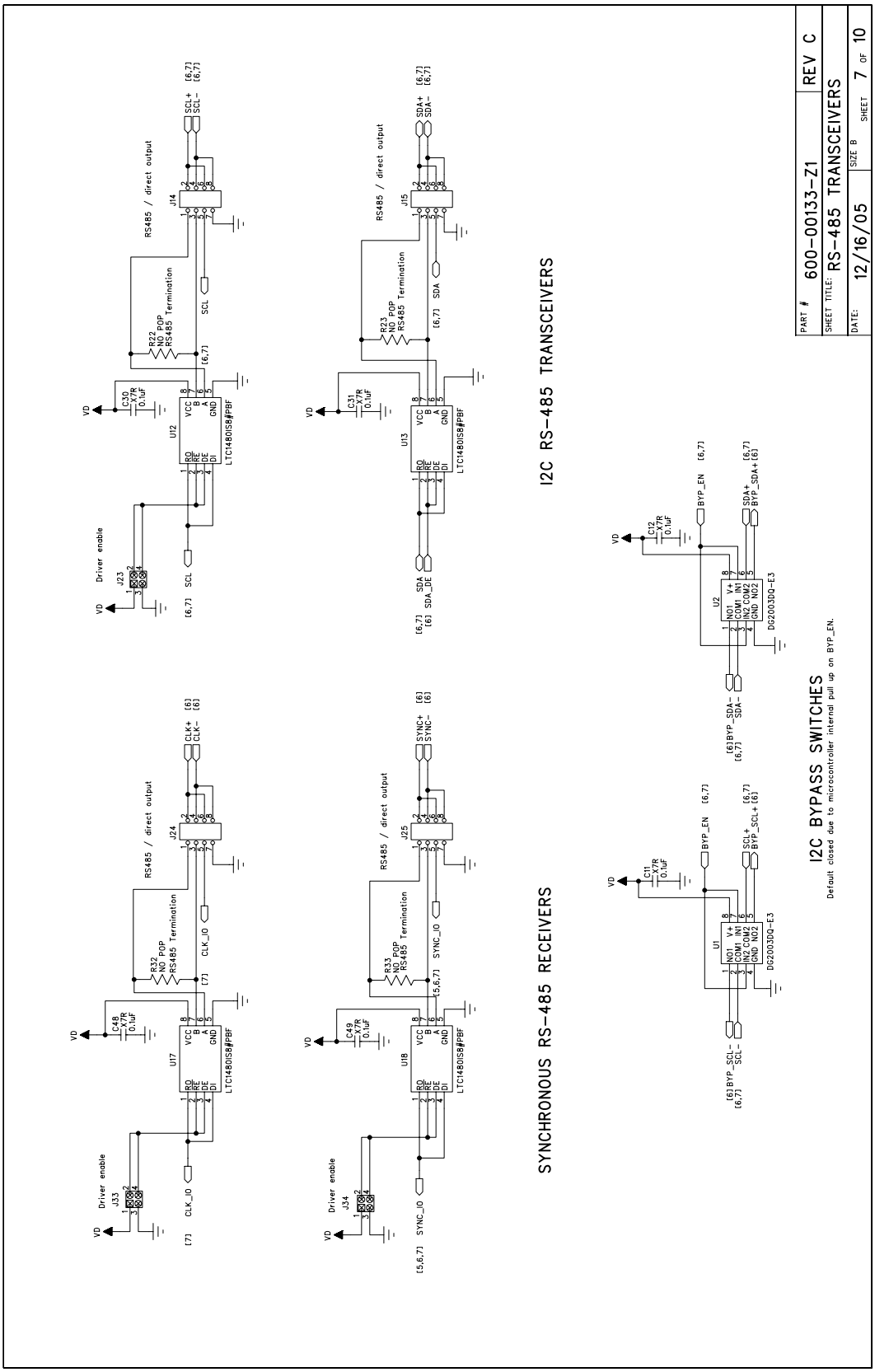

CS3301/02 signals
INA: differential analog input
INB: differential analog input
OUTR: rough output to modulator
OUTF: fine output to modulator
MUX: input select by CS5378
GAIN: gain select by CS5378
PWDN: power down mode enable
LPWR: low power mode enable
CLK: clock input to CS3301
GUARD: guard output from CS3302
DIFFERENTIAL AMPLIFIER
ANTI-ALIAS FILTER
OUTPUT TO MODULATOR
ROUTE AS QUAD GROUP
CS3301 MCLK INPUT
CS3302 GUARD OUTPUT
INPUT RC FILTERS
COMMON MODE BIAS
CS3301 20k ohm
CS3302 18M ohm
NOBIAS no pop
INA+/INA-
ROUTE AS DIFF PAIR
INB+/INB-
ROUTE AS DIFF PAIR
INPUT PROTECTION
ANALOG INPUTS
ROUTE AS DIFF PAIR
BNC_IN+
NO POP
BNC_IN-
NO POP
PART # 600-00133-Z1
REV C
SHEET TITLE: ANALOG INPUTS / AMPLIFIER
DATE: 12/16/05
SIZE B
SHEET 2 OF 10

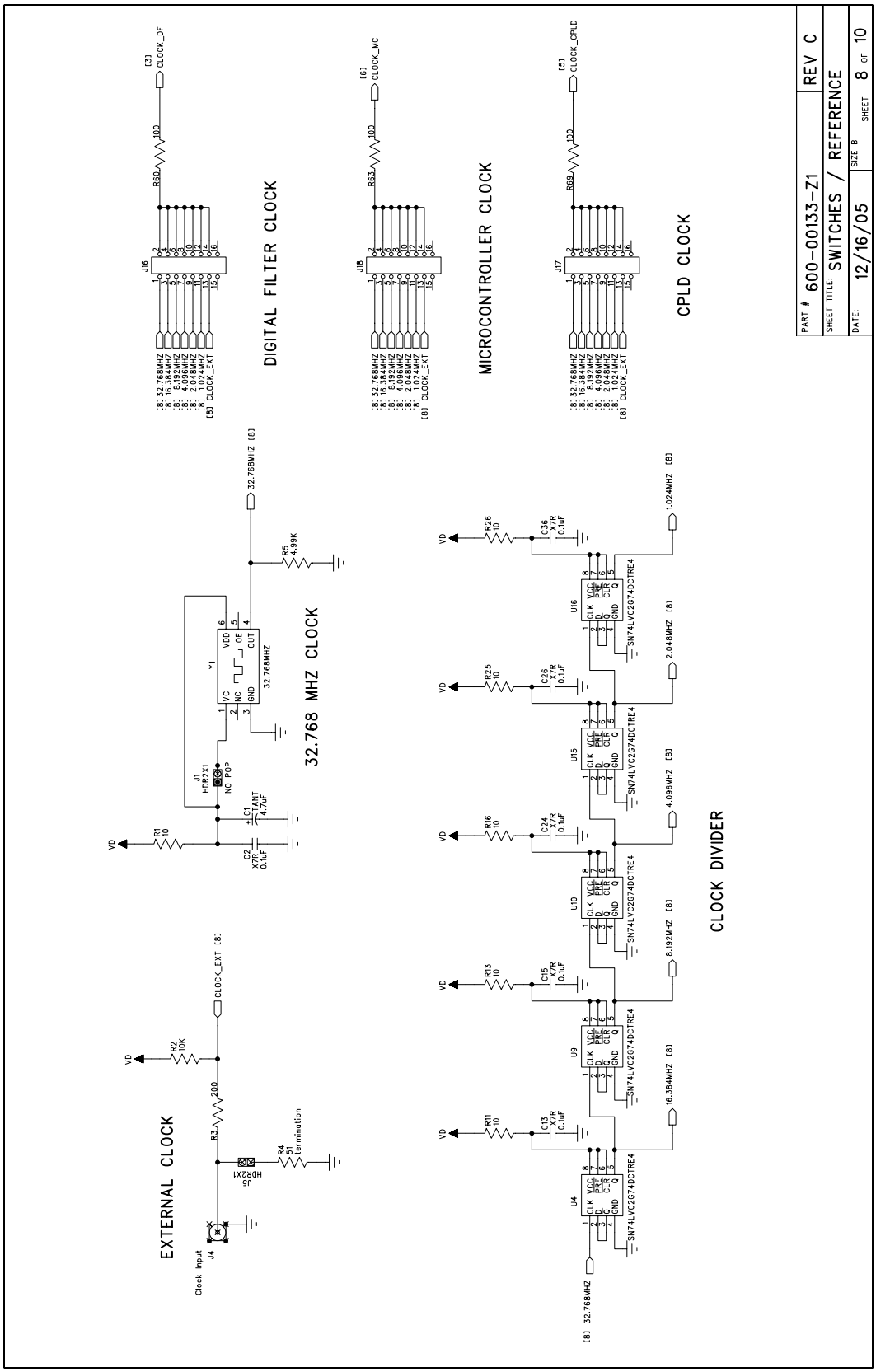

SERIAL CHIP SELECT
DIGITAL FILTER
DIGITAL FILTER RESET
CS5378 SIGNALS
BOOT EPROM
MODULATOR + TEST DAC
CS5373A SIGNALS
PART # 600-00133-Z1
REV C
SHEET TITLE: MODULATOR / DAC / FILTER
DATE: 12/16/05
SIZE B
SHEET 3 OF 10

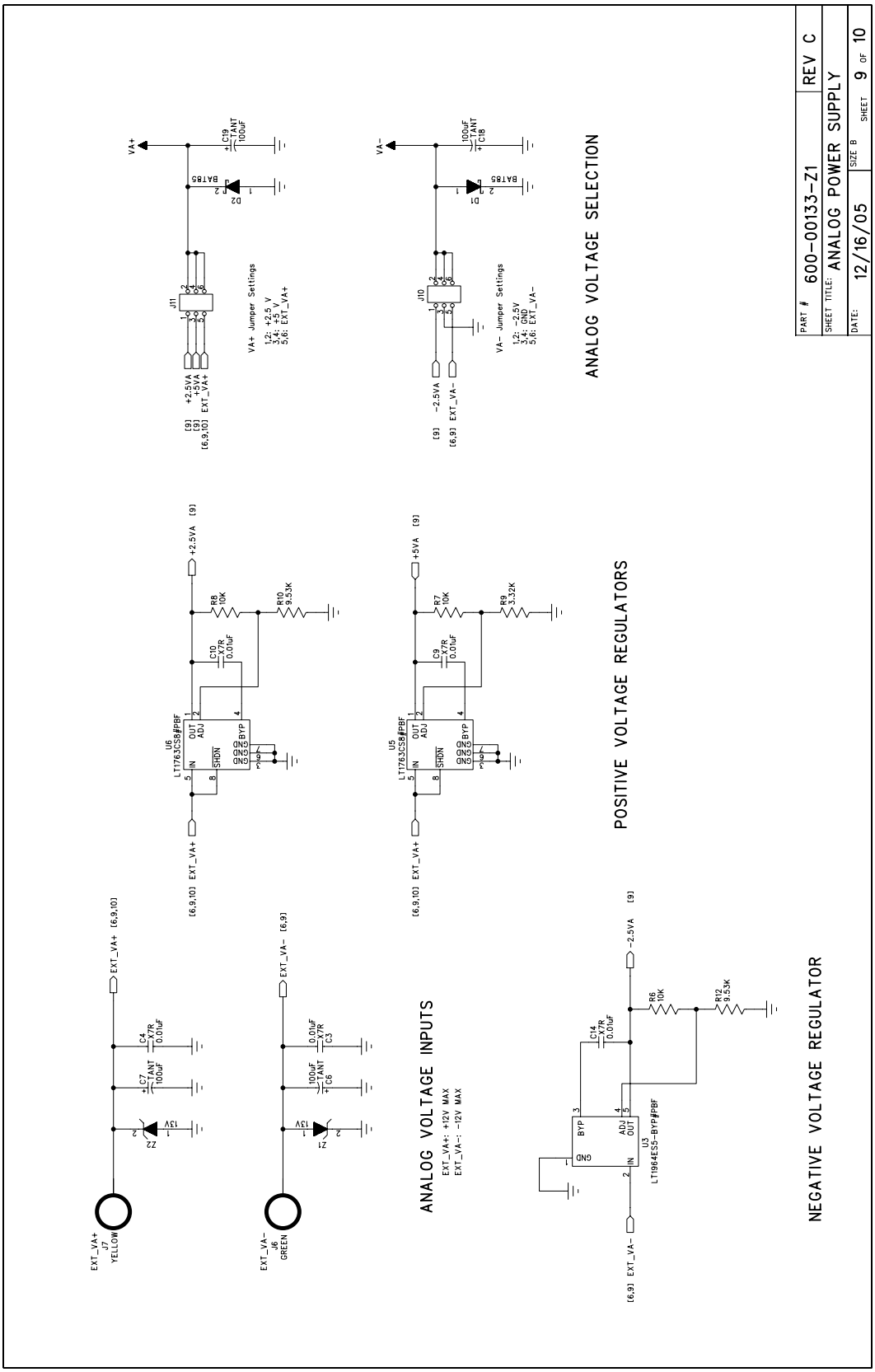

VOLTAGE REFERENCE
DIP SWITCHES
EXTERNAL SYNC / TIME BREAK
EXTERNAL RESET
SPARE INVERTERS
PART # 600-00133-Z1
REV C
SHEET TITLE: SWITCHES / REFERENCE
DATE: 12/16/05
SIZE B
SHEET 4 OF 10

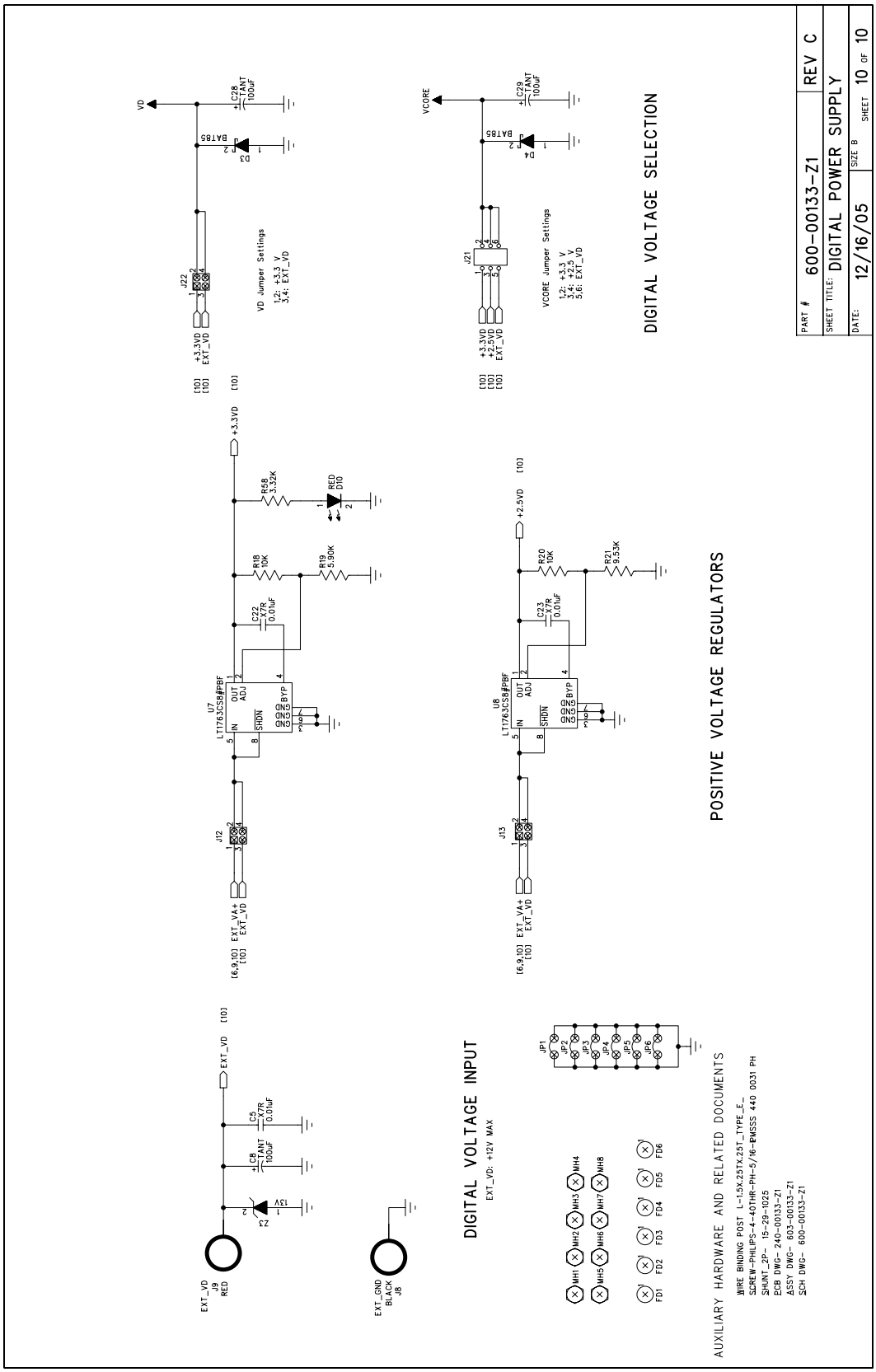

XILINX CPLD
JTAG PROGRAMMING PORT
PART # 600-00133-Z1
REV C
SHEET TITLE: XILINX CPLD
DATE: 12/16/05
SIZE B
SHEET 5 OF 10


MICROCONTROLLER SIGNALS
CPLD: Digital control signals to CPLD
AIN: analog input to microcontroller ADC
C2D: debugger data input / output
C2CK: debugger clock input
RESET_MC: microcontroller reset output
VBUS: USB power connection
D: USB differential data transceiver
SYNC: raw synchronization output to CS5378
SYNC_IO: synchronization input from RS485
SYNC_MC: re-timed synchronization output
TIMEB: time break output
CLOCK_MC: external clock input
TX: UART transmit
RX: UART receive
DRDY_MC: data ready input
SCK_MC: serial clock
MISO_MC: serial data
MOSI_MC: serial data
SS_MC: serial chip select output
SDA: I2C data to/from RS485
SCL: I2C clock from RS485
SDA_DE: I2C data driver enable
BYP_EN: I2C clock / data bypass
EXTERNAL CONNECTOR
CLK: synchronous master clock input
SYNC: synchronous sync signal input
SCL: I2C clock input
SDA: I2C data input / output
BYP_SDA: I2C clock pass through
BYP_SCL: I2C data pass through
TX: UART transmit direct connection
RX: UART receive direct connection
EXT_VA-: negative power supply input
EXT_VA+: positive power supply input
PART # 600-00133-Z1
REV C
SHEET TITLE: MICROCONTROLLER
DATE: 12/16/05
SIZE B
SHEET 6 OF 10
ADC INPUT
C2 DEBUG INTERFACE
MICRO RESET
MICROCONTROLLER
EXTERNAL CONNECTOR
USB INTERFACE
CB05IF320FQ
SP0503BAHTL
292304-1
Resistors set pin 1 voltage
Short to send SYNC_IO directly to digital filter.
NO POP


I2C RS-485 TRANSCEIVERS
SYNCHRONOUS RS-485 RECEIVERS
I2C BYPASS SWITCHES
Default closed due to microcontroller internal pull up on BYP_EN.
PART # 600-00133-Z1
REV C
SHEET TITLE: RS-485 TRANSCEIVERS
DATE: 12/16/05
SIZE B
SHEET 7 OF 10


EXTERNAL CLOCK
32.768 MHZ CLOCK
DIGITAL FILTER CLOCK
MICROCONTROLLER CLOCK
CPLD CLOCK
CLOCK DIVIDER
PART # 600-00133-Z1
REV C
SHEET TITLE: SWITCHES / REFERENCE
DATE: 12/16/05
SIZE B
SHEET 8 OF 10


ANALOG VOLTAGE SELECTION
POSITIVE VOLTAGE REGULATORS
ANALOG VOLTAGE INPUTS
NEGATIVE VOLTAGE REGULATOR
VA+ Jumper Settings
VA- Jumper Settings
PART # 600-00133-Z1
REV C
SHEET TITLE: ANALOG POWER SUPPLY
DATE: 12/16/05
SIZE B
SHEET 9 OF 10


DIGITAL VOLTAGE SELECTION
POSITIVE VOLTAGE REGULATORS
DIGITAL VOLTAGE INPUT
EXT_VD: +12V MAX
AUXILIARY HARDWARE AND RELATED DOCUMENTS
WIRE BINDING POST L-1.5X.25TX.25T_TYPE_E_
SCREW-PHILPS-4-40THR-PH-5/16-PWSSS 440 0031 PH
SHUNT_2P- 15-29-1025
PCB DWG- 240-00133-Z1
ASSY DWG- 603-00133-Z1
SCH DWG- 600-00133-Z1
VD Jumper Settings
1,2: +3.3 V
3,4: EXT_VD
VCORE Jumper Settings
1,2: +3.3 V
3,4: +2.5 V
5,6: EXT_VD
PART # 600-00133-Z1
REV C
SHEET TITLE: DIGITAL POWER SUPPLY
DATE: 12/16/05
SIZE B
SHEET 10 OF 10

7. REVISION HISTORY

Revision	Date	Changes
DB1	FEB 2006	Initial Release.
DB2	APR 2006	Minor correction.
DB3	AUG 2006	Corrected PDF printing problem.