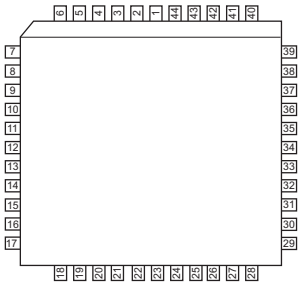
A6832

Data Sheet
26185.110F

DABiC-5 32-Bit Serial Input Latched Sink Drivers

A6832SEP/A6832EEP
44-pin PLCC



ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{OUT} ..... **40 V**
Logic Supply Voltage, V_{DD} ..... **7 V**
Input Voltage Range, V_{IN} ..... **–0.3 V to V_{DD} +0.3 V**
Continuous Output Current, I_{OUT} ..... **125 mA**
Package Power Dissipation, P_D, *see* chart, page 5
Operating Temperature Range
Ambient Temperature, T_A ..... **–20°C to +85°C**
Storage Temperature, T_S ..... **–55°C to +150°C**

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

Intended originally to drive thermal printheads, the A6832 has been optimized for low output-saturation voltage, high-speed operation, and pin configurations that are the most convenient for the tight space requirements of high-resolution printheads. These integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 125 mA peak current. The combination of bipolar and MOS technologies gives the A6832 arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar npn open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor-based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high. MOS serial data outputs permit cascading for interface applications requiring additional drive lines.

The A6832 is supplied in a 44-lead plastic leaded chip carrier (package suffix *EP*), for surface-mount applications requiring minimum area. These devices are lead (Pb) free, with 100% matte tin plated leadframes.

FEATURES

- 3.3 V to 5 V logic supply range
- To 10 MHz data input rate
- Schmitt trigger inputs for improved noise immunity
- Low-power CMOS logic and latches
- 40 V current sink outputs
- Low saturation voltage
- –40°C operation available

APPLICATIONS

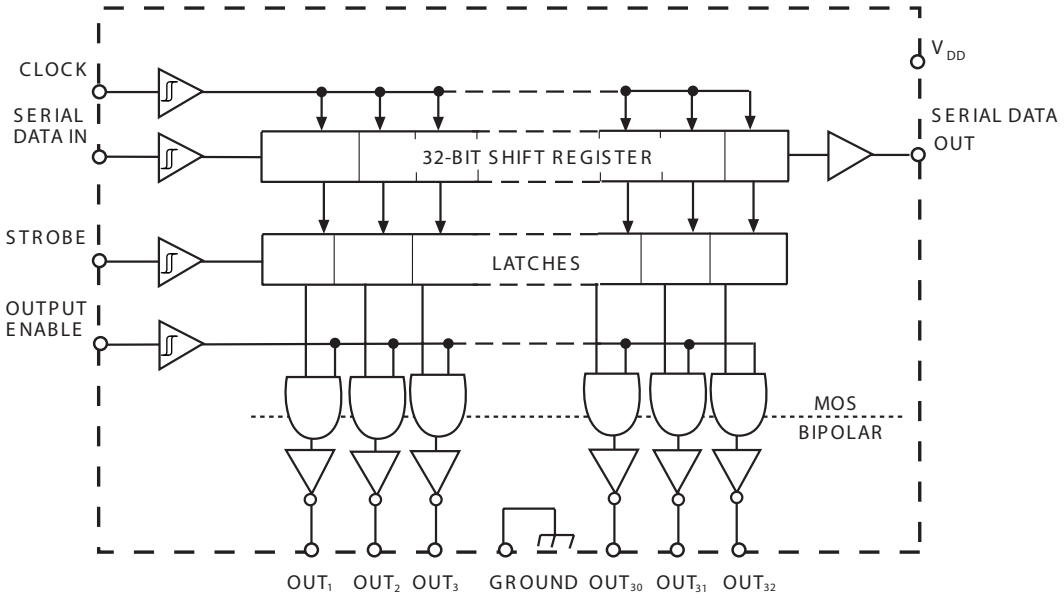
- Thermal printheads
- Multiplexed LED displays
- Incandescent lamps

Use the following complete part numbers when ordering:

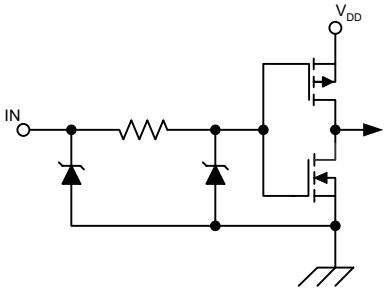
Part Number	Pins	Package	Operating Temperature
A6832SEP-T	44	PLCC	–20°C to +85°C
A6832EEP-T	44	PLCC	–40°C to +85°C

A6832
DABiC-5 32-Bit Serial-Input Latched Sink Drivers

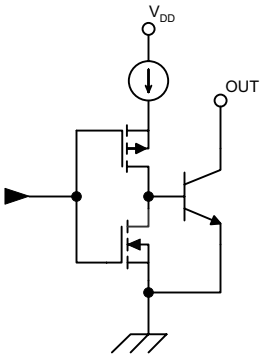
Functional Block Diagram



Typical Input Circuit



Typical Output Driver



Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

A6832
DABiC-5 32-Bit Serial-Input Latched Sink Drivers

ELECTRICAL CHARACTERISTICS[1] Unless otherwise noted: T_A = 25°C, logic supply operating voltage V_{dd} = 3.0 V to 5.5 V

Characteristic	Symbol	Test Conditions	V_{dd} = 3.3 V			V_{dd} = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 40 V	–	–	10	–	–	10	µA
Collector–Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	–	–	275	–	–	275	mV
		I_{OUT} = 100 mA	–	–	550	–	–	550	mV
Input Voltage	$V_{IN(1)}$		2.2	–	–	3.3	–	–	V
	$V_{IN(0)}$		–	–	1.1	–	–	1.7	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	–	< 0.01	1.0	–	< 0.01	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0 V	–	<–0.01	–1.0	–	<–0.01	–1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = –200 µA	2.8	3.05	–	4.5	4.75	–	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	–	0.15	0.3	–	0.15	0.3	V
Maximum Clock Frequency[2]	f_c		10	–	–	10	–	–	MHz
Logic Supply Current	$I_{DD(1)}$	One output on, I_{OUT} = 100 mA	–	–	6.0	–	–	6.0	mA
	$I_{DD(0)}$	All outputs off	–	–	100	–	–	100	µA
Output Enable-to-Output Delay	$t_{dis(BQ)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	$t_{en(BQ)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	$t_{p(STH-QH)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Fall Time	t_f	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Rise Time	t_r	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	I_{OUT} = ±200 µA	–	50	–	–	50	–	ns

[1]Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.
[2]Operation at a clock frequency greater than the specified minimum value is possible but not warranteed.

Truth Table

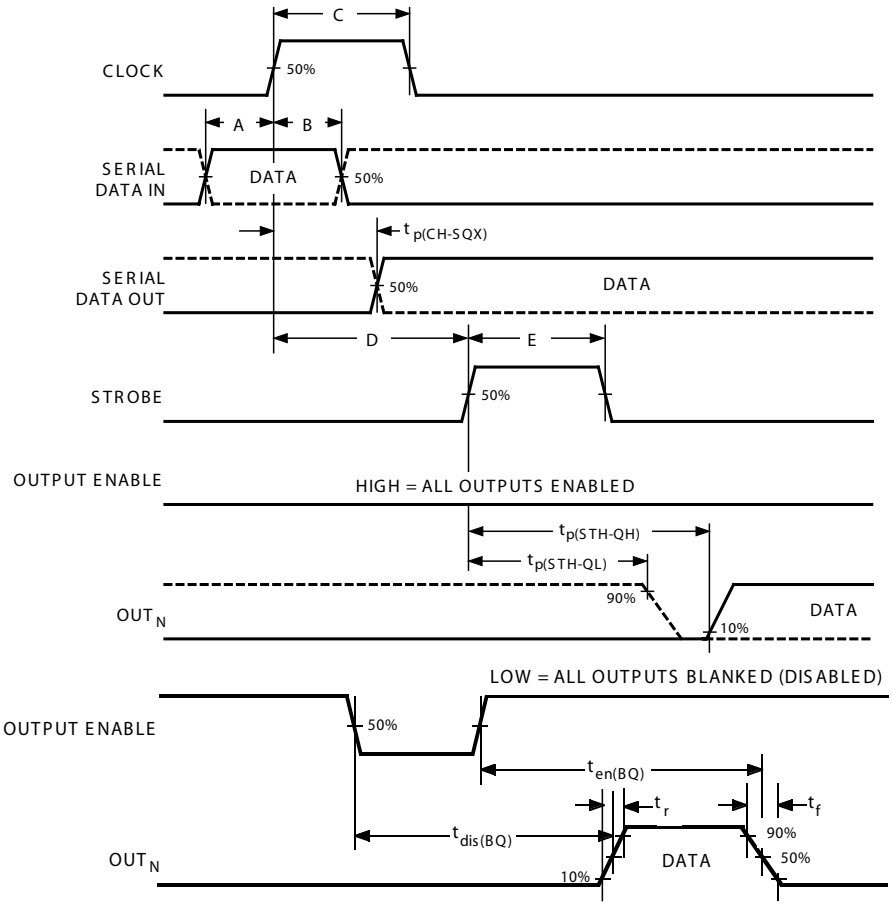
Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable Input	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	L	H H H ... H H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

A6832
DABiC-5 32-Bit Serial-Input Latched Sink Drivers

Timing Requirements and Specifications
(Logic Levels are V_{DD} and Ground)



Key	Description	Symbol	Time (ns)
A	Data Active Time Before Clock Pulse (Data Set-Up Time)	$t_{su(D)}$	25
B	Data Active Time After Clock Pulse (Data Hold Time)	$t_{h(D)}$	25
C	Clock Pulse Width	$t_{w(CH)}$	50
D	Time Between Clock Activation and Strobe	$t_{su(C)}$	100
E	Strobe Pulse Width	$t_{w(STH)}$	50

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

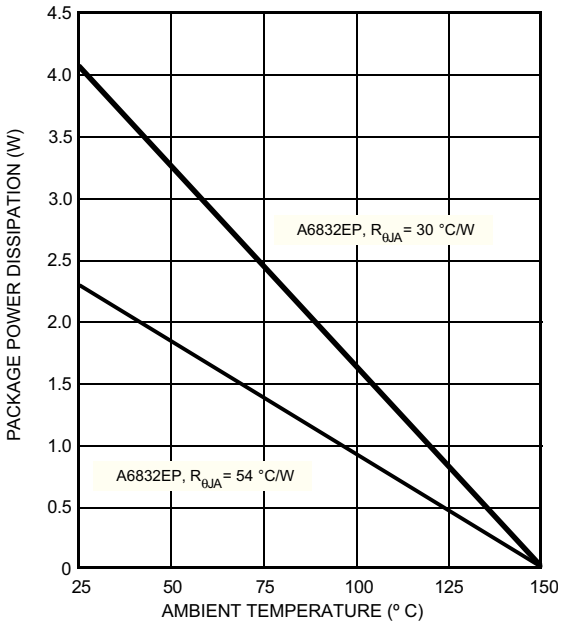
Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, the output sink drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input high, the outputs are controlled by the state of their respective latches.

Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

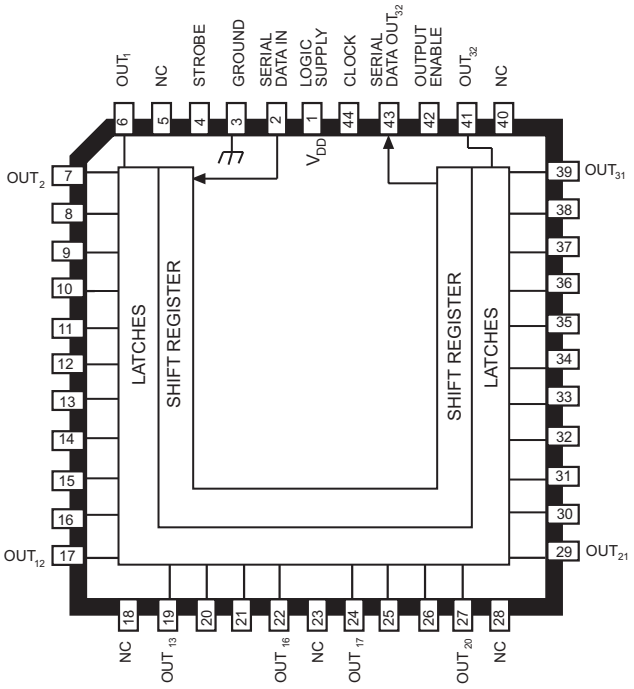
A6832
DABiC-5 32-Bit Serial-Input Latched Sink Drivers

Allowable Power Dissipation, P_D*



*Additional thermal information is available on the Allegro Web site.

A6832SEP/A6832EEP

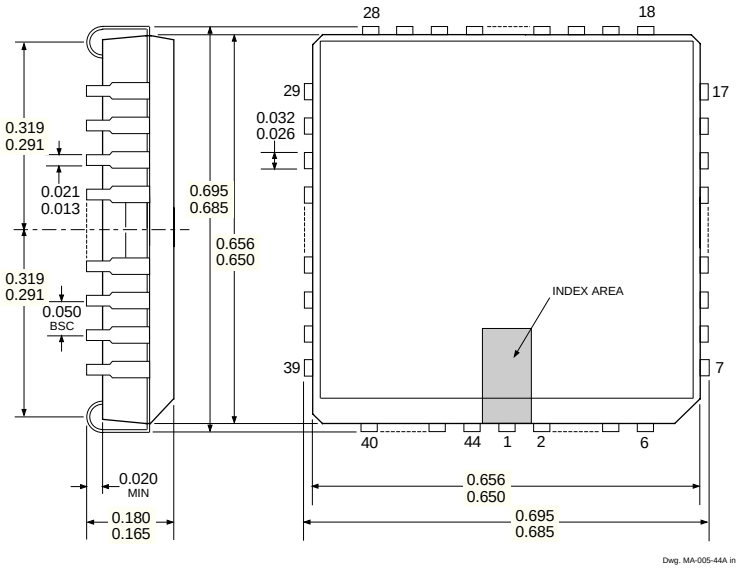


Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

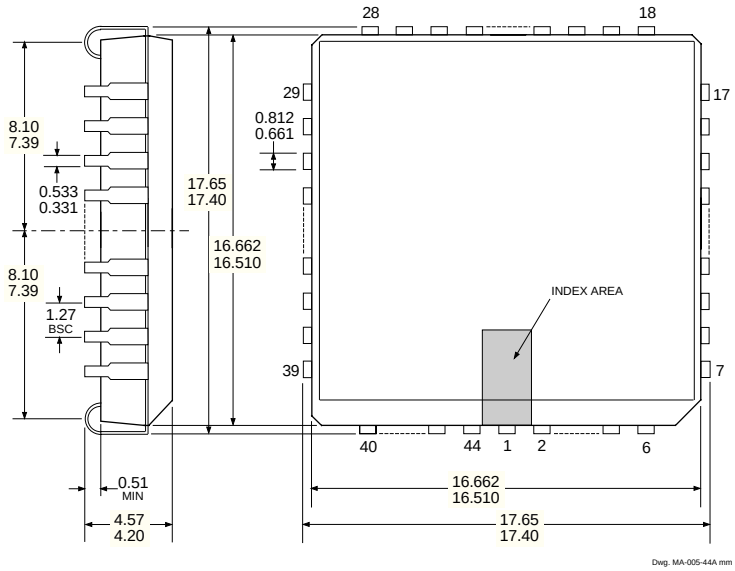
A6832
DABiC-5 32-Bit Serial-Input Latched Sink Drivers

A6832SEP and A6832EEP

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

Allegro MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

A6832
DABiC-5 32-Bit Serial-Input Latched Sink Drivers

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Allegro® MicroSystems, Inc.
www.allegromicro.com
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000