74LVC132A

Quad 2-input NAND Schmitt trigger

Rev. 01 — 15 December 2006 Product data sheet

1. General description

The 74LVC132A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC132A provides four 2-input NAND gates with Schmitt trigger inputs. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The inputs switch at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the input hysteresis voltage V_H.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environment.

2. Features

- Wide supply voltage range from 2.3 V to 3.6 V
- 5 V tolerant inputs for interfacing with 5 V logic
- CMOS low power consumption
- Direct interface with TTL levels
- Unlimited rise and fall times
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM JESD22-A114-D exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101-C exceeds 1000 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Applications

- Wave and pulse shaper
- Astable multivibrator
- Monostable multivibrator.

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC132AD	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC132APW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC132ABQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

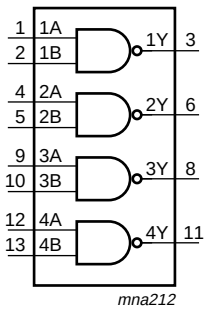


Fig 1. Logic symbol

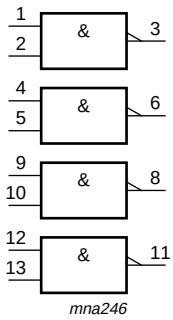


Fig 2. IEC logic symbol

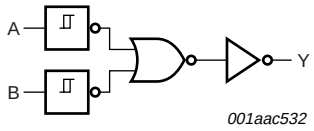


Fig 3. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

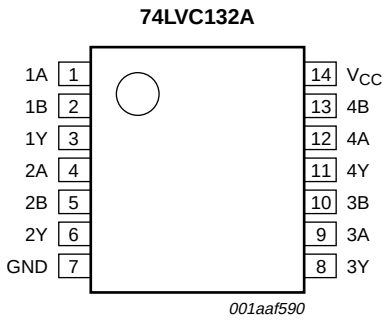
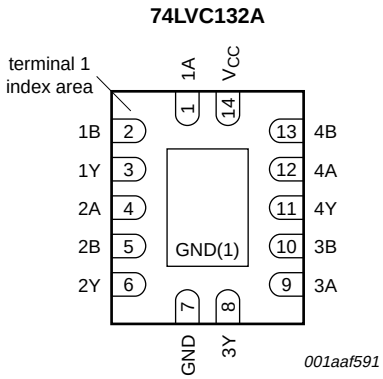


Fig 4. Pin configuration SO14 and TSSOP14



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1B	2	data input
1Y	3	data output
2A	4	data input
2B	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3B	10	data input
4Y	11	data output
4A	12	data input
4B	13	data input
V_{CC}	14	supply voltage

7. Functional description

Table 3. Function table[1]

Input		Output
nA	**nB**	**nY**
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
V_I	input voltage		[1]	–0.5	+6.5	V
V_O	output voltage		[1]	–0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		–50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} − 0.2	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	V_{CC} − 0.45	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	V_{CC} − 0.5	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	V_{CC} − 0.5	-	-	V
		I_O = −18 mA; V_{CC} = 3.0 V	V_{CC} − 0.6	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	V_{CC} − 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} − 0.6 V; I_O = 0 A	-	5	500	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	4.0	-	pF
T_{amb} = −40 °C to +125 °C						
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} − 0.3	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	V_{CC} − 0.6	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	V_{CC} − 0.65	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	V_{CC} − 0.65	-	-	V
		I_O = −18 mA; V_{CC} = 3.0 V	V_{CC} − 0.75	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	V_{CC} − 1	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 3.6 V	-	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	-	±20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} − 0.6 V; I_O = 0 A	-	-	5	mA

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[2]						
		V_{CC} = 1.2 V		-	18.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		2.0	7.2	12.8	2.0	16.0	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	4.0	7.6	1.5	9.6	ns
		V_{CC} = 2.7 V		1.5	3.8	7.6	1.5	9.6	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	3.4	6.4	1.5	8.0	ns
$t_{sk(o)}$	output skew time		[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	10.5	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	10.8	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	11.4	-	-	-	pF

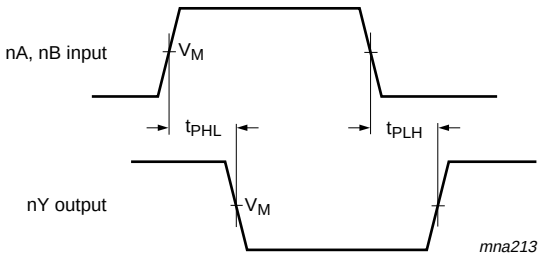
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

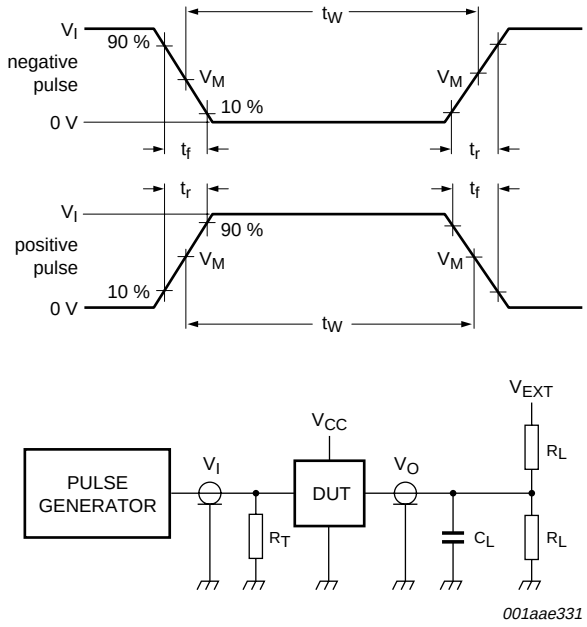
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 6. The input (nA, nB) to output (nY) propagation delays



Test data is given in Table 8. Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 7. Load circuitry for switching times

Table 8. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

13. Transfer characteristics

Table 9. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Figure 8 and Figure 9					
		V_{CC} = 1.2 V	0.2	1.0	0.2	1.0	V
		V_{CC} = 1.65 V	0.4	1.3	0.4	1.3	V
		V_{CC} = 1.95 V	0.6	1.5	0.6	1.5	V
		V_{CC} = 2.3 V	0.8	1.7	0.8	1.7	V
		V_{CC} = 2.5 V	0.9	1.7	0.9	1.7	V
		V_{CC} = 2.7 V	1.1	2	1.1	2	V
		V_{CC} = 3.0 V	1.2	2	1.2	2	V
		V_{CC} = 3.6 V	1.2	2	1.2	2	V
V_{T-}	negative-going threshold voltage	see Figure 8 and Figure 9					
		V_{CC} = 1.2 V	0.12	0.75	0.12	0.75	V
		V_{CC} = 1.65 V	0.15	0.85	0.15	0.85	V
		V_{CC} = 1.95 V	0.25	0.95	0.25	0.95	V
		V_{CC} = 2.3 V	0.4	1.1	0.4	1.1	V
		V_{CC} = 2.5 V	0.4	1.2	0.4	1.2	V
		V_{CC} = 2.7 V	0.8	1.4	0.8	1.4	V
		V_{CC} = 3.0 V	0.8	1.5	0.8	1.5	V
		V_{CC} = 3.6 V	0.8	1.5	0.8	1.5	V
V_H	hysteresis voltage	($V_{T+} - V_{T-}$); see Figure 8, Figure 9 and Figure 10					
		V_{CC} = 1.2 V	0.1	1.0	0.1	1.0	V
		V_{CC} = 1.65 V	0.2	1.15	0.2	1.15	V
		V_{CC} = 1.95 V	0.2	1.25	0.2	1.25	V
		V_{CC} = 2.3 V	0.3	1.3	0.3	1.3	V
		V_{CC} = 2.5 V	0.3	1.3	0.3	1.3	V
		V_{CC} = 2.7 V	0.3	1.1	0.3	1.1	V
		V_{CC} = 3.0 V	0.3	1.2	0.3	1.2	V
		V_{CC} = 3.6 V	0.3	1.2	0.3	1.2	V

14. Waveforms transfer characteristics

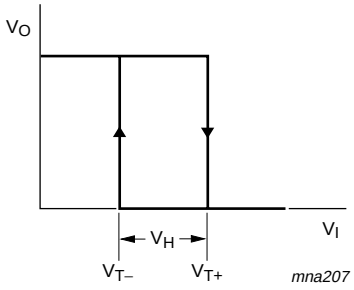


Fig 8. Transfer characteristic

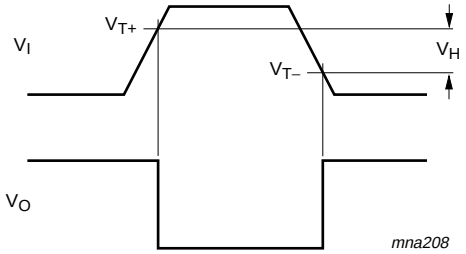


Fig 9. Definition of V_{T+}, V_{T-} and V_H

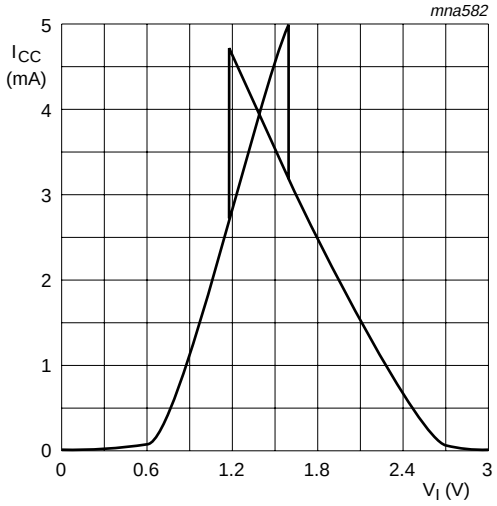
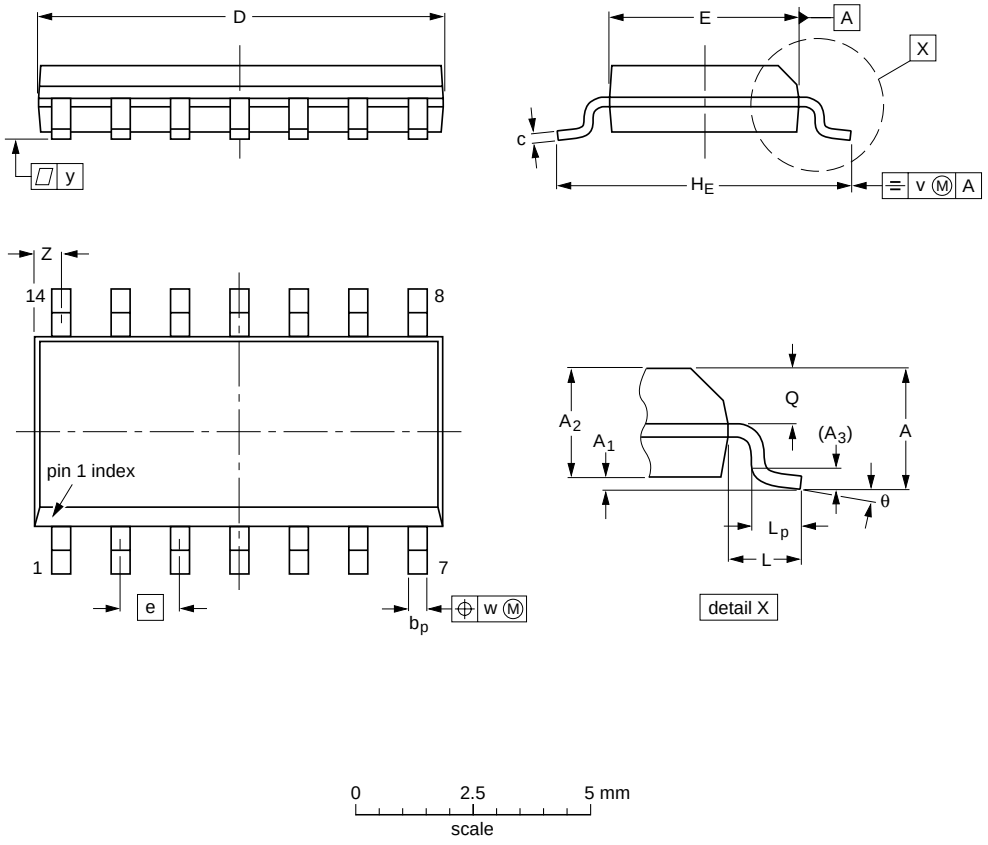


Fig 10. Typical transfer characteristic; V_{CC} = 3.3 V

15. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

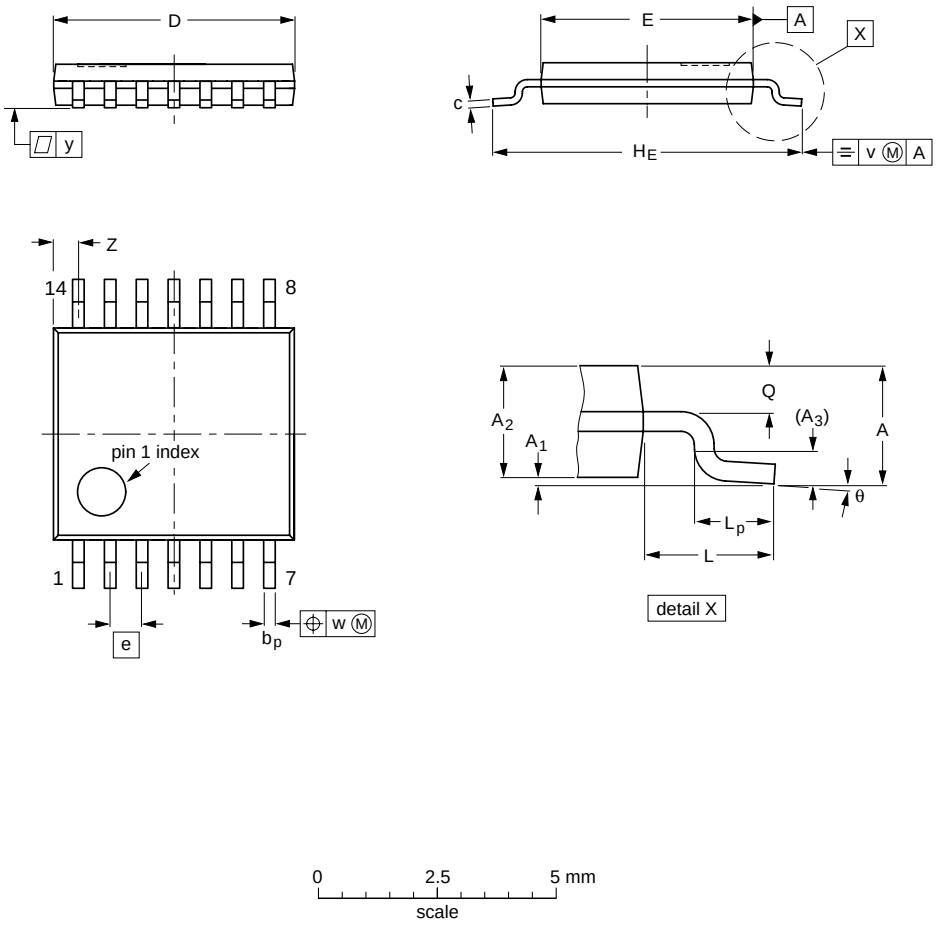
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

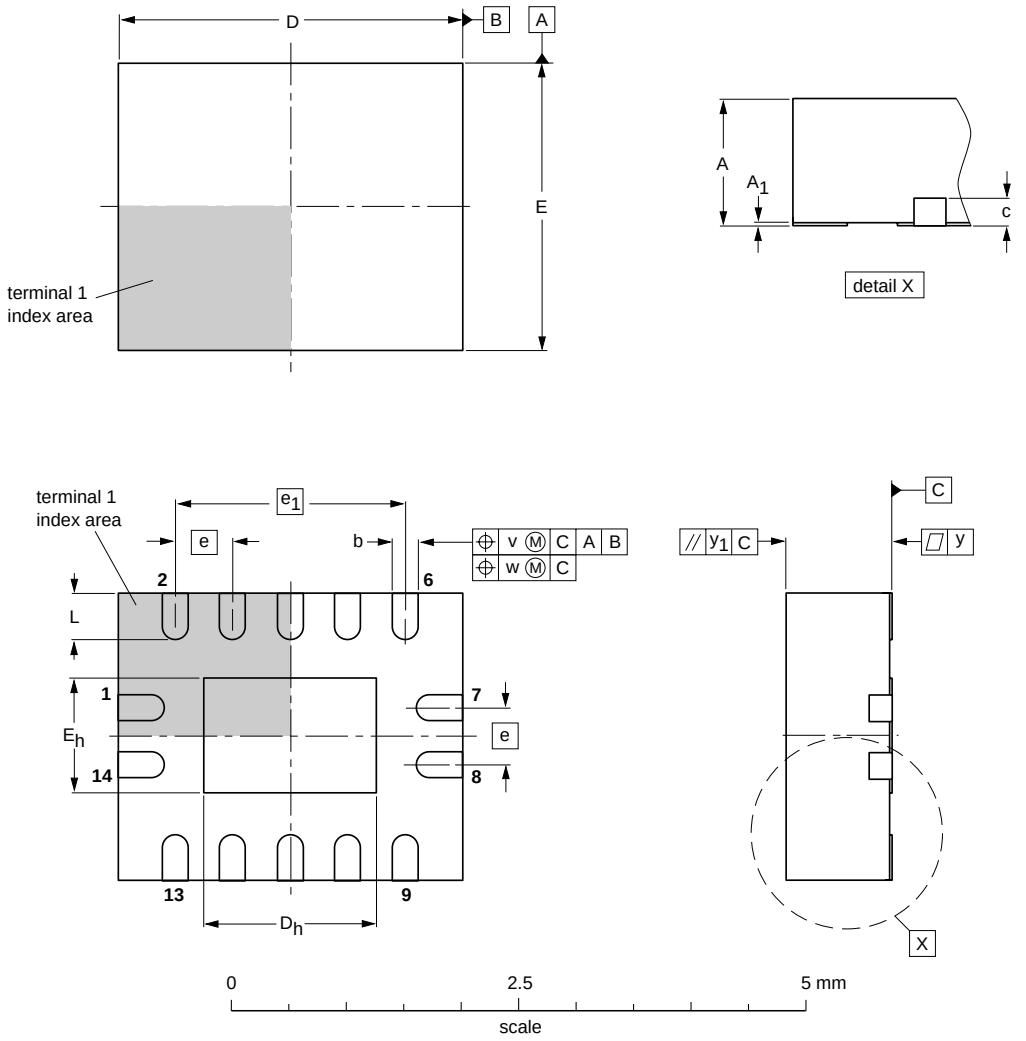
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT762-1 (DHVQFN14)

16. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

17. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC132A_1	20061215	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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