74AUP1G885

Low-power dual function gate

Rev. 01.00 — 26 January 2006 Preliminary data sheet

1. General description

The 74AUP1G885 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Schmitt-trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial Power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74AUP1G885 provides two functions in one device.The output state of the outputs (1Y, 2Y) is determined by the inputs (A, B and C). The output 1Y provides the boolean funtion: $1Y = A \times C$. The output 2Y provides the boolean funtion: $2Y = \overline{A} \times B + A \times \overline{C}$

2. Features

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114-C Class 3A exceeds 4000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101-C exceeds 1000 V
- Low static power consumption; $I_{CC} = 0.9\ \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

PHILIPS

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 0.8 V		-	17.3	-	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 1.1 V to 1.3 V		1.1	5.2	9.7	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 1.4 V to 1.6 V		1.2	3.7	5.9	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 1.65 V to 1.95 V		1.1	3.0	4.8	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 2.3 V to 2.7 V		1.1	2.4	3.6	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 3.0 V to 3.6 V		1.1	2.1	3.1	ns
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 0.8 V		-	21.5	-	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 1.1 V to 1.3 V		1.7	6.0	12.7	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 1.4 V to 1.6 V		1.7	4.2	7.2	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 1.65 V to 1.95 V		1.4	3.3	5.8	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 2.3 V to 2.7 V		1.2	2.6	4.1	ns
		C_L = 5 pF; R_L = 1 MΩ; V_{CC} = 3.0 V to 3.6 V		1.1	2.3	3.5	ns
C_I	input capacitance			-	0.8	-	pF
C_{PD}	power dissipation capacitance	V_{CC} = 1.8 V; f = 1 MHz	[1] [2]	-	3.1	-	pF
		V_{CC} = 3.3 V; f = 1 MHz	[1] [2]	-	4.1	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1G885DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP1G885GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1

5. Marking

Table 3: Marking

Type number	Marking code
74AUP1G885DC	pS8
74AUP1G885GT	pS8

6. Functional diagram

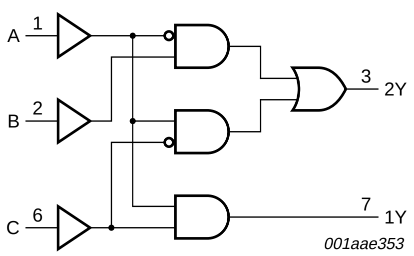


Fig 1. Logic diagram

7. Pinning information

7.1 Pinning

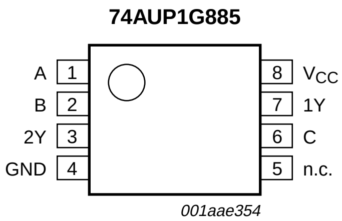


Fig 2. Pin configuration SOT765-1 (VSSOP8)

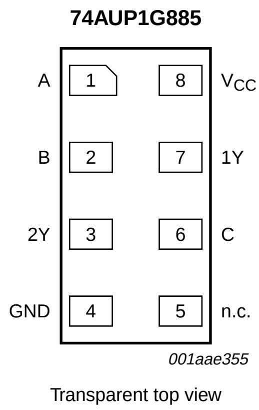


Fig 3. Pin configuration SOT833-1 (XSON8)

7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
A	1	data input A
B	2	data input B
2Y	3	data output 2Y
GND	4	ground (0 V)
n.c.	5	not connected
C	6	data input C
1Y	7	data output 1Y
V_{CC}	8	supply voltage

8. Functional description

8.1 Function table

Table 5: Function table [1]

Input			Output	
A	**B**	**C**	**1Y**	**2Y**
L	L	L	L	L
H	L	L	L	H
L	H	L	L	H
H	H	L	L	H
L	L	H	L	L
H	L	H	H	L
L	H	H	L	H
H	H	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		-	–50	mA
V_O	output voltage	active mode	[1]	–0.5	V_{CC} + 0.5	V
		Power-down mode	[1]	–0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}		-	±20	mA
I_{CC}	quiescent supply current			-	+50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	300	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

10. Recommended operating conditions

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature		−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 0.8 V to 3.6 V	0	200	ns/V

11. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 0.8 V	0.70 × V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 0.8 V	-	-	0.30 × V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 μA; V_{CC} = 0.8 V to 3.6 V	V_{CC} − 0.1	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.75 × V_{CC}	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.11	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.32	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V

Table 8: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I_{CC}	quiescent supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	40	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}	-	0.8	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V	-	1.7	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 0.8 V	0.70 × V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 0.8 V	-	-	0.30 × V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA; V_{CC} = 0.8 V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.7 × V_{CC}	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.03	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.30	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V

Table 8: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 20\ \mu A$; $V_{CC} = 0.8\ V$ to $3.6\ V$		-	-	0.1	V
		$I_O = 1.1\ mA$; $V_{CC} = 1.1\ V$		-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7\ mA$; $V_{CC} = 1.4\ V$		-	-	0.37	V
		$I_O = 1.9\ mA$; $V_{CC} = 1.65\ V$		-	-	0.35	V
		$I_O = 2.3\ mA$; $V_{CC} = 2.3\ V$		-	-	0.33	V
		$I_O = 3.1\ mA$; $V_{CC} = 2.3\ V$		-	-	0.45	V
		$I_O = 2.7\ mA$; $V_{CC} = 3.0\ V$		-	-	0.33	V
		$I_O = 4.0\ mA$; $V_{CC} = 3.0\ V$		-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; $V_{CC} = 0\ V$ to $3.6\ V$		-	-	±0.5	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 0\ V$ to $3.6\ V$; $V_{CC} = 0\ V$		-	-	±0.5	μA
ΔI_{OFF}	additional power-off leakage current	V_I or $V_O = 0\ V$ to $3.6\ V$; $V_{CC} = 0\ V$ to $0.2\ V$		-	-	±0.6	μA
I_{CC}	quiescent supply current	V_I = GND or V_{CC}; $I_O = 0\ A$; $V_{CC} = 0.8\ V$ to $3.6\ V$		-	-	0.9	μA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC} - 0.6\ V$; $I_O = 0\ A$; $V_{CC} = 3.3\ V$	[1]	-	-	50	μA
$T_{amb} = -40\ °C$ to $+125\ °C$							
V_{IH}	HIGH-state input voltage	$V_{CC} = 0.8\ V$		$0.75 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9\ V$ to $1.95\ V$		$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\ V$ to $2.7\ V$		1.6	-	-	V
		$V_{CC} = 3.0\ V$ to $3.6\ V$		2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 0.8\ V$		-	-	$0.25 \times V_{CC}$	V
		$V_{CC} = 0.9\ V$ to $1.95\ V$		-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 2.3\ V$ to $2.7\ V$		-	-	0.7	V
		$V_{CC} = 3.0\ V$ to $3.6\ V$		-	-	0.9	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = -20\ \mu A$; $V_{CC} = 0.8\ V$ to $3.6\ V$		$V_{CC} - 0.11$	-	-	V
		$I_O = -1.1\ mA$; $V_{CC} = 1.1\ V$		$0.6 \times V_{CC}$	-	-	V
		$I_O = -1.7\ mA$; $V_{CC} = 1.4\ V$		0.93	-	-	V
		$I_O = -1.9\ mA$; $V_{CC} = 1.65\ V$		1.17	-	-	V
		$I_O = -2.3\ mA$; $V_{CC} = 2.3\ V$		1.77	-	-	V
		$I_O = -3.1\ mA$; $V_{CC} = 2.3\ V$		1.67	-	-	V
		$I_O = -2.7\ mA$; $V_{CC} = 3.0\ V$		2.40	-	-	V
		$I_O = -4.0\ mA$; $V_{CC} = 3.0\ V$		2.30	-	-	V

Table 8: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 20\ \mu A$; $V_{CC} = 0.8$ V to 3.6 V		-	-	0.11	V
		$I_O = 1.1$ mA; $V_{CC} = 1.1$ V		-	-	$0.33 \times V_{CC}$	V
		$I_O = 1.7$ mA; $V_{CC} = 1.4$ V		-	-	0.41	V
		$I_O = 1.9$ mA; $V_{CC} = 1.65$ V		-	-	0.39	V
		$I_O = 2.3$ mA; $V_{CC} = 2.3$ V		-	-	0.36	V
		$I_O = 3.1$ mA; $V_{CC} = 2.3$ V		-	-	0.50	V
		$I_O = 2.7$ mA; $V_{CC} = 3.0$ V		-	-	0.36	V
		$I_O = 4.0$ mA; $V_{CC} = 3.0$ V		-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; $V_{CC} = 0$ V to 3.6 V		-	-	±0.75	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V		-	-	±0.75	μA
ΔI_{OFF}	additional power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V		-	-	±0.75	μA
I_{CC}	quiescent supply current	V_I = GND or V_{CC}; $I_O = 0$ A; $V_{CC} = 0.8$ V to 3.6 V		-	-	1.4	μA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 3.3$ V	[1]	-	-	75	μA

[1] One input at $V_{CC} - 0.6$ V, other input at V_{CC} or GND.

12. Dynamic characteristics

Table 9: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 5

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$T_{amb} = 25$ °C; $C_L = 5$ pF						
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	see Figure 4				
		$V_{CC} = 0.8$ V	-	17.3	-	ns
		$V_{CC} = 1.1$ V to 1.3 V	1.1	5.2	9.7	ns
		$V_{CC} = 1.4$ V to 1.6 V	1.2	3.7	5.9	ns
		$V_{CC} = 1.65$ V to 1.95 V	1.1	3.0	4.8	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.1	2.4	3.6	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.1	2.1	3.1	ns
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	see Figure 4				
		$V_{CC} = 0.8$ V	-	21.5	-	ns
		$V_{CC} = 1.1$ V to 1.3 V	1.7	6.0	12.7	ns
		$V_{CC} = 1.4$ V to 1.6 V	1.7	4.2	7.2	ns
		$V_{CC} = 1.65$ V to 1.95 V	1.4	3.3	5.8	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.2	2.6	4.1	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.1	2.3	3.5	ns

Table 9: Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 5

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = 25 °C; C_L = 10 pF						
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	see Figure 4				
		V_{CC} = 0.8 V	-	20.8	-	ns
		V_{CC} = 1.1 V to 1.3 V	1.2	6.1	11.4	ns
		V_{CC} = 1.4 V to 1.6 V	1.4	4.3	7.2	ns
		V_{CC} = 1.65 V to 1.95 V	1.4	3.6	5.7	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	2.9	4.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.4	2.7	3.9	ns
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	see Figure 4				
		V_{CC} = 0.8 V	-	25.0	-	ns
		V_{CC} = 1.1 V to 1.3 V	1.8	6.9	14.4	ns
		V_{CC} = 1.4 V to 1.6 V	1.9	4.8	8.5	ns
		V_{CC} = 1.65 V to 1.95 V	1.9	3.9	6.6	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.1	4.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.4	2.8	4.3	ns
T_{amb} = 25 °C; C_L = 15 pF						
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	see Figure 4				
		V_{CC} = 0.8 V	-	24.3	-	ns
		V_{CC} = 1.1 V to 1.3 V	1.3	6.9	13.0	ns
		V_{CC} = 1.4 V to 1.6 V	1.7	4.9	8.0	ns
		V_{CC} = 1.65 V to 1.95 V	1.5	4.1	6.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	3.4	5.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.7	3.1	4.4	ns
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	see Figure 4				
		V_{CC} = 0.8 V	-	28.5	-	ns
		V_{CC} = 1.1 V to 1.3 V	2.1	7.7	16.0	ns
		V_{CC} = 1.4 V to 1.6 V	2.2	5.4	9.4	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	4.4	7.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.8	3.6	5.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.7	3.3	4.8	ns
T_{amb} = 25 °C; C_L = 30 pF						
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	see Figure 4				
		V_{CC} = 0.8 V	-	34.7	-	ns
		V_{CC} = 1.1 V to 1.3 V	2.4	9.2	17.7	ns
		V_{CC} = 1.4 V to 1.6 V	2.5	6.5	10.6	ns
		V_{CC} = 1.65 V to 1.95 V	2.5	5.4	8.5	ns
		V_{CC} = 2.3 V to 2.7 V	2.6	4.5	6.4	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	4.2	5.7	ns

Table 9: Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 5

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	see Figure 4					
		V_{CC} = 0.8 V		-	38.9	-	ns
		V_{CC} = 1.1 V to 1.3 V		2.6	10.0	20.5	ns
		V_{CC} = 1.4 V to 1.6 V		2.6	6.9	11.9	ns
		V_{CC} = 1.65 V to 1.95 V		2.7	5.7	9.5	ns
		V_{CC} = 2.3 V to 2.7 V		2.5	4.7	6.9	ns
		V_{CC} = 3.0 V to 3.6 V		2.4	4.4	6.1	ns
T_{amb} = 25 °C							
C_{PD}	power dissipation capacitance	f = 1 MHz	[2] [3]				
		V_{CC} = 0.8 V		-	2.7	-	pF
		V_{CC} = 1.1 V to 1.3 V		-	2.9	-	pF
		V_{CC} = 1.4 V to 1.6 V		-	3.0	-	pF
		V_{CC} = 1.65 V to 1.95 V		-	3.1	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	3.5	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	4.1	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[3] The condition is V_I = GND to V_{CC}.

Table 10: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 5

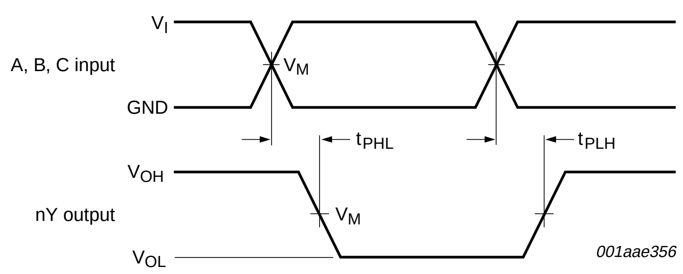
Symbol	Parameter	Conditions	−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Max	Min	Max	
C_L = 5 pF							
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	see Figure 4					
		V_{CC} = 1.1 V to 1.3 V	0.9	12.8	0.9	14.2	ns
		V_{CC} = 1.4 V to 1.6 V	1.0	7.8	1.0	8.6	ns
		V_{CC} = 1.65 V to 1.95 V	0.9	6.2	0.9	6.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	4.1	1.0	4.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.6	1.0	4.1	ns
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	see Figure 4					
		V_{CC} = 1.1 V to 1.3 V	1.4	12.8	1.4	14.2	ns
		V_{CC} = 1.4 V to 1.6 V	1.4	7.8	1.4	8.7	ns
		V_{CC} = 1.65 V to 1.95 V	1.2	6.5	1.2	7.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	4.7	1.0	5.2	ns
		V_{CC} = 3.0 V to 3.6 V	0.9	3.8	0.9	4.2	ns
C_L = 10 pF							
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	see Figure 4					
		V_{CC} = 1.1 V to 1.3 V	1.2	14.6	1.2	16.1	ns
		V_{CC} = 1.4 V to 1.6 V	1.2	8.7	1.2	9.6	ns
		V_{CC} = 1.65 V to 1.95 V	1.3	6.8	1.3	7.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.2	4.8	1.2	5.4	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	4.1	1.3	4.6	ns
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	see Figure 4					
		V_{CC} = 1.1 V to 1.3 V	1.7	14.6	1.7	16.1	ns
		V_{CC} = 1.4 V to 1.6 V	1.5	9.1	1.5	10.1	ns
		V_{CC} = 1.65 V to 1.95 V	1.7	7.2	1.7	8.0	ns
		V_{CC} = 2.3 V to 2.7 V	1.3	5.4	1.3	5.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	4.6	1.3	5.1	ns
C_L = 15 pF							
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	see Figure 4					
		V_{CC} = 1.1 V to 1.3 V	1.2	16.2	1.2	17.9	ns
		V_{CC} = 1.4 V to 1.6 V	1.4	9.7	1.4	10.8	ns
		V_{CC} = 1.65 V to 1.95 V	1.4	7.6	1.4	8.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.6	5.4	1.6	6.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.6	4.7	1.6	5.3	ns
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	see Figure 4					
		V_{CC} = 1.1 V to 1.3 V	1.9	16.3	1.9	18.0	ns
		V_{CC} = 1.4 V to 1.6 V	2.4	10.3	2.4	11.4	ns
		V_{CC} = 1.65 V to 1.95 V	1.8	8.2	1.8	9.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.6	6.0	1.6	6.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	5.2	1.5	5.8	ns

Table 10: Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 5

Symbol	Parameter	Conditions	−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Max	Min	Max	
C_L = 30 pF							
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, C to 1Y	see Figure 4					
		V_{CC} = 1.1 V to 1.3 V	2.3	20.9	2.3	23.0	ns
		V_{CC} = 1.4 V to 1.6 V	2.5	12.2	2.5	13.5	ns
		V_{CC} = 1.65 V to 1.95 V	2.4	9.4	2.4	10.4	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	7.0	2.4	7.7	ns
		V_{CC} = 3.0 V to 3.6 V	2.3	6.6	2.3	7.3	ns
t_{PHL}, t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A, B to 2Y	see Figure 4					
		V_{CC} = 1.1 V to 1.3 V	2.6	21.5	2.6	23.7	ns
		V_{CC} = 1.4 V to 1.6 V	2.6	13.2	2.6	14.5	ns
		V_{CC} = 1.65 V to 1.95 V	2.7	10.5	2.7	11.6	ns
		V_{CC} = 2.3 V to 2.7 V	2.5	7.6	2.5	8.4	ns
		V_{CC} = 3.0 V to 3.6 V	2.4	7.1	2.4	7.9	ns

13. Waveforms



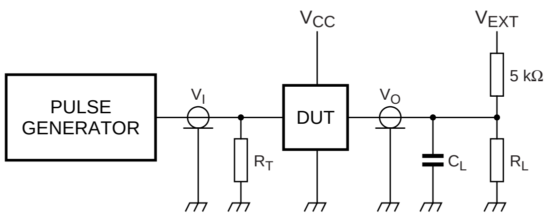
Measurement points are given in Table 11.

Logic levels: V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 4. The data input (A, B, C) to output (nY) propagation delays

Table 11: Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{CC}	≤ 3.0 ns



Test data is given in Table 12.

Definitions for test circuit:

R_L = Load resistance

C_L = Load capacitance including jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator

V_{EXT} = External voltage for measuring switching times.

Fig 5. Load circuitry for switching times

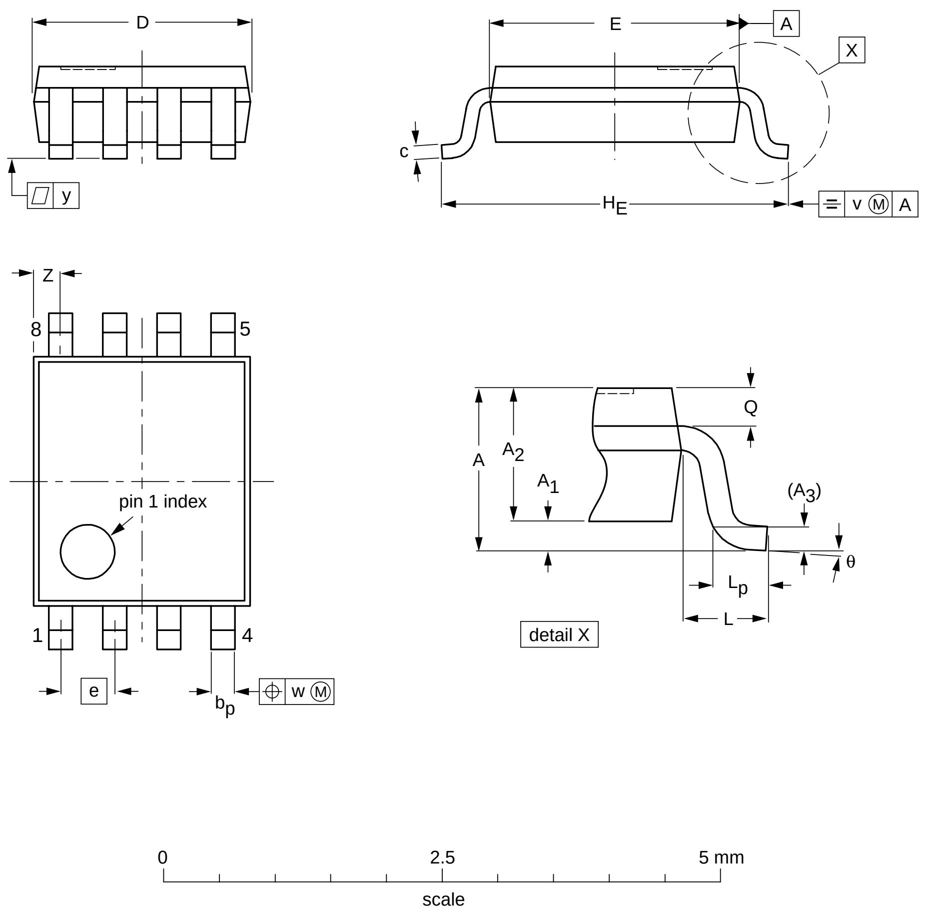
Table 12: Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2 × V_{CC}

[1] For measuring enable and disable times R_L = 5 kΩ, for measuring propagation delays, setup and hold times and pulse width R_L = 1 MΩ.

14. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

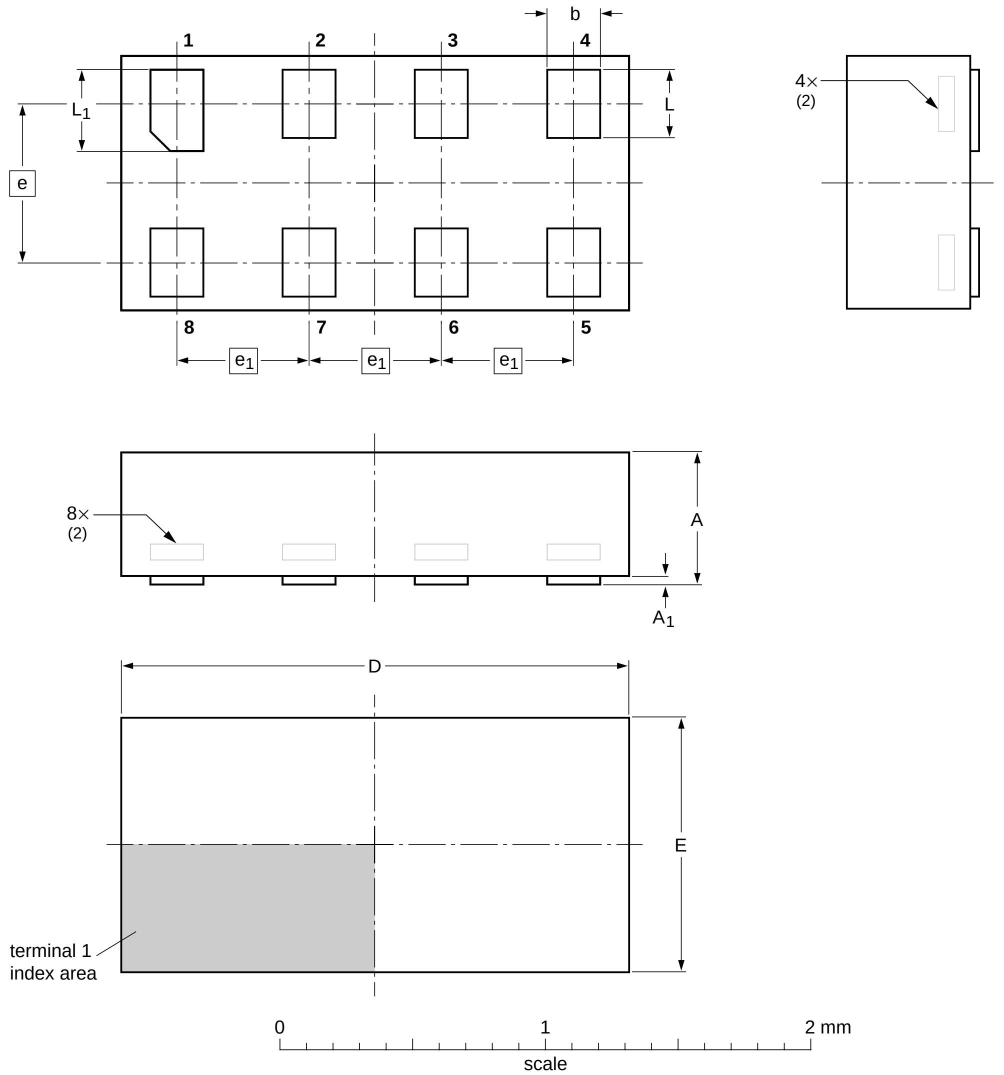
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 6. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~04-07-22~~ 04-11-09

Fig 7. Package outline SOT833-1 (XSON8)

15. Abbreviations

Table 13: Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor Transistor Logic

16. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74AUP1G885_1	<tbd>	Preliminary data sheet	-	-	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

Date of release: 26 January 2006

Document number: 74AUP1G885_1

Published in The Netherlands