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SSD1818

Advance Information

CMOS

LCD Segment / Common Driver with Controller

SSD1818 is a single-chip CMOS LCD driver with controllers for dot-matrix graphic liquid crystal display system. It consists of 169 high-voltage driving outputs for driving maximum 104 Segments, 64 Commons and 1 icon line.

SSD1818 consists of 104 x 65 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through 8-bit Parallel or 4-wire Serial Interface. 6800-series, 8080-series compatible Parallel Interface and Serial Peripheral Interface can be selected by hardware configuration.

SSD1818 embeds DC-DC Converter with booster capacitors, On-Chip Oscillator and Bias Divider with integrated stabilizing capacitors so as to reduce the number of external components. With the advanced design for low power consumption, stable LCD operating voltage and flexible die layout, SSD1818 is suitable for any portable battery-driven applications requiring long operation period with compact size.

FEATURES

104 x 64 + 1 Icon Line
Single Supply Operation, 2.4 V - 3.5V
Minimum -12.0V LCD Driving Output Voltage
Low Current Sleep Mode
On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
2X / 3X / 4X/ 5X On-Chip DC-DC Converter
On-Chip Oscillator
On-Chip Bias Divider with integrated stabilizing capacitors
Programmable bias ratio [1/4-1/9]
8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface and Serial Peripheral Interface
On-Chip 104 X 65 Graphic Display Data RAM
Row Re-mapping and Column Re-mapping
Vertical Scrolling
Display Offset Control
64 Level Internal Contrast Control
Programmable LCD Driving Voltage Temperature Coefficients
Programmable MUX ratio [2-64 MUX] (Partial display mode)
Available in Gold Bump Die

ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Default Bias	Package Form	Reference
SSD1818Z	104	64 + 1	1/9, 1/7	Gold Bump Die	

BLOCK DIAGRAM

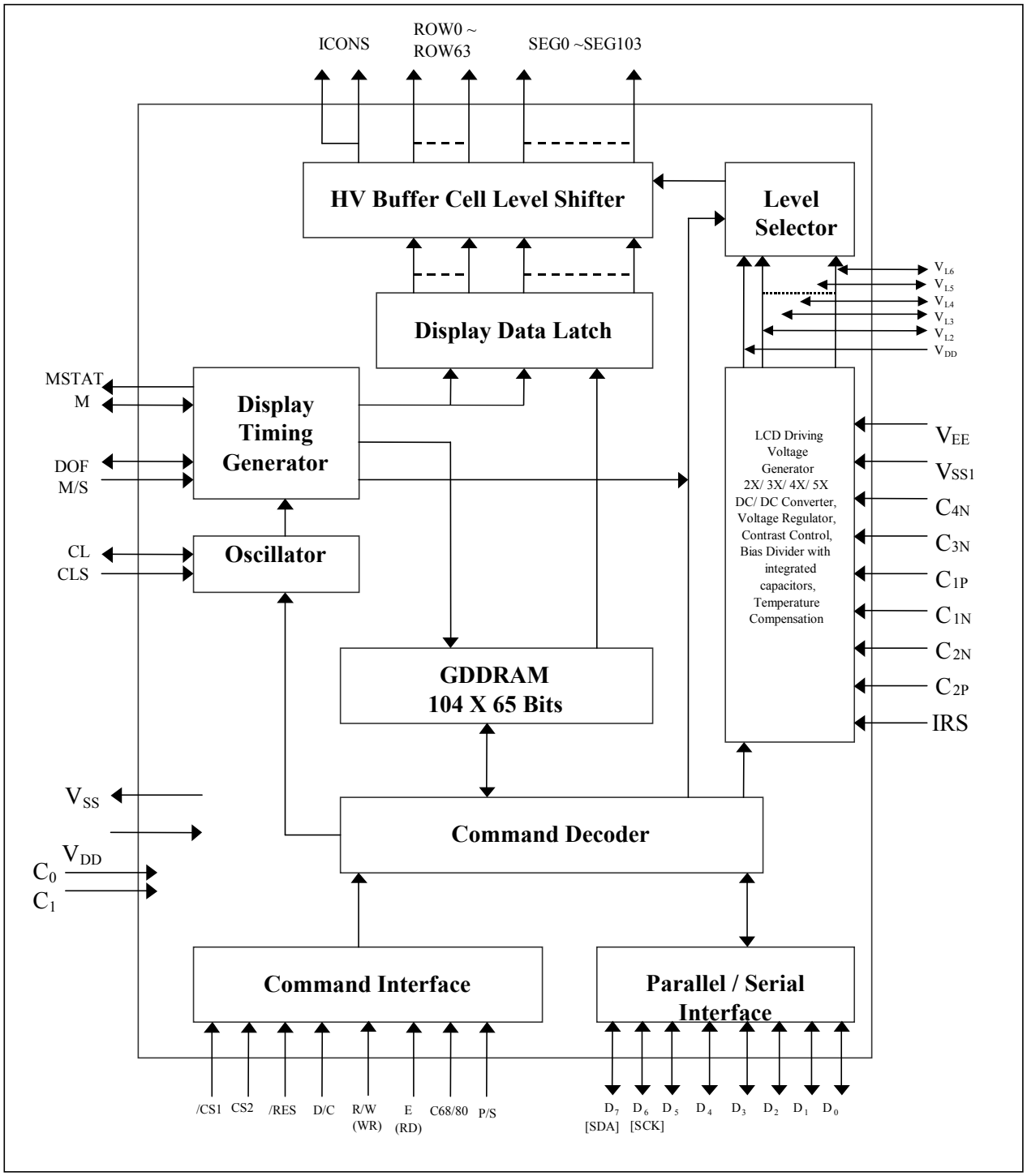
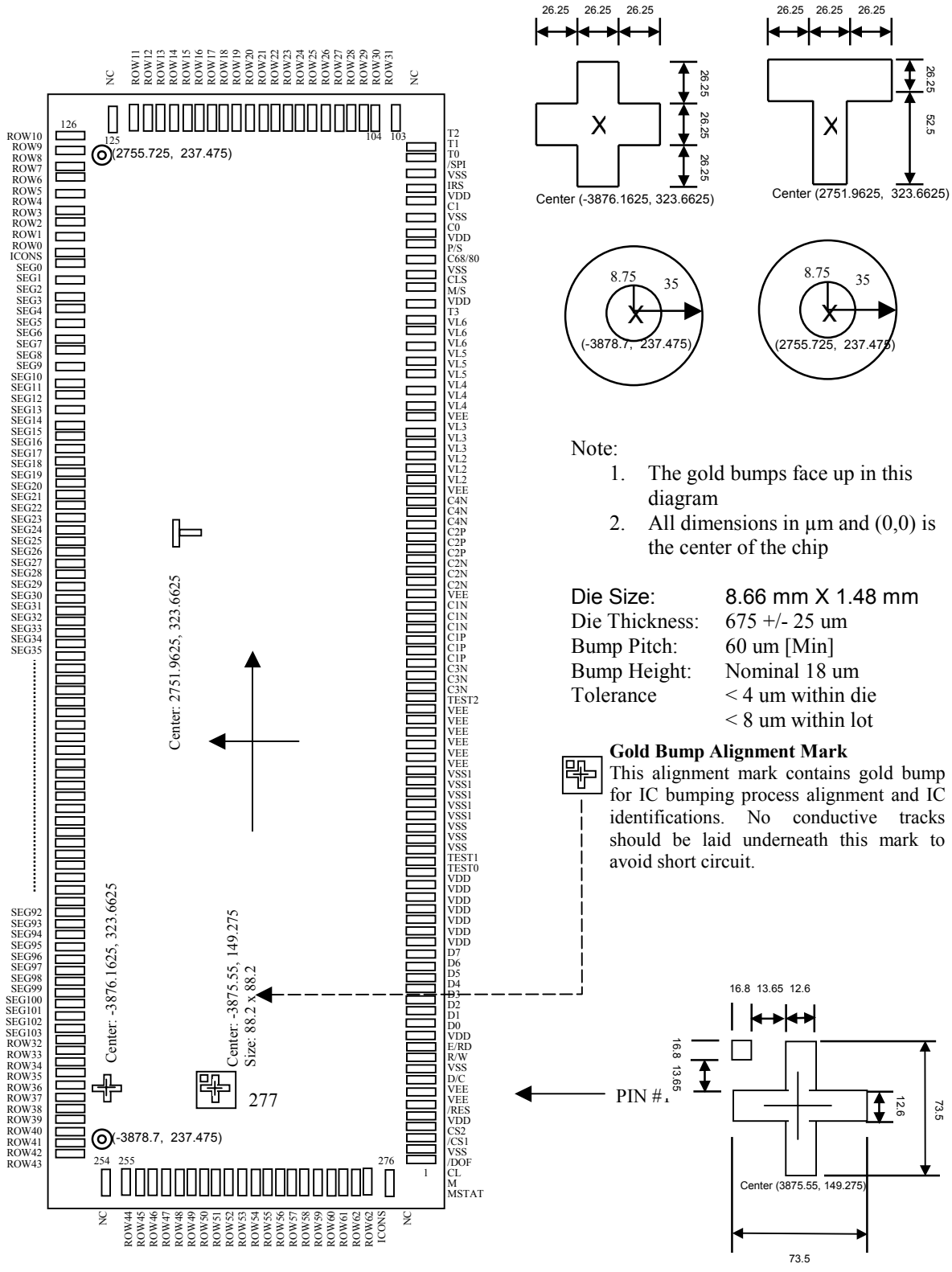


Figure 1 - Block Diagram

DIE PAD ARRANGEMENT



Note:

1. The gold bumps face up in this diagram
2. All dimensions in μm and (0,0) is the center of the chip

Die Size:	8.66 mm X 1.48 mm
Die Thickness:	675 +/- 25 um
Bump Pitch:	60 um [Min]
Bump Height:	Nominal 18 um
Tolerance	< 4 um within die
	< 8 um within lot

Gold Bump Alignment Mark
This alignment mark contains gold bump for IC bumping process alignment and IC identifications. No conductive tracks should be laid underneath this mark to avoid short circuit.

Figure 2 – SSD1818 Pin Assignment

Table 2 - SSD1818 Series Bump Die Pad Coordinates (Bump center)

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	MSTAT	-3873.80	-581.35	51	C3N	-27.48	-581.35	101	T1	3799.95	-581.35
2	M	-3797.50	-581.35	52	C1P	48.83	-581.35	102	T2	3876.25	-581.35
3	CL	-3721.20	-581.35	53	C1P	125.13	-581.35	103	NC	4178.48	-655.03
4	$\overline{DOF}$	-3644.90	-581.35	54	C1P	201.43	-581.35	104	ROW31	4178.48	-594.83
5	VSS	-3568.60	-581.35	55	C1N	277.73	-581.35	105	ROW30	4178.48	-534.63
6	$\overline{CS}$	-3492.30	-581.35	56	C1N	354.03	-581.35	106	ROW29	4178.48	-474.43
7	CS2	-3416.00	-581.35	57	C1N	430.33	-581.35	107	ROW28	4178.48	-414.23
8	VDD	-3339.70	-581.35	58	VEE	506.63	-581.35	108	ROW27	4178.48	-354.03
9	$\overline{RES}$	-3263.40	-581.35	59	C2N	582.93	-581.35	109	ROW26	4178.48	-293.83
10	VEE	-3178.35	-581.35	60	C2N	659.23	-581.35	110	ROW25	4178.48	-233.63
11	VEE	-3102.05	-581.35	61	C2N	735.53	-581.35	111	ROW24	4178.48	-173.43
12	D/ $\overline{C}$	-3017.00	-581.35	62	C2P	811.83	-581.35	112	ROW23	4178.48	-113.23
13	VSS	-2940.70	-581.35	63	C2P	888.13	-581.35	113	ROW22	4178.48	-53.03
14	R/ $\overline{W}$	-2864.40	-581.35	64	C2P	964.43	-581.35	114	ROW21	4178.48	7.18
15	E/ $\overline{RD}$	-2788.10	-581.35	65	C4N	1040.73	-581.35	115	ROW20	4178.48	67.38
16	VDD	-2711.80	-581.35	66	C4N	1117.03	-581.35	116	ROW19	4178.48	127.58
17	D0	-2635.50	-581.35	67	C4N	1193.33	-581.35	117	ROW18	4178.48	187.78
18	D1	-2557.63	-581.35	68	VEE	1269.63	-581.35	118	ROW17	4178.48	247.98
19	D2	-2481.33	-581.35	69	VL2	1345.93	-581.35	119	ROW16	4178.48	308.18
20	D3	-2403.10	-581.35	70	VL2	1422.23	-581.35	120	ROW15	4178.48	368.38
21	D4	-2325.23	-581.35	71	VL2	1498.53	-581.35	121	ROW14	4178.48	428.58
22	D5	-2248.93	-581.35	72	VL3	1574.83	-581.35	122	ROW13	4178.48	488.78
23	D6	-2172.63	-581.35	73	VL3	1651.13	-581.35	123	ROW12	4178.48	548.98
24	D7	-2096.33	-581.35	74	VL3	1727.43	-581.35	124	ROW11	4178.48	609.18
25	VDD	-2020.03	-581.35	75	VEE	1803.73	-581.35	125	NC	4178.48	663.25
26	VDD	-1943.73	-581.35	76	VL4	1880.03	-581.35	126	ROW10	3834.60	587.83
27	VDD	-1867.43	-581.35	77	VL4	1956.33	-581.35	127	ROW9	3774.40	587.83
28	VDD	-1791.13	-581.35	78	VL4	2032.63	-581.35	128	ROW8	3714.20	587.83
29	VDD	-1714.83	-581.35	79	VL5	2108.93	-581.35	129	ROW7	3654.00	587.83
30	VDD	-1638.53	-581.35	80	VL5	2185.23	-581.35	130	ROW6	3593.80	587.83
31	VDD	-1562.23	-581.35	81	VL5	2261.53	-581.35	131	ROW5	3533.60	587.83
32	TEST0	-1485.93	-581.35	82	VL6	2337.83	-581.35	132	ROW4	3473.40	587.83
33	TEST1	-1409.63	-581.35	83	VL6	2414.13	-581.35	133	ROW3	3413.20	587.83
34	VSS	-1333.33	-581.35	84	VL6	2490.60	-581.35	134	ROW2	3353.00	587.83
35	VSS	-1257.03	-581.35	85	T3	2566.73	-581.35	135	ROW1	3292.80	587.83
36	VSS	-1180.73	-581.35	86	VDD	2651.78	-581.35	136	ROW0	3232.60	587.83
37	VSS1	-1095.68	-581.35	87	M/ $\overline{S}$	2728.08	-581.35	137	ICONS	3172.40	587.83
38	VSS1	-1019.38	-581.35	88	CLS	2804.38	-581.35	138	SEG0	3112.20	587.83
39	VSS1	-943.08	-581.35	89	VSS	2880.68	-581.35	139	SEG1	3052.00	587.83
40	VSS1	-866.78	-581.35	90	C68/ $\overline{80}$	2956.98	-581.35	140	SEG2	2991.80	587.83
41	VSS1	-790.48	-581.35	91	P/ $\overline{S}$	3033.28	-581.35	141	SEG3	2931.60	587.83
42	VEE	-714.18	-581.35	92	VDD	3109.58	-581.35	142	SEG4	2871.40	587.83
43	VEE	-637.88	-581.35	93	C0	3185.88	-581.35	143	SEG5	2811.20	587.83
44	VEE	-561.58	-581.35	94	VSS	3262.18	-581.35	144	SEG6	2751.00	587.83
45	VEE	-485.28	-581.35	95	C1	3338.48	-581.35	145	SEG7	2690.80	587.83
46	VEE	-408.98	-581.35	96	VDD	3414.78	-581.35	146	SEG8	2630.60	587.83
47	VEE	-332.68	-581.35	97	IRS	3491.08	-581.35	147	SEG9	2570.40	587.83
48	TEST2	-256.38	-581.35	98	VSS	3567.38	-581.35	148	SEG10	2510.20	587.83
49	C3N	-180.08	-581.35	99	$\overline{SPI}$	3643.68	-581.35	149	SEG11	2450.00	587.83
50	C3N	-103.78	-581.35	100	T0	3723.65	-581.35	150	SEG12	2389.80	587.83

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
151	SEG13	2329.60	587.83	201	SEG63	-680.40	587.83	251	ROW41	-3690.40	587.83
152	SEG14	2269.40	587.83	202	SEG64	-740.60	587.83	252	ROW42	-3750.60	587.83
153	SEG15	2209.20	587.83	203	SEG65	-800.80	587.83	253	ROW43	-3810.80	587.83
154	SEG16	2149.00	587.83	204	SEG66	-861.00	587.83	254	NC	-4178.48	663.25
155	SEG17	2088.80	587.83	205	SEG67	-921.20	587.83	255	ROW44	-4178.48	609.18
156	SEG18	2028.60	587.83	206	SEG68	-981.40	587.83	256	ROW45	-4178.48	548.98
157	SEG19	1968.40	587.83	207	SEG69	-1041.60	587.83	257	ROW46	-4178.48	488.78
158	SEG20	1908.20	587.83	208	SEG70	-1101.80	587.83	258	ROW47	-4178.48	428.58
159	SEG21	1848.00	587.83	209	SEG71	-1162.00	587.83	259	ROW48	-4178.48	368.38
160	SEG22	1787.80	587.83	210	SEG72	-1222.20	587.83	260	ROW49	-4178.48	308.18
161	SEG23	1727.60	587.83	211	SEG73	-1282.40	587.83	261	ROW50	-4178.48	247.98
162	SEG24	1667.40	587.83	212	SEG74	-1342.60	587.83	262	ROW51	-4178.48	187.78
163	SEG25	1607.20	587.83	213	SEG75	-1402.80	587.83	263	ROW52	-4178.48	127.58
164	SEG26	1547.00	587.83	214	SEG76	-1463.00	587.83	264	ROW53	-4178.48	67.38
165	SEG27	1486.80	587.83	215	SEG77	-1523.20	587.83	265	ROW54	-4178.48	7.18
166	SEG28	1426.60	587.83	216	SEG78	-1583.40	587.83	266	ROW55	-4178.48	-53.03
167	SEG29	1366.40	587.83	217	SEG79	-1643.60	587.83	267	ROW56	-4178.48	-113.23
168	SEG30	1306.20	587.83	218	SEG80	-1703.80	587.83	268	ROW57	-4178.48	-173.43
169	SEG31	1246.00	587.83	219	SEG81	-1764.00	587.83	269	ROW58	-4178.48	-233.63
170	SEG32	1185.80	587.83	220	SEG82	-1824.20	587.83	270	ROW59	-4178.48	-293.83
171	SEG33	1125.60	587.83	221	SEG83	-1884.40	587.83	271	ROW60	-4178.48	-354.03
172	SEG34	1065.40	587.83	222	SEG84	-1944.60	587.83	272	ROW61	-4178.48	-414.23
173	SEG35	1005.20	587.83	223	SEG85	-2004.80	587.83	273	ROW62	-4178.48	-474.43
174	SEG36	945.00	587.83	224	SEG86	-2065.00	587.83	274	ROW63	-4178.48	-534.63
175	SEG37	884.80	587.83	225	SEG87	-2125.20	587.83	275	ICONS	-4178.48	-594.83
176	SEG38	824.60	587.83	226	SEG88	-2185.40	587.83	276	NC	-4178.48	-655.03
177	SEG39	764.40	587.83	227	SEG89	-2245.60	587.83	277	NC	-3875.55	149.28
179	SEG41	644.00	587.83	229	SEG91	-2366.00	587.83				
180	SEG42	583.80	587.83	230	SEG92	-2426.20	587.83				
181	SEG43	523.60	587.83	231	SEG93	-2486.40	587.83				
182	SEG44	463.40	587.83	232	SEG94	-2546.60	587.83				
183	SEG45	403.20	587.83	233	SEG95	-2606.80	587.83				
184	SEG46	343.00	587.83	234	SEG96	-2667.00	587.83				
185	SEG47	282.80	587.83	235	SEG97	-2727.20	587.83				
186	SEG48	222.60	587.83	236	SEG98	-2787.40	587.83				
187	SEG49	162.40	587.83	237	SEG99	-2847.60	587.83				
188	SEG50	102.20	587.83	238	SEG100	-2907.80	587.83				
189	SEG51	42.00	587.83	239	SEG101	-2968.00	587.83				
190	SEG52	-18.20	587.83	240	SEG102	-3028.20	587.83				
191	SEG53	-78.40	587.83	241	SEG103	-3088.40	587.83				
192	SEG54	-138.60	587.83	242	ROW32	-3148.60	587.83				
193	SEG55	-198.80	587.83	243	ROW33	-3208.80	587.83				
194	SEG56	-259.00	587.83	244	ROW34	-3269.00	587.83				
195	SEG57	-319.20	587.83	245	ROW35	-3329.20	587.83				
196	SEG58	-379.40	587.83	246	ROW36	-3389.40	587.83				
197	SEG59	-439.60	587.83	247	ROW37	-3449.60	587.83				
198	SEG60	-499.80	587.83	248	ROW38	-3509.80	587.83				
199	SEG61	-560.00	587.83	249	ROW39	-3570.00	587.83				
200	SEG62	-620.20	587.83	250	ROW40	-3630.20	587.83				

Bump Size

PAD#	X [um]	Y [um]
1 – 102	50.05	50.05
103 – 124	66.675	40.95
125	66.675	28.7
126 – 253	40.95	66.675
254	66.675	28.7
255 – 276	66.675	40.95
277	88.2	88.2
1 – 102	50.05	50.05

PIN DESCRIPTION

MSTAT

This pin is the static indicator driving output. It is only active in master operation. The frame signal output pin, M, should be used as the back plane signal for the static indicator. The duration of overlapping can be programmable. This pin, MSTAT, becomes high impedance if the chip is operating in slave mode. Please see the Extended Command Table for reference.

M

This pin is the frame signal input/output. In master mode, the pin supplies frame signal to slave devices. In slave mode, the pin receives frame signal from the master device.

CL

This pin is the system clock input/output. When the internal oscillator is enabled (CLS pin pulled high), and the master mode is enabled (M/$\overline{S}$ pin pulled high), this pin supplies system clock signal to the slave device. When internal oscillator is disabled and the slave mode is enabled, the pin receives system clock signal from the master device or external clock source.

$\overline{DOF}$

This pin is the display blanking signal control pin. In master mode, this pin supplies “display on” or “display off” signal (blanking signal) to slave devices. In slave mode, this pin receives “display on” or “display off” signal from the master device.

$\overline{CS1}$, CS2

These pins are the chip select inputs. The chip is enabled for MCU communication only when $\overline{CS1}$ is pulled low and CS2 is pulled high.

$\overline{RES}$

This pin is the reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for completing the reset procedure is 1us.

D/$\overline{C}$

This pin is Data/Command control pin. When the pin is pulled high, the input at D_7-D_0 is treated as display data. When the pin is pulled low, the input at D_7-D_0 will be transferred to the command register. For detailed relationship with other MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/$\overline{W}$ ($\overline{WR}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as Read/Write (R/$\overline{W}$) selection input. Read mode will be carried out when this pin is pulled high and write mode when this pin is pulled low.

When 8080 interface mode is selected, this pin will be the Write ($\overline{WR}$) input. Data write operation is initiated when this pin is pulled low and the chip is selected.

E($\overline{RD}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/ write operation is initiated when this pin is pulled high and the chip is selected.

When 8080 interface mode is selected, this pin receives the Read ($\overline{RD}$) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.

D_7-D_0

These pins are the 8-bit bi-directional data bus in parallel interface mode. D_7 is the MSB while D_0 is the LSB. When serial mode is selected, D_7 is the serial data input (SDA) and D_6 is the serial clock input (SCK).

V_{DD}

These pins are the Chip's Power Supply pin. These pins are also act as the reference for the DC-DC Converter output and the LCD driving voltages.

V_{SS}

These pins are the grounding of the chip. They are also act as the reference for the logic pins.

V_{SS1}

These pins are the inputs for internal DC-DC converter. The voltage of generated, V_{EE}, equals to the multiple factors times the potential different between these pins, V_{SS1}, and V_{DD}. The multiple factors, 2X, 3X, 4X or 5X are selected by different connections of the external capacitors. All voltage levels are referenced to V_{DD}.

Note: the potential of Vss_1 at this input pin must lower than or equal to V_{SS}.

V_{EE}

This is the most negative voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter. The internal DC-DC converter is turned on when the internal voltage booster option is enabled. Please refer to the Set Power Control Register command for detail description.

When using internal DC-DC converter as voltage generator, voltage at this pin is used for internal referencing only. It CANNOT be used for driving external circuitry.

C_{1P}, C_{1N}, C_{2N}, C_{2P} C_{3N} and C_{4N}

When internal DC-DC voltage converter is used, external capacitor(s) is/are connected between these pins. Different connections result in different DC-DC converter multiple factors, for example, 2X, 3X, 4X or 5X. For detailed connections, please refer to the voltage converter section in the functional block description.

V_{L2}, V_{L3}, V_{L4} and V_{L5}

These pins are outputs with voltage levels equal to the LCD driving voltage. All these voltage levels are referenced to V_{DD}. The voltage levels can be supplied externally or generated by the internal bias divider. The bias divider is turned on when the output op-amp buffers are enabled. Please refer to the Set Power Control Register command for detail description.

The voltage potential relationship of these pins are given as:

$V_{DD} > V_{L2} > V_{L3} > V_{L4} > V_{L5} > V_{L6}$

In addition, assume the bias factor is known as a,

VL2 - VDD = 1/a * (VL6 - VDD)

VL3 - VDD = 2/a * (VL6 - VDD)

VL4 - VDD = (a-2)/a * (VL6 - VDD)

VL5 - VDD = (a-1)/a * (VL6 - VDD)

V_{L6}

This pin outputs the most negative LCD driving voltage level. The V_{L6} can be supplied externally or generated by the internal regulator. Please refer to the Set Power Control Register command for detail description.

M/$\overline{S}$

This pin is the master/slave mode selection input. When this pin is pulled high, master mode is selected. CL, M, MSTAT and DOF signals will be the output pins for slave devices.
When this pin is pulled low, slave mode is selected. CL, M, DOF are input pins getting signal from master device. The state of MSTAT will be high impedance.

CLS

This pin is the internal clock enable pin. When this pin is pulled high, internal clock is enabled.
The internal clock will be disabled when CLS is pulled low. Under such circumstances, an external clock source must be fed into the CL pin.

C68/$\overline{80}$

This pin is the MCU parallel interface selection input. When the pin is pulled high, 6800 series interface is selected. When the pin is pulled low, 8080 series interface is selected.

If Serial Interface is selected (P/$\overline{S}$ pulled low), the setting of this pin is ignored. The C68/$\overline{80}$ pin must be connected to a known logic state (either high or low).

P/$\overline{S}$

This pin is the serial/parallel interface selection input. When this pin is pulled high, parallel interface mode is selected. When this pin is pulled low, serial interface will be selected.

Note1: For serial mode, D0, D1, D2, D3, D4, D5, R/$\overline{W}$ ($\overline{WR}$), E/($\overline{RD}$) are recommended to connect to Vss.
Note2: Read back operation is only available in parallel mode.

C1, C0

These two pins should connect to V_{DD} operation.

IRS

This is the input pin to enable the internal resistors network for the voltage regulator. This pin should be connected to VDD for any circumstances.

$\overline{SPI}$

This is the input pin to enable the circuitry for providing serial interface. This pin must be connected to low at any circumstances. When the $\overline{SPI}$ pin and the P/$\overline{S}$, selection input are both pulled low, the serial interface is enabled. When the $\overline{SPI}$ pin is pulled low and the P/$\overline{S}$ selection input is pulled high, the parallel interface is enabled.

NC/TEST0 – TEST2/T0 – T3

These are the No Connection pins. These pins should be left open individually.
Remarks: These pins should not be connected together.

ROW0 - ROW63

These pins provide the Common driving signals to the LCD panel. Please refer to the Table 3 on Page 11 for the COM signal mapping.

SEG0 - SEG103

These pins provide the LCD segment driving signals. The output voltage level of these pins is V_{DD} during sleep mode or standby mode.

ICONS

There are two ICONS pins (pin137 and 275) on the chip. Both pins output exactly the same signal. The reason for duplicating these pins is to enhance the flexibility of the LCD layout.

Table 3 – Example of ROW pin assignment for programmable MUX of SSD1818

Pad	SSD1818
ROW0	COM0
ROW1	COM1
ROW2	COM2
ROW3	COM3
ROW4	COM4
ROW5	COM5
ROW6	COM6
ROW7	COM7
ROW8	COM8
ROW9	COM9
ROW10	COM10
ROW11	COM11
ROW12	COM12
ROW13	COM13
ROW14	COM14
ROW15	COM15
ROW16	COM16
ROW17	COM17
ROW18	COM18
ROW19	COM19
ROW20	COM20
ROW21	COM21
ROW22	COM22
ROW23	COM23
ROW24	COM24
ROW25	COM25
ROW26	COM26
ROW27	COM27
ROW28	COM28
ROW29	COM29
ROW30	COM30
ROW31	COM31
ROW32	COM32
ROW33	COM33
ROW34	COM34
ROW35	COM35
ROW36	COM36
ROW37	COM37
ROW38	COM38
ROW39	COM39
ROW40	COM40
ROW41	COM41
ROW42	COM42
ROW43	COM43
ROW44	COM44
ROW45	COM45
ROW46	COM46
ROW47	COM47
ROW48	COM48
ROW49	COM49
ROW50	COM50
ROW51	COM51
ROW52	COM52
ROW53	COM53
ROW54	COM54
ROW55	COM55
ROW56	COM56
ROW57	COM57
ROW58	COM58
ROW59	COM59
ROW60	COM60
ROW61	COM61
ROW62	COM62
ROW63	COM63

Note: X-Row pin will output non-selected COM signal

FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder and Command Interface

This module determines whether the input signal is interpreted as data or command. Input is directed to this module based on the input of the D/$\overline{C}$ pin.

If the D/$\overline{C}$ pin is high, input is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D_7-D_0 is interpreted as a Command. It will be decoded and written to the corresponding command register.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/$\overline{W}$ ($\overline{WR}$), D/$\overline{C}$, E/($\overline{RD}$), $\overline{CS1}$ and CS2.

Read cycle

R/$\overline{W}$ ($\overline{WR}$) input high indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3.

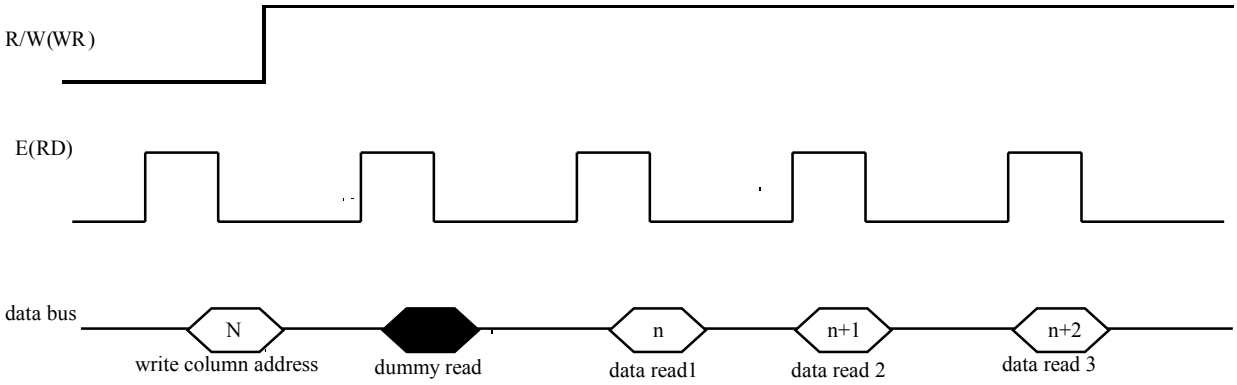


Figure 3 - Display Data Read Back Procedure - Insertion of Dummy Read

Write cycle

R/$\overline{W}$ ($\overline{WR}$) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the D/$\overline{C}$ input. The E($\overline{RD}$) input serves as data latch signal (clock) when high, provided that the $\overline{CS1}$ is pulled low and the CS2 is pulled high respectively.

Please refer to Figure 9 on Page 34 for Parallel Interface Timing Diagram of 6800-series microprocessors.

MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), E/($\overline{RD}$), R/$\overline{W}$ ($\overline{WR}$), D/$\overline{C}$, $\overline{CS1}$ and CS2.

Read cycle

E($\overline{RD}$) input serves as data read latch signal (clock) when low, provided that $\overline{CS1}$ is pulled low and the CS2 is pulled high respectively. The D/$\overline{C}$ signal determines whether the receiving signal is a display data read or a status register read signal. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Write cycle

R/$\overline{W}$ ($\overline{WR}$) input serves as data write latch signal(clock) when high, provided that $\overline{CS1}$ and CS2 are low and high respectively. The D/$\overline{C}$ signal determines whether the receiving signal is a display data write or a command register write signal.
Please refer to Figure 10 on Page 35 for Parallel Interface Timing Diagram of 8080-series microprocessor.

MPU Serial interface

The serial interface consists of serial clock SCK (D_6), serial data SDA (D_7), D/$\overline{C}$, $\overline{CS1}$ and CS2. Input to SDA is shifted into a 8-bit shift register on every rising edge of SCK in the order of D_7, D_6,... D_0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock.

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

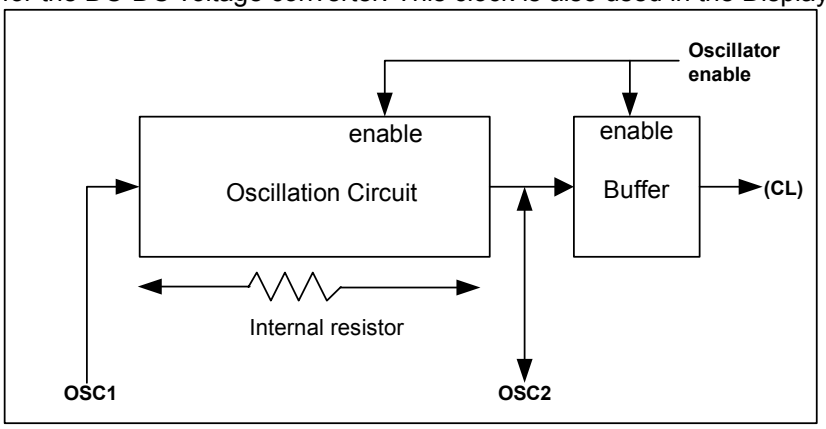


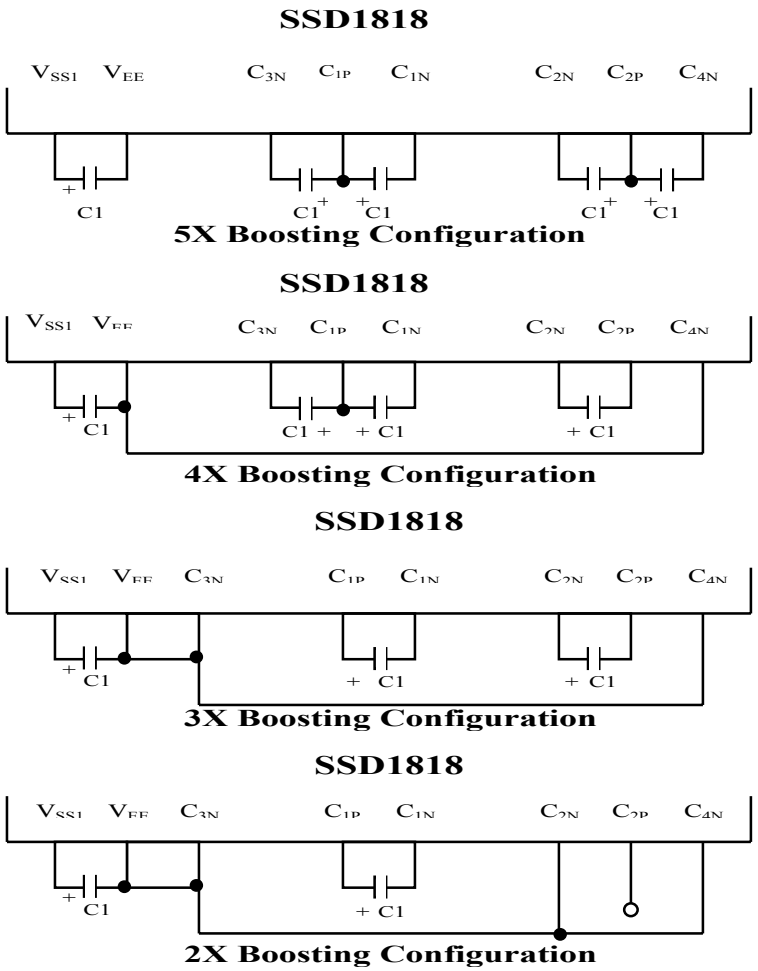
Figure 4 - Oscillator

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output. With reference to V_{DD}, it takes a single supply input, V_{SS}, and generate necessary voltage levels. This block consists of:

1. 2X, 3X, 4X and 5X DC-DC voltage converter

The built-in DC-DC voltage converter is used to generate the negative voltage with reference to VDD from the voltage input (VSS1). For SSD1818, it is possible to produce 2X, 3X, 4X or 5X boosting from the potential different between V_{SS1} - V_{DD}. Detailed configurations of the DC-DC converter for different boosting multiples are given in Figure 5.



Remarks:

1. C1= 0.47 – 1.0uF
2. Boosting input from V_{SS1}
3. V_{SS1} should be lower potential than or equal to V_{SS}
4. All voltages are referenced to V_{DD}

Figure 5 - DC-DC Converter Configurations

2. Voltage Regulator (Voltages referenced to V_{DD})
Internal (IRS pin = H) feedback gain can control the LCD driving contrast curves.
If internal resistor network is enabled, eight settings can be selected through software command.

3. Contrast Control (Voltage referenced to V_{DD})

Software control of the 64-contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

$$V_{L6} - V_{DD} = Gain * [1 + (\frac{18 + \alpha}{81})] * V_{ref}$$

α stands for the contrast set (0 to 63)

Gain = (1 + Rb/Ra), the reference value is shown in table 5.

Register ratio D2 D1 D0	Thermal Gradient = -0.07 %/°C
0 0 0	2.92
0 0 1	3.40
0 1 0	3.89
0 1 1	4.37
1 0 0	4.85
1 0 1	5.23
1 1 0	5.72
1 1 1	6.19

Gain value at different register ratio and thermal gradient settings

V_{ref} is a fixed IC–internal voltage supply and its voltage at room temperature (25 °C) is shown in table 6 for reference.

Type	Thermal Gradient	V_{ref}
TC 0	-0.07 %/°C	-1.08V
TC 2	-0.13 %/°C	-1.12V
TC 4	-0.26 %/°C	-1.09V
TC 7	-0.29 %/°C	-1.10V

V_{ref} values at different thermal gradient settings

The voltage regulator output for different gain/contrast settings is shown in figure 6.

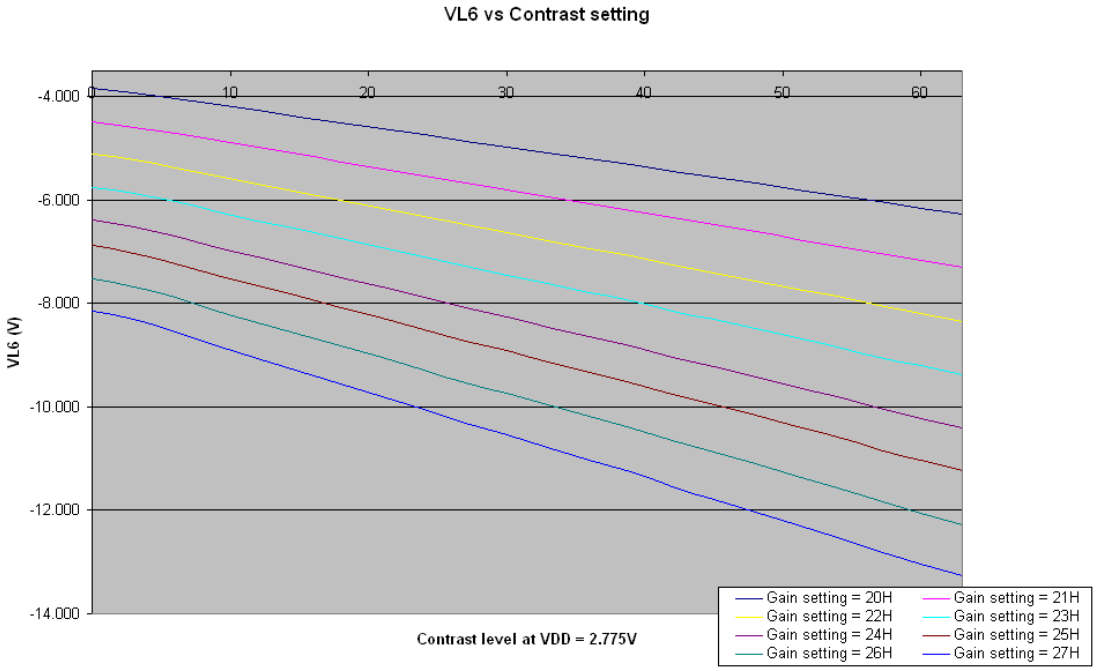


Figure 6– Voltage Regulator Output for different Gain/Contrast Settings

4. Bias Ratio Selection circuitry
The bias ratios can be software selected from 1/4, 1/5, 1/6, 1/7, 1/8 and 1/9.
Since there will be slightly different in command pattern for different MUX, please refer to Command Descriptions section of this data sheet.

5. Self adjust temperature compensation circuitry
This block provides 4 different compensation settings to satisfy various liquid crystal temperature grades by software control. Default temperature coefficient (TC) setting is TC0.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 104 x 65 = 6760 bits. Table 4 on Page 17 is a description of the GDDRAM address map.
For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.
For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. Table 4 on Page 17 shows the case in which the display start line register is set to 38h.
For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage.

RAM	RAM	Normal	00h	01h	02h	03h	---	64h	65h	66h	67h	Common Pins	
RAM	Colum	Remapped	67h	66h	65h	64h	---	03h	02h	01h	00h	Normal	Remapped
00h	Page 0	DB0 (LSB)				---						8	55
01h		DB1				---						9	54
02h		DB2				---						10	53
03h		DB3				---						11	52
04h		DB4				---						12	51
05h		DB5				---						13	50
06h		DB6				---						14	49
07h		DB7 (MSB)				---						15	48
08h	Page 1	DB0 (LSB)				---						16	47
09h		DB1				---						17	46
0Ah		DB2				---						18	45
0Bh		DB3				---						19	44
0Ch		DB4				---						20	43
0Dh		DB5				---						21	42
0Eh		DB6				---						22	41
0Fh		DB7 (MSB)				---						23	40
10h	Page 2	DB0 (LSB)				---						24	39
11h		DB1				---						25	38
12h		DB2				---						26	37
13h		DB3				---						27	36
14h		DB4				---						28	35
15h		DB5				---						29	34
16h		DB6				---						30	33
17h		DB7 (MSB)				---						31	32
18h	Page 3	DB0 (LSB)				---						32	31
19h		DB1				---						33	30
1Ah		DB2				---						34	29
1Bh		DB3				---						35	28
1Ch		DB4				---						36	27
1Dh		DB5				---						37	26
1Eh		DB6				---						38	25
1Fh		DB7 (MSB)				---						39	24
20h	Page 4	DB0 (LSB)				---						40	23
21h		DB1				---						41	22
22h		DB2				---						42	21
23h		DB3				---						43	20
24h		DB4				---						44	19
25h		DB5				---						45	18
26h		DB6				---						46	17
27h		DB7 (MSB)				---						47	16
28h	Page 5	DB0 (LSB)				---						48	15
29h		DB1				---						49	14
2Ah		DB2				---						50	13
2Bh		DB3				---						51	12
2Ch		DB4				---						52	11
2Dh		DB5				---						53	10
2Eh		DB6				---						54	9
2Fh		DB7 (MSB)				---						55	8
30h	Page 6	DB0 (LSB)				---						56	7
31h		DB1				---						57	6
32h		DB2				---						58	5
33h		DB3				---						59	4
34h		DB4				---						60	3
35h		DB5				---						61	2
36h		DB6				---						62	1
37h		DB7 (MSB)				---						63	0
38h	Page 7	DB0 (LSB)				---						0	63
39h		DB1				---						1	62
3Ah		DB2				---						2	61
3Bh		DB3				---						3	60
3Ch		DB4				---						4	59
3Dh		DB5				---						5	58
3Eh		DB6				---						6	57
3Fh		DB7 (MSB)				---						7	56
	Page 8	DB0 (LSB)				---						ICONS	ICONS
		Segment Pins	0	1	2	3	---	100	101	102	103		

Remarks : DB0 – DB7 represent the data bit of the GDDRAM

Table 4 - Graphic Display Data RAM (GDDRAM) Address Map with Display Start Line set to 38h

Reset Circuit

This block includes Power On Reset (POR) circuitry and the hardware reset pin, $\overline{RES}$. The POR and Hardware reset performs the same reset function. Once $\overline{RES}$ receives a reset pulse, all internal circuitry will start to initialize. Minimum pulse width the reset sequence is 1us. Status of the chip after reset is given by:
Display is turned OFF
Default Display Mode: 104 x 64 + 1 Icon Line
Normal segment and display data column address mapping (Seg0 mapped to Row address 00h)
Read-modify-write mode is OFF
Power control register is set to 000b
Shift register data clear in serial interface
Bias ratio is set to default: 1/9
Static indicator is turned OFF
Display start line is set to GDDRAM column 0
Column address counter is set to 00h
Page address is set to 0
Normal scan direction of the COM outputs
Contrast control register is set to 20h
Test mode is turned OFF
Temperature Coefficient is set to TC0
Note: Please find more explanation in the Applications Note attached at the back of the specification.

Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.
64 MUX: 104 + 65 = 169

HV Buffer Cell (Level Shifter)

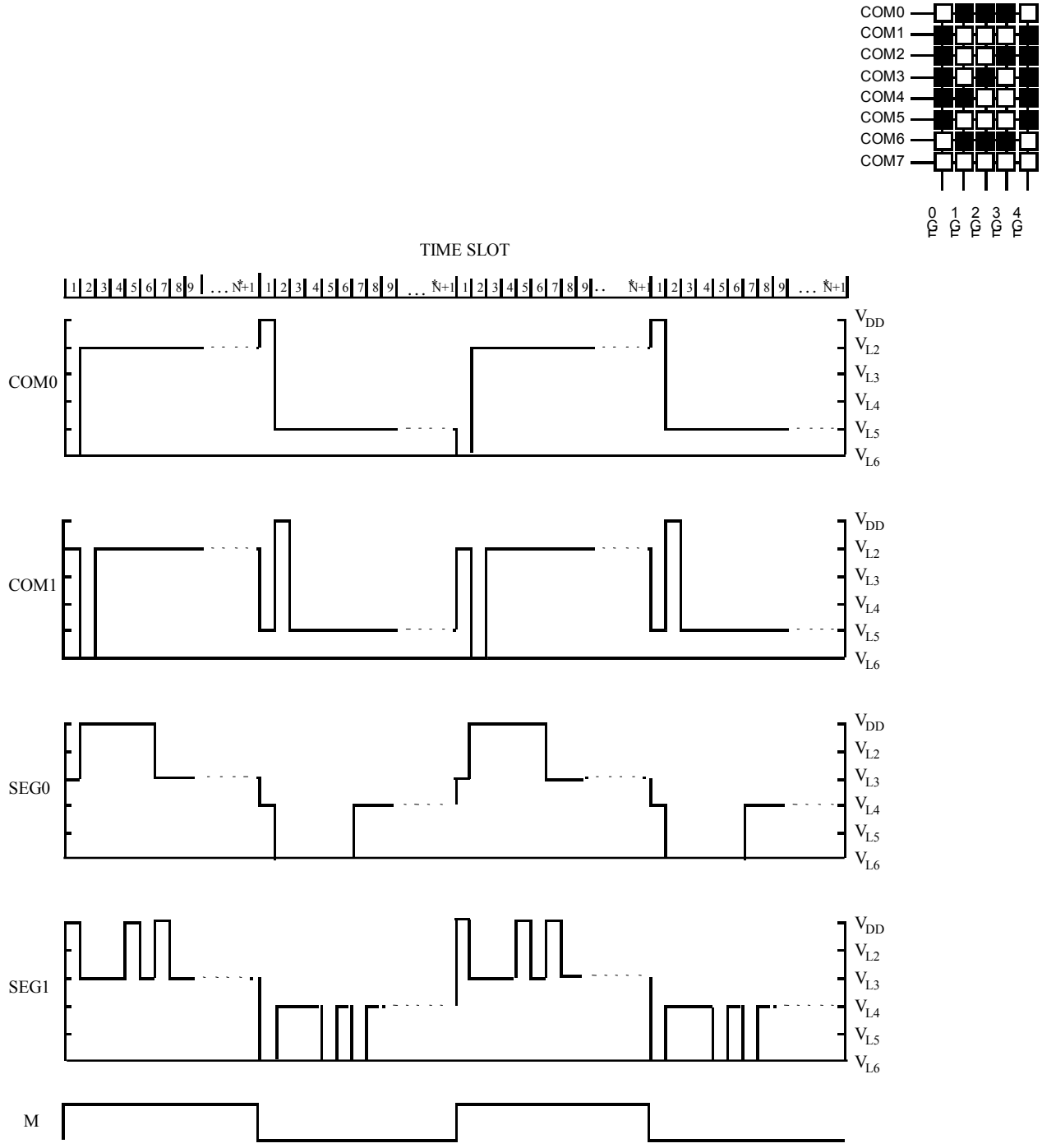
HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with reference an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Level Selector

Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

LCD Panel Driving Waveform

Figure 7 is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms illustrate the desired multiplex scheme.



* Note 1: N+1 is the number of multiplex ratio including Icon.

Figure 7 - LCD Driving Waveform for Displaying "0"

COMMAND TABLE

Bit Pattern	Command	Description
$0000X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The lower nibble of column address is reset to 0000b after POR
$0001X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The higher nibble of column address is reset to 0000b after POR.
$00100X_2X_1X_0$	Set Internal Regulator Resistor Ratio	Feedback gain of the internal regulator generating VL6 increases as $X_2X_1X_0$ increased from 000b to 111b. After POR, $X_2X_1X_0$ = 100b
$00101X_2X_1X_0$	Set Power Control Register	X_0=0: turns off the output op-amp buffer (POR) X_0=1: turns on the output op-amp buffer X_1=0: turns off the internal regulator (POR) X_1=1: turns on the internal regulator X_2=0: turns off the internal voltage booster (POR) X_2=1: turns on the internal voltage booster
$01X_5X_4X_3X_2X_1X_0$	Set Display Start Line	Set GDDRAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000 after POR.
10000001 ** $X_5X_4X_3X_2X_1X_0$	Set Contrast Control Register	Select contrast level from 64 contrast steps. Contrast increases (VL6 decreases) as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 100000b after POR
$1010000X_0$	Set Segment Re-map	X_0=0: column address 00h is mapped to SEG0 (POR) X_0=1: column address 67h is mapped to SEG0 Refer to Table 4 on page 17 for example.
$1010001X_0$	Set LCD Bias	X_0=0: POR default bias: 1/9 X_0=1: alternate bias: 1/7 For other bias ratio settings, see “Set 1/4 Bias Ratio” and “Set Bias Ratio” in Extended Command Set.
$1010010X_0$	Set Entire Display On/Off	X_0=0: normal display (POR) X_0=1: entire display on
$1010011X_0$	Set Normal/Reverse Display	X_0=0: normal display (POR) X_0=1: reverse display
$1010111X_0$	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
$1011X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0-8) for read/write using $X_3X_2X_1X_0$
$1100X_3$ * * *	Set COM Output Scan Direction	X_3=0: normal mode (POR) X_3=1: remapped mode, COM0 to COM[N-1] becomes COM[N-1] to COM0 when Multiplex ratio is equal to N. See Table 4 on page 17 for detail mapping.
11100000	Set Read-Modify-Write Mode	Read-Modify-Write mode will be entered in which the column address will not be increased during display data read. After POR, Read-modify-write mode is turned OFF.
11100010	Software Reset	Initialize internal status registers
11101110	Set End of Read-Modify-Write Mode	Exit Read-Modify-Write mode. RAM Column address before entering the mode will be restored. After POR, Read-modify-write mode is OFF.

1010110X_0 * * * * * * X_1X_0 Set Indicator On/Off	Indicator Display Mode	This second byte command is required ONLY when "Set Indicator On" command is sent. X_0 = 0: indicator off (POR, second command byte is not required) X_0 = 1: indicator on (second command byte required) X_1X_0 = 00: indicator off X_1X_0 = 01: indicator on and blinking at ~1 second interval X_1X_0 = 10: indicator on and blinking at ~1/2 second interval X_1X_0 = 11: indicator on constantly
11100011	NOP	Command result in No Operation
11110000	Test Mode Reset	Reserved for IC testing. Do NOT use
1111 * * * *	Set Test Mode	Reserved for IC testing. Do NOT use.
10101110 10100101	Set Power Save Mode	(Standby or Sleep) Standby or sleep mode will be entered using compound commands. Issue compound commands "Set Display Off" followed by "Set Entire Display On".

Table 5 - Write Command Table (D/$\overline{C}$ =0, R/$\overline{W}$ ($\overline{WR}$)=0, E($\overline{RD}$)=1)

Bit Pattern	Command	Description
10101000 00$X_5X_4X_3X_2X_1X_0$	Set Multiplex Ratio	To select multiplex ratio N from 2 to the maximum multiplex ratio (POR value) for each member (including icon line). Max. MUX ratio: 64 MUX: 65 N = $X_5X_4X_3X_2X_1X_0$ + 2, e.g. N = 001111b + 2 = 17
10101001 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set Bias Ratio (X_1X_0) Set TC Value ($X_4X_3X_2$) Modify Osc. Freq. ($X_7X_6X_5$)	X_1X_0 = 00(POR) 01 10 11 1/9 or 1/7 1/5 1/6 1/8 $X_4X_3X_2$ = 000: (TC0) Typ. –0.07 $X_4X_3X_2$ = 010: (TC2) Typ. –0.13 $X_4X_3X_2$ = 100: (TC4) Typ. –0.26 $X_4X_3X_2$ = 111: (TC7) Typ. –0.29 $X_4X_3X_2$ = 001, 011, 101, 110: Reserved Increase the value of $X_7X_6X_5$ will increase the oscillator frequency and vice versa. Default Mode: $X_7X_6X_5$ = 011 (POR) : Typ. 21.5kHz Remarks: By software program the multiplex ratio, the typical oscillator frequency is listed above.
1010101X_0	Set 1/4 Bias Ratio	X_0 = 0: use normal setting (POR) X_0 = 1: fixed at 1/4 bias regardless of other bias setting commands

11010100 00$X_5X_4$0000	Set Total Frame Phases	The On/Off of the Static Icon is given by 3 phases / 1 phase overlapping of the M and MSTAT signals. This command set total phases of the M/MSTAT signals for each frame. The more the total phases, the less the overlapping time and thus the lower the effective driving voltage. X_5X_4 = 00: 5 phases X_5X_4 = 01: 7 phases X_5X_4 = 10: 9 phases (POR) X_5X_4 = 11: 16 phases
11010011 00$X_5X_4X_3X_2X_1X_0$	Set Display Offset	After POR, $X_5X_4X_3X_2X_1X_0$ = 0 After setting MUX ratio less than default value, data will be displayed at Center of display matrix. To move display towards Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = L To move display away from Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = 64-L Note: max. value of L = (POR default MUX ratio – display MUX)/2
1101000X_0	ICON Mode	X_0 = 0 : icon off (POR) X_0 = 1 : icon mode on
11010110 001111X_1X_0	Enable Band Gap Reference Circuit	X_1X_0 = 00 01 10 11(POR) 100 ms 200 ms 400 ms 800 ms Approx. band gap clock period This command should execute if divider is used without capacitor at VL2 to VL5. Recommendation: set the band gap clock period to approx. 200ms
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D_7=0: indicates the driver is ready for command. D_7=1: indicates the driver is Busy. D_6=0: indicates reverse segment mapping with column address. D_6=1: indicates normal segment mapping with column address. D_5=0: indicates the display is ON. D_5=1: indicates the display is OFF. D_4=0: initialization is completed. D_4=1: initialization process is in progress after RES or software reset. $D_3D_2D_1D_0$ = 1001 or 0011, the 4-bit is fixed to either 1001 or 0011 which could be used to identify as Solomon Systech Device.

Table 6 - Extended Command Table

Note: Command patterns other than that given in Command Table and Extended Command Table are prohibited. Otherwise, unexpected result will occur.

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$ ($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode, input Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided in serial interface mode.
In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode.

Also, a dummy read is required before first valid data is read. See Figure 3 on page 12 in Functional Block Descriptions section for detail waveform diagram.

To write data to the GDDRAM, input Low to R/$\overline{W}$ ($\overline{WR}$) pin and High to D/$\overline{C}$ pin for both 6800-series and 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.
It should be noted that, after the automatic column address increment, the pointer will NOT wrap round to 0. The pointer will exit the memory address space after accessing the last column. Therefore, the pointer should be re-initialized when progress to another page address

D/$\overline{C}$	R/$\overline{W}$ ($\overline{WR}$)	Action	Auto Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

Table 7 - Automatic Address Increment

COMMAND DESCRIPTIONS

Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor sets for different regulator gain when using internal regulator resistor network (IRS pin pulled high). In other words, this command is used to select which contrast curve from the eight possible selections. Please refer to Functional Block Descriptions section for detail calculation of the LCD driving voltage.

Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three related power sub-circuits could be turned on/off by this command.
Internal voltage booster is used to generate the negative voltage supply (V_{EE}) from the voltage input (V_{SS1} - V_{DD}). An external negative power supply is required if this option is turned off.
Internal regulator is used to generate the LCD driving voltage, V_{L6}, from the negative power supply, V_{EE}.
Output op-amp buffer is the internal divider for dividing the different voltage levels (V_{L2}, V_{L3}, V_{L4}, V_{L5}) from the internal regulator output, V_{L6}. External voltage sources should be fed into this driver if this circuit is turned off.

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0 and so on. Display start line values of 0 to 63 are assigned to Page 0 to 7.
Please refer to Table 4 on Page 17 as an example for display start line set to 56 (38h).

Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing the LCD driving voltage, V_{L6}, provided by the On-Chip power circuits. V_{L6} is set with 64 steps (6-bit) in the contrast control register by a set of compound commands.
See Figure 8 for the contrast control flow.

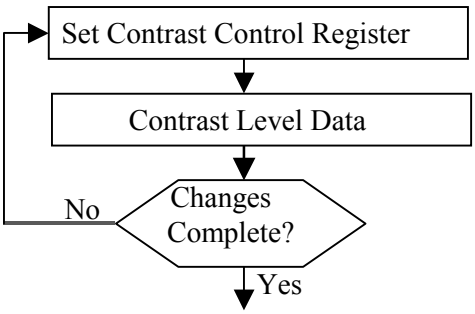


Figure 8 - Contrast Control Flow Set Segment Re-map

This command changes the mapping between the display data column addresses and segment drivers. It allows flexibility in mechanical layout of LCD glass design. Please refer to Table 4 on Page 17 for example.

Set LCD Bias

This command is used to select a suitable bias ratio required for driving the particular LCD panel in use.
The selectable values of this command for 64 MUX are 1/9 or 1/7.
For other bias ratio settings, extended commands should be used.

Set Entire Display On/Off

This command forces the entire display, including the icon row, to be illuminated regardless of the contents of the GDDRAM. In addition, this command has higher priority than the normal/reverse display.
This command is used together with “Set Display ON/OFF” command to form a compound command for entering power save mode. See “Set Power Save Mode” later in this section.

Set Normal/Reverse Display

This command turns the display to be either normal or reverse. In normal display, a RAM data of 1 indicates an illumination on the corresponding pixel, while in reverse display, a RAM data of 0 will turn on the pixel. It should be noted that the icon line will not affect, that is not reverse by this command.

Set Display On/Off

This command is used to turn the display on or off. When display off is issued with entire display is on, power save mode will be entered. See “Set Power Save Mode” later in this section for details.

Set Page Address

This command enters the page address from 0 to 8 to the RAM page register for read/write operations. Please refer to Table 4 on Page 17 for detail mapping.

Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. See Table 4 on Page 17 for the relationship between turning on or off of this feature.
In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

Set Read-Modify-Write Mode

This command puts the chip in read-modify-write mode in which:

1. column address is saved before entering the mode
2. column address is increased only after display data write but not after display data read.

This Read-Modify-Write mode is used to save the MCU's loading when a very portion of display area is being updated frequently.
As reading the data will not change the column address, it could be get back from the chip and do some operation in the MCU. Then the updated data could be write back to the GDDRAM with automatic address increment.
After updating the area, "Set End of Read-Modify-Write Mode" is sent to restore the column address and ready for next update sequence.

Software Reset

Issuing this command causes some of the chip's internal status registers to be initialized:
Read-Modify-Write mode is off
Static indicator is turned OFF
Display start line register is cleared to 0
Column address counter is cleared to 0
Page address is cleared to 0
Normal scan direction of the COM outputs
Internal regulator resistors Ratio is set to 4
Contrast control register is set to 20h

Set End of Read-Modify-Write Mode

This command relieves the chip from read-modify-write mode. The column address before entering read-modify-write mode will be restored no matter how much modification during the read-modify-write mode.

Set Indicator On/Off

This command turns on or off the static indicator driven by the M and MSTAT pins.
When the "Set Indicator On" command is sent, the second command byte "Indicator Display Mode" must be followed. However, the "Set Indicator Off" command is a single byte command and no second byte command is required.
The status of static indicator also controls whether standby mode or sleep mode will be entered, after issuing the power save compound command. See "Set Power Save Mode" later in this section.

NOP

A command causing the chip takes No Operation.

Set Test Mode

This command forces the driver chip into its test mode for internal testing of the chip. Under normal operation, users should NOT use this command.

Set Power Save Mode

Entering Standby or Sleep Mode should be done by using a compound command composed of "Set Display ON/OFF" and "Set Entire Display ON/OFF" commands. When "Set Entire Display ON" is issued when display is OFF, either Standby Mode or Sleep Mode will be entered.
The status of the Static Indicator will determine which power save mode is entered. If static indicator is off, the Sleep Mode will be entered:

Internal oscillator and LCD power supply circuits are stopped
Segment and Common drivers output V_{DD} level
The display data and operation mode before sleep are held
Internal display RAM can still be accessed
If the static indicator is on, the chip enters Standby Mode which is similar to sleep mode except addition with:
Internal oscillator is on
Static drive system is on
Please also be noted that during Standby Mode, if the software reset command is issued, Sleep Mode will be entered. Both power save modes can be exited by the issue of a new software command or by pulling Low at hardware pin $\overline{RES}$.

Status register Read

This command is issued by pulling $D/\overline{C}$ Low during a data read (refer to Figure 9 on Page 34 and Figure 10 on Page 35 for parallel interface waveforms). It allows the MCU to monitor the internal status of the chip.
No status read is provided for serial mode.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features designed for the chip.

Set Multiplex Ratio

This command switches default multiplex ratio to any multiplex mode from 2 to the maximum multiplex ratio (POR value), including the icon line. Max. MUX ratio: 65
The chip pins ROW0-ROW63 will be switched to corresponding COM signal output, see Table 8 on Page 29 for examples of 18 multiplex (including icon line) settings with and without 7 lines display offset for different MUX.
It should be noted that after changing the display multiplex ratio, the bias ratio may also need to be adjusted to make display contrast consistent.

Set Bias Ratio

Except the 1/4 bias, all other available bias ratios could be selected using this command plus the “Set LCD Bias” command.
For detail setting values and POR default, please refer to the extended command table, Table 6 on Page 21.

Set Temperature Coefficient (TC) Value

One out of 4 different temperature coefficient settings is selected by this command in order to match various liquid crystal temperature grades. Please refer to the extended command table, Table 6 on Page 21, for detailed TC values.

Modify Oscillator Frequency

The oscillator frequency can be fine tuned by applying this command. Since the oscillator frequency will be affected by some other factors, this command is not recommended for general usage. Please contact SOLOMON Systech Limited application engineers for more detail explanation on this command.

Set 1/4 Bias Ratio

This command sets the bias ratio directly to 1/4. This bias ratio is especially designed for use in under 12 MUX display.

In order to restore to other bias ratio, this command must be executed, with LSB=0, before the “Set Multiplex ratio” or “Set LCD Bias” command is sent.

Set Total Frame Phases

The total number of phases for one display frame is set by this command.
The Static Icon is generated by the overlapping of the M and MSTAT signals. These two pins output either V_{SS} or V_{DD} at same frequency but with phase different.
To turn on the Static Icon, 3 phases overlapping is applied to these signals, while 1 phase overlapping is given to the Off status.
The more the total number of phases in one frame, the less the overlapping time and thus the lower the effective driving voltage at the Static Icon on the LCD panel.

Set Display Offset

This command should be sent ONLY when the multiplex ratio is set less than the default value.
When a lesser multiplex ratio is set, the display will be mapped in the middle (y-direction) of the LCD, see the no offset columns on Table 8 on Page 29. Use this command could move the display vertically within the 64 commons.
To make the Reduced-MUX Com 0 (Com 0 after reducing the multiplex ratio) towards the Row 0 direction for L lines, the 6-bit data in second command should be given by L. An example for 7 line moving towards to Com0 direction is given on Table 8 on Page 29.
To move in the other direction by L lines, the 6-bit data should be given by 64-L.
Please note that the display is confined within the default multiplex value. That is the maximum value of L is given by the half of the default value minus the reduced-multiplex ratio. For an odd display MUX after reduction, moving away from Row 0 direction will has 1 more step.

Set Icon Mode

This command enables or disables the icon mode. It should be noticed that the default setting (POR) will not enable the icon mode.

Enable Band Gap Reference Circuit

This command enables or disables the band gap reference circuit. It should be noticed that this command should be executed if divider is used without capacitor at VL2 to VL5. There are four selections on the band gap clock period. We recommended to set the band gap clock period to 128T in normal operation.

	SSD1818	
	No Offset	7 lines Offset
ROW0	X	X
ROW1	X	X
ROW2	X	X
ROW3	X	X
ROW4	X	X
ROW5	X	X
ROW6	X	X
ROW7	X	X
ROW8	X	X
ROW9	X	X
ROW10	X	X
ROW11	X	X
ROW12	X	X
ROW13	X	X
ROW14	X	X
ROW15	X	X
ROW16	X	COM0
ROW17	X	COM1
ROW18	X	COM2
ROW19	X	COM3
ROW20	X	COM4
ROW21	X	COM5
ROW22	X	COM6
ROW23	COM0	COM7
ROW24	COM1	COM8
ROW25	COM2	COM9
ROW26	COM3	COM10
ROW27	COM4	COM11
ROW28	COM5	COM12
ROW29	COM6	COM13
ROW30	COM7	COM14
ROW31	COM8	COM15
ROW32	COM9	COM16
ROW33	COM10	X
ROW34	COM11	X
ROW35	COM12	X
ROW36	COM13	X
ROW37	COM14	X
ROW38	COM15	X
ROW39	COM16	X
ROW40	X	X
ROW41	X	X
ROW42	X	X
ROW43	X	X
ROW44	X	X
ROW45	X	X
ROW46	X	X
ROW47	X	X
ROW48	X	X
ROW49	X	X
ROW50	X	X
ROW51	X	X
ROW52	X	X
ROW53	X	X
ROW54	X	X
ROW55	X	X
ROW56	X	X
ROW57	X	X
ROW58	X	X
ROW59	X	X
ROW60	X	X
ROW61	X	X
ROW62	X	X
ROW63	X	X

Table 8 - ROW pin assignment for COM signals for SSD1818 in an 18 MUX display (including icon line) without/with 7 lines display offset towards ROW0

Note: X-Row pin will output non-selected COM signal

MAXIMUM RATINGS

Table 9 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{EE}		0 to –12.0	V
Vin	Input Voltage	VSS-0.3 to VDD+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC CHARACTERISTICS

Table 10 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.4	2.7	3.5	V V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 4X DC-DC Converter Enabled, Write accessing, Tcyc =3.3MHz, Typ. Osc. Freq., Display On, no panel attached.	-	480	600	µA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{EE} = -8.1V, Voltage Generator Disabled, R/$\overline{W}$ ($\overline{WR}$) Halt, Typ. Osc. Freq., Display On, V_{L6} - V_{DD} = -9V, no panel attached.	-	50	100	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{EE} = -8.1V, Voltage Generator On, 4x DC-DC Converter Enabled, R/$\overline{W}$ ($\overline{WR}$) Halt, Typ. Osc. Freq., Display On, V_{L6} - V_{DD} = -9V, no panel attached.	-	120	200	µA
I_{SB}	Standby Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Typ. Osc. Freq., R/$\overline{W}$ ($\overline{WR}$) halt.	-	5	10	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, R/$\overline{W}$ ($\overline{WR}$) halt.	-	1	5	µA
V_{EE}	LCD Driving Voltage Generator Output (V_{EE} Pin)	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	-12.0	-	-1.8	V
V_{LCD}	LCD Driving Voltage Input (V_{EE} Pin)	Voltage Generator Disabled.	-12.0	-	-1.8	V
V_{OH1}	Logic High Output Voltage	Iout=-100mA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Logic Low Output Voltage	Iout=100mA	0	-	0.1* V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Enabled (V_{L6} voltage depends on Int/Ext Contrast Control)	V_{EE}-0.5	-	V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Disable	-	floating	-	V
V_{IH1}	Logic High Input voltage		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2* V_{DD}	V

V_{L2} V_{L3} V_{L4} V_{L5} V_{L6}	LCD Display Voltage Output (V_{L2}, V_{L3}, V_{L4}, V_{L5}, V_{L6} Pins)	Voltage reference to V_{DD}, Bias Divider Enabled, 1:a bias ratio	-	$1/a*V_{L6}$	-	V
			-	$2/a*V_{L6}$	-	V
			-	$(a-2)/a*V_{L6}$	-	V
			-	$(a-1)/a*V_{L6}$	-	V
			-	V_{L6}	-	V
V_{L2} V_{L3} V_{L4} V_{L5} V_{L6}	LCD Display Voltage Input (V_{L2}, V_{L3},V_{L4}, V_{L5}, V_{L6} Pins)	Voltage reference to V_{DD}, External Voltage Generator, Bias Divider Disabled	V_{L3}	-	V_{DD}	V
			V_{L4}	-	V_{L2}	V
			V_{L5}	-	V_{L3}	V
			V_{L6}	-	V_{L4}	V
			-12V	-	V_{L5}	V
I_{OH}	Logic High Output Current Source	Vout = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
ΔV_{L6}	Variation of V_{L6} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-3	0	3	%
TC0	Temperature Coefficient Compensation Flat Temperature Coefficient (POR)	Voltage Regulator Enabled	0	-0.07	-0.11	%/°C
TC2	Temperature Coefficient 2*		-0.11	-0.13	-0.15	%/°C
TC4	Temperature Coefficient 4*		-0.15	-0.26	-0.28	%/°C
TC7	Temperature Coefficient 7*		-0.28	-0.29	-0.30	%/°C

The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref} \text{ at } 50^{o}C - V_{ref} \text{ at } 0\ ^{o}C}{50\ ^{o}C - 0\ ^{o}C} \times \frac{1}{V_{ref} \text{ at } 25\ ^{o}C} \times 100\ \%$$

AC CHARACTERISTICS

Table 11 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Fosc	Oscillation Frequency of Display Timing Generator	Internal Oscillator Enabled (default), VDD = 2.7V Remark: Oscillation Frequency vs. Temperature change (-20°C to 70°C): -0.5%/°C *	17.2	21.5	24.7	kHz
F_{FRM}	Frame Frequency	104 x 64 Graphic Display Mode, Display ON, Internal Oscillator Enabled		$\frac{Fosc}{4x65}$		Hz
		104 x 64 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., Fext, feeding to CL pin.		$\frac{Fext}{4x65}$		Hz

Remarks: Fext stands for the frequency value of external clock feeding to the CL pin
Fosc stands for the frequency value of internal oscillator
Frequency limits are based on the software command set: set multiplex ratio to 64 MUX

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	- -	- -	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	- -	- -	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 12 - Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA = -35 to 85°C)

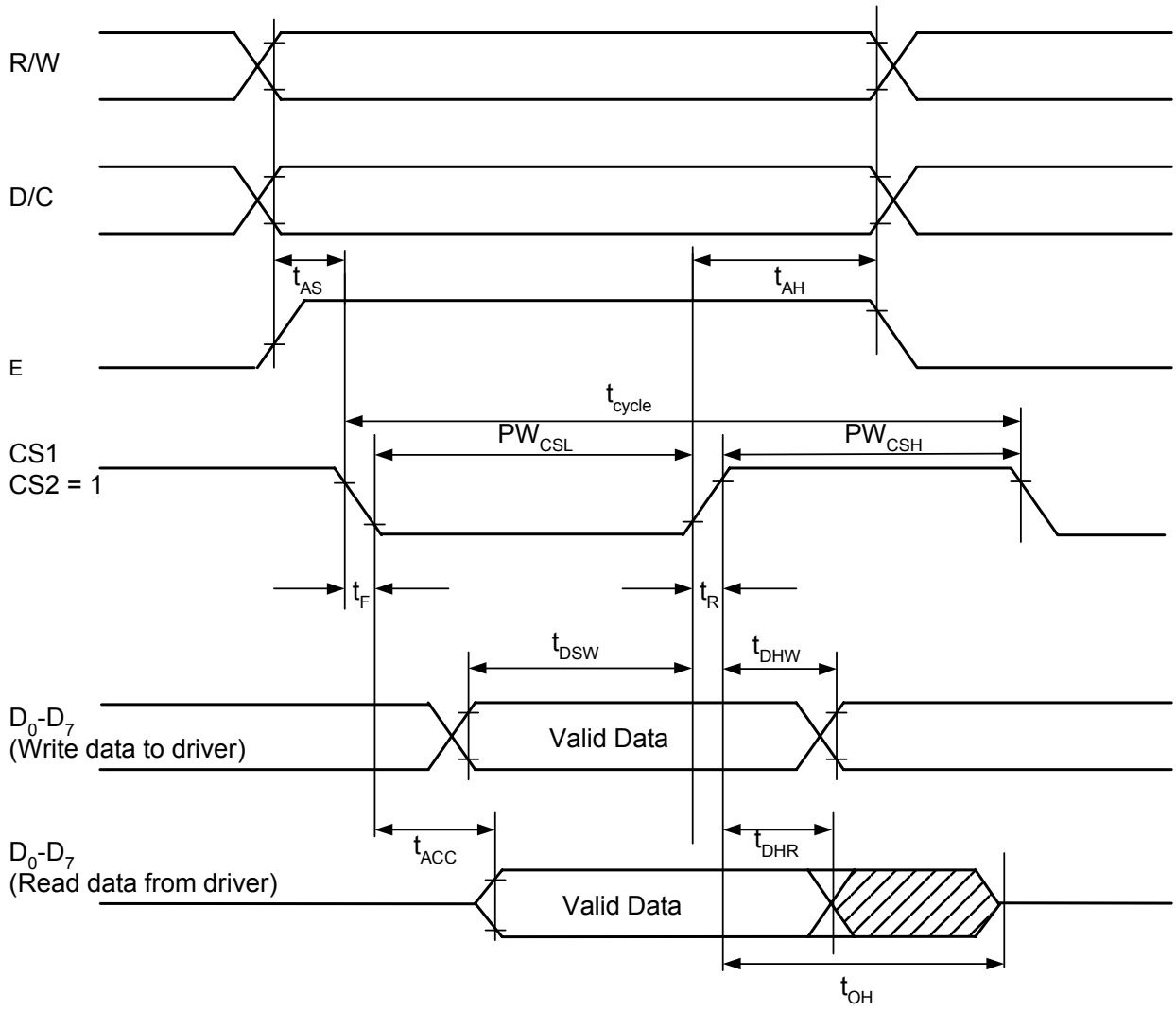


Figure 9 - 6800-series MPU Parallel Interface Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	- -	- -	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	- -	- -	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 13 - Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA = -35 to 85°C)

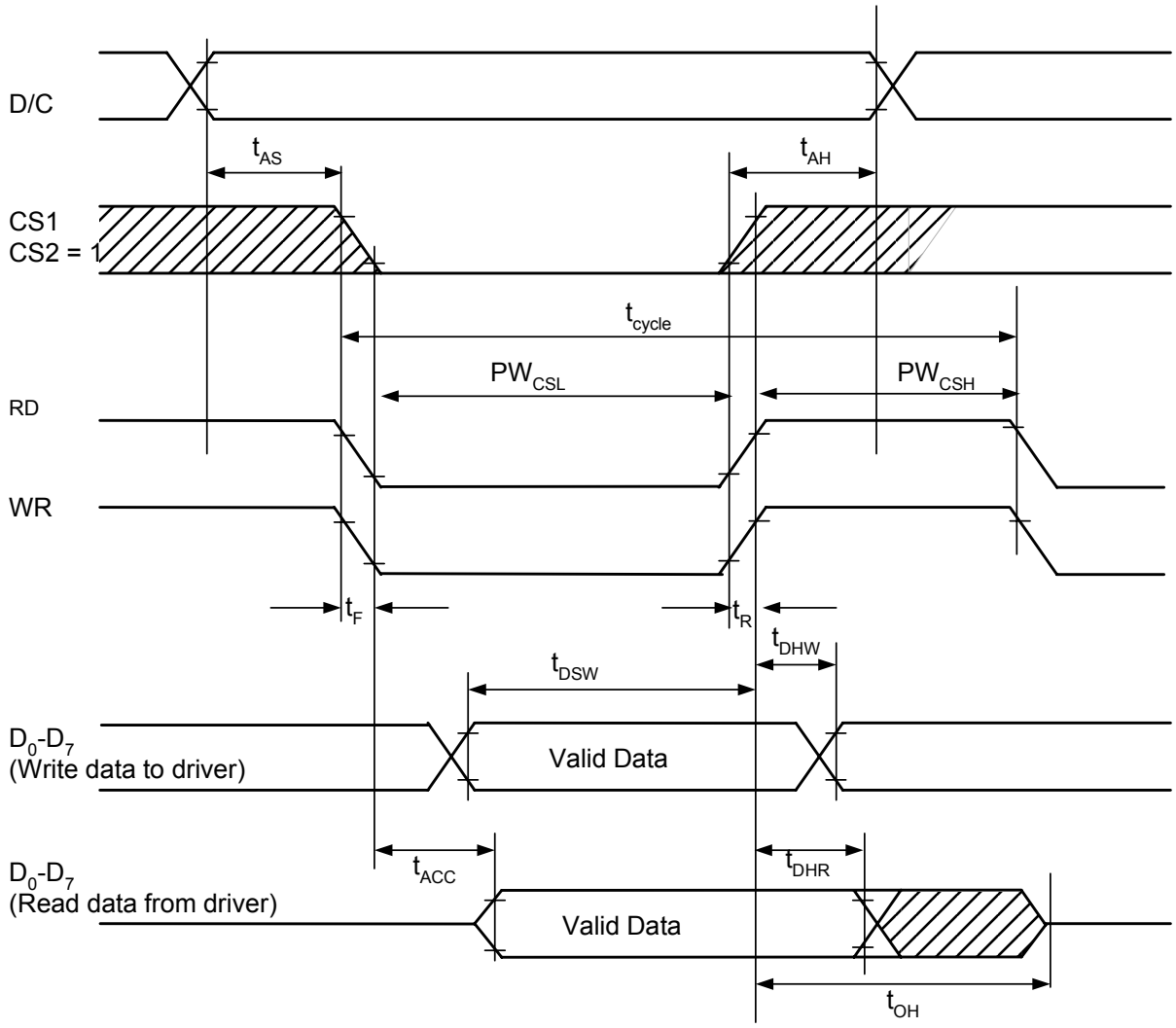


Figure 10 - 8080-series MPU Parallel Interface Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
T_{CLKL}	Clock Low Time	100	-	-	ns
T_{CLKH}	Clock High Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time (for D7 input)	120	- -	- -	ns
t_{CSH}	Chip Select Hold Time (for D0 input)	60	- -	- -	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 14 - Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA = -35 to 85°C)

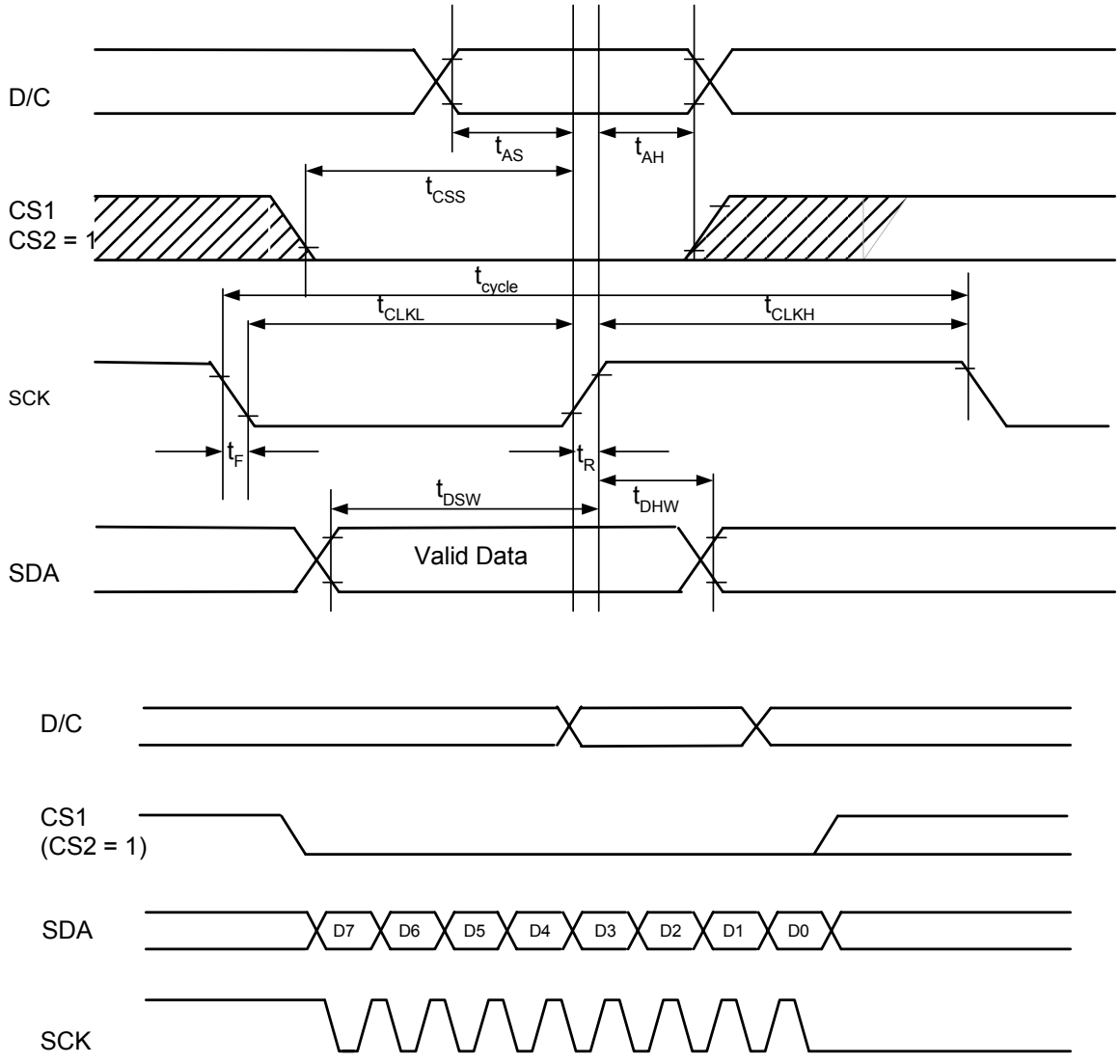
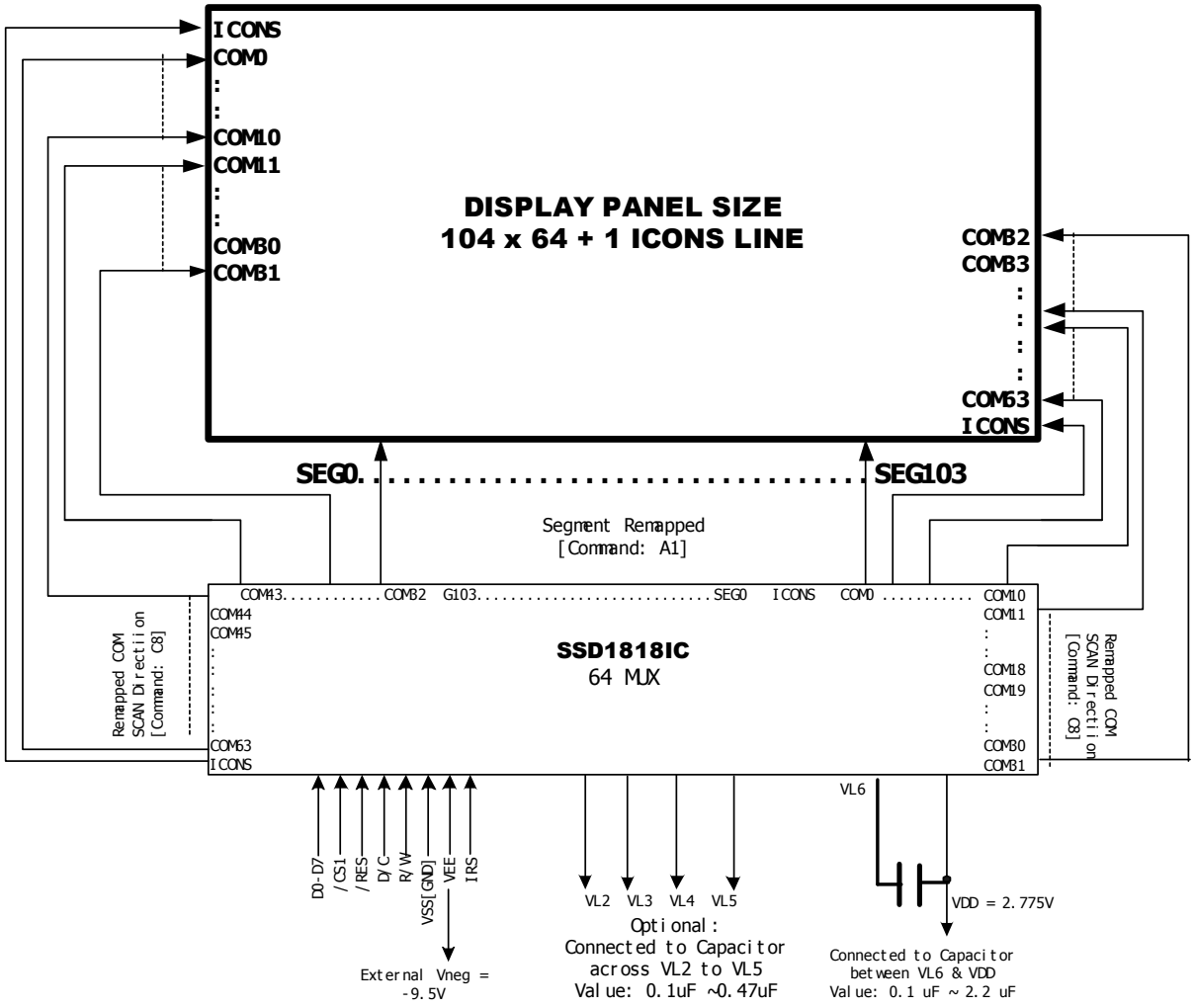


Figure 11 - Serial Interface Characteristics

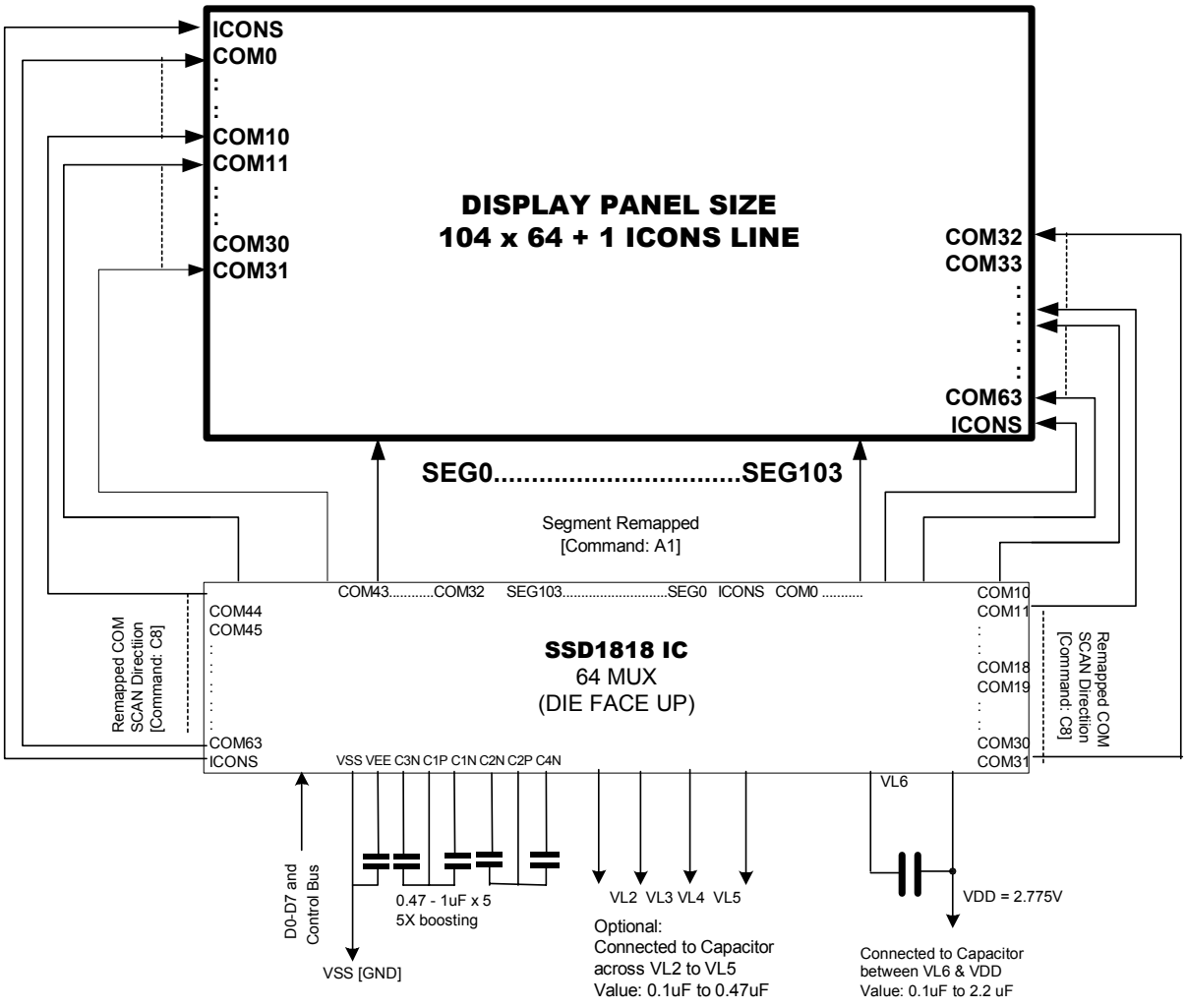
APPLICATION EXAMPLES



Logic pin connections not specified above:

Pins connected to VDD: CS2, E/$\overline{RD}$, M/$\overline{S}$, CLS, C68/$\overline{80}$, P/$\overline{S}$, $\overline{HPM}$
Pins connected to VSS: VSS1
Pins floating: $\overline{DOF}$, CL

Figure 12 - Application Circuit of 104 x 64 plus an icon line using SSD1818, configured with: external VEE, internal regulator, divider mode enabled (Command: 2B), 6800-series MPU parallel interface, internal oscillator and master mode



Logic pin connections not specified above:

Pins connected to VDD: CS2, E/$\overline{RD}$, M/$\overline{S}$, CLS, C68/$\overline{80}$, P/$\overline{S}$, $\overline{HPM}$
Pins connected to VSS: VSS1

Pins floating: $\overline{DOF}$, CL

Figure 13 - Application Circuit of 104 x 64 plus an icon line using SSD1818, configured with all internal power control circuit enabled, 6800-series MPU parallel interface, internal oscillator and master mode.

Initialization Routine

	Command (Hex) (Refer to Figure 12: All internal power control circuit enable)	**Command (Hex)** (Refer to Figure 13: External V_{EE}, Internal regulator and divider enable)	**Description**
1	E2	E2	Software Reset
2	2F	2B	Set power control register
3	24	24	Set internal resistor gain = 24h
4	81 20	81 20	Set contrast level = 20h
5	D6 2D	D6 2D	Enable band gap reference circuit Set band gap clock period = 128T
6	A0	A0	Set Column address is map to SEG0
7	C0	C0	Set Row address is map to COM0
8	A4	A4	Set entire display on/off = Normal display
9	A6	A6	Set normal / reverse display = Normal display
10	AF	AF	Set Display On
Example	Internal booster, regulator and divider are enabled. V_{OP} = approx. -8.527V with reference to V_{DD}	External booster, Internal regulator and divider are enabled. V_{OP} = approx. -8.546V with reference to V_{DD}	