S75NSI28NDE Based MCPs

1.8 Volt-only, Stacked Multi-Chip Product (MCP) x16 MirrorBit™ Flash Memory and DRAM

128 Mb Multiplexed, Simultaneous Read/Write, Burst Mode Code Flash Memory
256 Mb Multiplexed, Burst Mode Data Flash Memory
128 Mb SDR DRAM

Data Sheet

ADVANCE INFORMATION

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Publication Number S75NSI28NDE_00 **Revision** A **Amendment** 2 **Issue Date** September 23, 2005

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Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

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S75NSI28NDE based MCPs

1.8 Volt-only, Stacked Multi-Chip Product (MCP) xI6 MirrorBit™ Flash Memory and DRAM

I28 Mb Multiplexed, Simultaneous Read/Write, Burst Mode Code Flash Memory
256 Mb Multiplexed, Burst Mode Data Flash Memory
I28 Mb SDR DRAM

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

MCP Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speed**
  - — Flash = 66MHz, 80MHz
  - — DRAM = 133MHz
- **Packages:**
  - — 11.0 x 10.0 x 1.0 mm 133-ball FBGA
- **Operating Temperature**
  - — -25°C to +85°C

General Description

The S75NS Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of

- NS family multiplexed 110-nm Code Flash memory die
- KS family multiplexed 110-nm Data Flash memory die
- SDR DRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to the individual data sheets (included in this document) for further details

SDR DRAM DENSITY = 128M

		Data Flash Density		
		128 Mb	**256 Mb**	**512 Mb**
Code Flash Density	128 Mb		S75NS128NDE	
	256 Mb			
	512 Mb			

Product Selector Guide

Device/ Model#	Code Flash Density	Data Flash Density	DRAM Density	Flash Speed (MHz)	DRAM Speed (MHz)	Supplier	Package
S75NS128NDE-NK	128 Mb	256 Mb	128 Mb	66	133	DRAM Type 1	NMA133MCP
S75NS128NDE-NJ				80			

S75NSI28NDE Based MCPs

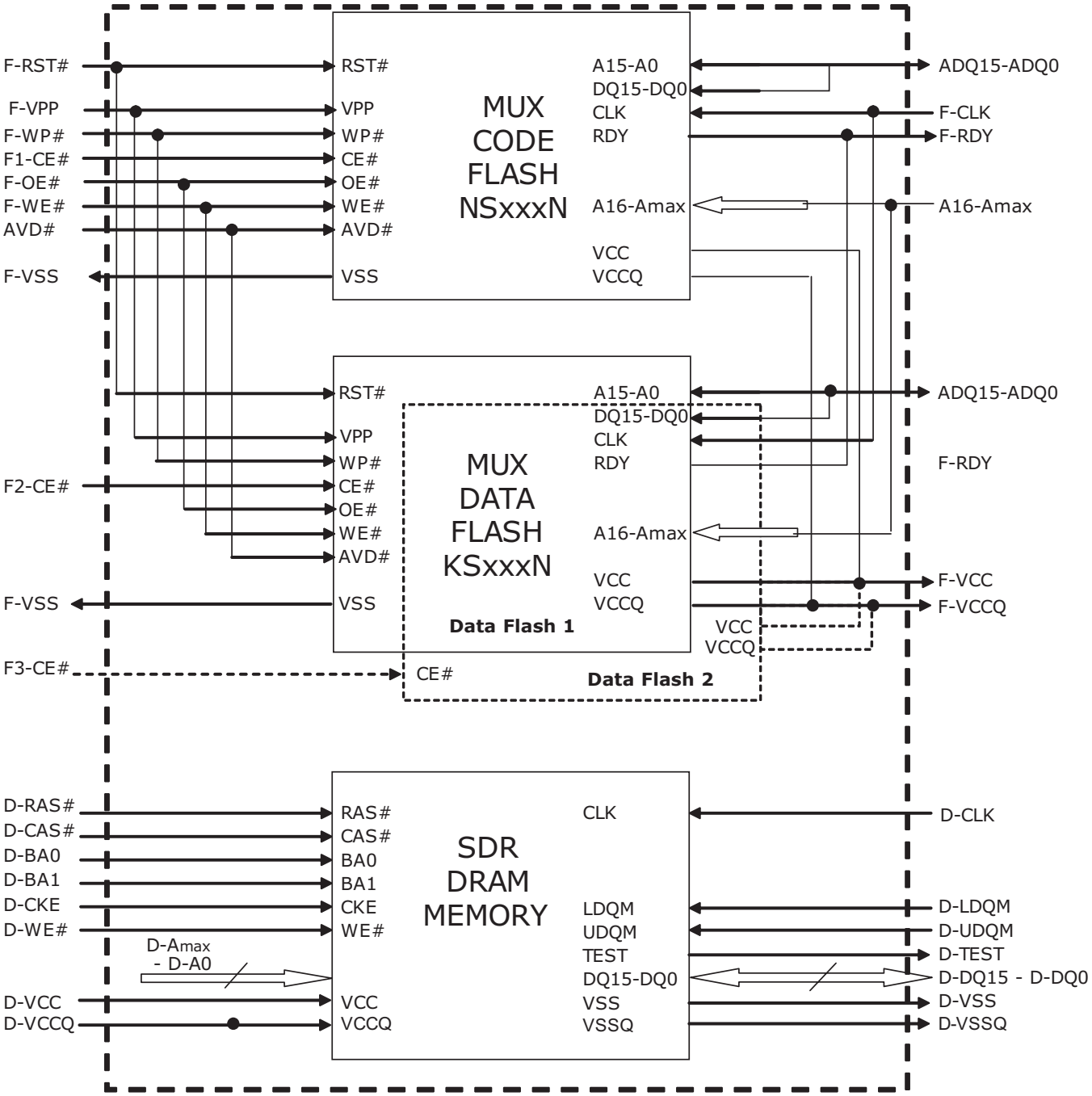
S29NS-N MirrorBit™ Flash Module

Mobile SDRAM Type I

S99KS256N MirrorBit™ Flash Family

MCP Revision Summary

MCP Block Diagrams

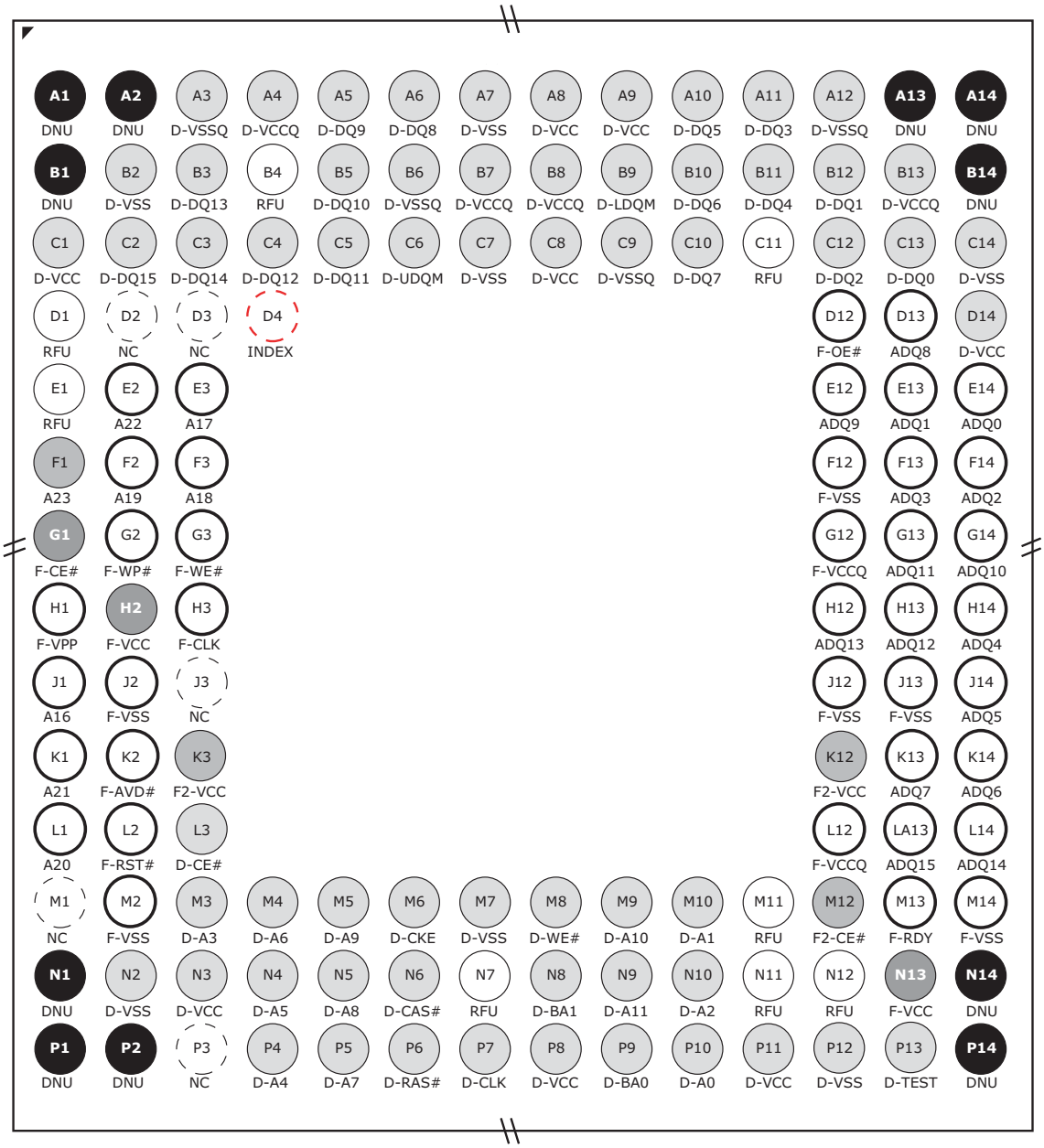


Notes:

1. *Amax indicates highest address bit for memory component:*
   a. Amax = A23 for NS128N, A23 for KS128N
   b. Amax = A11 for 128 Mb DDR DRAM
2. *For Flash, A0-A15 is tied to DQ0 – DQ15.*

Connection Diagrams

l28 Mb Code Flash + 256 Mb Data Flash +l28 Mb SDR SDRAM Pinout



Legend

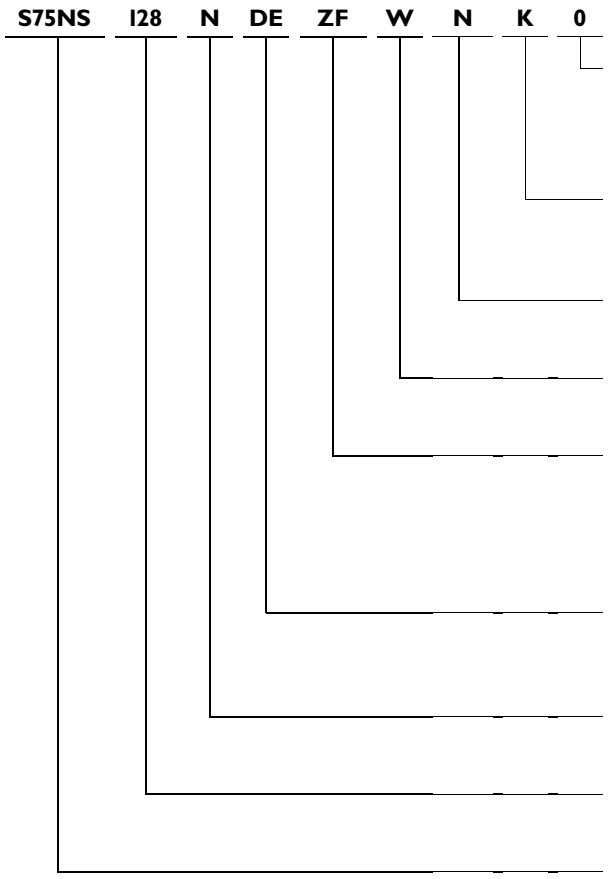
- Do Not Use
- Code Flash Only
- Data Flash Only
- Flash Shared
- DRAM Only
- Reserved for Future Use
- No Connect
- Index Location

Input/Output Descriptions

A23–A0	=	Flash Address inputs
DQ15–DQ0	=	Flash Data input/output
F1-CE#	=	Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.
F2-CE#	=	Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.
F3-CE#	=	Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.
F-OE#	=	Flash Output Enable input. Asynchronous relative to CLK for Burst mode.
F-WE#	=	Flash Write Enable input.
F-VCC	=	Flash device power supply (1.7 V - 1.95V).
F-VCCQ	=	Flash Input/Output Buffer power supply.
F-VSS	=	Flash Ground
F-RDY	=	Flash ready output. Indicates the status of the Burst read. VOL = data valid.
F-CLK	=	Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
F-AVD#	=	Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. VIL = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. VIH= device ignores address inputs
F-RST#	=	Flash hardware reset input. VIL= device resets and returns to reading array data
F-WP#	=	Flash hardware write protect input. VIL = disables program and erase functions in the four outermost sectors.
F-VPP	=	Flash accelerated input. At VHH, accelerates programming; automatically places device in unlock bypass mode. At VIL, disables all program and erase functions. Should be at VIH for all other conditions.
D-A11–D-A0	=	DRAM Address inputs
D-DQ15–D-DQ0	=	DRAM Data input/output
D-CLK	=	DRAM System Clock
D-CE#	=	DRAM Chip Select
D-CKE	=	DRAM Clock Enable
D-BA1-BA0	=	DRAM Bank Select
D-RAS#	=	DRAM Row Address Strobe
D-CAS#	=	DRAM Column Address Strobe
D-DM1–D-DM0	=	DRAM Data Input/Output Mask
D-WE#	=	DRAM Write Enable input
D-VSSQ	=	DRAM Input/Output Buffer ground
D-VCCQ	=	DRAM Input/Output Buffer power supply
D-VCC	=	DRAM device power supply
D-UDQS	=	DRAM Upper Data Strobe, output with read data and input with write data
D-LDQS	=	DRAM Lower Data Strobe, output with read data and input with write data
D-CLK#	=	DDR Clock for negative edge of CLK
RFU	=	Reserved for Future Use
NC	=	No Connect
D-TEST	=	Internal Test mode pin for DDR DRAM only. Do not apply any signal on this pin

Ordering Information

The order number (Valid Combination) is formed by the following:



PACKING TYPE
0 = Tray
2 = 7" Tape and Reel
3 = 13" Tape and Reel

MODEL NUMBER
K = DRAM Type 1, 66MHz Flash/133MHz DRAM
J = DRAM Type 1, 80MHz Flash/133MHz DRAM

PACKAGE MODIFIER
N = SDR DRAM, 133-ball, 11x10 mm, FBGA Multi-Chip Package

TEMPERATURE RANGE
W = Wireless (–25°C to +85°C)

PACKAGE TYPE
ZF = Thin profile Fine-pitch BGA Pb-free package (0.5mm pitch, 1.02 mm height)
ZJ = Thin profile Fine-pitch BGA Pb-free (LF35) package (0.5mm pitch, 1.02 mm height)

DRAM AND DATA FLASH DENSITY
DE = 128 Mb DRAM, 256Mb Data Flash
D0 = 128 Mb DRAM, No Data Flash

PROCESS TECHNOLOGY
N = 110 nm, MirrorBit™ Technology

CODE FLASH DENSITY
128 = 128 Mb

PRODUCT FAMILY
S75NS Multi-chip Product (MCP)
1.8 V Multiplexed, SRW, Burst Mode Code Flash
1.8V Multiplexed, Burst Mode Data Flash
SDR DRAM on Split Bus

NS256N + I28 Mb DDR DRAM		Flash Speed (MHz)	DRAM Speed (MHz)	Temperature Range	Material Set	Supplier
Ordering Number	Package Marking					
S75NS128NDEZFWNK	75NS128NDEZFWNK	66	133	-25°C to 85°C	LF	DRAM Type 1
S75NS128NDEZFWNJ	75NS128NDEZFWNJ	80				DRAM Type 1
S75NS128NDEZJWNK	75NS128NDEZJWNK	66	133	-25°C to 85°C	LF35	DRAM Type 1
S75NS128NDEZJWNJ	75NS128NDEZJWNJ	80				DRAM Type 1

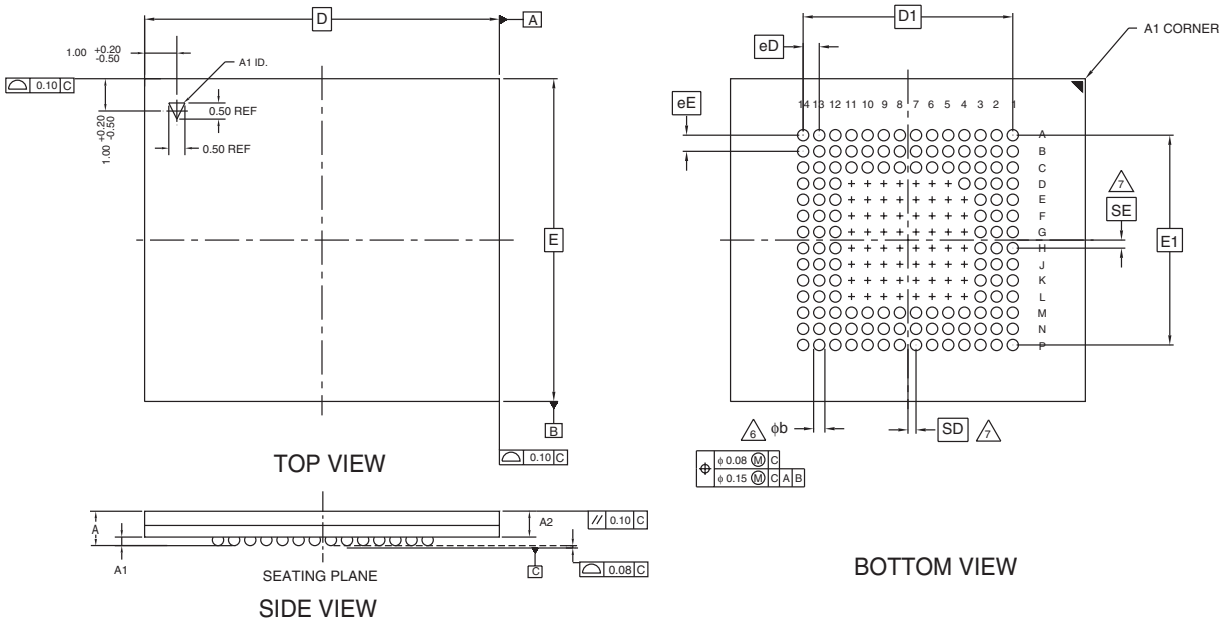
Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*
3. *For specifications, refer to the CellularRam 2A module.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Physical Dimensions

NMAI33 - Thin profile Fine-pitch Ball Grid Array (BGA) MCP II x I0 mm



PACKAGE	NMA 133			
JEDEC	N/A			
D x E	11.00 mm x 10.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	1.10	1.20	1.30	PROFILE
A1	0.20	0.25	0.30	BALL HEIGHT
A2	0.90	0.96	1.02	BODY THICKNESS
D	10.9	11.00	11.10	BODY SIZE
E	9.90	10.00	10.10	BODY SIZE
D1	6.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	133			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SE / SD	0.25 BSC.			SOLDER BALL PLACEMENT
	D5-D11,E4-E11,F4-F11 G4-G11, H4-H11, J4-J11 K4-K11,L4-L11			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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S29NS-N MirrorBit™ Flash Module

S29NS256N, S29NSI28N
256/128 Megabit (16/8M x 16-bit), CMOS 1.8 Volt-only Simultaneous Read/Write, Multiplexed, Burst Mode Flash Memory

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

- **Single 1.8 volt read, program and erase (1.70 to 1.95 volt)**
- **VersatileIO™ Feature**
  - Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{CCQ} pin
  - 1.8 V compatible I/O signals
- **Multiplexed Data and Address for reduced I/O count**
  - A15–A0 multiplexed as DQ15–DQ0
  - Addresses are latched by AVD# control input when CE# low
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- **Read access times at 80/66 MHz**
  - Burst access times of 9/11 ns at industrial temperature range
  - Asynchronous random access times of 80 ns
  - Synchronous random access times of 80 ns
- **Burst length**
  - Continuous linear burst
  - 8/16/32 word linear burst with wrap around
  - 8/16/32 word linear burst without wrap around
- **Secured Silicon Sector region**
  - 256 words accessible through a command sequence, 128 words for the Factory Secured Silicon Sector and 128 words for the Customer Secured Silicon Sector.
- **Power dissipation (typical values, 8 bits switching, C_L = 30 pF) @80 MHz**
  - Continuous Burst Mode Read: 35 mA
  - Simultaneous Operation: 50 mA
  - Program/Erase: 19 mA
  - Standby mode: 20 µA
- **Sector Architecture**
  - Four 16 K word sectors in upper-most address range
  - Two-hundred-fifty-five 64Kword sectors (S29NS256N) and One-hundred-twenty-seven 64 Kword sectors (S29NS128N)
  - Sixteen banks (S29NS128N and S29NS256N)
- **High Performance**
  - Typical word programming time of 40 µs
  - Typical effective word programming time of 9.4 µs utilizing a 32-Word Write Buffer at Vcc Level
  - Typical effective word programming time of 6 µs utilizing a 32-Word Write Buffer at V_{PP} Level
  - Typical sector erase time of 350 ms for 16 Kword sectors and 800 ms sector erase time for 64 Kword sectors

Security features

- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors to prevent program or erase operations within that sector using a user-defined 64-bit password
- **Hardware Sector Protection**
  - WP# protects the two highest sectors
  - All sectors locked when $V_{PP} = V_{IL}$
- **Handshaking feature**
  - Provides host system with minimum possible latency by monitoring RDY
- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
  - Backwards compatible with Am29F and Am29LV families
- **Manufactured on 110 nm MirrorBit™ process technology**
- **Cycling endurance: 100,000 cycles per sector typical**
- **Data retention: 20 years typical**
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation

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- **Program Suspend/Resume**
  - Suspends a programming operation to read data from a sector other than the one being programmed, then resume the programming operation
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

General Description

The S29NS256N and S29NS128N are 256 Mb, and 128 Mb (respectively) 1.8 Volt-only, Simultaneous Read/Write, Burst Mode Flash memory devices, organized as 16,777,216, 8,388,608, and 4,194,304 words of 16 bits each. These devices use a single V_{CC} of 1.70 to 1.95 V to read, program, and erase the memory array. A 9.0-volt V_{PP}, may be used for faster program performance if desired. These devices can also be programmed in standard EPROM programmers.

The devices are offered at the following speeds:

Clock Speed	Burst Access (ns)	Synch. Initial Access (ns)	Asynch. Initial Access (ns)	Output Loading
80 MHz	9	80	80	30 pF
66 MHz	11.0	80	80	

The devices operate within the temperature range of −25 °C to +85 °C, and are offered in Very Thin FBGA packages.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into sixteen banks. The device allows a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.The devices are structured as shown in the following tables:

S29NS256N			
Bank 0-14 Sectors		**Bank 15 Sectors**	
Quantity	**Size**	**Quantity**	**Size**
240	64 Kwords	4	16 Kwords
		15	64 Kwords
240 Mb total		16 Mb total	

S29NS128N			
Bank 0-14 Sectors		**Bank 15 Sectors**	
Quantity	**Size**	**Quantity**	**Size**
120	64 Kwords	4	16 Kwords
		7	64 Kwords
120 Mb total		8 Mb total	

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{CCQ} pin.

The devices use Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the devices additionally require Ready (RDY) and Clock (CLK). This implementation allows easy interface with minimal glue logic to microprocessors/microcontrollers for high performance read operations.

The devices offer complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device are similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bit** DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The devices are fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The devices also offer three types of data protection at the sector level. **Persistent Sector Protection** provides in-system, command-enabled protection of any combination of sectors using a single power supply at V_{CC}. **Password Sector Protection** prevents unauthorized write and erase operations in any combination of sectors through a user-defined 64-bit password. When at V_{IL}, **WP#** locks the highest two sectors. Finally, when V_{PP} is at V_{IL}, all sectors are locked.

The devices offer two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster program times by requiring only two write cycles to program data instead of four. Additionally, **Write Buffer Programming** is available on this family of devices. This feature provides superior programming performance by grouping locations being programmed.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm - an internal algorithm that automatically preprograms the array (if it is not already fully programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The **Program Suspend/Program Resume** feature enables the user to put program on hold to read data from any sector that is not selected for programming. If a read is needed from the Persistent Protection area, Dynamic Protection area, or the CFI area, after an program suspend, then the user must use the proper command sequence to enter and exit this region. The program suspend/resume functionality is also available when programming in erase suspend (1 level depth only).

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Persistent Protection area, Dynamic Protection area, or the CFI area, after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a memory array program or erase operation is complete by using the device status bit DQ7 (Data# Polling), DQ6/DQ2 (toggle bits), DQ5 (exceeded timing limit), DQ3 (sector erase start timeout state indicator), and DQ1 (write to buffer abort). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. **The device is fully erased when shipped from the factory**.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers two types of data protection at the sector level. When at V_{IL}, **WP#** locks the two outermost boot sectors at the top of memory.

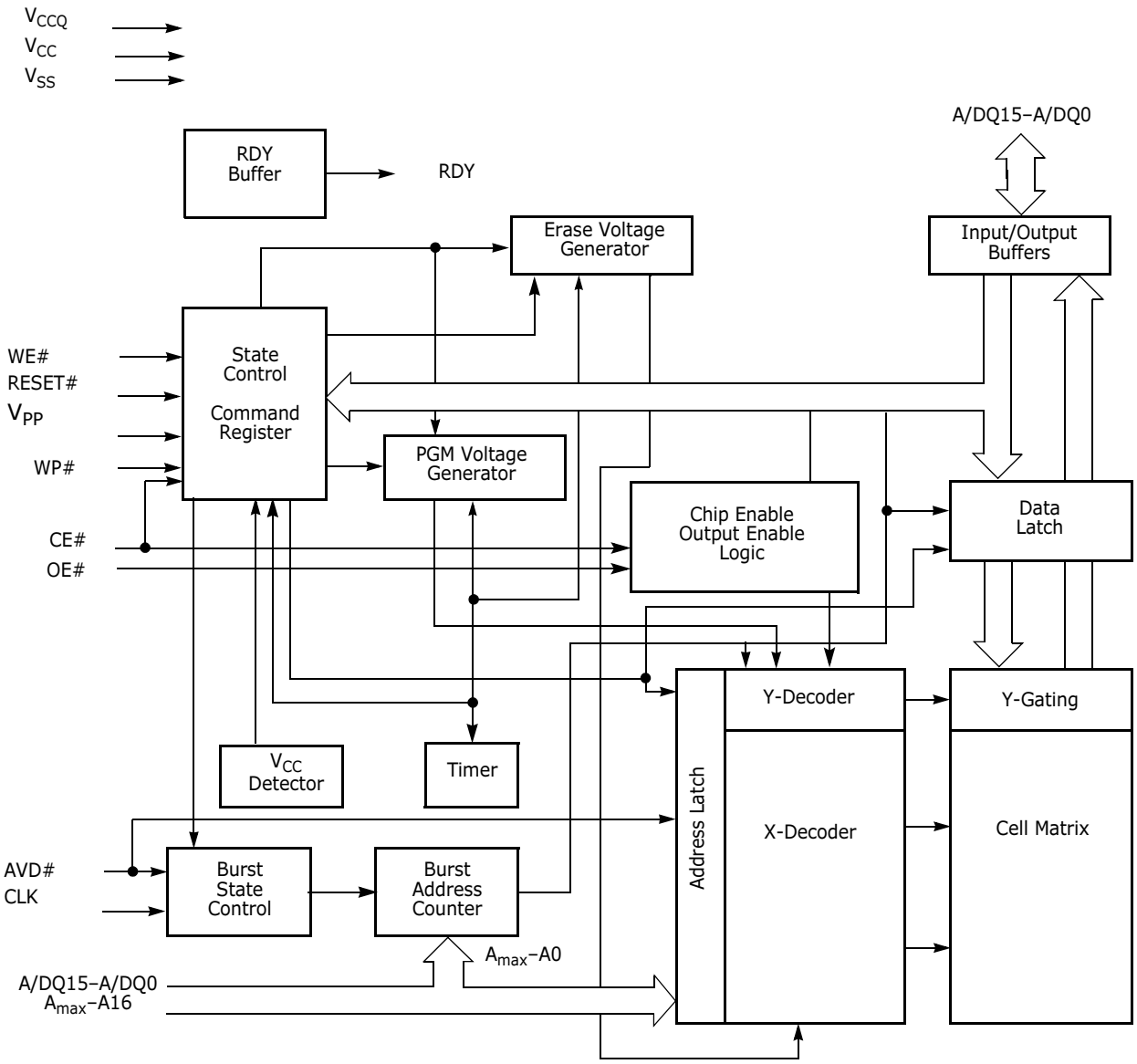
When the V_{PP} pin = V_{IL}, the entire flash memory array is protected.

Spansion LLC Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector. The data is programmed using hot electron injection.

Product Selector Guide

Description	**S29NS256N, S29NS128N**	
Burst Frequency	**80 MHz**	**66 MHz**
Max Initial Synchronous Access Time, ns (T_{IACC})	80	80
Max Burst Access Time, ns (T_{BACC})	9	11.0
Max Asynchronous Access Time, ns (T_{ACC})	80	80
Max CE# Access Time, ns (T_{CE})		
Max OE# Access Time, ns (T_{OE})	9	11.0

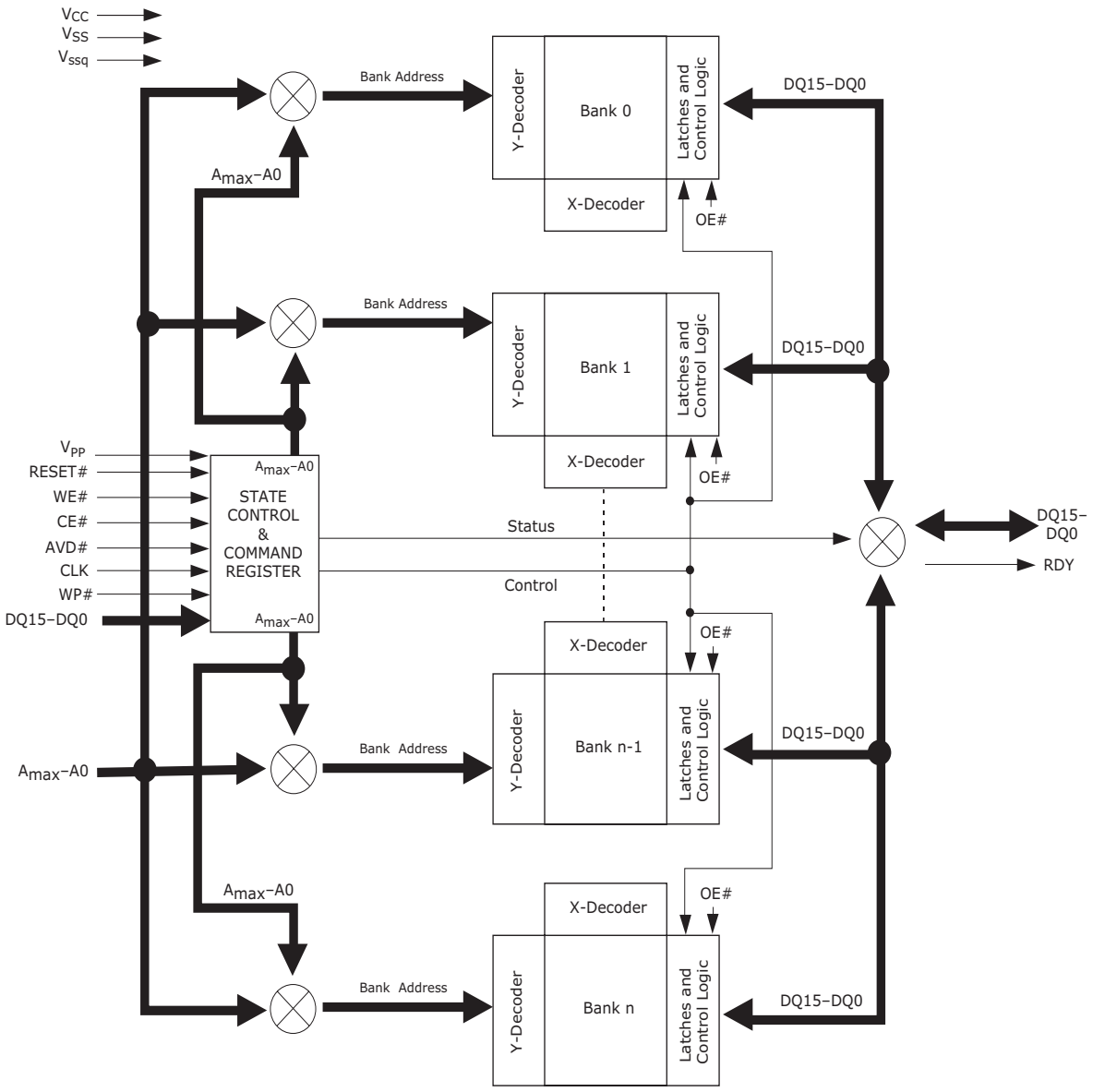
Block Diagram



Notes:

4. A_{max} indicates the highest order address bit. A_{max} equals A23 for NS256N, and A22 for NS128N.

Block Diagram of Simultaneous Operation Circuit



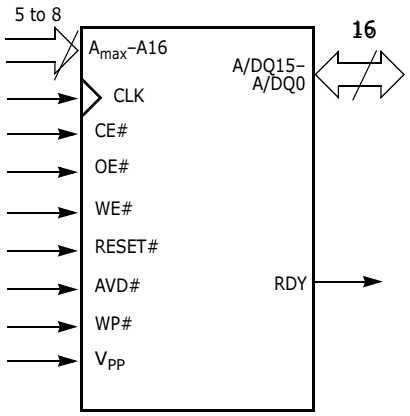
Notes:

1. *A15–A0 are multiplexed with DQ15–DQ0.*
2. *Amax indicates the highest order address bit. A23 (NS256N), and A22 (NS128N).*
3. *n = 15 for NS256N and NS128N.*

Input/Output Descriptions

A23–A16	=	Address Inputs, S29NS256N
A22–A16	=	Address Inputs, S29NS128N
A/DQ15–A/DQ0	=	Multiplexed Address/Data input/output
CE#	=	Chip Enable Input. Asynchronous relative to CLK for the Burst mode.
OE#	=	Output Enable Input. Asynchronous relative to CLK for the Burst mode.
WE#	=	Write Enable Input.
V_{CC}	=	Device Power Supply (1.70 V–1.95 V).
V_{CCQ}	=	Input/Output Power Supply (1.70 V–1.95 V).
V_{SS}	=	Ground
V_{SSQ}	=	Input/Output Ground
NC	=	No Connect; not connected internally
RDY	=	Ready output; indicates the status of the Burst read. V_{OL}= data invalid. V_{OH} = data valid.
CLK	=	The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
AVD#	=	Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15–A0 are multiplexed, address bits Amax–A16 are address only). V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs
RESET#	=	Hardware reset input. V_{IL}= device resets and returns to reading array data
WP#	=	Hardware write protect input. V_{IL} = disables writes to SA257–258 (S29NS256N), or SA129–130 (S29NS128N). Should be at V_{IH} for all other conditions.
V_{PP}	=	At 9 V, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions.

Logic Symbol



A_{max} indicates the highest order address bit.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table I. Device Bus Operations

Operation	CE#	OE#	WE#	A_{max}–16	A/DQ15–0	RESET#	CLK	AVD#
Asynchronous Read	L	L	H	Addr In	I/O	H	L	
Write	L	H	L	Addr In	I/O	H	H/L	
Standby (CE#)	H	X	X	X	HIGH Z	H	H/L	X
Hardware Reset	X	X	X	X	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	H	H	Addr In	Addr In	H		
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	X	Burst Data Out	H		H
Terminate current Burst read cycle	H	X	H	X	HIGH Z	H		X
Terminate current Burst read cycle via RESET#	X	X	H	X	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	H	H	X	I/O	H		

Legend: *L = Logic 0, H = Logic 1, X = Don't Care.*

VersatileIO™ (V_{IO}) Control

The VersatileIO (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{CCQ} pin.

Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must assert a valid address on A_{max}–A16 and A/DQ15–A/DQ0 while AVD# and CE# are at V_{IL}. WE# should remain at V_{IH}. Note that CLK must remain at V_{IL} during asynchronous read operations. The rising edge of AVD# latches the address, after which the system can drive OE# to V_{IL}. The data will appear on A/DQ15–A/DQ0. (See Figure 14, on page 80.) Since the memory array is divided into banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

Requirements for Synchronous (Burst) Read Operation

The device is capable of seven different burst read modes: continuous burst read; 8-, 16-, and 32-word linear burst reads with wrap around; and 8-, 16-, and 32-word linear burst reads without wrap around.

Continuous Burst

When the device first powers up, it is enabled for asynchronous read operation. The device is automatically enabled for burst mode and addresses are latched on the first rising edge of CLK input, while AVD# is held low for one clock cycle.

Prior to activating the clock signal, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst session. The system would then write the Set Configuration Register command sequence.

The initial word is output t_{IACC} after the rising edge of the first CLK cycle. Subsequent words are output t_{BACC} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. **Note that the device has a fixed internal address boundary that occurs every 128 words, starting at address 00007Fh. The transition from the highest address 7FFFFFh to 000000h is also a boundary crossing**. During a boundary crossing, there is a no additional latency between the valid read at address 00007F and the valid read at address 000080 (or between addresses offset from these values by the same multiple of 128 words) for frequencies equal to or lower than 66 Mhz. For frequencies higher than 66 Mhz, there is a latency of 1 cycle.

During the time the device is outputting data with the starting burst address not divisible by four, additional waits are required. The RDY output indicates this condition to the system by deasserting.

Table 2 through Table 5 shows the address latency as a function of variable wait states.

Table 2. Address Latency for 7, 6, and 5 Wait States

Word										
0	7, 6, and 5 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	**1 ws**	D4	D5	D6	D7	D8
2		D2	D3	**1 ws**	**1 ws**	D4	D5	D6	D7	D8
3		D3	**1 ws**	**1 ws**	**1 ws**	D4	D5	D6	D7	D8

Table 3. Address Latency for 4 Wait States

Word										
0	4 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	**1 ws**	D4	D5	D6	D7	D8	D9
3		D3	**1 ws**	**1 ws**	D4	D5	D6	D7	D8	D9

Table 4. Address Latency for 3 Wait States

Word										
0	3 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	**1 ws**	D4	D5	D6	D7	D8	D9	D10

Table 5. Address Latency for 2 Wait States

Word										
0	2 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	D4	D5	D6	D7	D8	D9	D10	D11

Table 6 through Table 9 show the address/boundary crossing latency for variable wait state if a boundary crossing occurs during initial access

Table 6. Address/Boundary Crossing Latency for 7, 6, and 5 Wait States

Word										
0	7, 6, and 5 ws	D0	D1	D2	D3	**1 ws**	D4	D5	D6	D7
1		D1	D2	D3	**1 ws**	**1 ws**	D4	D5	D6	D7
2		D2	D3	**1 ws**	**1 ws**	**1 ws**	D4	D5	D6	D7
3		D3	**1 ws**	**1 ws**	**1 ws**	**1 ws**	D4	D5	D6	D7

Table 7. Address/Boundary Crossing Latency for 4 Wait States

Word										
0	4 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	**1 ws**	D4	D5	D6	D7	D8
2		D2	D3	**1 ws**	**1 ws**	D4	D5	D6	D7	D8
3		D3	**1 ws**	**1 ws**	**1 ws**	D4	D5	D6	D7	D8

Table 8. Address/Boundary Crossing Latency for 3 Wait States

Word										
0	3 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	**1 ws**	D4	D5	D6	D7	D8	D9
3		D3	**1 ws**	**1 ws**	D4	D5	D6	D7	D8	D9

Table 9. Address/Boundary Crossing Latency for 2 Wait States

Word										
0	2 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	**1 ws**	D4	D5	D6	D7	D8	D9	D10

The device will continue to output continuous, sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system asserts CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 1 on page 18. The reset command does *not* terminate the burst read operation.

If the host system crosses a 128 word line boundary while reading in burst mode, and the device is not programming or erasing, no additional latency will occur as described above. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide asynchronous read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

8-, 16-, and 32-Word Linear Burst with Wrap Around

These three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 10.)

Table I0. Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h, 18-1Fh...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh, 30-3Fh...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh, 60-7Fh...

As an example: if the starting address in the 8-word mode is 3Ah, and the burst sequence would be 3A-3B-3C-3D-3E-3F-38-39h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wraps back to the first address in the selected address group and terminates the burst read. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 128 words; thus, no wait states are inserted (except during the initial access).**

8-, 16-, and 32-Word Linear Burst without Wrap Around

In these modes, a fixed number of words (predefined as 8, 16, or 32 words) are read from consecutive addresses starting with the initial word, which is written to the device. When the address is at the end of the group address range (see Burst Address Groups Table), the burst read operation stops and the RDY output goes low. There is no group limitation and is different from the Linear Burst with Wrap Around.

As an example, for 8-word length Burst Read, if the starting address written to the device is 3A, the burst sequence would be 3A-3B-3C-3D-3E-3F-40-41h, and the read operation will be terminated after all eight words. The 16-word and 32-word modes would operate in a similar fashion

and continuously read to the predefined 16 or 32 words accordingly. **Note: In this burst read mode, the address pointer may cross the boundary that occurs every 128 words.**

Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after AVD# is driven active before data will be available. Upon power up, the device defaults to the maximum of seven total cycles. The total number of wait states is programmable from two to seven cycles. For further details, see "Set Configuration Register Command Sequence".

Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, burst length, RDY configuration, and synchronous mode active.

Handshaking Feature

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the configuration register to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in one of the other banks of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 23, on page 88 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-program and read-while-erase current specifications.

Writing Commands/Command Sequences

The device has inputs/outputs that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 14-17 indicates the address space that each sector occupies. The device address space is divided into multiple banks. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "sector address" is the address bits required to uniquely select a sector.

Refer to the DC Characteristics table for write mode current specifications. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program and Erase Operations

The device offers accelerated program and erase operation through the V_{PP} function. V_{PP} is primarily intended to allow faster manufacturing throughput at the factory and not to be used in system operations.

If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program and erase operations. The system can then use the abbreviated Embedded Programming

command and Write Buffer Load command sequence provided by the Unlock Bypass mode. Note that if a "Write-to-Buffer-Abort Reset" is required while in Unlock Bypass mode, the **full 3-cycle RESET command sequence must be used to reset the device**. Removing V_{HH} from the V_{PP} input, upon completion of the embedded program or erase operation, returns the device to normal operation. Note that sectors must be unlocked prior to raising V_{PP} to V_{HH}. *Note that the V_{PP} pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the V_{PP} pin must not be left floating or unconnected; inconsistent behavior of the device may result*.

When at V_{IL}, V_{PP} locks all sectors. V_{PP} should be at V_{IH} for all other conditions.

Write Buffer Programming Operation

Write Buffer Programming allows the system to write a maximum of **32** words in one programming operation. This results in a faster effective word programming time than the standard "word" programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. At this point, the system writes the number of "**word locations minus 1**" that will be loaded into the page buffer at the Sector Address in which programming will occur. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the "Program Buffer to Flash" confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. (NOTE: The number loaded = the number of locations to program minus 1. For example, if the system will program 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the "write-buffer-page" address. All subsequent address/data pairs **must** fall within the "selected-write-buffer-page", and be loaded in sequential order.

The "write-buffer-page" is selected by using the addresses A_{MAX}-A5 where A_{MAX} is A23 for S29NS256N, and A22 for S29NS128N.

The "write-buffer-page" addresses **must be the same for all address/data pairs loaded into the write buffer**. (This means Write Buffer Programming **cannot** be performed across multiple "write-buffer-pages". This also means that Write Buffer Programming **cannot** be performed across multiple sectors. If the system attempts to load programming data outside of the selected "write-buffer-page", the operation will ABORT.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer. Write buffer locations must be loaded in sequential order.

Note that if a Write Buffer address location is loaded multiple times, the "address/data pair" counter **will be decremented for every data load operation**. Also, the **last data loaded** at a location before the "Program Buffer to Flash" confirm command will be programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements **for each data load operation**, **NOT for each unique write-buffer-address location**.

Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" command at the Sector Address. Any other address/data write combinations will abort the Write Buffer Programming operation. The device will then "go busy". The Data Bar polling techniques should be used while monitoring the **last address location loaded into the write buffer**. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then data bar poll at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer "embedded" programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device will return to READ mode.

The Write Buffer Programming Sequence can be ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the "Number of Locations to Program" step.
- Write to an address in a sector different than the one specified during the "Write-Buffer-Load" command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the "Starting Address" during the "write buffer data loading" stage of the operation.
- Write data other than the "Confirm Command" after the specified number of "data load" cycles.

The ABORT condition is indicated by DQ1 = 1, DQ7 = DATA# (for the "last address location loaded"), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A "Write-to-Buffer-Abort reset" command sequence is required when using the Write-Buffer-Programming features in Unlock Bypass mode. **Note: The Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress**.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed. Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. However, programming the same word address multiple times without intervening erases requires a modified programming method. Please contact your local Spansion™ representative for details.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output from the internal register (which is separate from the memory array) on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. The autoselect codes can also be accessed in-system.

When verifying sector protection, the sector address must appear on the appropriate highest order address bits. The remaining address bits are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0. The autoselect codes can also be accessed in-system through the command register. The command sequence is illustrated in Table , "," on page 62. *Note that if a Bank Address (BA) on address bits A23, A22, A21, and A20 for the NS256N, A22, A21, A20, and A19 for the NS128N, is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes, the host system must issue the autoselect command via the command register, as shown in Table , "," on page 62.

Advanced Sector Protection and Unprotection

This advanced security feature provides an additional level of protection to all sectors against inadvertent program or erase operations.

The advanced sector protection feature disables both programming and erase operations in any sector while the advanced sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented using either of the two methods

- Hardware method
- Software method

Persistent/Password Sector Protection is achieved by using the software method while the sector protection with WP# pin is achieved by using the hardware method.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used.

- Persistent Mode Lock Bit
- Password Mode Lock Bit

If the customer decides to continue using the Persistent Sector Protection method, they must set the **Persistent Mode Lock Bit**. This will permanently set the part to operate only using Persistent Sector Protection. However, if the customer decides to use the Password Sector Protection method, they must set the **Password Mode Lock Bit**. This will permanently set the part to operate only using Password Sector Protection.

It is important to remember that setting either the **Persistent Mode Lock Bit** or the **Password Mode Lock Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone. If both are selected to be set at the same time, the operation will abort.** This is done so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Sector Protection Mode.

The device is shipped with all sectors unprotected. Spansion offers the option of programming and protecting sectors at the factory prior to shipping the device through Spansion programming services. Contact an Spansion representative for details.

Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

- Persistent Sector Protection

A software enabled command sector protection method that replaces the old 12 V controlled protection method.

- Password Sector Protection

A highly sophisticated software enabled protection method that requires a password before changes to certain sectors or sector groups are permitted

- WP# Hardware Protection

A write protect pin (WP#) can prevent program or erase operations in the outermost sectors.The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Persistently Locked**—A sector is protected and cannot be changed.
- **Dynamically Locked**—The sector is protected and can be changed by a simple command
- **Unlocked**—The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of "bits" namely Persistent Protection Bit (PPB), Dynamic Protection Bit (DYB), and Persistent Protection Bit Lock (PPB Lock) are used to achieve the desired sector protection scheme:

Persistent Protection Bit (PPB)

PPB is used to as an advanced security feature to protect individual sectors from being programmed or erased thereby providing additional level of protection. Every sector is assigned a Persistent Protection Bit.

Each PPB is individually programmed through the **PPB Program Command**. However all PPBs are erased in parallel through the **All PPB Erase Command**. Prior to erasing, these bits don't have to be pre programmed. The Embedded Erase algorithm automatically preprograms and verifies prior to an electrical erase. The system is not required to provide any controls or timings during these operations.

The PPBs retain their state across power cycles because they are Non-Volatile. The PPBs has the same endurance as the flash memory.

Persistent Protection Bit Lock (PPB Lock Bit) in Persistent Sector Protection Mode

PPB Lock Bit is a global volatile bit and provides an additional level of protection to the sectors. When **programmed (set to "0")**, all the PPBs are locked and hence none of them can be changed. When **erased (cleared to "1")**, the PPBs are changeable. There is only one PPB Lock Bit in every device. Only a hardware reset or a power-up clears the PPB Lock Bit. It is to be noted that there is no software solution, i.e. command sequence to unlock the PPB Lock Bit.

Once all PPBs are configured to the desired settings, the PPB Lock Bit may be set (programmed to "0"). The PPB Lock Bit is set by issuing the PPB Lock Bit Set Command. Programming or setting the PPB Lock Bit disables program and erase commands to all the PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock Bit is to go through a hardware or powerup reset. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can disable the PPB Lock Bit to prevent any further changes to the PPBs during system operation.

Dynamic Protection Bit (DYB)

DYB is a security feature used to protect individual sectors from being programmed or erased inadvertently. It is a volatile protection bit and is assigned to each sector. Upon power-up or a hardware reset, the contents of all DYBs are set (programmed to "0"). Each DYB can be individually modified through the DYB Set Command or the DYB Clear Command.

The Protection Status for a particular sector is determined by the status of the PPB and the DYB relative to that sector. For the sectors that have the PPBs cleared (erased to "1"), the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Set or Clear command sequences, the DYBs will be set (programmed to "0") or cleared (erased to "1"), thus placing each sector in the protected or unprotected state respectively. These states are the so-called Dynamic Locked or Unlocked states due to the fact that they can switch back and forth between the protected and unprotected states. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set (programmed to "0") or cleared (erased to "1") as often as needed.

When the parts are first shipped, the PPBs are cleared (erased to "1") and upon power up or reset, the DYBs are set (programmed to "0"). The PPB Lock Bit defaults to the cleared state (erased to "1") after power up and the PPBs retain their previous state as they are non-volatile.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set or Clear command for the dynamic sectors signify protected or unprotected state of the sectors respectively. However, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again will lock the PPBs, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB Lock Bit Set command early in the boot code, and protect the boot code by holding WP# = V_{IL}. Note that the PPB and DYB bits have the same function when V_{PP} = V_{HH} as they do when V_{PP} = V_{IH}.

Table II. Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
1	1	1	Sector Unprotected
0	1	1	Sector Protected through DYB
1	0	1	Sector Protected through PPB
0	0	1	Sector Protected through PPB and DYB
1	1	0	Sector Unprotected
0	1	0	Sector Protected through DYB
1	0	0	Sector Protected through PPB
0	0	0	Sector Protected through PPB and DYB

Table 11 contains all possible combinations of the DYB, PPB, and PPB Lock relating to the status of the sector.

In summary, if the PPB is set (programmed to "0"), and the PPB Lock is set (programmed to "0"), the sector is protected and the protection can not be removed until the next power cycle clears (erase to "1") the PPB Lock Bit. Once the PPB Lock Bit is cleared (erased to "1"), the sector can be persistently locked or unlocked. Likewise, if both PPB Lock Bit or PPB is cleared (erased to "1") the sector can then be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program or erase command to a protected sector enables status polling and returns to read mode without having modified the contents of the protected sector.

The programming of the DYB, PPB, and PPB Lock for a given sector can be verified by writing individual status read commands DYB Status, PPB Status, and PPB Lock Status to the device.

Persistent Sector Protection Mode Lock Bit

A Persistent Mode Lock Bit exists to guarantee that the device remain in software sector protection. Once programmed (set to "0"), the Persistent Mode Lock Bit prevents programming of the Password Mode Lock Bit. This guarantees that now, a hacker cannot place the device in Password Sector Protection Mode.

Password Sector Protection

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection Mode and the Password Sector Protection Mode:

- When the device is first powered up, or comes out of a reset cycle, the **PPB Lock Bit is set to the locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock Bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a **one-time programmable (OTP)** region of the flash memory. Once the Password Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock Bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 1 µs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

64-bit Password

The 64-bit Password is located in a non-erasable region of the FLash and is accessible through the use of the Password Program and Verify commands (see "Password Protection Command Set Definitions" section on page 57). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Password Mode Lock Bit

In order to select the Password Sector Protection scheme, the customer must first program the password. Spansion LLC recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

- It permanently sets the device to operate using the Password Sector Protection Mode. It is not possible to reverse this function.
- It also disables *all further commands* to the password region. All program and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Sector Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Lock Bit, there will be no way to clear the PPB Lock Bit.

The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. **The Password Mode Lock Bit is not erasable.** Once Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

Persistent Protection Bit Lock (PPB Lock Bit) in Password Sector Protection Mode

The Persistent Protection Bit Lock (PPB Lock Bit) is a volatile bit that reflects the state of the Password Mode Lock Bit after power-up reset. If the Password Mode Lock Bit is also set, after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command to enter the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1".

If the Password Mode Lock Bit is not set (device is operating in the default Persistent Protection Mode). The Password Unlock command is ignored in Persistent Sector Protection Mode.

Hardware Data Protection Mode

The device offers two types of data protection at the sector level:

- When WP# is at V_{IL}, the two outermost sectors at the top are locked (device specific).
- When V_{PP} is at V_{IL}, all sectors are locked.
  SA257 and SA258 are locked (S29NS256N)
  SA129 and SA130 are locked (S29NS128N)

The write protect pin (WP#) adds a final level of hardware program and erase protection to the boot sectors. The boot sectors are the two sectors containing the highest set of addresses in these top-boot-configured devices. For the none boot option, the WP# hardware feature is not available. **When this pin is low it is not possible to change the contents of these top sectors.** These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the two outermost sectors. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the "top" boot sectors. If the system asserts V_{IH} on the WP# pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

WP# Boot Sector Protection

The WP# signal will be latched at a specific time in the embedded program or erase sequence. To prevent a write to the top two sectors, WP# must be asserted (WP#=V_{IL}) on the last write cycle of the embedded sequence (i.e., 4th write cycle in embedded program, 6th write cycle in embedded erase).

If selecting multiple sectors for erasure: The WP# protection status is latched only on the 6th write cycle of the embedded sector erase command sequence when the first sector is selected. If additional sectors are selected for erasure, they are subject to the WP# status that was latched on the 6th write cycle of the command sequence.

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Low VCC Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when VCC is greater than VLKO.

Write Pulse "Glitch" Protection

Noise pulses of less than t_{WEP} on WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up

Lock Register

The Lock Register consists of 3 bits. Each of these bits are non-volatile and read-only. DQ15-DQ3 are reserved and are undefined.

Table l2. Lock Register

DQ15-3	DQ2	DQ1	DQ0
Undefined	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC}. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enters this mode when addresses and clock remain stable for t_{ACC} + 20 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15 for the timing diagram.

V_{CC} Power-up and Power-down Sequencing

The device imposes no restrictions on V_{CC} power-up or power-down sequencing. Asserting RESET# to V_{IL} is required during the entire V_{CC} power sequence until the respective supplies reach their operating voltages. Once V_{CC} attains its operating voltage, de-assertion of RESET# to V_{IH} is permitted.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 words in length. All reads outside of the 256 word address range will return non-valid data. The Factory Indicator Bit (DQ7) is used to indicate whether or not the Factory Secured Silicon Sector is locked when shipped from the factory. The Customer Indicator Bit (DQ6) is used to indicate whether or

not the Customer Secured Silicon Sector is locked when shipped from the factory. The Factory Secured Silicon bits are permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN and customer code once the product is shipped to the field.

Spansion offers the device with a Factory Secured Silicon Sector that is locked and a Customer Secured Silicon Sector that is either locked or is lockable. The Factory Secured Silicon Sector is always protected when shipped from the factory, and has the Factory Indicator Bit (DQ7) permanently set to a "1". The Customer Secured Silicon Sector is shipped unprotected, allowing customers to utilize that sector in any manner they choose. Once the Customer Secured Silicon Sector area is protected, the Customer Indicator Bit will be permanently set to "1."

The system accesses the Secured Silicon Sector through a command sequence (see "Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence" section on page 49). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by sector SA0 of the memory array. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. While Secured Silicon Sector access is enabled, Memory Array read access, program operations, and erase operations to all sectors other than SA0 are also available. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

Factory Locked: Factor Secured Silicon Sector Programmed and Protected At the Factory

In a factory sector locked device, the Factory Secured Silicon Sector is protected when the device is shipped from the factory. The Factory Secured Silicon Sector cannot be modified in any way. The device is pre programmed with both a random number and a secure ESN. The Factory Secured Silicon Sector is located at addresses 000000h–00007Fh.

The device is available pre programmed with one of the following:

- A random, secure ESN only within the Factor Secured Silicon Sector
- Customer code within the Customer Secured Silicon Sector through the Spansion™ programming services
- Both a random, secure ESN and customer code through the Spansion™ programming services.

Table I3. Secured Silicon Sector Addresses

Sector	Sector Size	Address Range
Customer	128 words	000080h-0000FFh
Factory	128 words	000000h-00007Fh

Customers may opt to have their code programmed by Spansion through the Spansion™ programming services. Spansion programs the customer's code, with or without the random ESN. The devices are then shipped from Spansion's factory with the Factory Secured Silicon Sector and Customer Secured Silicon Sector permanently locked. Contact an Spansion representative for details on using Spansion's Spansion™ programming services.

Customer Secured Silicon Sector

If the security feature is not required, the Customer Secured Silicon Sector can be treated as an additional Flash memory space. The Customer Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (V_{PP}) and unlock bypass functions are not available when programming the Customer Secured Silicon Sector, but reading the first Bank through the last bank is available. The Customer Secured Silicon Sector is located at addresses 000080h–0000FFh.

The Customer Secured Silicon Sector area can be protected by writing the Secured Silicon Sector Protection Bit Lock command sequence.

Once the Customer Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing SA0 in the memory array.

The Customer Secured Silicon Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the Customer Secured Silicon Sector area and none of the bits in the Customer Secured Silicon Sector memory space can be modified in any way.

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 14–. To terminate reading CFI data, the system must write the reset command.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact the local sales representative for copies of these documents.

Table I4. CFI Query Identification String

Addresses	Data		Description
	S29NS256N	S29NS128N	
10h 11h 12h	0051h 0052h 0059h		Query Unique ASCII string "QRY"
13h 14h	0002h 0000h		Primary OEM Command Set
15h 16h	0040h 0000h		Address for Primary Extended Table
17h 18h	0000h 0000h		Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h		Address for Alternate OEM Extended Table (00h = none exists)

Table I5. System Interface String

Addresses	Data		Description
	S29NS256N	S29NS128N	
1Bh	0017h		V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h		V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h		V_{PP} Min. voltage (00h = no V_{PP} pin present) Refer to 4Dh
1Eh	0000h		V_{PP} Max. voltage (00h = no V_{PP} pin present) Refer to 4Eh
1Fh	0006h		Typical timeout per single byte/word write 2^N µs
20h	0009h		Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah		Typical timeout per individual block erase 2^N ms
22h	0000h		Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0003h		Max. timeout for byte/word write 2^N times typical
24h	0001h		Max. timeout for buffer write 2^N times typical
25h	0002h		Max. timeout per individual block erase 2^N times typical
26h	0000h		Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table I6. Device Geometry Definition

Addresses	Data		Description
	S29NS256N	S29NS128H	
27h	0019h	0018h	Device Size = 2^N byte
28h 29h	0001h 0000h		Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0006h 0000h		Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0002h		Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	00FEh 0000h 0000h 0002h	007Eh 0000h 0000h 0002h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	0003h 0000h 0080h 0000h		Erase Block Region 2 Information
35h 36h 37h 38h	0000h 0000h 0000h 0000h		Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h		Erase Block Region 4 Information

Table I7. Primary Vendor-Specific Extended Query (Sheet I of 3)

Addresses	Data		Description
	S29NS256N	S29NS128N	
40h 41h 42h	0050h 0052h 0049h		Query-unique ASCII string “PRI”
43h	0031h		Major version number, ASCII
44h	0034h		Minor version number, ASCII
45h	0010h		Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h		Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h		Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0000h		Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0008h		Sector Protect/Unprotect scheme 08 = Advanced Sector Protection

Table I7. Primary Vendor-Specific Extended Query (Sheet 2 of 3)

Addresses	Data		Description
	S29NS256N	S29NS128N	
4Ah	00F0h	0078h	Simultaneous Operation Number of Sectors in all banks except boot bank
4Bh	0001h		Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h		Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h		V_{PP} (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h		V_{PP} (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0003h		Top/Bottom Boot Sector Flag 0001h = Top/Middle Boot Device, 0002h = Bottom Boot Device, 03h = Top Boot Device
50h	0001h		Program Suspend. 00h = not supported
51h	0001h		Unlock Bypass 00 = Not Supported, 01=Supported
52h	0008h		Secured Silicon Sector (Customer OTP Area) Size 2^N bytes
53h	0008h		Hardware Reset Low Time-out during an embedded algorithm to read mode Maximum 2^N ns
54h	0008h		Hardware Reset Low Time-out not during an embedded algorithm to read mode Maximum 2^N ns
55h	0005h		Erase Suspend Time-out Maximum 2^N ns
56h	0005h		Program Suspend Time-out Maximum 2^N ns
57h	0010h	0010h	Bank Organization: X = Number of banks
58h	0010h	0008h	Bank 0 Region Information. X = Number of sectors in bank
59h	0010h	0008h	Bank 1 Region Information. X = Number of sectors in bank
5Ah	0010h	0008h	Bank 2 Region Information. X = Number of sectors in bank
5Bh	0010h	0008h	Bank 3 Region Information. X = Number of sectors in bank
5Ch	0010h	0008h	Bank 4 Region Information. X = Number of sectors in bank
5Dh	0010h	0008h	Bank 5 Region Information. X = Number of sectors in bank
5Eh	0010h	0008h	Bank 6 Region Information. X = Number of sectors in bank
5Fh	0010h	0008h	Bank 7 Region Information. X = Number of sectors in bank
60h	0010h	0008h	Bank 8 Region Information. X = Number of sectors in bank
61h	0010h	0008h	Bank 9 Region Information. X = Number of sectors in bank
62h	0010h	0008h	Bank 10 Region Information. X = Number of sectors in bank
63h	0010h	0008h	Bank 11 Region Information. X = Number of sectors in bank
64h	0010h	0008h	Bank 12 Region Information. X = Number of sectors in bank

Table I7. Primary Vendor-Specific Extended Query (Sheet 3 of 3)

Addresses	Data		Description
	S29NS256N	S29NS128N	
65h	0010h	0008h	Bank 13 Region Information. X = Number of sectors in bank
66h	0010h	0008h	Bank 14 Region Information. X = Number of sectors in bank
67h	0013h	000Bh	Bank 15 Region Information. X = Number of sectors in bank
68h	0002h		Process Technology. 00h = 230 nm, 01h = 170 nm, 02h = 130 nm/110 nm

Table I8. Sector Address Table, S29NS256N (Sheet I of 5)

Bank	Sector	Sector Size	Address Range
Bank 0	SA0	64 Kwords	000000h–00FFFFh
	SA1	64 Kwords	010000h–01FFFFh
	SA2	64 Kwords	020000h–02FFFFh
	SA3	64 Kwords	030000h–03FFFFh
	SA4	64 Kwords	040000h–04FFFFh
	SA5	64 Kwords	050000h–05FFFFh
	SA6	64 Kwords	060000h–06FFFFh
	SA7	64 Kwords	070000h–07FFFFh
	SA8	64 Kwords	080000h–08FFFFh
	SA9	64 Kwords	090000h–09FFFFh
	SA10	64 Kwords	0A0000h–0AFFFFh
	SA11	64 Kwords	0B0000h–0BFFFFh
	SA12	64 Kwords	0C0000h–0CFFFFh
	SA13	64 Kwords	0D0000h–0DFFFFh
	SA14	64 Kwords	0E0000h–0EFFFFh
	SA15	64 Kwords	0F0000h–0FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 2	SA32	64 Kwords	200000h–20FFFFh
	SA33	64 Kwords	210000h–21FFFFh
	SA34	64 Kwords	220000h–22FFFFh
	SA35	64 Kwords	230000h–23FFFFh
	SA36	64 Kwords	240000h–24FFFFh
	SA37	64 Kwords	250000h–25FFFFh
	SA38	64 Kwords	260000h–26FFFFh
	SA39	64 Kwords	270000h–27FFFFh
	SA40	64 Kwords	280000h–28FFFFh
	SA41	64 Kwords	290000h–29FFFFh
	SA42	64 Kwords	2A0000h–2AFFFFh
	SA43	64 Kwords	2B0000h–2BFFFFh
	SA44	64 Kwords	2C0000h–2CFFFFh
	SA45	64 Kwords	2D0000h–2DFFFFh
	SA46	64 Kwords	2E0000h–2EFFFFh
	SA47	64 Kwords	2F0000h–2FFFFFh

Table 18. Sector Address Table, S29NS256N (Sheet 2 of 5)

Bank	Sector	Sector Size	Address Range
Bank 1	SA16	64 Kwords	100000h–10FFFFh
	SA17	64 Kwords	110000h–11FFFFh
	SA18	64 Kwords	120000h–12FFFFh
	SA19	64 Kwords	130000h–13FFFFh
	SA20	64 Kwords	140000h–14FFFFh
	SA21	64 Kwords	150000h–15FFFFh
	SA22	64 Kwords	160000h–16FFFFh
	SA23	64 Kwords	170000h–17FFFFh
	SA24	64 Kwords	180000h–18FFFFh
	SA25	64 Kwords	190000h–19FFFFh
	SA26	64 Kwords	1A0000h–1AFFFFh
	SA27	64 Kwords	1B0000h–1BFFFFh
	SA28	64 Kwords	1C0000h–1CFFFFh
	SA29	64 Kwords	1D0000h–1DFFFFh
	SA30	64 Kwords	1E0000h–1EFFFFh
	SA31	64 Kwords	1F0000h–1FFFFFh
Bank 4	SA64	64 Kwords	400000h–40FFFFh
	SA65	64 Kwords	410000h–41FFFFh
	SA66	64 Kwords	420000h–42FFFFh
	SA67	64 Kwords	430000h–43FFFFh
	SA68	64 Kwords	440000h–44FFFFh
	SA69	64 Kwords	450000h–45FFFFh
	SA70	64 Kwords	460000h–46FFFFh
	SA71	64 Kwords	470000h–47FFFFh
	SA72	64 Kwords	480000h–48FFFFh
	SA73	64 Kwords	490000h–49FFFFh
	SA74	64 Kwords	4A0000h–4AFFFFh
	SA75	64 Kwords	4B0000h–4BFFFFh
	SA76	64 Kwords	4C0000h–4CFFFFh
	SA77	64 Kwords	4D0000h–4DFFFFh
	SA78	64 Kwords	4E0000h–4EFFFFh
	SA79	64 Kwords	4F0000h–4FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 3	SA48	64 Kwords	300000h–30FFFFh
	SA49	64 Kwords	310000h–31FFFFh
	SA50	64 Kwords	320000h–32FFFFh
	SA51	64 Kwords	330000h–33FFFFh
	SA52	64 Kwords	340000h–34FFFFh
	SA53	64 Kwords	350000h–35FFFFh
	SA54	64 Kwords	360000h–36FFFFh
	SA55	64 Kwords	370000h–37FFFFh
	SA56	64 Kwords	380000h–38FFFFh
	SA57	64 Kwords	390000h–39FFFFh
	SA58	64 Kwords	3A0000h–3AFFFFh
	SA59	64 Kwords	3B0000h–3BFFFFh
	SA60	64 Kwords	3C0000h–3CFFFFh
	SA61	64 Kwords	3D0000h–3DFFFFh
	SA62	64 Kwords	3E0000h–3EFFFFh
	SA63	64 Kwords	3F0000h–3FFFFFh
Bank 6	SA96	64 K words	600000h–60FFFFh
	SA97	64 K words	610000h–61FFFFh
	SA98	64 K words	620000h–62FFFFh
	SA99	64 K words	630000h–63FFFFh
	SA100	64 K words	640000h–64FFFFh
	SA101	64 K words	650000h–65FFFFh
	SA102	64 K words	660000h–66FFFFh
	SA103	64 K words	670000h–67FFFFh
	SA104	64 K words	680000h–68FFFFh
	SA105	64 K words	690000h–69FFFFh
	SA106	64 K words	6A0000h–6AFFFFh
	SA107	64 K words	6B0000h–6BFFFFh
	SA108	64 K words	6C0000h–6CFFFFh
	SA109	64 K words	6D0000h–6DFFFFh
	SA110	64 K words	6E0000h–6EFFFFh
	SA111	64 K words	6F0000h–6FFFFFh

Table 18. Sector Address Table, S29NS256N (Sheet 3 of 5)

Bank	Sector	Sector Size	Address Range
Bank 5	SA80	64 Kwords	500000h–50FFFFh
	SA81	64 Kwords	510000h–51FFFFh
	SA82	64 Kwords	520000h–52FFFFh
	SA83	64 Kwords	530000h–53FFFFh
	SA84	64 Kwords	540000h–54FFFFh
	SA85	64 Kwords	550000h–55FFFFh
	SA86	64 Kwords	560000h–56FFFFh
	SA87	64 Kwords	570000h–57FFFFh
	SA88	64 Kwords	580000h–58FFFFh
	SA89	64 Kwords	590000h–59FFFFh
	SA90	64 Kwords	5A0000h–5AFFFFh
	SA91	64 Kwords	5B0000h–5BFFFFh
	SA92	64 Kwords	5C0000h–5CFFFFh
	SA93	64 Kwords	5D0000h–5DFFFFh
	SA94	64 Kwords	5E0000h–5EFFFFh
	SA95	64 Kwords	5F0000h–5FFFFFh
Bank 8	SA128	64 Kwords	800000h–80FFFFh
	SA129	64 Kwords	810000h–81FFFFh
	SA130	64 Kwords	820000h–82FFFFh
	SA131	64 Kwords	830000h–83FFFFh
	SA132	64 Kwords	840000h–84FFFFh
	SA133	64 Kwords	850000h–85FFFFh
	SA134	64 Kwords	860000h–86FFFFh
	SA135	64 Kwords	870000h–87FFFFh
	SA136	64 Kwords	880000h–88FFFFh
	SA137	64 Kwords	890000h–89FFFFh
	SA138	64 Kwords	8A0000h–8AFFFFh
	SA139	64 Kwords	8B0000h–8BFFFFh
	SA140	64 Kwords	8C0000h–8CFFFFh
	SA141	64 Kwords	8D0000h–8DFFFFh
	SA142	64 Kwords	8E0000h–8EFFFFh
	SA143	64 Kwords	8F0000h–8FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 7	SA112	64 K words	700000h–70FFFFh
	SA113	64 K words	710000h–71FFFFh
	SA114	64 K words	720000h–72FFFFh
	SA115	64 K words	730000h–73FFFFh
	SA116	64 K words	740000h–74FFFFh
	SA117	64 K words	750000h–75FFFFh
	SA118	64 K words	760000h–76FFFFh
	SA119	64 K words	770000h–77FFFFh
	SA120	64 K words	780000h–78FFFFh
	SA121	64 K words	790000h–79FFFFh
	SA122	64 K words	7A0000h–7AFFFFh
	SA123	64 K words	7B0000h–7BFFFFh
	SA124	64 K words	7C0000h–7CFFFFh
	SA125	64 K words	7D0000h–7DFFFFh
	SA126	64 K words	7E0000h–7EFFFFh
	SA127	64 K words	7F0000h–7FFFFFh
Bank 10	SA160	64 Kwords	A00000h–A0FFFFh
	SA161	64 Kwords	A10000h–A1FFFFh
	SA162	64 Kwords	A20000h–A2FFFFh
	SA163	64 Kwords	A30000h–A3FFFFh
	SA164	64 Kwords	A40000h–A4FFFFh
	SA165	64 Kwords	A50000h–A5FFFFh
	SA166	64 Kwords	A60000h–A6FFFFh
	SA167	64 Kwords	A70000h–A7FFFFh
	SA168	64 Kwords	A80000h–A8FFFFh
	SA169	64 Kwords	A90000h–A9FFFFh
	SA170	64 Kwords	AA0000h–AAFFFFh
	SA171	64 Kwords	AB0000h–ABFFFFh
	SA172	64 Kwords	AC0000h–ACFFFFh
	SA173	64 Kwords	AD0000h–ADFFFFh
	SA174	64 Kwords	AE0000h–AEFFFFh
	SA175	64 Kwords	AF0000h–AFFFFFh

Table 18. Sector Address Table, S29NS256N (Sheet 4 of 5)

Bank	Sector	Sector Size	Address Range
Bank 9	SA144	64 Kwords	900000h–90FFFFh
	SA145	64 Kwords	910000h–91FFFFh
	SA146	64 Kwords	920000h–92FFFFh
	SA147	64 Kwords	930000h–93FFFFh
	SA148	64 Kwords	940000h–94FFFFh
	SA149	64 Kwords	950000h–95FFFFh
	SA150	64 Kwords	960000h–96FFFFh
	SA151	64 Kwords	970000h–97FFFFh
	SA152	64 Kwords	980000h–98FFFFh
	SA153	64 Kwords	990000h–99FFFFh
	SA154	64 Kwords	9A0000h–9AFFFFh
	SA155	64 Kwords	9B0000h–9BFFFFh
	SA156	64 Kwords	9C0000h–9CFFFFh
	SA157	64 Kwords	9D0000h–9DFFFFh
	SA158	64 Kwords	9E0000h–9EFFFFh
	SA159	64 Kwords	9F0000h–9FFFFFh
Bank 12	SA192	64 Kwords	C00000h–C0FFFFh
	SA193	64 Kwords	C10000h–C1FFFFh
	SA194	64 Kwords	C20000h–C2FFFFh
	SA195	64 Kwords	C30000h–C3FFFFh
	SA196	64 Kwords	C40000h–C4FFFFh
	SA197	64 Kwords	C50000h–C5FFFFh
	SA198	64 Kwords	C60000h–C6FFFFh
	SA199	64 Kwords	C70000h–C7FFFFh
	SA200	64 Kwords	C80000h–C8FFFFh
	SA201	64 Kwords	C90000h–C9FFFFh
	SA202	64 Kwords	CA0000h–CAFFFFh
	SA203	64 Kwords	CB0000h–CBFFFFh
	SA204	64 Kwords	CC0000h–CCFFFFh
	SA205	64 Kwords	CD0000h–CDFFFFh
	SA206	64 Kwords	CE0000h–CEFFFFh
	SA207	64 Kwords	CF0000h–CFFFFFh

Bank	Sector	Sector Size	Address Range
Bank 11	SA176	64 Kwords	B00000h–B0FFFFh
	SA177	64 Kwords	B10000h–B1FFFFh
	SA178	64 Kwords	B20000h–B2FFFFh
	SA179	64 Kwords	B30000h–B3FFFFh
	SA180	64 Kwords	B40000h–B4FFFFh
	SA181	64 Kwords	B50000h–B5FFFFh
	SA182	64 Kwords	B60000h–B6FFFFh
	SA183	64 Kwords	B70000h–B7FFFFh
	SA184	64 Kwords	B80000h–B8FFFFh
	SA185	64 Kwords	B90000h–B9FFFFh
	SA186	64 Kwords	BA0000h–BAFFFFh
	SA187	64 Kwords	BB0000h–BBFFFFh
	SA188	64 Kwords	BC0000h–BCFFFFh
	SA189	64 Kwords	BD0000h–BDFFFFh
	SA190	64 Kwords	BE0000h–BEFFFFh
	SA191	64 Kwords	BF0000h–BFFFFFh
Bank 14	SA224	64 K words	E00000h–E0FFFFh
	SA225	64 K words	E10000h–E1FFFFh
	SA226	64 K words	E20000h–E2FFFFh
	SA227	64 K words	E30000h–E3FFFFh
	SA228	64 K words	E40000h–E4FFFFh
	SA229	64 K words	E50000h–E5FFFFh
	SA230	64 K words	E60000h–E6FFFFh
	SA231	64 K words	E70000h–E7FFFFh
	SA232	64 K words	E80000h–E8FFFFh
	SA233	64 K words	E90000h–E9FFFFh
	SA234	64 K words	EA0000h–EAFFFFh
	SA235	64 K words	EB0000h–EBFFFFh
	SA236	64 K words	EC0000h–ECFFFFh
	SA237	64 K words	ED0000h–EDFFFFh
	SA238	64 K words	EE0000h–EEFFFFh
	SA239	64 K words	EF0000h–EFFFFFh

Table 18. Sector Address Table, S29NS256N (Sheet 5 of 5)

Bank	Sector	Sector Size	Address Range
Bank 13	SA208	64 Kwords	D00000h–D0FFFFh
	SA209	64 Kwords	D10000h–D1FFFFh
	SA210	64 Kwords	D20000h–D2FFFFh
	SA211	64 Kwords	D30000h–D3FFFFh
	SA212	64 Kwords	D40000h–D4FFFFh
	SA213	64 Kwords	D50000h–D5FFFFh
	SA214	64 Kwords	D60000h–D6FFFFh
	SA215	64 Kwords	D70000h–D7FFFFh
	SA216	64 Kwords	D80000h–D8FFFFh
	SA217	64 Kwords	D90000h–D9FFFFh
	SA218	64 Kwords	DA0000h–DAFFFFh
	SA219	64 Kwords	DB0000h–DBFFFFh
	SA220	64 Kwords	DC0000h–DCFFFFh
	SA221	64 Kwords	DD0000h–DDFFFFh
	SA222	64 Kwords	DE0000h–DEFFFFh
	SA223	64 Kwords	DF0000h–DFFFFFh

Bank	Sector	Sector Size	Address Range
Bank 15	SA240	64 K words	F00000h–F0FFFFh
	SA241	64 K words	F10000h–F1FFFFh
	SA242	64 K words	F20000h–F2FFFFh
	SA243	64 K words	F30000h–F3FFFFh
	SA244	64 K words	F40000h–F4FFFFh
	SA245	64 K words	F50000h–F5FFFFh
	SA246	64 K words	F60000h–F6FFFFh
	SA247	64 K words	F70000h–F7FFFFh
	SA248	64 K words	F80000h–F8FFFFh
	SA249	64 K words	F90000h–F9FFFFh
	SA250	64 K words	FA0000h–FAFFFFh
	SA251	64 K words	FB0000h–FBFFFFh
	SA252	64 K words	FC0000h–FCFFFFh
	SA253	64 K words	FD0000h–FDFFFFh
	SA254	64 K words	FE0000h–FEFFFFh
	SA255	16 K words	FF0000h–FF3FFFh
	SA256	16 K words	FF4000h–FF7FFFh
	SA257	16 K words	FF8000h–FFBFFFh
	SA258	16 K words	FFC000h–FFFFFFh

Table 19. Sector Address Table, S29NSI28N (Sheet 1 of 3)

Bank	Sector	Sector Size	Address Range
Bank 0	SA0	64 Kwords	000000h–00FFFFh
	SA1	64 Kwords	010000h–01FFFFh
	SA2	64 Kwords	020000h–02FFFFh
	SA3	64 Kwords	030000h–03FFFFh
	SA4	64 Kwords	040000h–04FFFFh
	SA5	64 Kwords	050000h–05FFFFh
	SA6	64 Kwords	060000h–06FFFFh
	SA7	64 Kwords	070000h–07FFFFh

Bank	Sector	Sector Size	Address Range
Bank 4	SA32	64 Kwords	200000h–20FFFFh
	SA33	64 Kwords	210000h–21FFFFh
	SA34	64 Kwords	220000h–22FFFFh
	SA35	64 Kwords	230000h–23FFFFh
	SA36	64 Kwords	240000h–24FFFFh
	SA37	64 Kwords	250000h–25FFFFh
	SA38	64 Kwords	260000h–26FFFFh
	SA39	64 Kwords	270000h–27FFFFh

Table 19. Sector Address Table, S29NSI28N (Sheet 2 of 3)

Bank	Sector	Sector Size	Address Range
Bank 1	SA8	64 Kwords	080000h–08FFFFh
	SA9	64 Kwords	090000h–09FFFFh
	SA10	64 Kwords	0A0000h–0AFFFFh
	SA11	64 Kwords	0B0000h–0BFFFFh
	SA12	64 Kwords	0C0000h–0CFFFFh
	SA13	64 Kwords	0D0000h–0DFFFFh
	SA14	64 Kwords	0E0000h–0EFFFFh
	SA15	64 Kwords	0F0000h–0FFFFFh
Bank 2	SA16	64 Kwords	100000h–10FFFFh
	SA17	64 Kwords	110000h–11FFFFh
	SA18	64 Kwords	120000h–12FFFFh
	SA19	64 Kwords	130000h–13FFFFh
	SA20	64 Kwords	140000h–14FFFFh
	SA21	64 Kwords	150000h–15FFFFh
	SA22	64 Kwords	160000h–16FFFFh
	SA23	64 Kwords	170000h–17FFFFh
Bank 3	SA24	64 Kwords	180000h–18FFFFh
	SA25	64 Kwords	190000h–19FFFFh
	SA26	64 Kwords	1A0000h–1AFFFFh
	SA27	64 Kwords	1B0000h–1BFFFFh
	SA28	64 Kwords	1C0000h–1CFFFFh
	SA29	64 Kwords	1D0000h–1DFFFFh
	SA30	64 Kwords	1E0000h–1EFFFFh
	SA31	64 Kwords	1F0000h–1FFFFFh
Bank 8	SA64	64 Kwords	400000h–40FFFFh
	SA65	64 Kwords	410000h–41FFFFh
	SA66	64 Kwords	420000h–42FFFFh
	SA67	64 Kwords	430000h–43FFFFh
	SA68	64 Kwords	440000h–44FFFFh
	SA69	64 Kwords	450000h–45FFFFh
	SA70	64 Kwords	460000h–46FFFFh
	SA71	64 Kwords	470000h–47FFFFh

Bank	Sector	Sector Size	Address Range
Bank 5	SA40	64 Kwords	280000h–28FFFFh
	SA41	64 Kwords	290000h–29FFFFh
	SA42	64 Kwords	2A0000h–2AFFFFh
	SA43	64 Kwords	2B0000h–2BFFFFh
	SA44	64 Kwords	2C0000h–2CFFFFh
	SA45	64 Kwords	2D0000h–2DFFFFh
	SA46	64 Kwords	2E0000h–2EFFFFh
	SA47	64 Kwords	2F0000h–2FFFFFh
Bank 6	SA48	64 Kwords	300000h–30FFFFh
	SA49	64 Kwords	310000h–31FFFFh
	SA50	64 Kwords	320000h–32FFFFh
	SA51	64 Kwords	330000h–33FFFFh
	SA52	64 Kwords	340000h–34FFFFh
	SA53	64 Kwords	350000h–35FFFFh
	SA54	64 Kwords	360000h–36FFFFh
	SA55	64 Kwords	370000h–37FFFFh
Bank 7	SA56	64 Kwords	380000h–38FFFFh
	SA57	64 Kwords	390000h–39FFFFh
	SA58	64 Kwords	3A0000h–3AFFFFh
	SA59	64 Kwords	3B0000h–3BFFFFh
	SA60	64 Kwords	3C0000h–3CFFFFh
	SA61	64 Kwords	3D0000h–3DFFFFh
	SA62	64 Kwords	3E0000h–3EFFFFh
	SA63	64 Kwords	3F0000h–3FFFFFh
Bank 12	SA96	64 K words	600000h–60FFFFh
	SA97	64 K words	610000h–61FFFFh
	SA98	64 K words	620000h–62FFFFh
	SA99	64 K words	630000h–63FFFFh
	SA100	64 K words	640000h–64FFFFh
	SA101	64 K words	650000h–65FFFFh
	SA102	64 K words	660000h–66FFFFh
	SA103	64 K words	670000h–67FFFFh

Table 19. Sector Address Table, S29NSI28N (Sheet 3 of 3)

Bank	Sector	Sector Size	Address Range
Bank 9	SA72	64 Kwords	480000h–48FFFFh
	SA73	64 Kwords	490000h–49FFFFh
	SA74	64 Kwords	4A0000h–4AFFFFh
	SA75	64 Kwords	4B0000h–4BFFFFh
	SA76	64 Kwords	4C0000h–4CFFFFh
	SA77	64 Kwords	4D0000h–4DFFFFh
	SA78	64 Kwords	4E0000h–4EFFFFh
	SA79	64 Kwords	4F0000h–4FFFFFh
Bank 10	SA80	64 Kwords	500000h–50FFFFh
	SA81	64 Kwords	510000h–51FFFFh
	SA82	64 Kwords	520000h–52FFFFh
	SA83	64 Kwords	530000h–53FFFFh
	SA84	64 Kwords	540000h–54FFFFh
	SA85	64 Kwords	550000h–55FFFFh
	SA86	64 Kwords	560000h–56FFFFh
	SA87	64 Kwords	570000h–57FFFFh
Bank 11	SA88	64 Kwords	580000h–58FFFFh
	SA89	64 Kwords	590000h–59FFFFh
	SA90	64 Kwords	5A0000h–5AFFFFh
	SA91	64 Kwords	5B0000h–5BFFFFh
	SA92	64 Kwords	5C0000h–5CFFFFh
	SA93	64 Kwords	5D0000h–5DFFFFh
	SA94	64 Kwords	5E0000h–5EFFFFh
	SA95	64 Kwords	5F0000h–5FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 13	SA104	64 K words	680000h–68FFFFh
	SA105	64 K words	690000h–69FFFFh
	SA106	64 K words	6A0000h–6AFFFFh
	SA107	64 K words	6B0000h–6BFFFFh
	SA108	64 K words	6C0000h–6CFFFFh
	SA109	64 K words	6D0000h–6DFFFFh
	SA110	64 K words	6E0000h–6EFFFFh
	SA111	64 K words	6F0000h–6FFFFFh
Bank 14	SA112	64 K words	700000h–70FFFFh
	SA113	64 K words	710000h–71FFFFh
	SA114	64 K words	720000h–72FFFFh
	SA115	64 K words	730000h–73FFFFh
	SA116	64 K words	740000h–74FFFFh
	SA117	64 K words	750000h–75FFFFh
	SA118	64 K words	760000h–76FFFFh
	SA119	64 K words	770000h–77FFFFh
Bank 15	SA120	64 K words	780000h–78FFFFh
	SA121	64 K words	790000h–79FFFFh
	SA122	64 K words	7A0000h–7AFFFFh
	SA123	64 K words	7B0000h–7BFFFFh
	SA124	64 K words	7C0000h–7CFFFFh
	SA125	64 K words	7D0000h–7DFFFFh
	SA126	64 K words	7E0000h–7EFFFFh
	SA127	16 K words	7F0000h–7F3FFFh
	SA128	16 K words	7F4000h–7F7FFFh
	SA129	16 K words	7F8000h–7FBFFFh
	SA130	16 K words	7FC000h–7FFFFFh

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table on page 62 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the rising edge of AVD#. All data is latched on the rising edge of WE#. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

After the device accepts a Program Suspend command, the corresponding bank enters the program-suspend-read mode, after which the system can read data from any non-program-suspended sector within the same bank.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode.

See also VersatileIO™ (V_{IO}) Control and Requirements for Synchronous (Burst) Read Operation in the Device Bus Operations section for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, and Figure 13, on page 79 and Figure 14, on page 80 show the timings.

Set Configuration Register Command Sequence

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, RDY configuration, and synchronous mode active. The configuration register must be set before the device will enter burst mode.

The configuration register is loaded with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be D0h and address bits should be 555h. During the fourth cycle, the configuration code should be entered onto the data bus with the address bus set to address 000h. Once the data has been programmed into the configuration register, a software reset command is required to set the device into the correct state. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

Read Configuration Register Command Sequence

The configuration register can be read with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C6h and address bits should be 555h. During the fourth cycle, the configuration code should be read out of the data bus with the address bus set to address 000h. Once the data has been read from the configuration register, a software reset command is required to set the device into the correct set mode.

Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations.

Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. **Configuration Bit CR13–CR11** determine the setting (see Table 20).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 20. Programmable Wait State Settings

CR13	CR12	CR11	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7 (default)
1	1	0	Reserved
1	1	1	Reserved

Notes:

1. *Upon power-up or hardware reset, the default setting is seven wait states.*
2. *RDY will default to being active with data when the Wait State Setting is set to a total initial access cycle of 2.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

Programmable Wait State

The host system should set **CR13-CR11** to 101/100/011 for a clock frequency of 80/66 MHz for the system/device to execute at maximum speed.

Table 21 on page 45 describes the typical number of clock cycles (wait states) for various conditions.

Table 2l. Wait States for Handshaking

Conditions at Address	Typical No. of Clock Cycles after AVD# Low	
	80 MHz	66 MHz
Initial address (V_{CCQ} = 1.8 V)	7	6

Handshaking

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on the clock frequency.

The autoselect function allows the host system to determine whether the flash device is enabled for handshaking.

Burst Length Configuration

The device supports four different read modes: continuous mode, and 8, 16, and 32 word linear with or without wrap around modes. A continuous sequence (default) begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear read with wrap around begins on the starting address written to the device and then advances to the next 8 word boundary. The address pointer then returns to the 1st word after the previous eight word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 22 shows the **CR2-CR0** and settings for the four read modes.

Table 22. Burst Length Configuration

Burst Modes	Address Bits		
	CR2	CR1	CR0
Continuous	0	0	0
8-word linear	0	1	0
16-word linear	0	1	1
32-word linear	1	0	0

Notes:

1. *Upon power-up or hardware reset the default setting is continuous.*
2. *All other conditions are reserved.*

Burst Wrap Around

By default, the device will perform burst wrap around with **CR3** set to a '1'. Changing the **CR3** to a '0' disables burst wrap around.

RDY Configuration

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. **CR8** determines this setting; "1" for RDY active (default) with data, "0" for RDY active one clock cycle before valid data.

RDY Polarity

By default, the RDY pin will always indicate that the device is ready to handle a new transaction with **CR10** set to a '1'. In this case, the RDY pin is active high. Changing the **CR10** to a '0' sets the RDY pin to be active low. In this case, the RDY pin will always indicate that the device is ready to handle a new transaction when low.

Configuration Register

Table 23 shows the address bits that determine the configuration register settings for various device functions.

Table 23. Configuration Register

CR BIt	Function	Settings (Binary)
CR15	Reserved	0 = Default
CR14	Reserved	0 = Default
CR13 CR12 CR11	Programmable Wait State	000 = Data is valid on the 2nd active CLK edge after AVD# transition to V_{IH} 001 = Data is valid on the 3rd active CLK edge after AVD# transition to V_{IH} 010 = Data is valid on the 4th active CLK edge after AVD# transition to V_{IH} 011 = Data is valid on the 5th active CLK edge after AVD# transition to V_{IH} 100 = Data is valid on the 6th active CLK edge after AVD# transition to V_{IH} 101 = Data is valid on the 7th active CLK edge after AVD# transition to V_{IH} (default) 110 = Reserved 111 = Reserved
CR10	RDY Polarity	0 = RDY signal is active low 1 = RDY signal is active high (default)
CR9	Reserved	1 = Default
CR8	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
CR7	Reserved	1 = default
CR6	Reserved	1 = default
CR5	Reserved	0 = default
CR4	Reserved	0 = default
CR3	Burst Wrap Around	0 = No Wrap Around Burst 1 = Wrap Around Burst (default)
CR2 CR1 CR0	Burst Length	000 = Continuous (default) 010 = 8-Word Linear Burst 011 = 16-Word Linear Burst 100 = 32-Word Linear Burst (All other bit settings are reserved)

Note: *Device will be in the default state upon power-up or hardware reset.*

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. **Once erasure begins, however, the device ignores reset commands until the operation is complete**.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. **Once pro-**

gramming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Note: If DQ1 goes high during a Write Buffer Programming operation, the system must write the "Write to Buffer Abort Reset" command sequence to RESET the device to reading array data. The standard RESET command will not work. See Table on page 35 for details on this command sequence.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table on page 62 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank. Autoselect does not support simultaneous operations or burst mode.

Table 24. Device ID

Description	Address	Read Data	
		256N	**128N**
Manufacturer ID	(BA) + 00h	0001h	0001h
Device ID, Word 1	(BA) + 01h	2D7E	2C7Eh
Device ID, Word 2	(BA) + 0Eh	2D2F	2C35h
Device ID, Word 3	(BA) + 0Fh	2D00	2C00h
Revision ID	(BA) + 03h	TBD	
Sector Block Lock/Unlock	(SA) = 02h	0001 - Locked 0000 - Unlocked	
Indicator Bits	(BA) + 07h	DQ15 - DQ8 = Reserved DQ7 - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ6 - Customer Lock Bit 1 = Locked, 0 = Not Locked DQ5 Handshake Bit 1 = Reserved 0 = Standard Handshake DQ4 & DQ3 - WP# Protections Boot Code 01 = WP# Protects only the Top Boot Sectors DQ2-DQ0 = Reserved	

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address. The device ID is read in three cycles. During this time, other banks are still available to read the data from the memory.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is exe-

cuting an Embedded Program or embedded Erase algorithm. Table , "," on page 62 shows the address and data requirements for both command sequences.

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program faster than the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode.

During the unlock bypass mode only the command is valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

Program Command Sequence

Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table on page 62 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may causes that bank to set DQ5 = 1 (change-up condition). However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

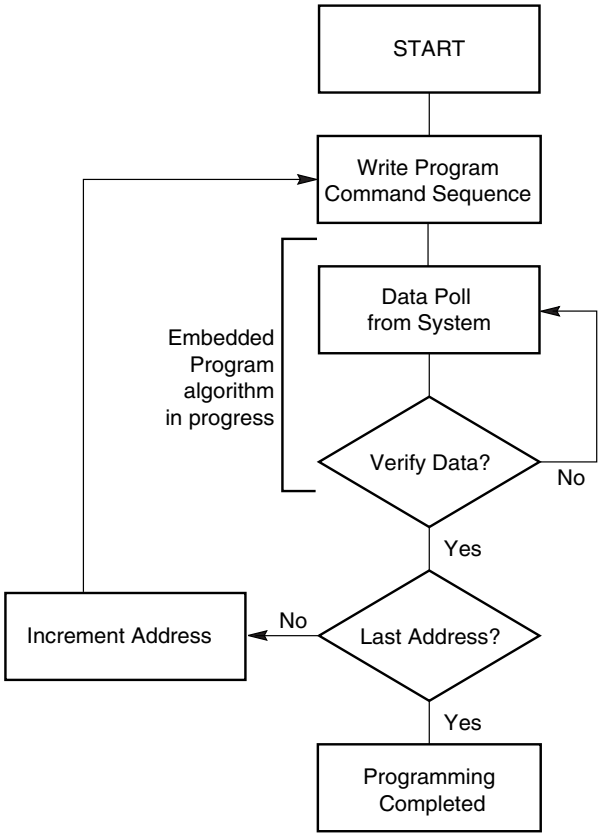
Program Command Sequence (Unlock Bypass Mode)

Once the device enters the unlock bypass mode, then a two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table on page 62 shows the requirements for the unlock bypass command sequences.

Accelerated Program

The device offers accelerated program operations through the V_{PP} input. When the system asserts V_{PP} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the V_{PP} input to accelerate the operation.

Figure 1 illustrates the algorithm for the program operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 16, on page 83 for timing diagrams.



Note: See Table for program command sequence.

Figure I. Program Operation

Write Buffer Programming Command Sequence

Write Buffer Programming Sequence allows for faster programming as compared to the standard Program Command Sequence. See Table 25 on page 52 for the program command sequence.

Table 25. Write Buffer Command Sequence

Sequence	Address	Data	Comment
Unlock Command 1	555	00AA	Not required in the Unlock Bypass mode
Unlock Command 2	2AA	0055	Same as above
Write Buffer Load	Starting Address	0025h	
Specify the Number of Program Locations	Starting Address	Word Count	Number of locations to program minus 1
Load 1st data word	Starting Address	Program Data	All addresses must be within write-buffer-page boundaries, but do not have to be loaded in any order
Load next data word	Write Buffer Location	Program Data	Same as above
...	...	...	Same as above
Load last data word	Write Buffer Location	Program Data	Same as above
Write Buffer Program Confirm	Sector Address	0029h	This command must follow the last write buffer location loaded, or the operation will ABORT
Device goes busy			
Status monitoring through DQ pins (Perform Data Bar Polling on the **Last Loaded Address**)			

Notes:

1. Write buffer addresses must be loaded in sequential order.

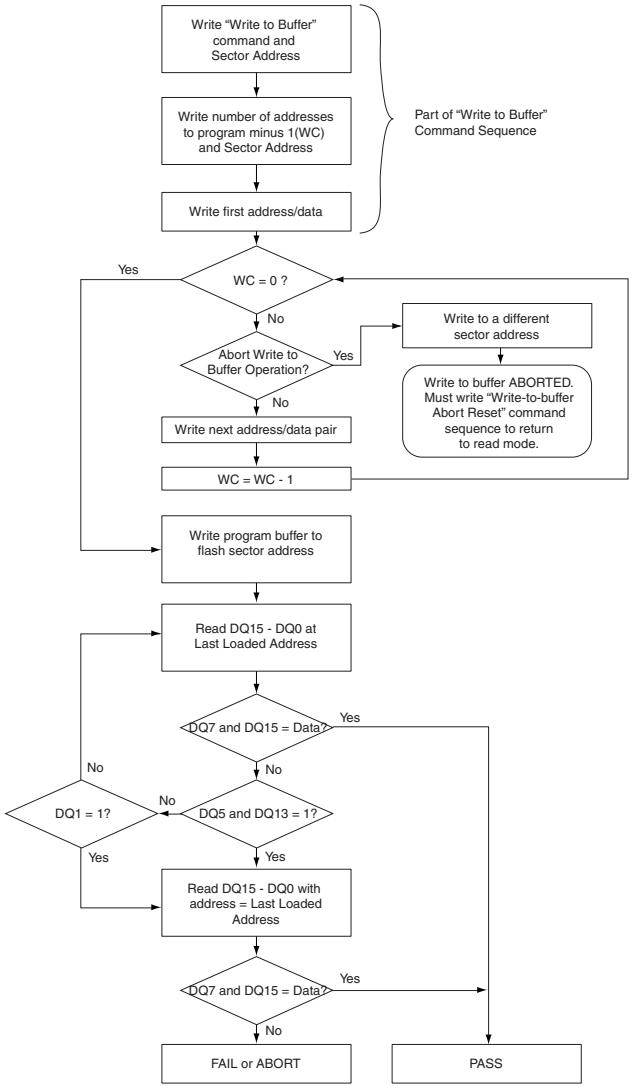


Figure 2. Write Buffer Programming Operation

Chip Erase Command Sequence

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table on page 62 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Sector Erase Command Sequence

Sector Erase Command Sequence

Sector erase in normal mode is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than t_{SEA}, sector erase accept, occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than t_{SEA}. Any sector erase address and command following the exceeded time-out may or may not be accepted. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.**

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase start timeout state indicator.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing banks. The system can determine the status of the erase operation by reading DQ7 or DQ6/ DQ2 in the erasing bank. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Accelerated Sector Erase

The device offers accelerated sector erase operation through the V_{PP} function. This method of erasing sectors is faster than the standard sector erase command sequence. **The accelerated sector erase function must not be used more than 100 times per sector.** In addition, accelerated sector erase should be performed at room temperature (30°C +-10°C).

The following procedure is used to perform accelerated sector erase:

1. Sectors to be erased must be PPB and DYB cleared. All sectors that remain locked will not be erased.
2. Apply 9 V to the V_{PP} input. This voltage must be applied at least 1 µs before executing step 3.
3. Issue the standard chip erase command.
4. Monitor status bits DQ2/DQ6 or DQ7 to determine when erasure is complete, just as in the standard erase operation. See Write Operation Status for further details.
5. Lower V_{PP} from 9 V to V_{CC}.

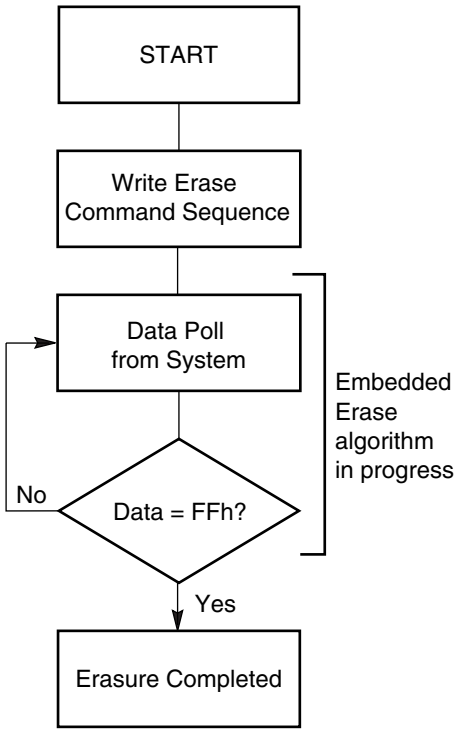


Figure 3. Erase Operation

Note: *See the section on DQ3 for information on the sector erase start timeout state indicator.*

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, program data to, any sector not selected for erasure. The system may also lock or unlock any sector while the erase operation is suspended. **The system must not write the sector lock/unlock command to sectors selected for erasure.** The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of t_{ESL}, erase suspend latency, to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) The system may also lock or unlock any sector while in the erase-suspend-read mode. Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Functions and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt a embedded programming operation or a "Write to Buffer" programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL}, program suspend latency, and updates the status bits. Addresses are defined when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One Time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system must write the Program Resume command (address bits are "don't care") to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

Lock Register Command Set Definitions

The Lock Register Command Set permits the user to one-time program the Persistent Protection Mode Lock Bit or Password Protection Mode Lock Bit. The Lock Command Set also allows for the reading of the Persistent Protection Mode Lock Bit or Password Protection Mode Lock Bit.

The Lock Register Command Set Entry command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Lock Register Command Set Entry** command disables reads and writes for Bank 0. Reads from other banks excluding Bank 0 are allowed.

- Lock Register Program Command
- Lock Register Read Command
- Lock Register Exit Command

The **Lock Register Command Set Exit** command **must** be issued after the execution of the commands to reset the device to read mode, and re-enables reads and writes for Bank 0.

For the device to be permanently set to the Persistent Protection Mode or the Password Protection Mode, the sequence of a Lock Register Command Set Exit command, must be initiated after issuing the **Persistent Protection Mode Lock Bit Program** and the **Password Protection Mode Lock Bit Program** commands. Note that if the **Persistent Protection Mode Lock Bit** and the **Password Protection Mode Lock Bit** are programmed at the same time, neither will be programmed.

Password Protection Command Set Definitions

The Password Protection Command Set permits the user to program the 64-bit password, verify the programming of the 64-bit password, and then later unlock the device by issuing the valid 64-bit password.

The **Password Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the Password Protection Command Set Entry command disables reads and writes for Bank 0. Reads for other banks excluding Bank 0 are allowed. *However Writes to any bank are not allowed.*

- Password Program Command
- Password Read Command
- Password Unlock Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. There is no special addressing order required for programming the password.

Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded

Program Algorithm with the cell remaining as a "0". The password is all 1's when shipped from the factory. All 64-bit password combinations are valid as a password.

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Lock Bit is not programmed. If the Password Mode Lock Bit is programmed and the user attempts to verify the Password, the device will always drive all 1's onto the DQ data bus.

The lower two address bits (A1–A0) are valid during the Password Read, Password Program, and Password Unlock.

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 1 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 1 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. The password is 64 bits long. A1 and A0 are used for matching. Writing the Password Unlock command does not need to be address order specific. An example sequence is starting with the lower address A1–A0= 00, followed by A1–A0= 01, A1–A0= 10, and A1–A0= 11.

Approximately 1 uSec is required for unlocking the device after the valid 64-bit password is given to the device. It is the responsibility of the microprocessor to keep track of the entering the portions of the 64-bit password with the Password Unlock command, the order, and when to read the PPB Lock bit to confirm successful password unlock. In order to re-lock the device into the Password Mode, the PPB Lock Bit Set command can be re-issued.

The **Password Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode, otherwise the device will hang. Note that issuing the **Password Protection Command Set Exit** command re-enables reads and writes for Bank 0.

Non-Volatile Sector Protection Command Set Definitions

The Non-Volatile Sector Protection Command Set permits the user to program the Persistent Protection Bits (PPBs), erase all of the Persistent Protection Bits (PPBs), and read the logic state of the Persistent Protection Bits (PPBs).

The **Non-Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Non-Volatile Sector Protection Command Set Entry** command disables reads and writes for *Active Bank*. Reads from other banks excluding *Active Bank* are allowed.

- PPB Program Command
- All PPB Erase Command
- PPB Status Read Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector addresses (A_{MAX}–A14) are written at the same time as the program command. If the PPB Lock Bit is set, the PPB Program command will not execute and the command will time-out without programming the PPB.

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs.

The device will preprogram all PPBs prior to erasing when issuing the All PPB Erase command. Also note that the total number of PPB program/erase cycles has the same endurance as the flash memory array.

The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device. See Figure 4, on page 59 for the PPB program/erase algorithm.

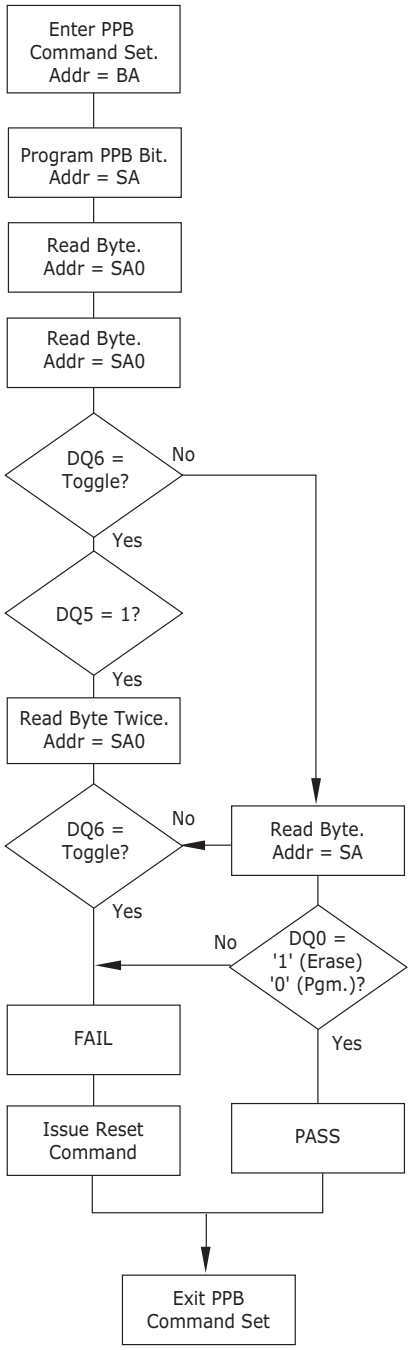


Figure 4. PPB Program/Erase Algorithm

Note: *The bank entered during entry is the* ***active bank****. Take for example the active bank is BA0. Any reads in BA0 will result in status reads of the PPB bit. If the user wants to set (programmed to "0") in a different bank other than the active bank, say for example BA5, then the*

active bank switches from BA0 to BA5. Reading in BA5 will result in status read of the bit whereas reading in BA0 will result in true data.

The **Non-Volatile Sector Protection Command Set Exit** command **must** be issued after the execution of the commands listed previously to reset the device to read mode. Note that issuing the **Non-Volatile Sector Protection Command Set Exit** command re-enables *reads and writes for Active Bank.*

After entering the PPB Mode

- The PPB Status Read (BA) is the Mode entry (BA)
- If PPB Program command is given, the new PPB Status Read (BA) will be the same (BA) as given in the PPB Program.
- If PPB Erase command is given, the new PPB Status Read (BA) is the same (BA) as given in the PPB Program or PPB Set Entry, whichever was last.
- During PPB Program or Erase Operation, PPB status read is not available. Only polling data is available in Bank0 and no other bank. Reading from all other banks will give core data.

Global Volatile Sector Protection Freeze Command Set

The Global Volatile Sector Protection Freeze Command Set permits the user to set the PPB Lock Bit and reading the logic state of the PPB Lock Bit.

The **Volatile Sector Protection Freeze Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Reads from all banks excluding mode entry bank are allowed.

- PPB Lock Bit Set Command
- PPB Lock Bit Status Read Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear (for Persistent Sector Protection Mode) or the Password Unlock command is executed (for Password Sector Protection Mode). If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle.

The programming state of the PPB Lock Bit can be verified by executing a PPB Lock Bit Status Read Command to the device.

The **Global Volatile Sector Protection Freeze Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Volatile Sector Protection Command Set

The Volatile Sector Protection Command Set permits the user to set the Dynamic Protection Bit (DYB), clear the Dynamic Protection Bit (DYB), and read the logic state of the Dynamic Protection Bit (DYB).

The **Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Volatile Sector Protection Command Set Entry** command disables reads and writes for the bank selected with the command. Reads for other banks excluding the selected bank are allowed.

- DYB Set Command
- DYB Clear Command
- DYB Status Read Command

The DYB Set/Clear command is used to set or clear a DYB for a given sector. The high order address bits (A23–A14 for the NS256N, and A22–A14 for the NS128N) are issued at the same time as the code 00h or 01h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are set at power-up or hardware reset.

The programming state of the DYB for a given sector can be verified by writing a DYB Status Read Command to the device.

Note: *The bank entered during entry is the active bank. Take for example the active bank is BA0. Any reads in BA0 will result in status reads of the DYB bit. If the user wants to set (programmed to "0") in a different bank other than the active bank, say for example BA5, then the active bank switches from BA0 to BA5. Reading in BA5 will result in status read of the bit whereas reading in BA0 will result in true data.*

The **Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Volatile Sector Protection Command Set Exit** command re-enables reads and writes for the bank selected.

Table 26. Command Definitions (Sheet I of 3)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (7)		1	RA	RD												
Reset (8)		1	XXX	F0												
Autoselect (9)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X00	0001						
	Device ID	6	555	AA	2AA	55	(BA) 555	90	(BA) X01	(Note 10)	(BA) X0E	(Note 10)	(BA) X0F	(Note 10)		
	Indicator Bits (11)	4	555	AA	2AA	55	(BA) 555	90	(BA) X0D	(Note 11)						
	Revision ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X03							
Unlock Bypass	Mode Entry	3	555	AA	2AA	55	555	20								
	Program (12)	2	XXX	A0	PA	PD										
	Reset (13)	2	BA	90	XXX	00										
CFI		1	55	98												
Program		4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer (17)		6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD		
Program Buffer to Flash		1	SA	29												
Write to Buffer Abort Reset (20)		3	555	AA	2AA	55	555	F0								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend / Program Suspend (14)		1	BA	B0												
Erase Resume / Program Resume (15)		1	BA	30												
Set Config. Register (28)		4	555	AA	2AA	55	555	D0	X00	CR						
Read Configuration Register		4	555	AA	2AA	55	555	C6	X00	CR						
Lock Register Command Set Definitions																
Lock	Lock Register Command Set Entry	3	555	AA	2AA	55	555	40								
	Lock Register Bits Program (Note 23)	2	XX	A0	00	data										
	Lock Register Bits Read	1	(BA0) 00	data												
	Lock Register Command Set Exit (note 24)	2	XX	90	XX	00										

Table 26. Command Definitions (Sheet 2 of 3)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Password Protection Command Set Definitions																
Password	Password Protection Command Set Entry	3	555	AA	2AA	55	555	60								
	Password Program (note 24, 26)	2	XX	A0	00/ 01/ 02/ 03	PWD 0/ PWD 1/ PWD 2/ PWD 3										
	Password Read (note 27)	4	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3						
	Password Unlock (note 26)	7	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3	00	29
	Password Protection Command Set Exit	2	XX	90	XX	00										
Non-Volatile Sector Protection Command Set Definitions																
PPB	Non-Volatile Sector Protection Command Set Entry	3	555	AA	2AA	55	(BA) 555	C0								
	PPB Program (29)	2	XX	A0	(BA) SA	00										
	All PPB Erase (Notes 19) (29)	2	XX	80	00	30										
	PPB Status Read	1	(BA) SA	RD (0)												
	Non-Volatile Sector Protection Command Set Exit	2	XX	90	XX	00										
Global Volatile Sector Protection Command Set Definitions																
PPB Lock Bit	Global Volatile Sector Protection Freeze Command Set Entry	3	555	AA	2AA	55	(BA) 555	50								
	PPB Lock Bit Set	2	XX	A0	XX	00										
	PPB Lock Bit Status Read	1	(BA) XX	RD (0)												
	Global Volatile Sector Protection Freeze Command Set Exit	2	XX	90	XX	00										

Table 26. Command Definitions (Sheet 3 of 3)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Secured Silicon Sector Command Definitions																
Secured Silicon Sector	Secured Silicon Sector Entry (Note 21)	3	555	AA	2AA	55	555	88								
	Secured Silicon Sector Program	2	XX	A0	00	data										
	Secured Silicon Sector Read	1	00	data												
	Secured Silicon Sector Exit (note 24)	4	555	AA	2AA	55	555	90	XX	00						
Volatile Sector Protection Command Set Definitions																
DYB	Volatile Sector Protection Command Set Entry (Note 21)	3	555	AA	2AA	55	(BA) 555	E0								
	DYB Set	2	XX	A0	(BA) SA	00										
	DYB Clear	2	XX	A0	(BA) SA	01										
	DYB Status Read	1	(BA) SA	RD(0)												
	Volatile Sector Protection Command Set Exit (note 24)	2	XX	90	XX	00										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

PD(0) = Secured Silicon Sector Lock Bit. PD(0), or bit[0].

PD(1) = Persistent Protection Mode Lock Bit. PD(1), or bit[1], must be set to '0' for protection while PD(2), bit[2] must be left as '1'.

PD(2) = Password Protection Mode Lock Bit. PD(2), or bit[2], must be set to '0' for protection while PD(1), bit[1] must be left as '1'.

PD(3) = Protection Mode OTP Bit. PD(3) or bit[3].

SA = Address of the sector to be verified (in autoselect mode) or erased. SA includes BA. Address bits A_{max}–A13 uniquely select any sector.

BA = Address of the bank (A23–A21 for S29NS256N, and A22–A20 for S29NS128N) that is being switched to autoselect mode, is in bypass mode, or is being erased.

CR = Configuration Register set by data bits D15-D0.

PWD3–PWD0 = Password Data. PD3–PD0 present four 16 bit combinations that represent the 64-bit Password

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0, if unprotected, DQ0 = 1.

RD(1) = DQ1 protection indicator bit. If protected, DQ1 = 0, if unprotected, DQ1 = 1.

RD(2) = DQ2 protection indicator bit. If protected, DQ2 = 0, if unprotected, DQ2 = 1.

RD(4) = DQ4 protection indicator bit. If protected, DQ4 = 0, if unprotected, DQ4 = 1.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A_{max}–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when bank is reading array data.*
8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
9. *The fourth cycle of the autoselect command sequence is a read cycle. The system must read device IDs across the 4th, 5th, and 6th cycles, The system must provide the bank address. See the Autoselect Command Sequence section for more information.*
10. *See Table 24 for description of bus operations.*
11. *See the "Autoselect Command Sequence" section on page 49.*
12. *The Unlock Bypass command sequence is required prior to this command sequence.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
15. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
16. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
17. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.*
18. *The entire four bus-cycle sequence must be entered for which portion of the password.*
19. *The ALL PPB ERASE command will pre-program all PPBs before erasure to prevent over-erasure of PPBs.*
20. *Command sequence resets device for next command after write-to-buffer operation.*
21. *Entry commands are needed to enter a specific mode to enable instructions only available within that mode.*
22. *Write Buffer Programming can be initiated after Unlock Bypass Entry.*
23. *If both the Persistent Protection Mode Locking Bit and the password Protection Mode Locking Bit are set a the same time, the command operation will abort and return the device to the default Persistent Sector Protection Mode.*
24. *The Exit command must be issued to reset the device into read mode. Otherwise the device will hang.*
25. *Note: Autoselect, CFI, OTP, Unlock Bypass Mode and all ASP modes cannot be nested with each other.*
26. *Only A7 - A0 (lower address bits) are used*
27. *A_{max}–A0 (all address bits) are used.*
28. *Requires the RESET# command to configure the configuration register.*
29. *See Figure 4 for details.*

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 28 on page 72 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. **Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page will return false status information.**

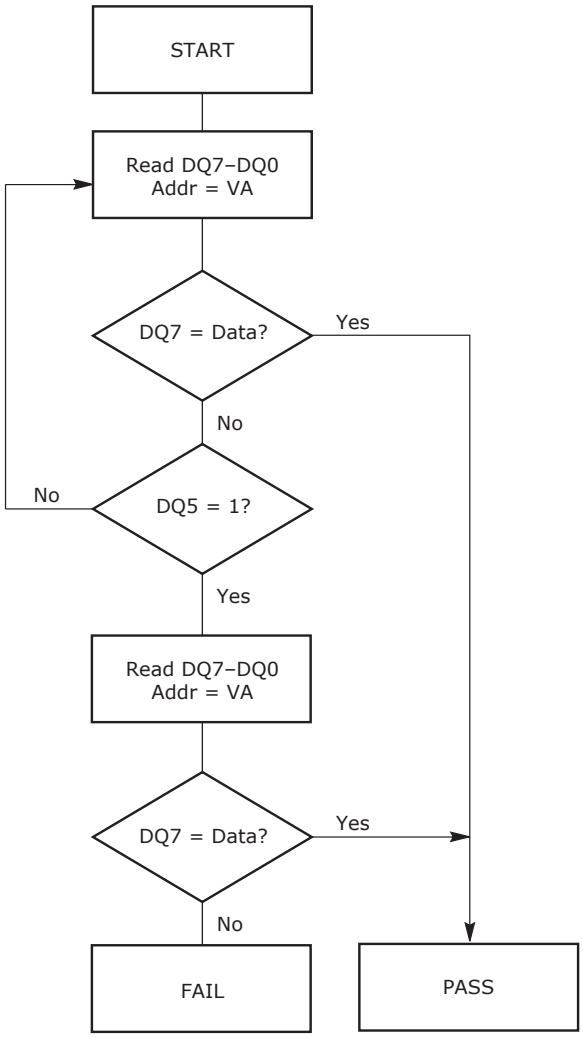
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately t_{PSP}, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{ASP}, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6–DQ0 may be still invalid. Valid data on DQ7–DQ0 will appear on successive read cycles.

Table 28 on page 72 shows the outputs for Data# Polling on DQ7. Figure 5, on page 67 shows the Data# Polling algorithm. Figure 19, on page 86 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RDY: Ready

The RDY pin is a dedicated status output that indicates valid output data on A/DQ15–A/DQ0 during burst (synchronous) reads. When RDY is asserted (RDY = V_{OH}), the output data is valid and can be read. When RDY is de-asserted (RDY = V_{OL}), the system should wait until RDY is re-asserted before expecting the next word of data.

In synchronous (burst) mode with CE# = OE# = V_{IL}, RDY is de-asserted under the following conditions: during the initial access; after crossing the internal boundary between addresses 7Eh and 7Fh (and addresses offset from these by a multiple of 64). The RDY pin will also switch during status reads when a clock signal drives the CLK input. In addition, RDY = V_{OH} when CE# = V_{IL} and OE# = V_{IH}, and RDY is Hi-Z when CE# = V_{IH}.

In asynchronous (non-burst) mode, the RDY pin does not indicate valid or invalid output data. Instead, RDY = V_{OH} when CE# = V_{IL}, and RDY is Hi-Z when CE# = V_{IH}.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase timeout.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. Note that OE# must be low during toggle bit status reads. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{ASP}, all sectors protected toggle time, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately t_{PSP} after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: (toggle bit flowchart), DQ6: Toggle Bit I (description), 20 (toggle bit timing diagram), and Table 27 on page 70 (compares DQ2 and DQ6).

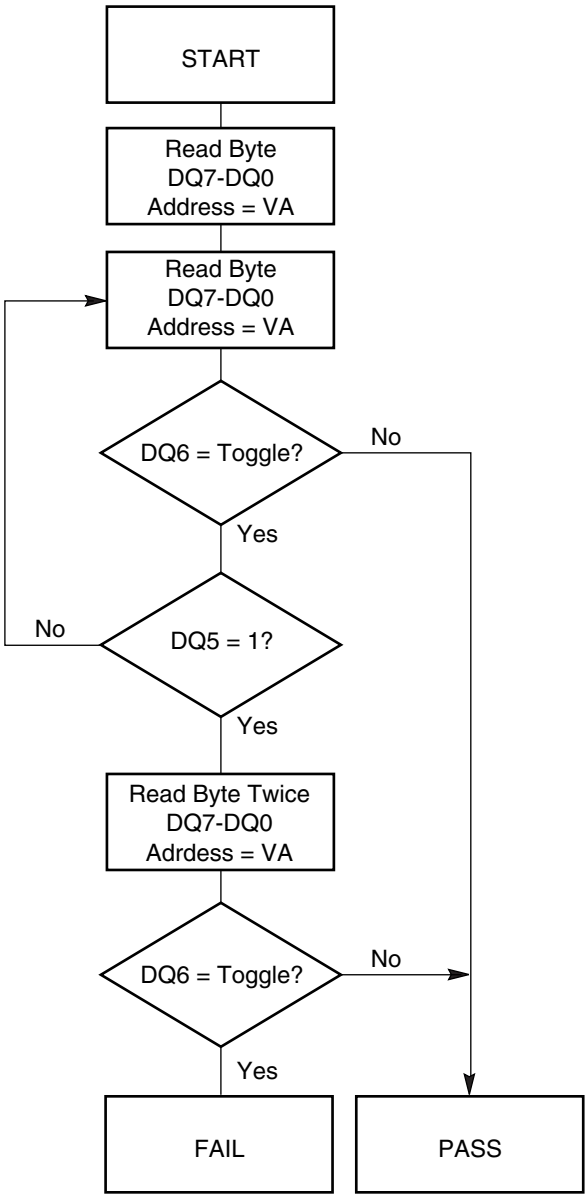
DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. Note that OE# must be low during toggle bit status reads. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sec-

tors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 28 on page 72 to compare outputs for DQ2 and DQ6.

See the following for additional information: (toggle bit flowchart), DQ6: Toggle Bit I (description), 20 (toggle bit timing diagram), and Table 27 on page 70 (compares DQ2 and DQ6).



Note:

The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.

Figure 6. Toggle Bit Algorithm

Table 27. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Start Timeout State Indicator

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 28 on page 72 shows the status of DQ3 relative to the other status bits.

DQ1: Write to Buffer Abort

DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a '1'. The system must issue the Write to Buffer Abort Reset command sequence to return the device to reading array data. See "Write Buffer Programming Operation" on page 23 for more details.

Table 28. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1 (Note 4)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A
Program Suspend Mode (Note 3)	Reading within Program Suspended Sector		Valid data for all address except the address being programed, which will return invalid data					
	Reading within Non-Program Suspended Sector		Data					
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	N/A
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	Data
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	N/A
Write to Buffer (Note 5)	BUSY State		DQ7#	Toggle	0	N/A	N/A	0
	Exceeded Timing Limits		DQ7#	Toggle	1	N/A	N/A	0
	ABORT State		DQ7#	Toggle	0	N/A	N/A	1

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *Data are invalid for addresses in a Program Suspended sector.*
4. *DQ1 indicates the Write to Buffer ABORT status during Write Buffer Programming operations.*
5. *The data-bar polling algorithm should be used for Write Buffer Programming operations. Note that DQ7# during Write Buffer Programming indicates the data-bar for DQ7 data* ***for the LAST LOADED WRITE-BUFFER ADDRESS location****.*

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Voltage with Respect to Ground, All Inputs and I/Os except V_{PP} (Note 1)	−0.5 V to V_{CC} + 0.5 V
V_{CC} (Note 1)	−0.5 V to +2.5 V
V_{PP} (Note 2)	−0.5 V to + 9.5 V
Output Short Circuit Current (Note 3)	100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is −0.5 V. During voltage transitions, input at I/Os may undershoot V_{SS} to −2.0 V for periods of up to 20 ns during voltage transitions inputs might overshooot to V_{CC} +0.5 V for periods up to 20 ns. See Figure 7. Maximum DC voltage on output and I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on V_{PP} is −0.5 V. During voltage transitions, V_{PP} may undershoot V_{SS} to −2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on V_{PP} is +9.5 V which may overshoot to +10.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

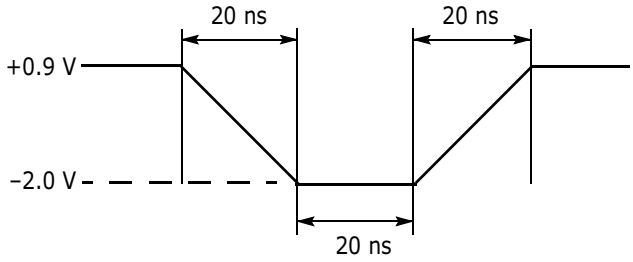


Figure 7. Maximum Negative Overshoot Waveform

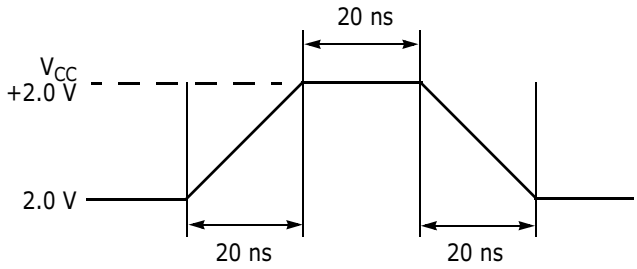


Figure 8. Maximum Positive Overshoot Waveform

Operating Ranges

Ambient Temperature (T_A)	−25°C to +85°C
Ambient Temperature (T_A) during Accelerated Sector Erase	+20°C to +40°C

V_{CC} Supply Voltages

V_{CC} min	+1.70 V
V_{CC} max	+1.95 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

CMOS Compatible

Parameter	Description	Test Conditions (Note 1)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{CCB}	V_{CC} Active Burst Read Current (Note 5)	CE# = V_{IL}, OE# = V_{IL}, burst length = 8	80 MHz		26	36	mA
			66 MHz		24	33	
		CE# = V_{IL}, OE# = V_{IL}, burst length = 16	80 MHZ		26	38	mA
			66 MHz		24	35	
		CE# = V_{IL}, OE# = V_{IL}, burst length = 32	80 MHZ		28	40	mA
			66 MHz		26	37	
		CE# = V_{IL}, OE# = V_{IL}, burst length = continuous	80 MHZ		30	42	mA
			66 MHz		28	39	
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 2)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		15	18	mA
			1 MHz		3	4	mA
I_{CC2}	V_{CC} Active Write Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}, $V_{PP} = V_{IH}$			19	52.5	mA
I_{CC3}	V_{CC} Standby Current (Note 4)	CE# = V_{IH}, RESET# = V_{IH} (Note 8)			20	70	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL} (Note 8)			80	150	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IL} (Note 8) (Note 9)			50	60	mA
I_{CC6}	V_{CC} Sleep Current	CE# = V_{IL}, OE# = V_{IH}			20	70	µA
I_{PPW}	Accelerated Program Current (Note 6)	V_{PP} = 9 V			20	30	mA
I_{PPE}	Accelerated Erase Current (Note 6)	V_{PP} = 9 V			20	30	mA
V_{IL}	Input Low Voltage			–0.5		0.4	V
V_{IH}	Input High Voltage			V_{IO} – 0.4		V_{IO} + 0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{IO} – 0.1			V
V_{ID}	Voltage for Accelerated Program			8.5		9.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 20 ns. Typical sleep mode current is equal to I_{CC3}.*
5. *Specifications assume 8 I/Os switching.*

6. *Not 100% tested. V_{PP} is not a power supply pin.*
7. *While measuring Output Leakage Current, CE# should be at V_{IH}.*
8. *$V_{IH} = V_{CC} \pm$ -0.2 V and $V_{IL} >$ -0.1V.*
9. *Clock Frequency 66 MHz and in Continuous Mode.*

Test Conditions

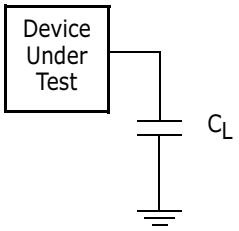
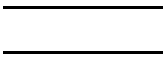
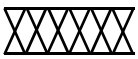
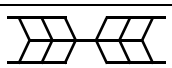


Figure 9. Test Setup

Table 29. Test Specifications

Test Condition	All Speeds	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	2.5 @ 80 MHz, 3 @ 66 MHz	ns
Input Pulse Levels	0.0–V_{CC}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Switching Waveforms

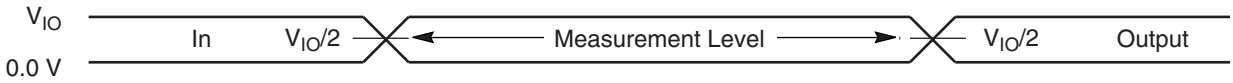


Figure 10. Input Waveforms and Measurement Levels

AC Characteristics

V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	1	ms

Notes:
1. *V_{CC} >+ V_{CCQ} - 100mV and VCC ramp rate is >1V/100µs*
2. *VCC ramp rate <1V/100µs, Hardware Reset will be required*

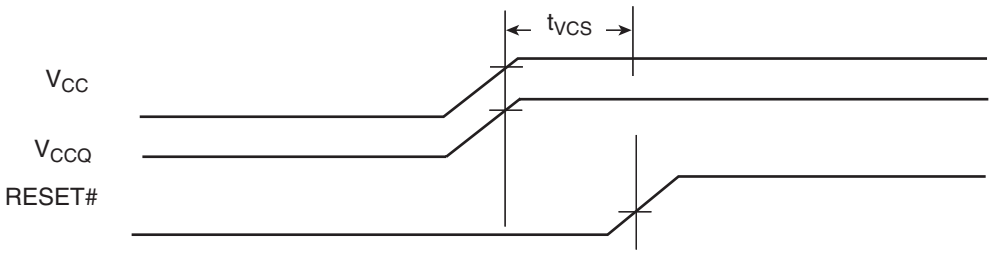


Figure 11. V_{CC} Power-up Diagram CLK Characterization

Parameter	Description		(80 MHz)	(66 MHz)	Unit
f_{CLK}	CLK Frequency	Max	80	66	MHz
t_{CLK}	CLK Period	Min	12.5	15.0	ns
t_{CH}	CLK High Time	Min	5	6.1	ns
t_{CL}	CLK Low Time				
t_{CR} (Note)	CLK Rise Time	Max	2.5	3	ns
t_{CF} (Note)	CLK Fall Time				

Notes:
1. *Not 100% tested.*

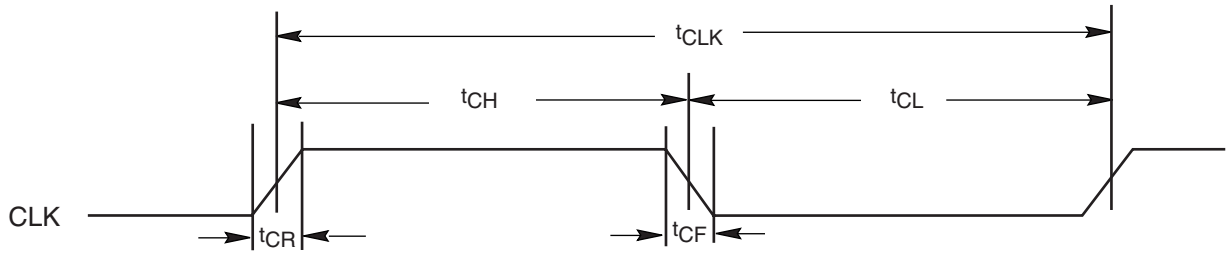


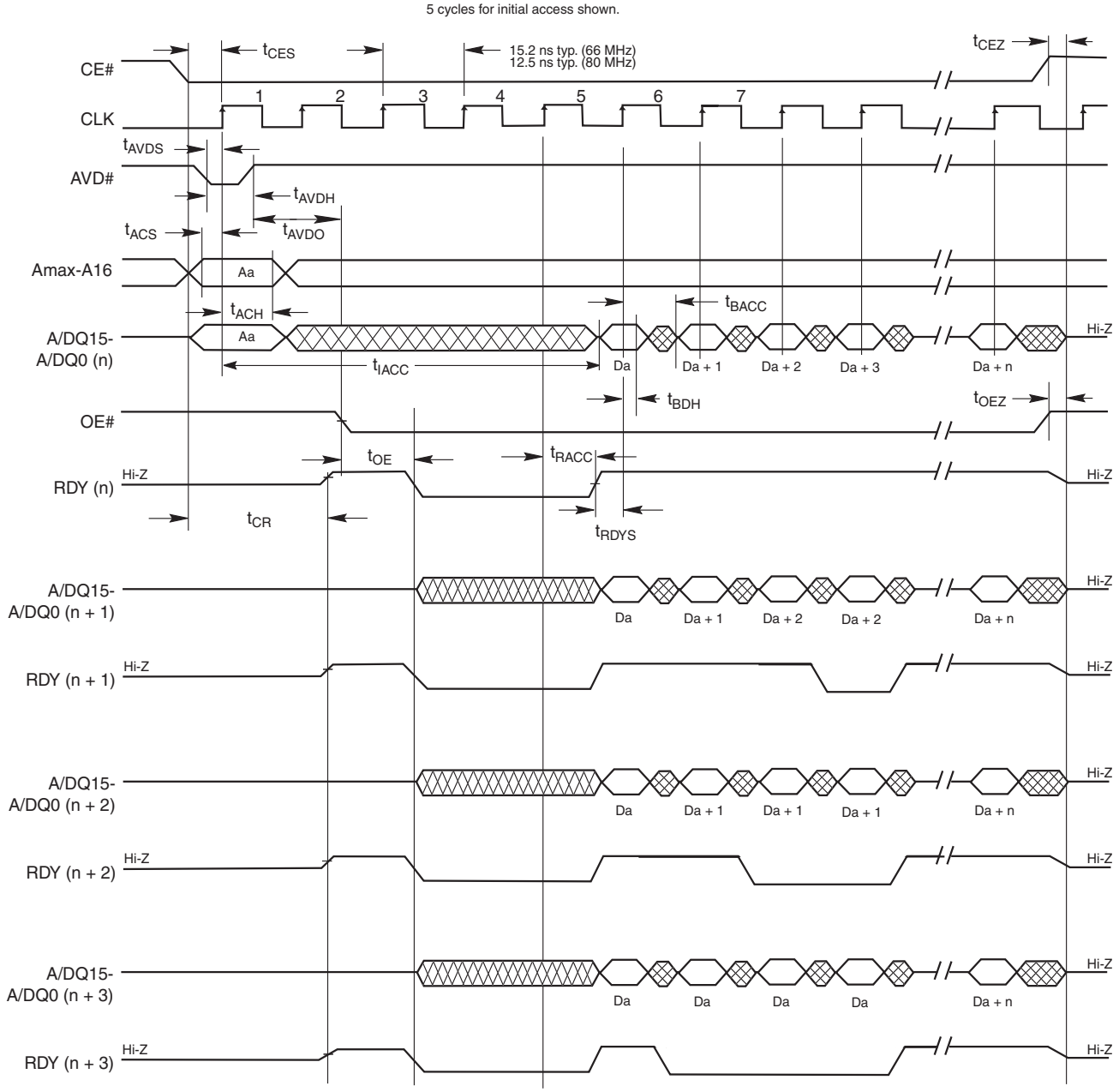
Figure 12. CLK Characterization

AC Characteristics

Synchronous/Burst Read

Parameter						
JEDEC	Standard	Description		(80 MHz)	(66 MHz)	Unit
	t_{IACC}	Initial Access Time	Max	80		ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	9	11.0	ns
	t_{AVDS}	AVD# Setup Time to CLK	Min	4	4	ns
	t_{AVDH}	AVD# Hold Time from CLK	Min	6	6	ns
	t_{AVDO}	AVD# High to OE# Low	Min	0		ns
	t_{ACS}	Address Setup Time to CLK	Min	4	4	ns
	t_{ACH}	Address Hold Time from CLK	Min	6	6	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	3	3	ns
	t_{OE}	Output Enable to Data, or RDY Valid	Max	9	11.0	ns
	t_{CEZ}	Chip Enable to High Z (Note)	Max	8	10	ns
	t_{OEZ}	Output Enable to High Z (Note)	Max	8	10	ns
	t_{CES}	CE# Setup Time to CLK	Min	4		ns
	t_{RDYS}	RDY Setup Time to CLK	Min	3.5	4	ns
	t_{RACC}	Ready access time from CLK	Max	9	11.0	ns

Note: *Not 100% tested.*



Notes:

1. *Figure shows total number of clock set to five.*
2. *If any burst address occurs at "address + 1", "address + 2", or "address +3", additional clock delays are inserted, and are indicated by RDY.*

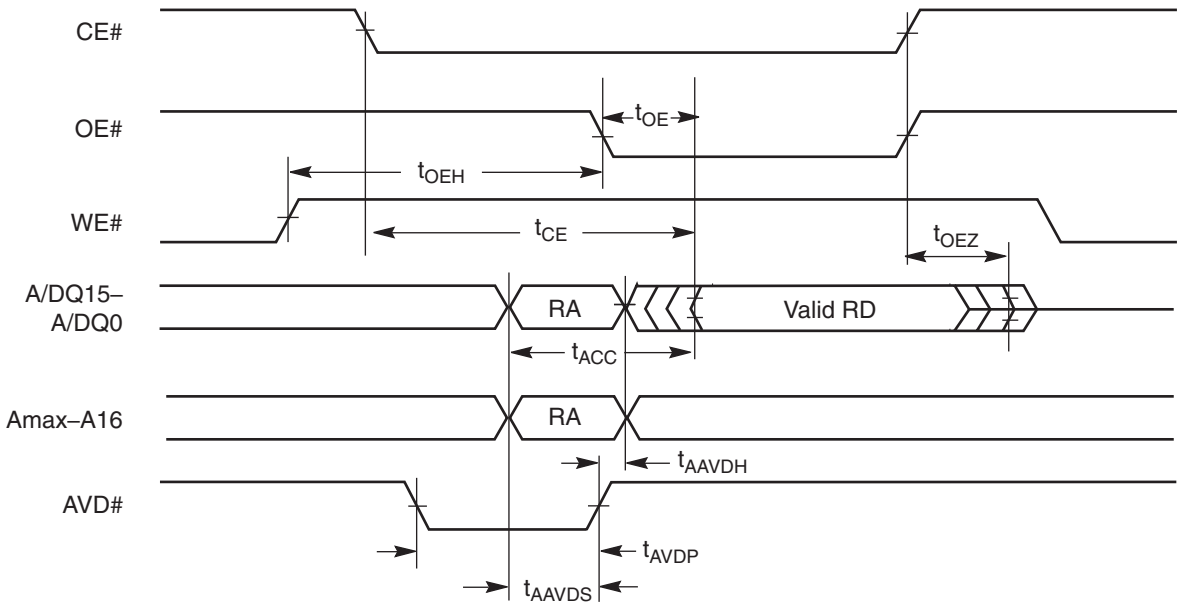
Figure 13. Burst Mode Read

AC Characteristics

Asynchronous Read

Parameter		Description			(80 MHz)	(66 MHz)	Unit
JEDEC	Standard						
	t_{CE}	Access Time from CE# Low		Max	80		ns
	t_{ACC}	Asynchronous Access Time		Max	80		ns
	t_{AVDP}	AVD# Low Time		Min	8		ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	4	4	ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	6	6	ns
	t_{OE}	Output Enable to Output Valid		Max	9	11.0	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	10		ns
	t_{OEZ}	Output Enable to High Z (See Note)		Max	10		ns

Note: *Not 100% tested.*



Note: *RA = Read Address, RD = Read Data.*

Figure 14. Asynchronous Mode Read

AC Characteristics

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{RP}	RESET# Pulse Width	Min	200	ns
	t_{RH}	Reset High Time Before Read	Min	10	µs

Note: *Not 100% tested.*

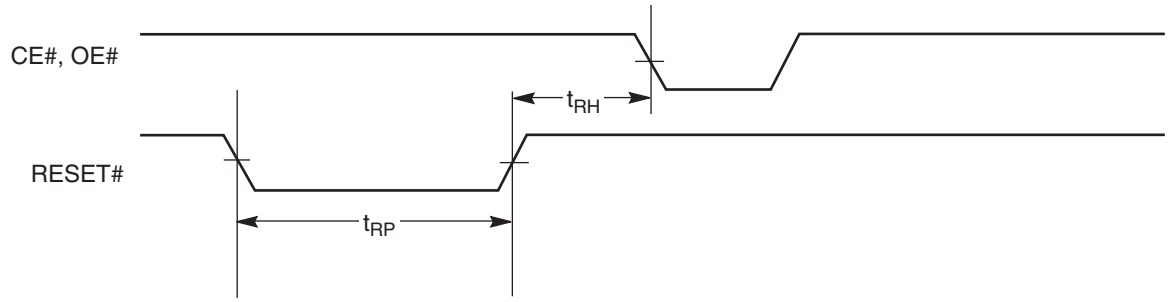


Figure 15. Reset Timings

AC Characteristics

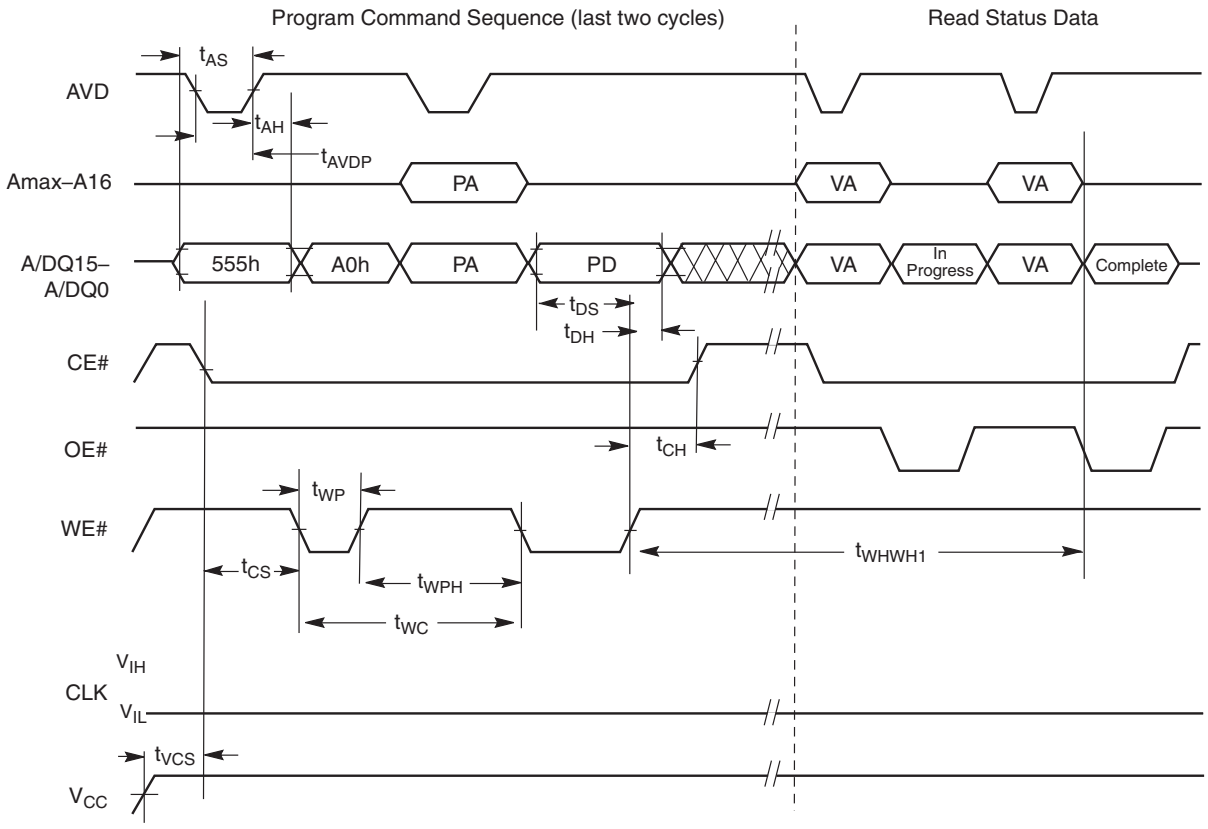
Erase/Program Operations

Parameter						
JEDEC	Standard	Description		(80 MHz)	(66 MHz)	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	45	45	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	4	4	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	6	6	ns
	t_{AVDP}	AVD# Low Time	Min	8		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	20	25	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write	Typ	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Typ	4	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Typ	0		ns
t_{WLWH}	t_{WP}/t_{WRL}	Write Pulse Width	Typ	30		ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Typ	20		ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0		ns
	t_{VPP}	V_{PP} Rise and Fall Time	Min	500		ns
	t_{VPS}	V_{PP} Setup Time (During Accelerated Programming)	Min	1		µs
	t_{VCS}	V_{CC} Setup Time	Min	50		µs
	t_{SEA}	Sector Erase Accept Time-out	Max	50		µs
	t_{ESL}	Erase Suspend Latency	Max	35		µs
	t_{PSL}	Program Suspend Latency	Max	35		µs
	t_{PSP}	Toggle Time During Programming Within a Protected Sector	Typ	1		µs
	t_{ASP}	Toggle Time During Sector Protection	Typ	100		µs
	t_{WEP}	Noise Pulse Margin on WE#	Max	3		ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*
3. *Does not include the preprogramming time.*

AC Characteristics

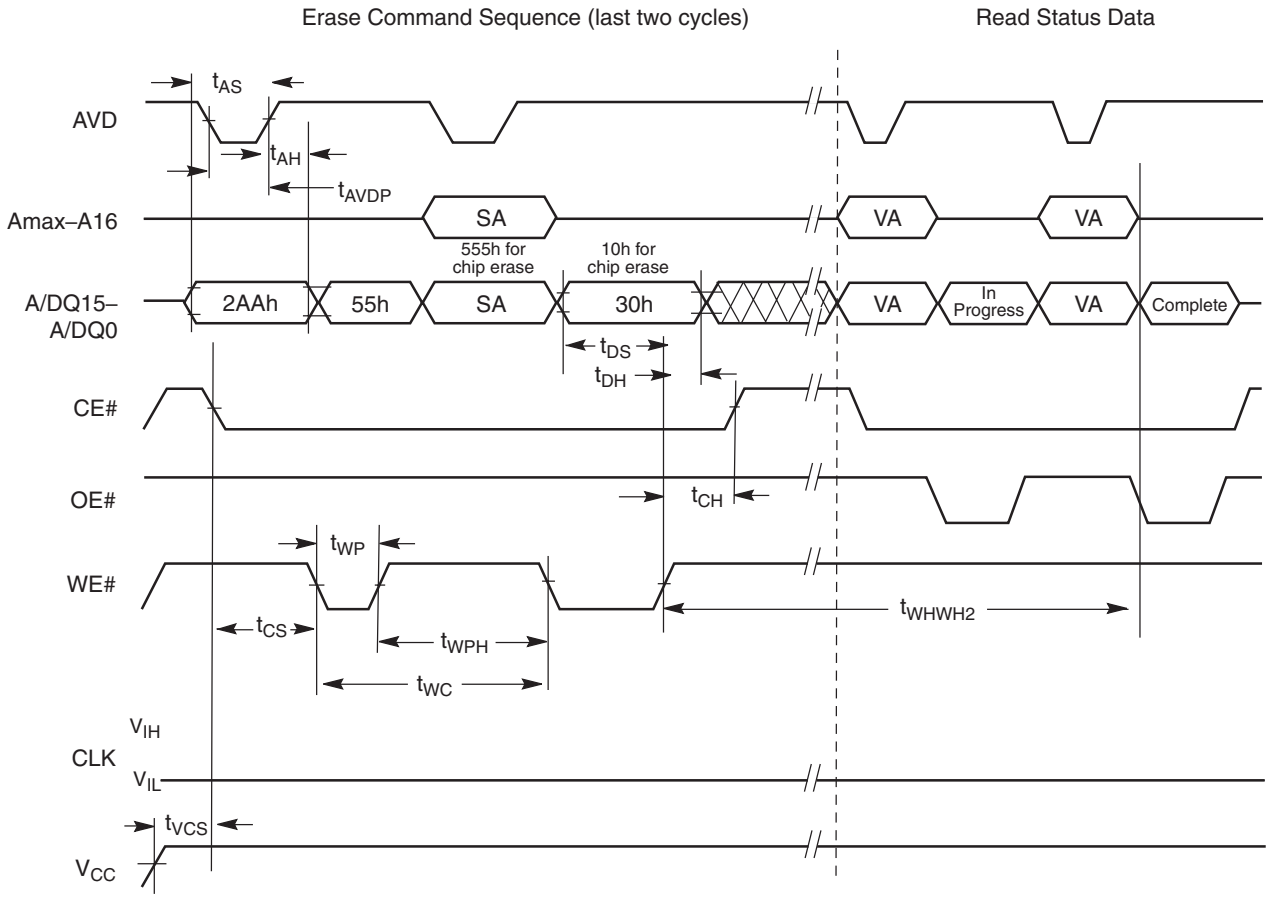


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A_{max}–A16 are don't care during command sequence unlock cycles.*

Figure 16. Program Operation Timings

AC Characteristics

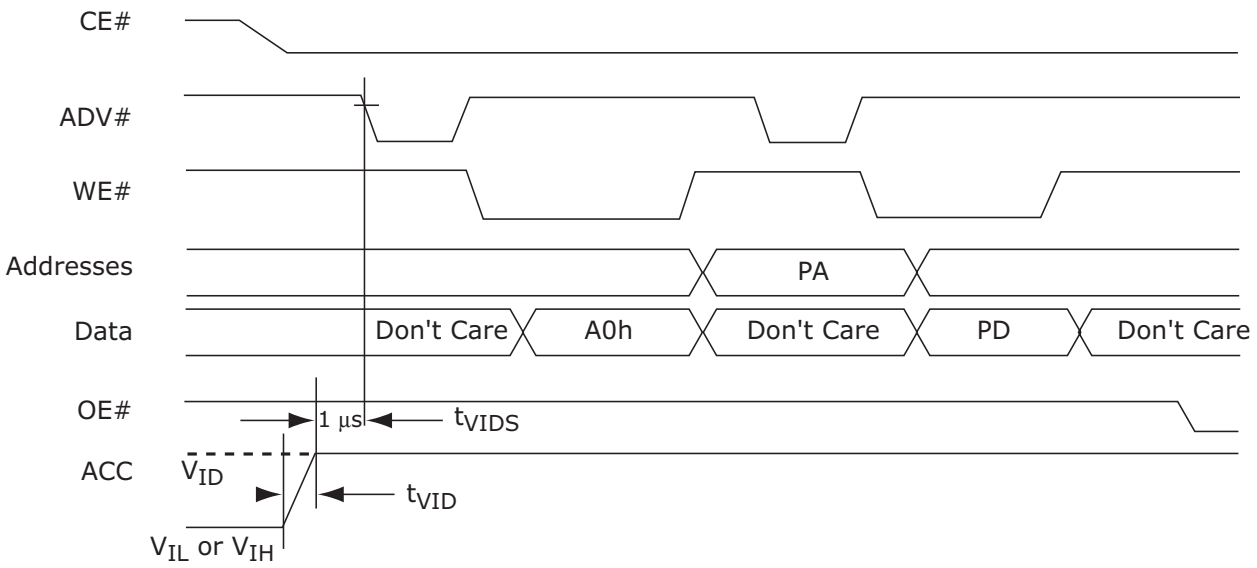


Notes:

1. *SA is the sector address for Sector Erase.*
2. *Address bits A_{max}–A16 are don't cares during unlock cycles in the command sequence.*

Figure 17. Chip/Sector Erase Operations

AC Characteristics

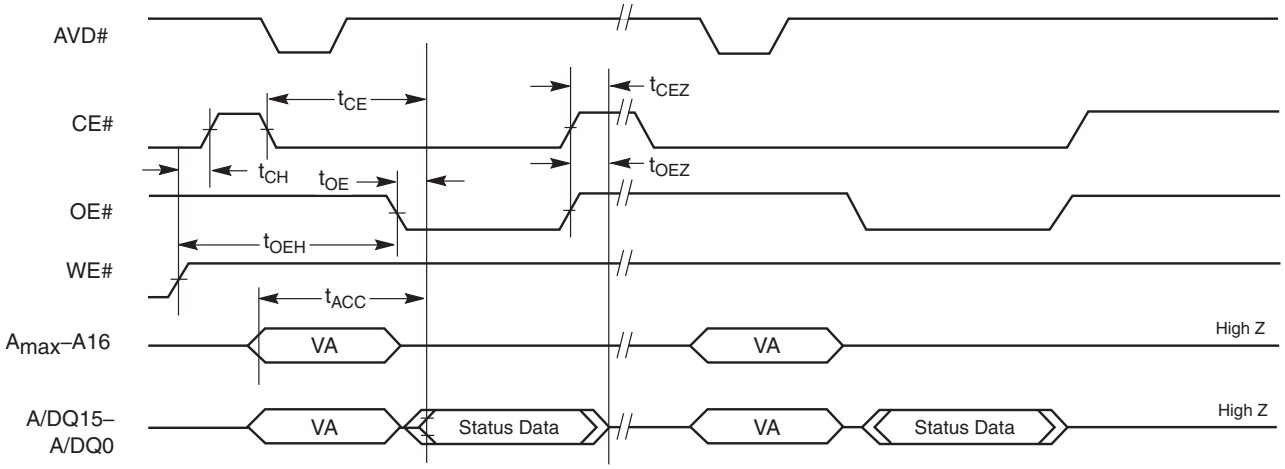


Notes:

1. *V_{PP} can be left high for subsequent programming pulses.*
2. *Use setup and hold times from conventional program operation.*

Figure 18. Accelerated Unlock Bypass Programming Timing

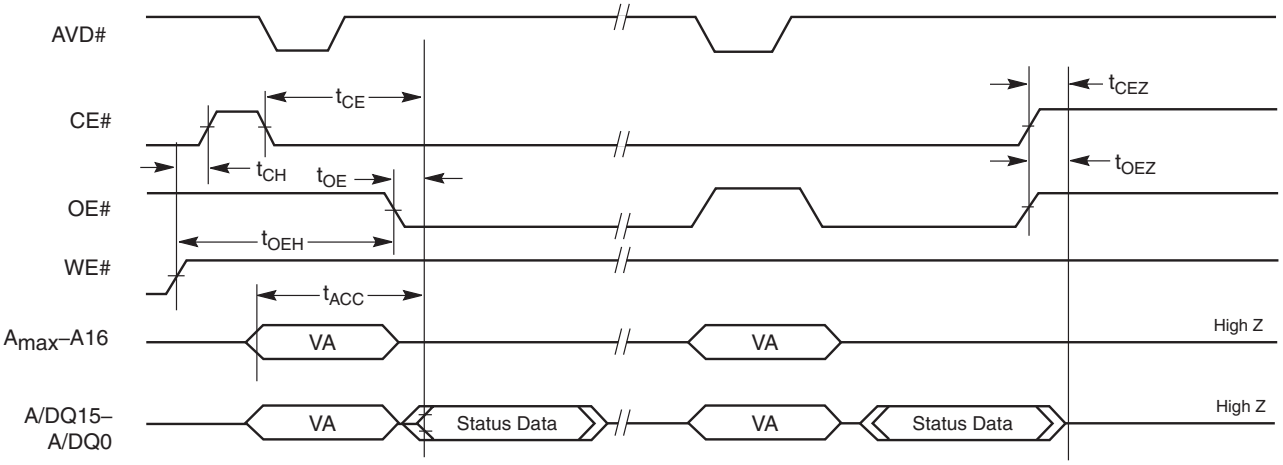
AC Characteristics



Notes:

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*

Figure 19. Data# Polling Timings (During Embedded Algorithm)

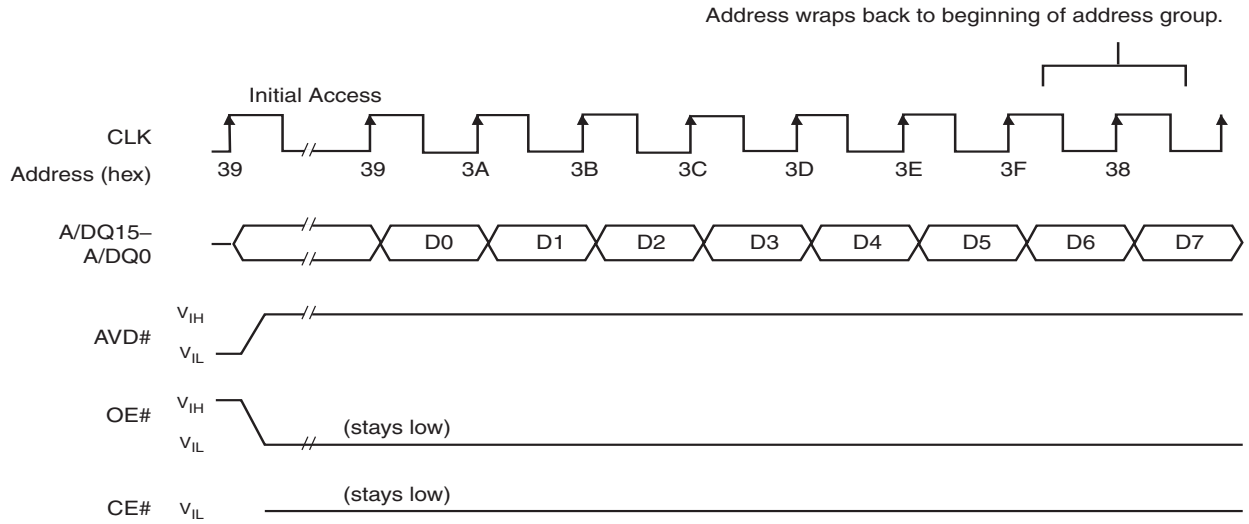


Notes:

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*

Figure 20. Toggle Bit Timings (During Embedded Algorithm)

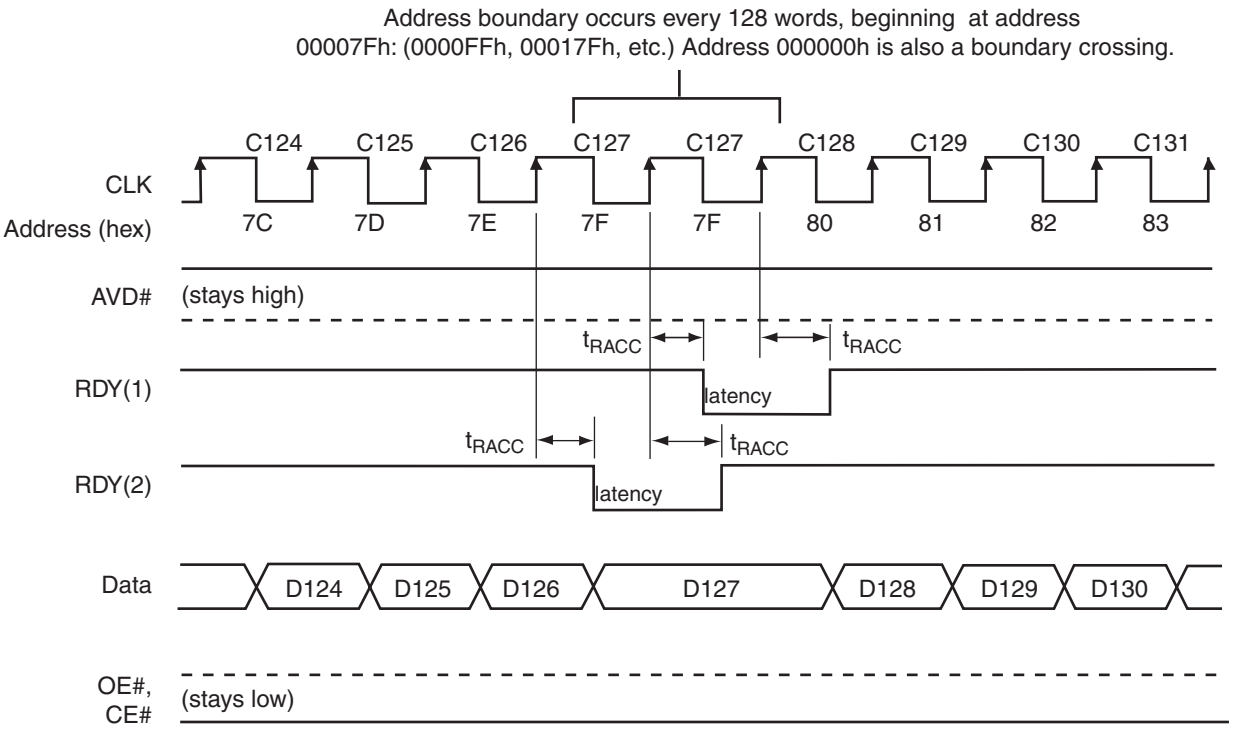
AC Characteristics



Note: *8-word linear burst mode shown. 16- and 32-word linear burst read modes behave similarly.*

D0 represents the first word of the linear burst.

Figure 21. 8-, 16-, and 32-Word Linear Burst Address Wrap Around

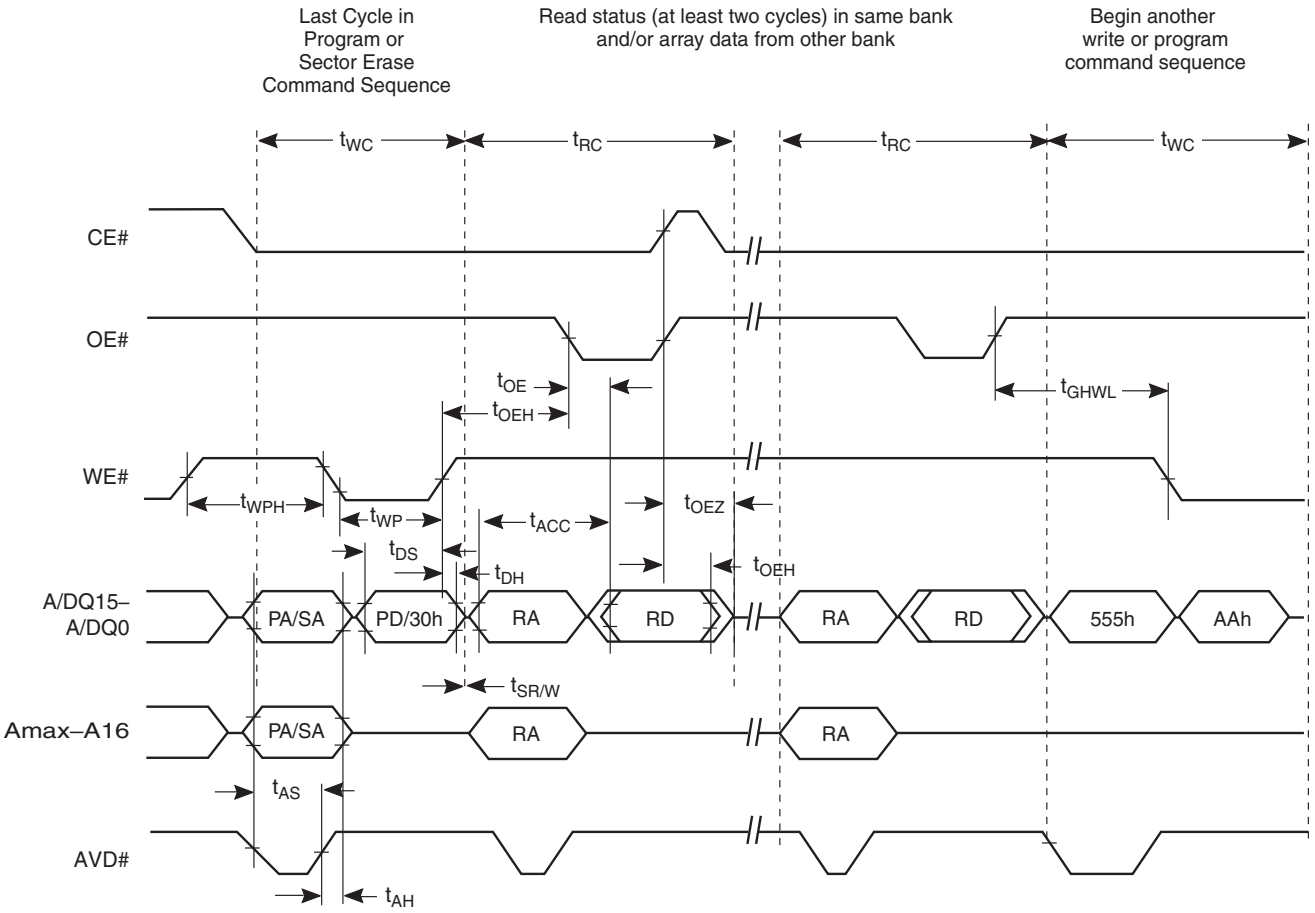


Notes:

1. *Cxx indicates the clock that triggers data Dxx on the outputs; for example, C60 triggers D60.*
2. *At frequencies less than or equal to 66 Mhz, there is no latency.*

Figure 22. Latency with Boundary Crossing

AC Characteristics



Note: *Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.*

Figure 23. Back-to-Back Read/Write Cycle Timings

Erase and Programming Performance

Parameter			Typ (Note l)	Max (Note 2)	Unit	Comments
Sector Erase Time	64 Kword	V_{CC}	0.8	3.5	s	Excludes 00h programming prior to erasure (Note 5)
	16 Kword	V_{CC}	<0.15	2		
Chip Erase Time		V_{CC}	154 (NS256N) 77 (NS128N)	308 (NS256N) 154 (NS128N)	s	
		V_{PP}	131 (NS256N) 66 (NS128N)	262 (NS256N) 132 (NS128N)		
Single Word Programming Time		V_{CC}	40	400	µs	
		V_{PP}	24	240		
Effective Word Programming Time utilizing Program Write Buffer		V_{CC}	9.4	94	µs	
		V_{PP}	6	60		
Total 32-Word Buffer Programming Time		V_{CC}	300	3000	µs	
		V_{PP}	192	1920		
Chip Programming Time (Note 4)		V_{CC}	157.3 (NS256N) 78.6 (NS128N)	314.6 (NS256N) 157.3 (NS128N)	s	Excludes system level overhead (Note 6)
		V_{PP}	100.7 (NS256N) 50.3 (NS128N)	201.3 (NS256N) 100.7 (NS128N)		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 10,000 cycles typical. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.70 V, 100,000 cycles.*
3. *Effective write buffer specification is based upon a 32-word write buffer operation.*
4. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
5. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
6. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table for further information on command definitions.*

Device History

Device	Revision	Extended Code (Hex)	Major Reason(s) for Change
NS256N	ES1	0x012Eh	Initial release.
	ES2	0x012Dh	Errata Fix
NS128N	ES1	0x012Eh	Initial release, 66 MHz
	ES1	0x011Eh	Initial Release, 54 MHz

Flash Module Revision Summary

Revision A (April l6, 2004)

Initial Release.

Revision Al (June 28, 2004)

General Description

Corrected the effective temperature range to -25°C to +85°C.

Connection Diagram

Corrected pin B5 on the S29NS256N to A23.

Corrected pin B1 on the S29NS256N to V_{CC}.

Corrected pin B1 on the S29NS128N to V_{CC}.

Corrected pin B1 on the S29NS064N to V_{CC}.

Created separate illustrations for S29NS128N and S29NS064N.

Ordering Information

Corrected the Package Type offerings.

Valid Combinations table

Included package type description for S29NS064N device.
Completely revised format and layout.

8-, 16-, and 32-Word Linear Burst without Wrap Around

Corrected information in this section.

Lock Register

Section and table were substantially revised.

Programmable Wait State

Corrected information in this section.

Handshaking Feature

Corrected information in this section.

Autoselect Command Sequence

Corrected information in this section.

Physical Dimensions

Corrected the drawing for the S29NS064N device.

Write Buffer Command Sequence

Corrected the address for the Write Buffer Load sequence.

Revision A2 (September 9, 2004)

Connection Diagrams

Updated pin labels.

Ordering Information

Completely updated the OPN table.

Valid Combinations table

Updated this table.

Continuous Burst

Added information to this section.

Lock Register
Updated the lock register table.

Configuration Register
Updated the settings for CR15.

Device ID table
Updated the indicator bits information.

Figure 7
Updated the waveform.

Figure 21
Updated the waveform.

Revision A3 (November l6, 2004)

Table . ””
Updated the data values for addresses 45h, 53h, and 54h.

Global
Updated the synchronous and asynchronous access times.

Programmable Wait State
Updated this section.

Write Buffer Programming Command Sequence
Added a note to the table.

Revision A3a (April 5, 2005)

Global
Updated reference links.

Distinctive Characteristics
Added note to ACC is represented as V_{PP} in older documentation.

General Description
Added note regarding ACC and V_{PP}.

Block Diagram
Added same note regarding ACC and V_{PP}.

Added WP# term and arrow to State Control and Command Register block.

Block Diagram of Simultaneous Operation Circuit
Changed V_{PP} to V_{ssq}.

Added WP# term and arrow to State Control and Command Register block.

Added ACC term and arrow to State Control and Command Register block.

Added note to ACC is represented as V_{PP} in older documentation.

Input/Output Description
Added V_{PP} term adjacent to ACC term.

Tables 2, 3, 4, 5, 6, 7, 8, and 9
Change Wait State titles and columns in these tables.

Table 24
Changed Function column and Settings to represent Reserved CR Bits.

Table 27

Removed several bold lines between columns.

DC Characteristics

Reduced Typ and Max values for I_{CCB}.

Added note for clock frequency in continuous mode.

Erase & Programming Performance Table

Corrected Sector Erase Time Typ. Value for 64 Kword from 0.6 to 0.8 in Erase and Programming Performance table

Physical Dimensions (S29NS046N)

Replaced VDE044 with new package drawing.

Device History

Updated Device History table

Revision A4 Flash Module (April 2I, 2005)

Global Changes

Removed all ordering options and package information listed in revision A4 of the discrete data sheet.

Removed 64Mb density.

Removed 54MHz speed option.

Changed ACC to $V_{PP.}$

Read Access Times

Removed burst access for 54MHz.

Defined asynchronous random access and synchronous random access to 80 ns for all speed options.

DC Characteristics

CMOS Compatible Table.

Updated I_{CC3} and I_{CC6} values from 40µA to 70µA.

Mobile SDRAM Type I

I28 Mbit (8M x I6Bit) SDRAM

Features

- Temperature compensated self refresh (TCSR)
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes concurrent auto precharge, and Auto Refresh Modes
- Self Refresh Mode; standard and low power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Low voltage power supply
- Partial array self refresh power-saving mode
- Deep power-down mode
- Programmable output drive strength
- Operating temperature range:
  - — Extended (-25°C to +85°C)
- V_{DD}/V_{DDQ}: 1.8 V/1.8 V

Speed Options

Speed Grade	Clock Frequency	Access Time		Setup Time	Hold Time
		CL = 2	CL = 3		
-75	133 MHz	—	5.4 ns	2.5 ns	1 ns
	100 MHz	6 ns	—	2.5 ns	1 ns
-10	104 MHz	—	7 ns	2.5 ns	1 ns
	83.3 MHz	8 ns	—	2.5 ns	1 ns

Address Table

	8M x I6
Configuration	2 M x 16 x 4 banks
Refresh Count	4K
Row Addressing	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	512 (A1–A8)

General Description

The 128Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16s 32,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 128Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 128Mb SDRAM is designed to operate in 1.8V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, Deep Power-Down Mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

Functional Block Diagram

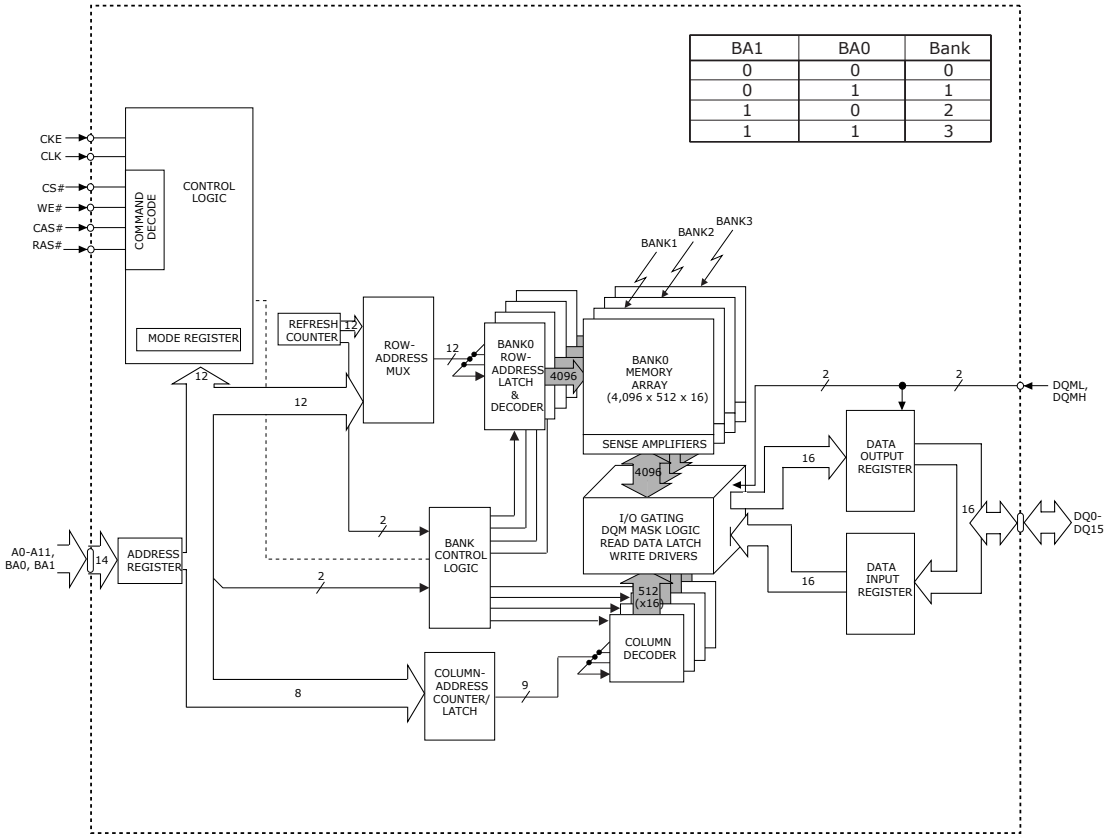


Figure 24. Block Diagram

Pin Descriptions

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable: CKE activates (High) and deactivates (Low) the CLK signal. Deactivating the clock provides Precharge Power-Down and Self Refresh operation (all banks idle), Active Power-Down (row active in any bank), Deep Power Down (all banks idle), or Clock Suspend operation (burst/ access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied High.
CS#	Input	Chip Select: CS# enables (registered Low) and disables (registered High) the command decoder. All commands are masked when CS# is registered High. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	Command Inputs: CAS#, RAS#, and WE# (along with CS#) define the command being entered.
LDQM, UDQM	Input	Input/Output Mask: DQM is sampled High and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a Write cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a Read cycle. LDQM corresponds to DQ0–DQ7, UDQM corresponds to DQ8–DQ15. LDQM and UDQM are considered same state when referenced as DQM.
BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the Active, Read, Write or Precharge command is being applied. These pins also select between the mode register and the extended mode register.
A0-A11	Input	Address Inputs: A0–A11 are sampled during the Active command (row address A0–A11) and Read/Write command (column-address A0–A7; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine if all banks are to be precharged (A10 High) or bank selected by BA0, BA1 (Low). The address inputs also provide the op-code during a Load Mode Register command.
DQ0-DQ15	I/O	Data Input/Output: Data bus
NC	—	Internally Not Connected: These could be left unconnected, but it is recommended they be connected or VSS. G1 is a no connect for this part but may be used as A12 in future designs.
V_{DDQ}	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
V_{SSQ}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
V_{DD}	Supply	Core Power Supply.
V_{SS}	Supply	Ground.

Functional Description

In general, the 128Mb SDRAMs (2 M x 16 x 4 banks) are quad-bank DRAMs that operate at 1.8V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each bank (x16 32,554,432-bit) is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0–A11 select the row). The address bits (A1–A8) registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power should be applied to V_{DD} and V_{DDQ} simultaneously. This time delay should not exceed 2ms. Once the power is applied to V_{DD} and V_{DDQ}, and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a Command Inhibit or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, Command Inhibit or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one Command Inhibit or NOP command having been applied, a Precharge command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two Auto refresh cycles must be performed. After the Auto refresh cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

In order to achieve low power consumption, there are two mode registers in the Mobile component, Mode Register and Extended Mode Register. The mode register is illustrated in Figure 25, Mode Register Definition, on page 99 (the extended mode register is illustrated in Figure 27).

The mode register defines the specific mode of operation of the SDRAM, including burst length, burst type, CAS latency, operating mode and write burst mode. The mode register is programmed via the Load Mode Register command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10, and M11 should be set to zero. M12 and M13 should be set to zero to prevent extended mode register.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4, Mode Register Definition, on page 9. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the Burst Terminate command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A8 when the burst length is set to two; by A2–A8 when the burst length is set to four; and by A3–A8 when the burst length is set to eight.

Table 30. Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within A Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0–A8 (location 0-y)			Cn, Cn+1, Cn+2, Cn+3, Cn+4..., …Cn-1, Cn…	Not Supported

Notes:

1. *For full-page accesses: y = 512.*
2. *For a burst length of two, A1–A8 select the block-of-two burst; A0 selects the starting column within the block.*
3. *For a burst length of four, A2–A8 select the block-of-four burst; A0–A1 select the starting column within the block.*
4. *For a burst length of eight, A3–A8 select the block-of-eight burst; A0–A2 select the starting column within the block.*
5. *For a full-page burst, the full row is selected and A0–A8 select the starting column.*
6. *Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.*
7. *For a burst length of one, A0–A8 select the unique column to be accessed, and mode register bit M3 is ignored.*

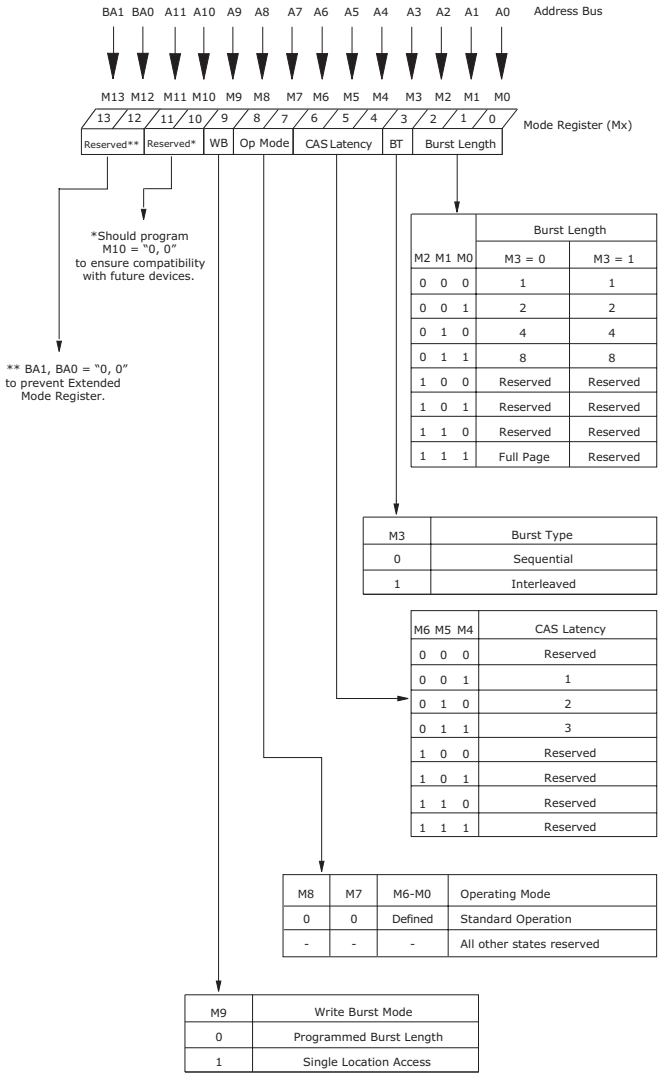


Figure 25. Mode Register Definition

The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 30.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a Read command and the availability of the first piece of output data. The latency can be set to one, two, or three clocks.

If a Read command is registered at clock edge *n*, and the latency is m clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - *1*), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access

times are met, if a read command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 26, CAS Latency. Table 31: CAS Latency, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

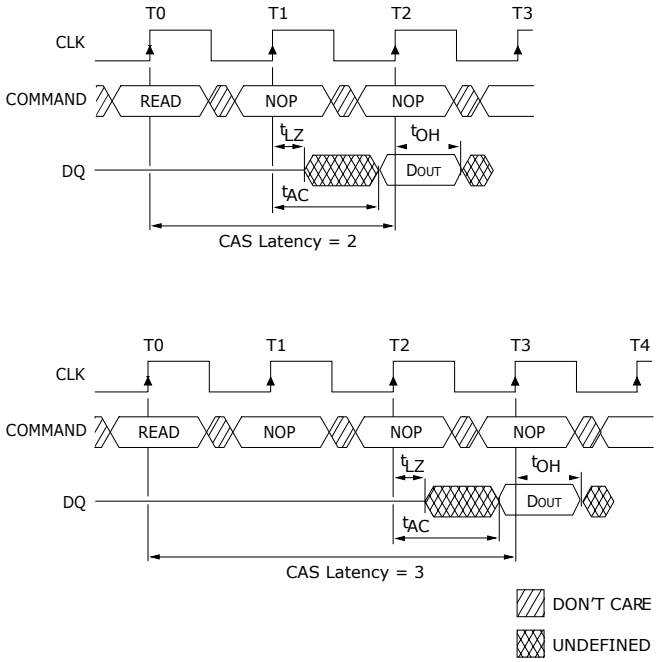


Figure 26. CAS Latency

Table 31. CAS Latency

Speed	Allowable Operating Frequency MHz	
	CAS Latency = 2	CAS Latency = 3
-75	≤ 100	≤ 133
-10	≤ 83.3	≤ 104

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both read and write bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both Read and Write bursts; when M9= 1, the programmed burst length applies to Read bursts, but write accesses are single-location (nonburst) accesses.

Extended Mode Register

The Extended Mode Register controls the functions beyond those controlled by the Mode Register. These additional functions are special features of the Mobile device. They include Temperature Compensated Self Refresh (TCSR) Control, Partial Array Self Refresh (PASR), and Output Drive Strength. Not programming the Extended Mode Register upon initialization, will result in default settings for the Low Power features. The Extended Mode will default to the +85°C setting for TCSR, full drive strength, and full array refresh.

The Extended Mode Register is programmed via the Mode Register Set command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be programmed with E6 through E11 set to "0". It must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

Once the values are entered the Extended Mode Register settings will be retained even after exiting Deep Power-Down.

Temperature Compensated Self Refresh

Temperature Compensated Self Refresh (TCSR) allows the controller to program the Refresh interval during Self Refresh mode, according to the case temperature of the Mobile device. This allows great power savings during Self Refresh during most operating temperature ranges. Only during extreme temperatures would the controller have to select the maximum TCSR level. This would guarantee data during Self Refresh.

Every cell in the SDRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. Historically, during Self Refresh, the refresh rate has been set to accommodate the worst case, or highest temperature range expected.

Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high, because the refresh rate was set to accommodate the higher temperatures. Adjusting the refresh rate by setting E4 and E3 allows the SDRAM to accommodate more specific temperature regions during Self Refresh. There are four temperature settings, which will vary the Self Refresh current according to the selected temperature. This selectable refresh rate will save power when the SDRAM is operating at normal temperatures.

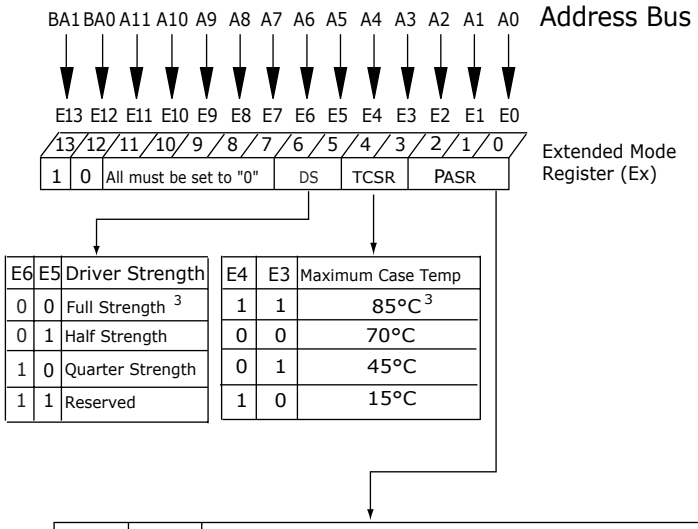
Partial Array Self Refresh

For further power savings during Self Refresh, the Partial Array Self Refresh (PASR) feature allows the controller to select the amount of memory that will be refreshed during Self Refresh. The refresh options are all banks (banks 0, 1, 2, and 3); two banks (banks 0 and 1); and one bank (bank 0). Also included in the refresh options are the 1/2 bank and 1/4 bank partial array self refresh (bank 0). Write and Read commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during Self Refresh. It is important to note that data in unused banks, or portions of banks, will be lost when PASR is used. Data will be lost in banks 1, 2, and 3 when the one bank option is used.

Driver Strength

Bits E5 and E6 of the extended mode register can be used to select the driver strength of the DQ outputs. This value should be set according to the application requirements. Full drive strength was carried over from standard SDRAM and is suitable to drive higher load systems. Full drive

strength is not recommended for loads under 30pF. Half drive strength is intended for multi-drop systems with various loads. This drive option is not recommended for loads under 15pF. Quarter drive strength is intended for lighter loads or point-to-point systems.



E6	E5	Driver Strength
0	0	Full Strength [3]
0	1	Half Strength
1	0	Quarter Strength
1	1	Reserved

E4	E3	Maximum Case Temp
1	1	85°C [3]
0	0	70°C
0	1	45°C
1	0	15°C

E2	E1	E0	Self Refresh Coverage
0	0	0	Four Banks [3]
0	0	1	Two Banks (Bank 0,1)
0	1	0	One Bank (Bank 0)
0	1	1	RFU
1	0	0	RFU
1	0	1	1/2 Bank (Bank 0) [4]
1	1	0	1/4 Bank (Bank 0) [5]
1	1	1	RFU

Figure 27. Extended Mode Register

Notes:

1. *E13 and E12 (BA1 and BA0) must be "1, 0" to select the extended mode register (vs. the base mode register).*
2. *RFU: Reserved for future use.*
3. *Default EMR values are full array for PASR, Full Drive Strength, and 85° for TCSR.*
4. *E11 = 0.*
5. *E10, E11 = 0.*

Commands

Table 32 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

Table 32. Truth Table I - Commands and DQM Operation

Name (Function)								
Command Inhibit (NOP)	H	X	X	X	X	X	X	
No Operation	L	H	H	H	X	X	X	
Active (Select bank and activate row)	L	L	H	H	X	Bank/ Row	X	3
Read (Select bank and column, and start Read burst)	L	H	L	H	L/H	Bank/Col	X	4
Write (Select bank and column, and start Write burst)	L	H	L	L	L/H	Bank/Col	Valid	4
Burst Terminate or Deep Power Down (Enter deep power down mode)	L	H	H	L	X	X	X	9, 10
Precharge (Deactivate row in bank or banks)	L	L	H	L	X	Bank, A10	X	5
Auto Refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
Load Mode Register/Load Extended Mode Register	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	X	X	X	X	L	X	Active	8
Write Inhibit/Output High-Z	X	X	X	X	H	X	High-Z	8

Notes:

1. *CKE is High for all commands shown except Self Refresh and Deep Power Down.*
2. *A0-A11 define op-code written to mode register.*
3. *A0–A11 provide row address, and BA0, BA1 determine which bank is made active.*
4. *A1–A8 provide column address; A10 High enables the auto precharge feature (non persistent), while A10 Low disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.*
5. *A10 Low: BA0, BA1 determine the bank being precharged. A10 High: All banks precharged and BA0, BA1 are "Don't Care."*
6. *This command is Auto Refresh if CKE is High, Self Refresh if CKE is Low.*
7. *Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE*
8. *Activates or deactivates the DQs during Writes (zero-clock delay) and Reads (two-clock delay). DQML controls DQ0-7, DQMH controls DQ8-15.*
9. *This command is Burst Terminate when CKE is high and Deep Power Down when CKE is low.*
10. *The purpose of the Burst Terminate command is to stop a data burst, thus the command could coincide with data on the bus. However the DQs column reads a don't care state to illustrate that the Burst Terminate command can occur when there is no data present.*

Command Inhibit

The Command Inhibit function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)

The No Operation (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Load Mode Register

The mode register is loaded via inputs A0–A11, BA0, BA1. See mode register heading in the Register Definition section. The Load Mode Register and Load Extended Mode Register commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until t_{MRD} is met.

The values of the mode register and extended mode register will be retained even when exiting deep power-down.

Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

Read

The Read command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A1–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered High, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered Low, the DQ will provide valid data.

Write

The Write command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A1–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered Low, the corresponding data will be written to memory; if the DQM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

Precharge

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific Read or Write command. A precharge of the bank/row that is addressed with the Read or Write command is automatically performed upon completion of the Read or Write burst, except in the full-page burst mode, where auto precharge does not apply. Auto precharge is non persistent in that it is either enabled or disabled for each individual Read or Write command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (t_{RP}) is completed. This is determined as if an explicit Precharge command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

Burst Terminate

The Burst Terminate command is used to truncate either fixed-length or full-page bursts. The most recently registered Read or Write command prior to the Burst Terminate command will be truncated, as shown in the Operation section of this data sheet.

Auto Refresh

Auto Refresh is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAMs. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an Auto Refresh command. The Auto Refresh command should not be issued until the minimum t_{RP} has been met after the Precharge command as shown in the operation section.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The 128Mb SDRAM requires 4,096 Auto Refresh cycles every 64ms (t_{REF}). Providing a distributed Auto Refresh command every 15.625µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 Auto Refresh commands can be issued in a burst at the minimum cycle rate (t_{RFC}), once every 64ms.

Self Refresh

The Self Refresh command can be used to retain data in the SDRAM, even if the rest of the system is powered down, as long as power is not completely removed from the SDRAM. When in the self refresh mode, the SDRAM retains data without external clocking. The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled (Low). Once the Self Refresh command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain Low.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to t_{RAS} and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back High. Once CKE is High, the SDRAM must have NOP commands issued (a minimum of two clocks) for t_{XSR} because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, Auto Refresh commands must be issued every 15.625µs or less as both Self Refresh and Auto Refresh utilize the row refresh counter.

Deep Power-down

The operating mode deep power-down achieves maximum power reduction by eliminating the power of the whole memory array of the device. Array data will not be retained once the device enters deep power-down mode.

This mode is entered by having all banks idle then CS# and WE# held low with RAS# and CAS# held high at the rising edge of the clock, while CKE is low. This mode is exited by asserting CKE high.

Operation

Bank/Row Activation

Before any Read or Write commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the Active command, which selects both the bank and the row to be activated (see Figure 28, Activating a Specific Row in a Specific Bank Register).

After opening a row (issuing an Active command), a Read or Write command may be issued to that row, subject to the t_{RCD} specification. $t_{RCD\ (MIN)}$ should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the Active command on which a Read or Write command can be entered. For example, a t_{RCD} specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 29, which covers any case where $2 < t_{RCD\ (MIN)}/t_{CK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent Active command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive Active commands to the same bank is defined by t_{RC}.

A subsequent Active command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive Active commands to different banks is defined by t_{RRD}.

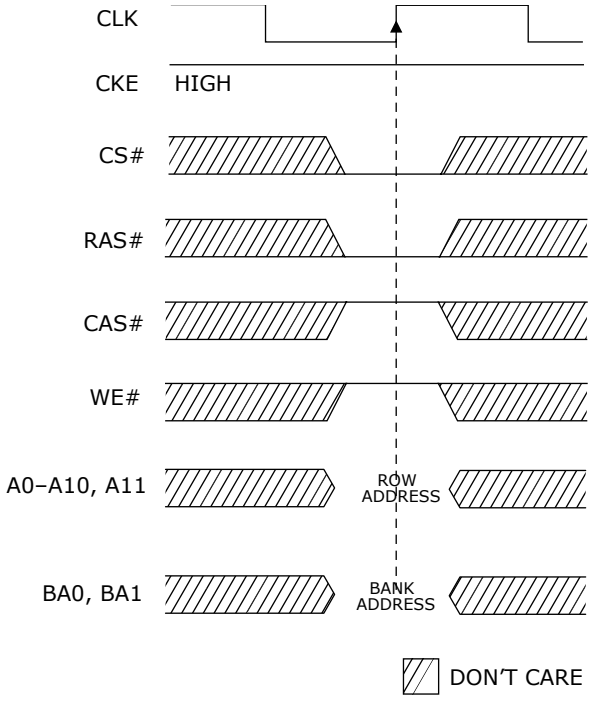


Figure 28. Activating a Specific Row in a Specific Bank Register

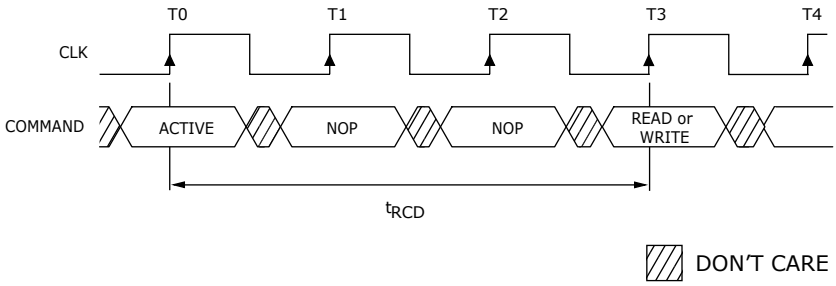


Figure 29. Meeting $t_{RCD\ (MIN)}$ when $2 < t_{RCD\ (MIN)}/t_{CK} \leq 3$

Reads

Read bursts are initiated with a Read command, as

shown in Figure 29.

The starting column and bank addresses are provided with the Read command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Read commands used in the following illustrations, auto precharge is disabled.

During Read bursts, the valid data-out element from the starting column address will be available following the CAS latency after the Read command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 26, "CAS Latency," on page 100, shows general timing for each possible CAS latency setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data from any Read burst may be truncated with a subsequent Read command, and data from a fixed length Read burst may be immediately followed by data from a Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new Read command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one.

This is shown in Figure 31, "Consecutive Read Bursts," on page 109, for CAS latencies of two and three; data element *n* + *3* is either the last of a burst of four or the last desired of a longer burst. The 128Mb SDRAM uses a pipelined architecture and therefore does not require the 2n rule associated with a prefetch architecture. A Read command can be initiated on any clock cycle following a previous Read command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 32, "Random Read Accesses," on page 109, or each subsequent Read may be performed to a different bank.

Data from any Read burst may be truncated with a subsequent Write command, and data from a fixed length Read burst may be immediately followed by data from a Write command (subject to bus turnaround limitations). The Write burst may be initiated on the clock edge immediately following the last (or last desired) data element from the Read burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQ go High-Z. In this case, at least a single cycle delay should occur between the last read data and the Write command.

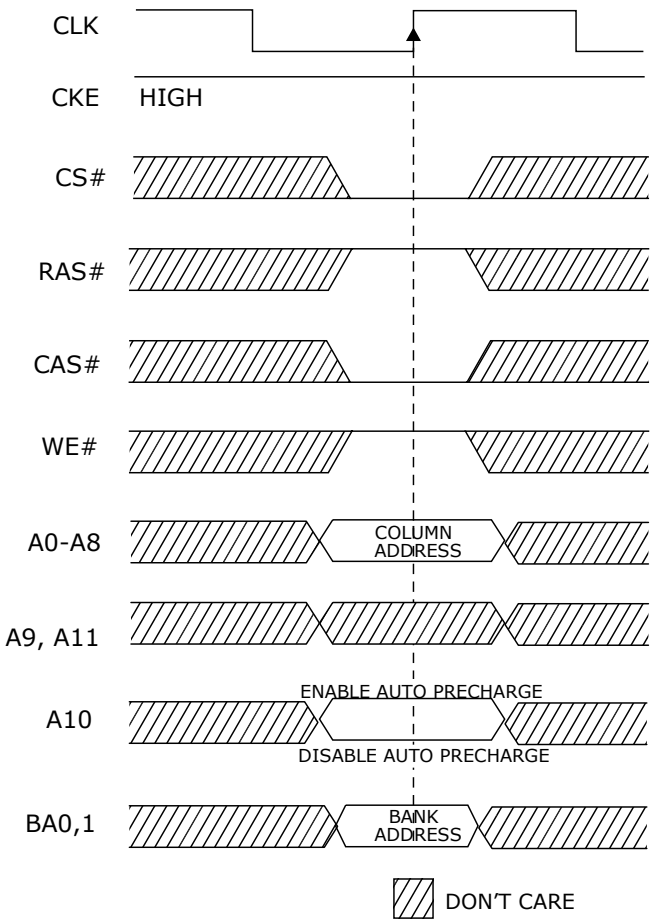


Figure 30. Read Command

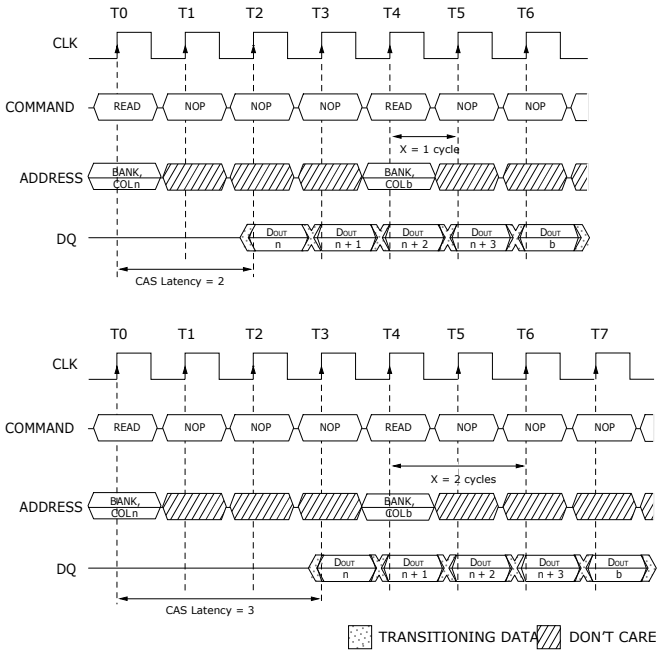


Figure 31. Consecutive Read Bursts

Note: *Each Read command may be to any bank. DQM is Low.*

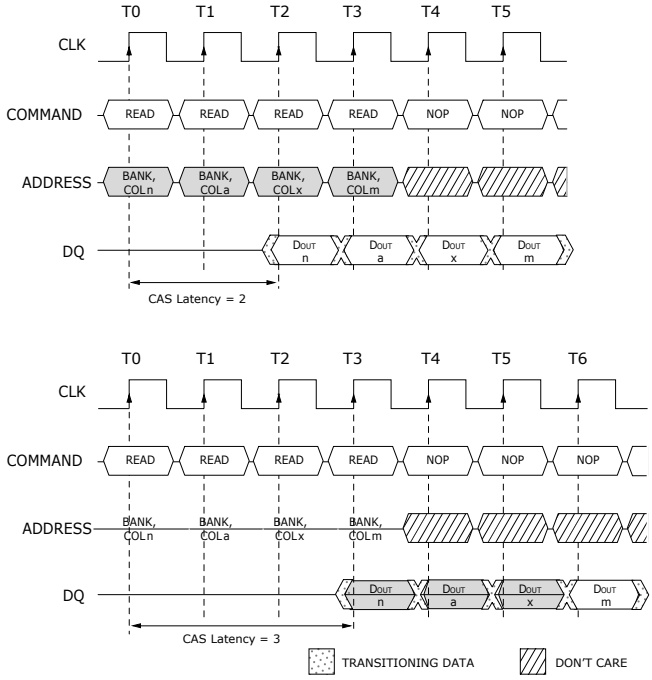


Figure 32. Random Read Accesses

Note: *Each Read command may be to any bank. DQM is low.*

The DQM input is used to avoid I/O contention, as shown in Figure 33 and Figure 34. The DQM signal must be asserted (High) at least two clocks prior to the Write command (DQM latency is two clocks for output buffers) to suppress data-out from the Read. Once the Write command is registered, the DQ will go High-Z (or remain High-Z), regardless of the state of the DQM signal,

provided the DQM was active on the clock just prior to the Write command that truncated the Read command. If not, the second Write will be an invalid Write. For example, if DQM was Low during T4 in Figure 35, then the Writes at T5 and T7 would be valid, while the Write at T6 would be invalid.

The DQM signal must be de-asserted prior to the Write command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 34 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and shows the case where the additional NOP is needed. A fixed-length Read burst may be followed by, or truncated with, a Precharge command to the same bank (provided that auto precharge was not activated), and a full-page burst may be truncated with a Precharge command to the same bank. The Precharge command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 35 for each possible CAS latency; data element *n + 3* is either the last of a burst of four or the last desired of a longer burst. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

In the case of a fixed-length burst being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the Precharge command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the Precharge command is that it can be used to truncate fixed-length or full-page bursts.

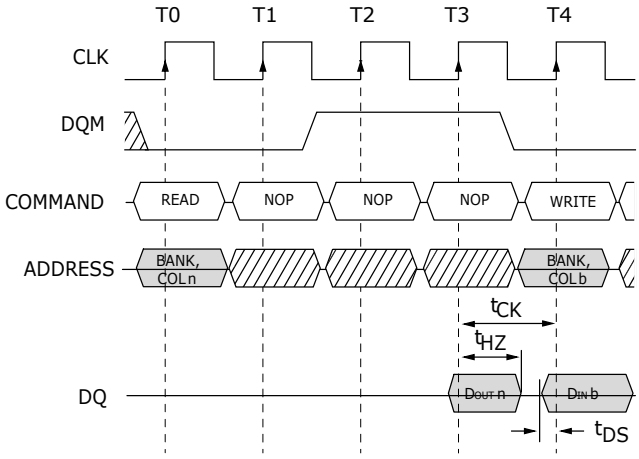


Figure 33. Read to Write

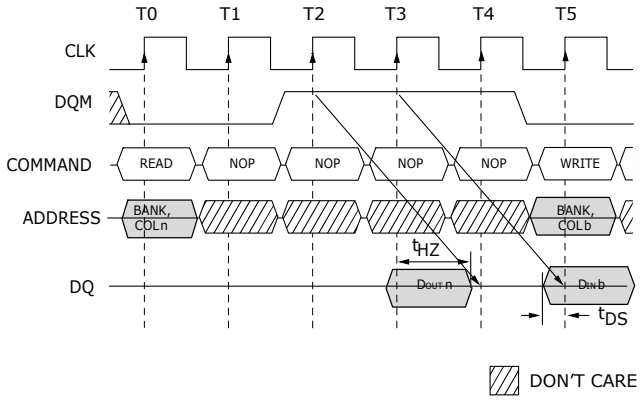


Figure 34. Read to Write with Extra Clock Cycle

Note: *A CAS latency of three is used for illustration. The Read command may be to any bank, and the Write command may be to any bank.*

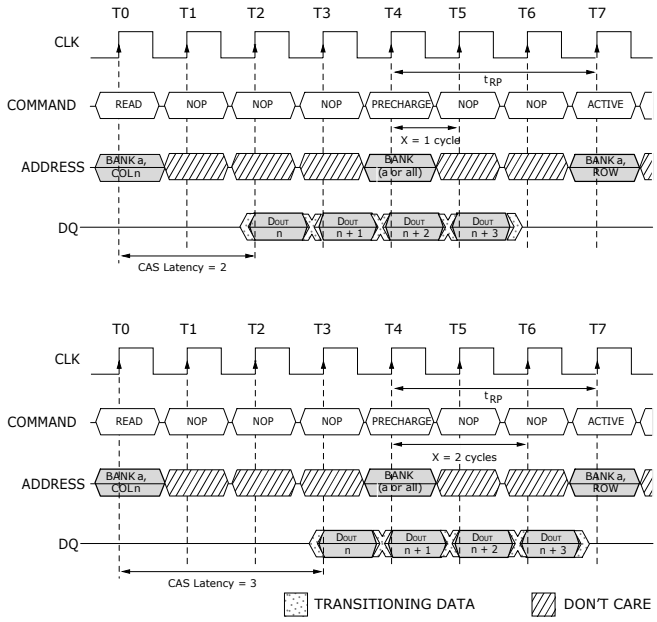


Figure 35. Read to Precharge

Note: *DQM is low.*

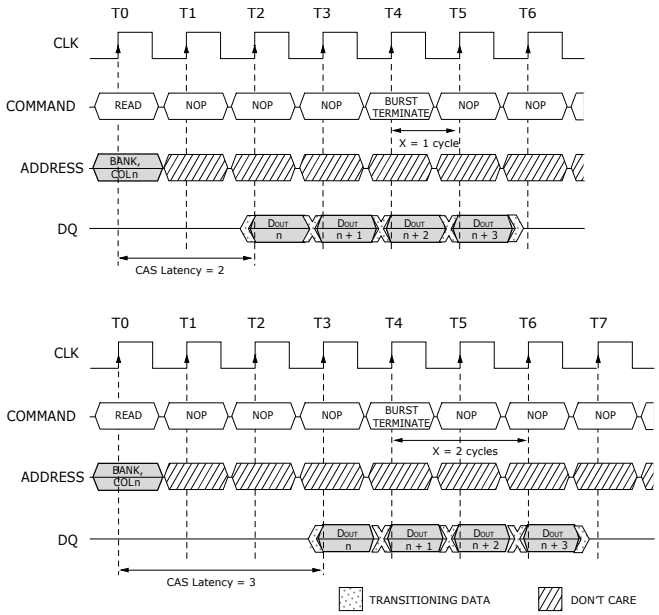


Figure 36. Terminating a Read Burst

Note: *DQM is low.*

Full-page Read bursts can be truncated with the Burst Terminate command, and fixed-length Read bursts may be truncated with a Burst Terminate command, provided that auto precharge was not activated. The Burst Terminate command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 36 for each possible CAS latency; data element *n + 3* is the last desired data element of a longer burst.

Writes

Write bursts are initiated with a Write command, as shown in Figure 37.

The starting column and bank addresses are provided with the Write command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, auto precharge is disabled.

During Write bursts, the first valid data-in element will be registered coincident with the Write command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored (see Figure 39). A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

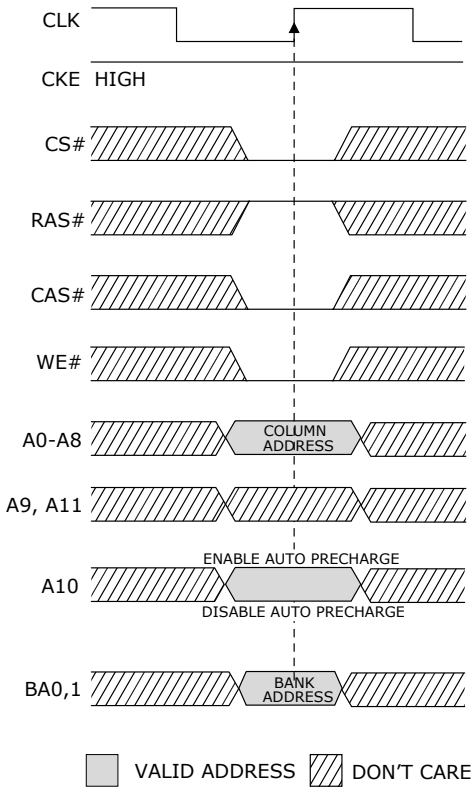


Figure 37. Write Command

Data for any Write burst may be truncated with a subsequent Write command, and data for a fixed length Write burst may be immediately followed by data for a Write command. The new Write command can be issued on any clock following the previous Write command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 40. Data *n + 1* is either the last of a burst of two or the last desired of a longer burst. The 128Mb SDRAM uses a pipelined architecture and therefore does not require the *2n* rule associated with a prefetch architecture. A Write command can be initiated on any clock cycle following a previous Write command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 40, or each subsequent Write may be performed to a different bank.

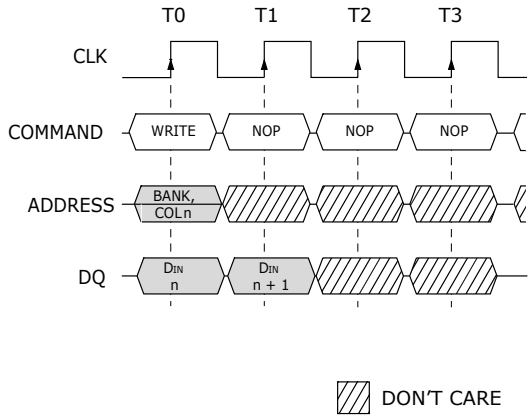


Figure 38. Write Burst

Note: *Burst length = 2. DQM is low.*

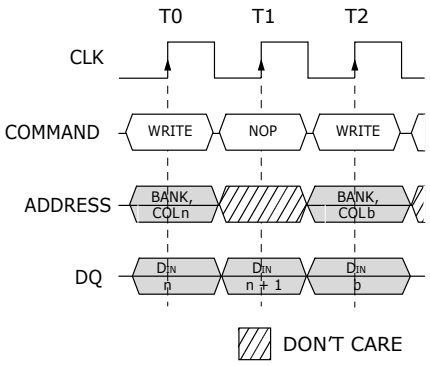


Figure 39. Write to Write

Note: *DQM is low. Each Write command may be to any bank.*

Data for any Write burst may be truncated with a subsequent Read command, and data for a fixed length Write burst may be immediately followed by a Read command. Once the Read command is registered, the data inputs will be ignored, and writes will not be executed. An example is shown in Figure 41. Data *n + 1* is either the last of a burst of two or the last desired of a longer burst.

Data for a fixed-length Write burst may be followed by, or truncated with, a Precharge command to the same bank (provided that auto precharge was not activated), and a full-page Write burst may be truncated with a Precharge command to the same bank. The Precharge command should be issued tWR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a t_{WR} of at least one clock plus time, regardless of frequency.

In addition, when truncating a Write burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the Precharge command. An example is shown in Figure 42. Data *n + 1* is either the last of a burst of two or the last desired of a longer burst. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

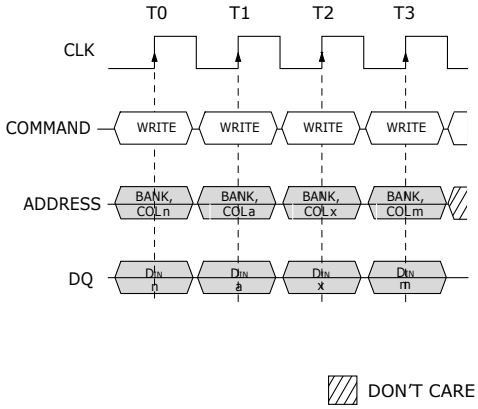


Figure 40. Random Write Cycles

Note: *Each Write command may be to any bank. DQM is low.*

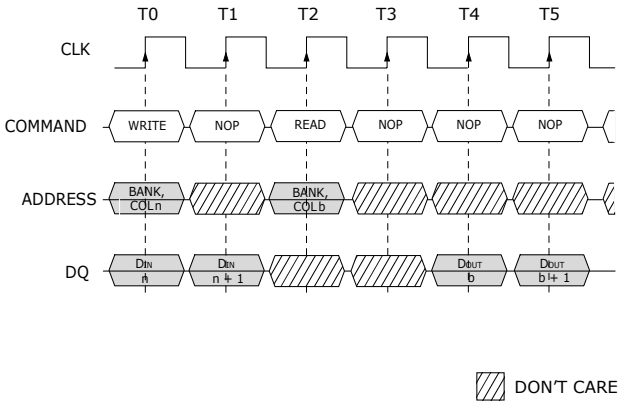


Figure 41. Write to Read

Note: *The Write command may be to any bank, and the Read command may be to any bank. DQM is low. CAS latency = 2 for illustration.*

In the case of a fixed-length burst being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the Precharge command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the Precharge command is that it can be used to truncate fixed-length or full-page bursts.

Fixed-length or full-page Write bursts can be truncated with the Burst Terminate command. When truncating a Write burst, the input data applied coincident with the Burst Terminate command will be ignored. The last data written (provided that DQM is Low at that time) will be the input data applied one clock previous to the Burst Terminate command. This is shown in Figure 44, where data *n* is the last desired data element of a longer burst.

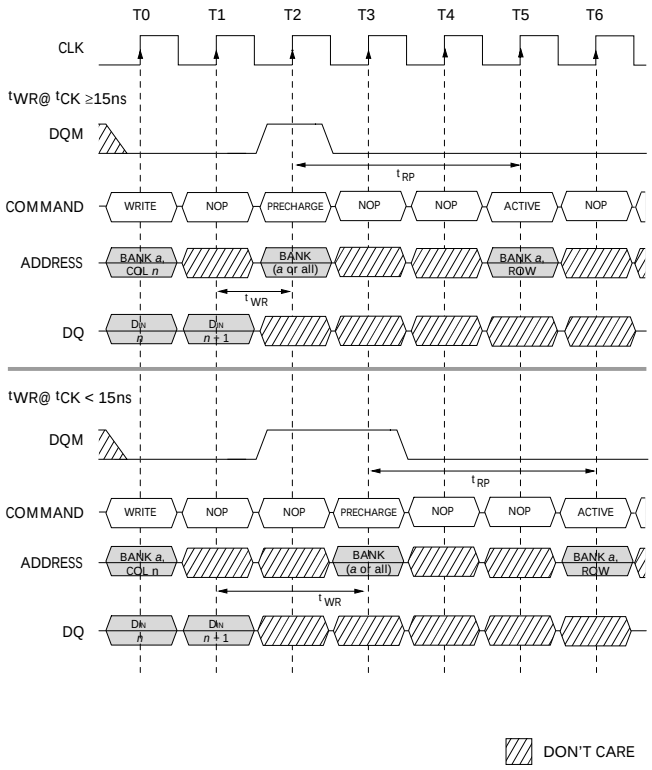


Figure 42. Write to Precharge

Note: *DQM could remain low in this example if the Write burst is a fixed length of two.*

Precharge

The Precharge command (see Figure 45) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank.

Power-down

Power-down occurs if CKE is registered low coincident with a NOP or Command Inhibit when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode. The power-down state is exited by registering a NOP or Command Inhibit and CKE High at the desired clock edge (meeting t_{CKS}). See Figure 43.

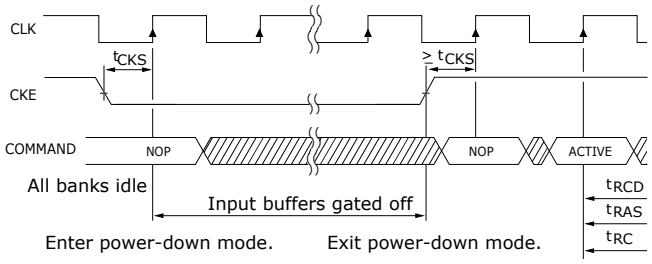


Figure 43. Power-Down

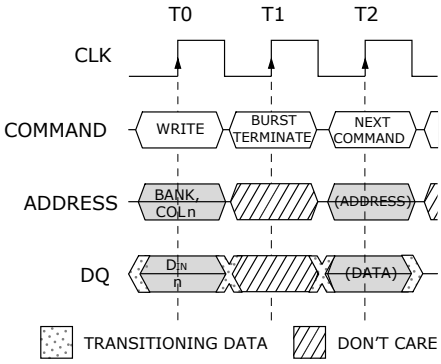


Figure 44. Terminating a Write Burst

Note: *DQMs are low.*

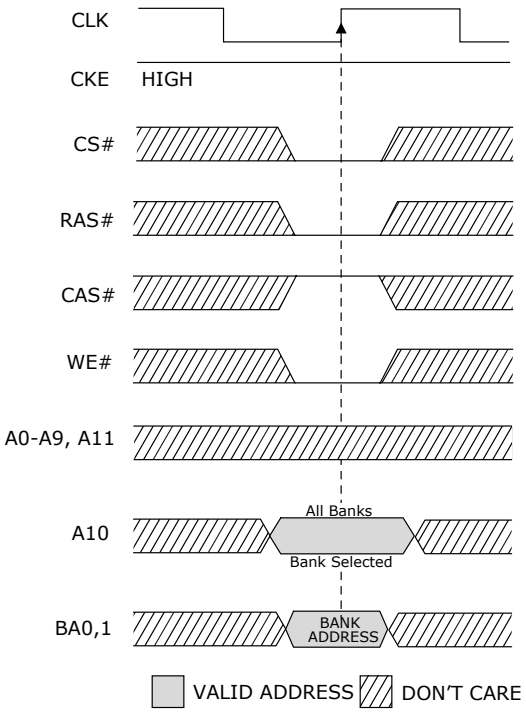


Figure 45. Precharge Command

Deep Power-down

Deep Power Down mode is a maximum power savings feature achieved by shutting off the power to the entire memory array of the device. Data on the memory array will not be retained once Deep Power Down mode is executed. Deep Power Down mode is entered by having all banks idle then CS# and WE# held low with RAS# and CAS# high at the rising edge of the clock, while CKE is low. CKE must be held low during deep power-down.

In order to exit Deep Power Down mode, CKE must be asserted high. After exiting, the following sequence is needed in order to enter a new command. Maintain NOP input conditions for a minimum of 100us. Issue Precharge commands for all banks. Issue eight or more AUTOREFRESH commands. The values of the mode register and extended mode register will be retained upon exiting deep power-down.

Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered low. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled Low, the next internal positive clock edge is suspended. Any command or data present on the input pins at the time of a suspended internal clock edge is ignored; any data present on the DQ pins remains driven; and burst counters are not incremented, as long as the clock is suspended. (See examples in Figure 46, and Figure 47.)

Clock suspend mode is exited by registering CKE High; the internal clock and related operation will resume on the subsequent positive clock edge.

Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all Write commands result in the access of a single column location (burst of one), regardless of the programmed burst length. Read commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

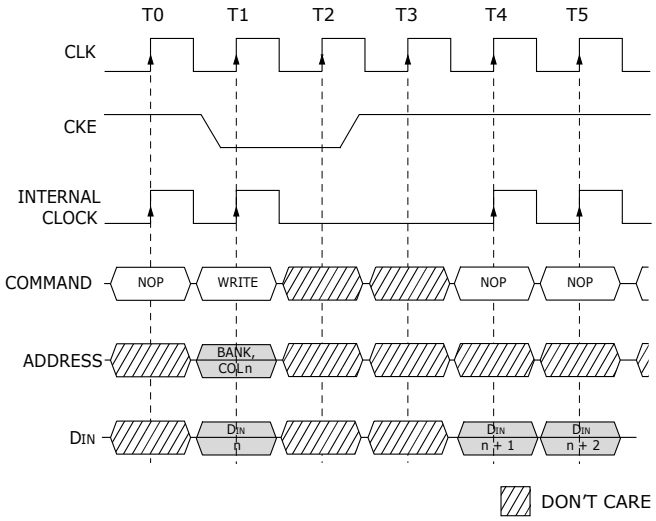


Figure 46. Clock Suspend During Write Burst

Note: *For this example, burst length = 4 or greater, and DM is low.*

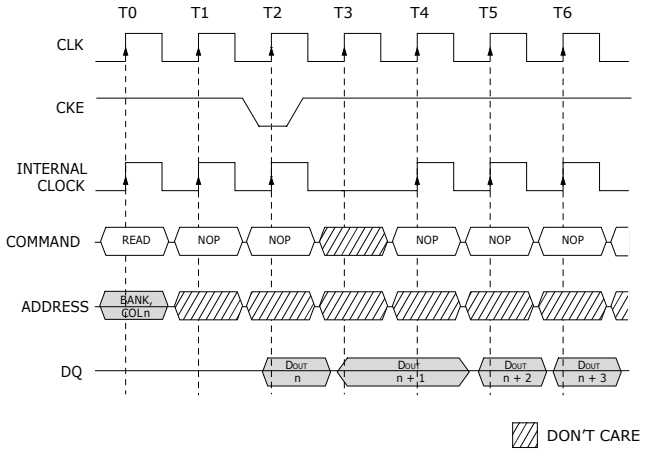


Figure 47. Clock Suspend During Read Burst

Note: *For this example, CAS latency = 2, burst length = 4 or greater, and DQM is low.*

Concurrent Auto Precharge

The SDRAM devices support Concurrent Auto precharge, which allows an access command (Read or Write) to another bank while an access command with auto precharge enabled is executing. Four cases where concurrent auto precharge occurs are defined below.

Read with Auto Precharge

1. Interrupted by a Read (with or without auto precharge): A Read to bank m will interrupt a Read on bank *n*, two or three clocks later, depending on CAS latency. The precharge to bank *n* will begin when the Read to bank *m* is registered (Figure 48).
2. Interrupted by a Write (with or without auto precharge): When a Write to bank *m* registers, a Read on bank *n* will be interrupted. DQM should be used two clocks prior to the Write command to prevent bus contention. The precharge to bank *n* will begin when the Write to bank m is registered (Figure 49).

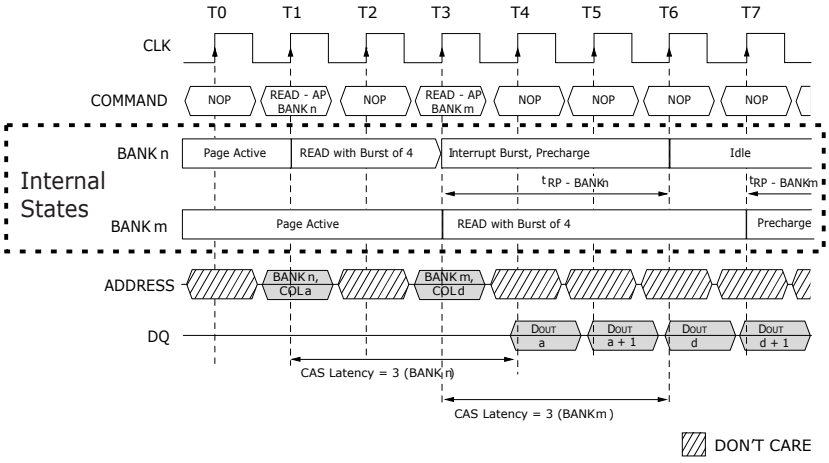


Figure 48. Read with Auto precharge Interrupted by a Read

Note: *DQM is low.*

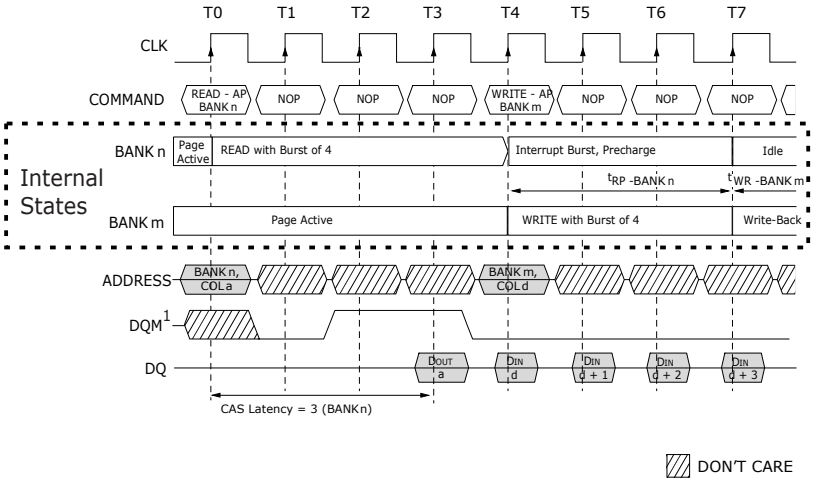


Figure 49. Read with Auto Precharge Interrupted by a Write

Note: *DQM is high at T2 to prevent D_{OUT}-a+1 from contending with D_{IN}-dat T4.*

Write with Auto Precharge

3. Interrupted by a Read (with or without auto precharge): When a Read to bank *m* registers, it will interrupt a Write on bank n, with the data-out appearing 2 or 3 clocks later, (depending on CAS latency). The precharge to bank *n* will begin after t_{WR} is met, where t_{WR} begins when the Read to bank *m* is registered. The last valid Write to bank n will be data-in registered one clock prior to the Read to bank *m* (Figure 50).
4. Interrupted by a Write (with or without auto precharge): When a Write to bank *m* registers, it will interrupt a Write on bank *n*. The precharge to bank *n* will begin after t_{WR} is met, where t_{WR} begins when the Write to bank *m* is registered. The last valid data Write to bank *n* will be data registered one clock prior to a Write to bank *m* (Figure 51).

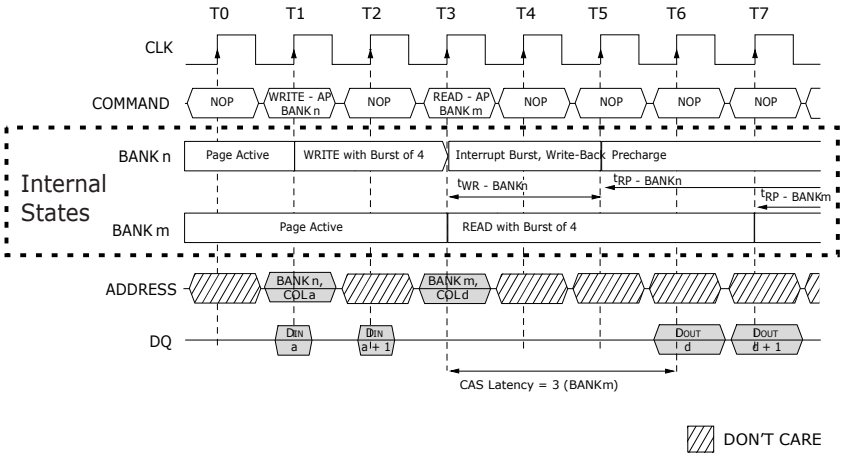


Figure 50. Write with Auto Precharge Interrupted by a Read

Note: *DQM is low.*

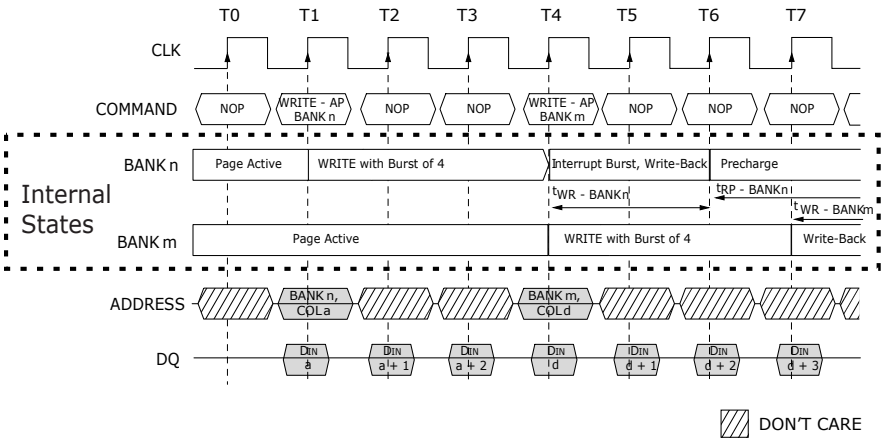


Figure 51. Write with Auto Precharge Interrupted by a Write

Note: *DQM is low.*

Table 33. Truth Table 2—CKE

CKE_{n-1}	CKE_n	Current State	$Command_n$	$Action_n$	Notes
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
		Clock Suspend	X	Maintain Clock Suspend	
		Deep Power-Down	X	Maintain Deep Power-Down	8
L	H	Power-Down	Command Inhibit or NOP	Exit Power-Down	5
		Deep Power-Down	X	Exit Deep Power-Down	8
		Self Refresh	Command Inhibit or NOP	Exit Self Refresh	6
		Clock Suspend	X	Exit Clock Suspend	7
H	L	All Banks Idle	Command Inhibit or NOP	Power-Down Entry	
		All Banks Idle	Burst Terminate	Deep Power-Down Entry	8
		All Banks Idle	Auto Refresh	Self Refresh Entry	
		Reading or Writing	Valid	Clock Suspend Entry	
H	H		See Truth Table 3		

Notes:

1. *CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.*
2. *Current state is the state of the SDRAM immediately prior to clock edge n.*
3. *$Command_n$ is the command registered at clock edge n, and $Action_n$ is a result of $Command_n$.*
4. *All states and sequences not shown are illegal or reserved.*
5. *Exiting power-down at clock edge n will put the device in the all banks idle state in time for clock edge n + 1 (provided that t_{CKS} is met).*
6. *Exiting self refresh at clock edge n will put the device in the all banks idle state once t_{XSR} is met. Command Inhibit or NOP commands should be issued on any clock edges occurring during the t_{XSR} period. A minimum of two NOP commands must be provided during t_{XSR} period.*
7. *After exiting clock suspend at clock edge n, the device will resume operation and recognize the next command at clock edge n + 1.*
8. *Deep power-down is a power-saving feature of this Mobile SDRAM device. This command is Burst Terminate when CKE is high and Deep Power Down when CKE is low.*

Table 34. Truth Table 3 — Current State Bank n, Command to Bank n

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	Command Inhibit (NOP/Continue previous operation)	
	L	H	H	H	No Operation (NOP/Continue previous operation)	
Idle	L	L	H	H	Active (Select and activate row)	
	L	L	L	H	Auto Refresh	7
	L	L	L	L	Load Mode Register	7
	L	L	H	L	Precharge	11
Row Active	L	H	L	H	Read (Select column and start Read burst)	10
	L	H	L	L	Write (Select column and start Write burst)	10
	L	L	H	L	Precharge (Deactivate row in bank or banks)	8
Read (Auto precharge disabled)	L	H	L	H	Read (Select column and start new Read burst)	10
	L	H	L	L	Write (Select column and start Write burst)	10
	L	L	H	L	Precharge (Truncate Read burst, start Precharge)	8
	L	H	H	L	Burst Terminate	9
Write (Auto precharge disabled)	L	H	L	H	Read (Select column and start Read burst)	10
	L	H	L	L	Write (Select column and start new Write burst)	10
	L	L	H	L	Precharge (Truncate Write burst, start Precharge)	8
	L	H	H	L	Burst Terminate	9

Notes:

1. *This table applies when CKE_{n-1} was High and CKE_n is High (see Table 33) and after t_{XSR} has been met (if the previous state was self refresh).*
2. *This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.*
3. *Current state definitions:*
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. *The following states must not be interrupted by a command issued to the same bank. Command Inhibit or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 34, and according to Table 35.*
   Precharging: Starts with registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an Active command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the row active state.
   Read w/Auto Precharge Enabled: Starts with registration of a Read command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
   Write w/Auto Precharge Enabled: Starts with registration of a Write command with auto precharge enabled and ends when
   t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
5. *The following states must not be interrupted by any executable command; Command Inhibit or NOP commands must be applied on each positive clock edge during these states.*
   Refreshing: Starts with registration of an Auto Refresh command and ends when t_{RC} is met. Once t_{RC} is met, the SDRAM will be in the all banks idle state.
   Accessing Mode Register: Starts with registration of a Load Mode Register command and ends when t_{MRD} has been met.
   Once t_{MRD} is met, the SDRAM will be in the all banks idle state.

Precharging All: Starts with registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, all banks will be in the idle state.

6. *All states and sequences not shown are illegal or reserved.*
7. *Not bank-specific; requires that all banks are idle.*
8. *May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.*
9. *Deep Power-Down is power-saving feature of this Mobile SDRAM device. This command is Burst Terminate when CKE is high and Deep Power Down when CKE is low.*
10. *Reads or Writes listed in the Command (Action) column include Reads or Writes with auto precharge enabled and Reads or Writes with auto precharge disabled.*
11. *Does not affect the state of the bank and acts as a NOP to that bank.*

Table 35. Truth Table 4 — Current State Bank n, Command to Bank m

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	Command Inhibit (NOP/Continue previous operation)	
	L	H	H	H	No Operation (NOP/Continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank *m*	
Row Activating, Active, or Precharging	L	L	H	H	Active (Select and activate row)	7
	L	H	L	H	Read (Select column and start Read burst)	7
	L	H	L	L	Write (Select column and start Write burst)	
	L	L	H	L	Precharge	
Read (Auto precharge disabled)	L	L	H	H	Active (Select and activate row)	
	L	H	L	H	Read (Select column and start Read burst)	7, 10
	L	H	L	L	Write (Select column and start Write burst)	7, 11
	L	L	H	L	Precharge	9
Write (Auto precharge disabled)	L	L	H	H	Active (Select and activate row)	
	L	H	L	H	Read (Select column and start Read burst)	7, 12
	L	H	L	L	Write (Select column and start new Write burst)	7, 13
	L	L	H	L	Precharge	9
Read (with Auto precharge)	L	L	H	H	Active (Select and activate row)	
	L	H	L	H	Read (Select column and start new Read burst)	7, 8 14
	L	H	L	L	Write (Select column and start Write burst)	7, 8, 15
	L	L	H	L	Precharge	9
Write (with Auto precharge)	L	L	H	H	Active (Select and activate row)	
	L	H	L	H	Read (Select column and start Read burst)	7, 8, 16
	L	H	L	L	Write (Select column and start new Write burst)	7, 8, 17
	L	L	H	L	Precharge	9

Notes:

1. *This table applies when CKE_{n-1} was high and CKE_n is high (see Table 33) and after t_{XSR} has been met (if the previous state was self refresh).*
2. *This table describes alternate bank operation, except where noted; i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.*
3. *Current state definitions:*
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   Read w/Auto Precharge Enabled: Starts with registration of a Read command with auto precharge enabled, and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

Write w/Auto Precharge Enabled: Starts with registration of a Write command with auto precharge enabled, and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

4. *Auto Refresh, Self Refresh and Load Mode Register commands may only be issued when all banks are idle.*
5. *A Burst Terminate command cannot be issued to another bank; it applies to the bank represented by the current state only.*
6. *All states and sequences not shown are illegal or reserved.*
7. *Reads or Writes to bank m listed in the Command (Action) column include Reads or Writes with auto precharge enabled and Reads or Writes with auto precharge disabled.*
8. *Concurrent Auto Precharge: Bank n will initiate the auto precharge command when its burst has been interrupted by bank m burst.*
9. *Burst in bank n continues as initiated.*
10. *For a Read without auto precharge interrupted by a Read (with or without auto precharge), the Read to bank m will interrupt the Read on bank n, CAS latency later (Figure 31).*
11. *For a Read without auto precharge interrupted by a Write (with or without auto precharge), the Write to bank m will interrupt the Read on bank n when registered (Figure 33, and Figure 34). DQM should be used one clock prior to the Write command to prevent bus contention.*
12. *For a Write without auto precharge interrupted by a Read (with or without auto precharge), the Read to bank m will interrupt the Write on bank n when registered (Figure 41), with the data-out appearing CAS latency later. The last valid Write to bank n will be data-in registered one clock prior to the Read to bank m.*
13. *For a Write without auto precharge interrupted by a Write (with or without auto precharge), the Write to bank m will interrupt the Write on bank n when registered (Figure 39). The last valid Write to bank n will be data-in registered one clock prior to the Read to bank m.*
14. *For a Read with auto precharge interrupted by a Read (with or without auto precharge), the Read to bank m will interrupt the Read on bank n, CAS latency later (Figure 48). The Precharge to bank n will begin when the Read to bank m is registered.*
15. *For a Read with auto precharge interrupted by a Write (with or without auto precharge), the Write to bank m will interrupt the Read on bank n when registered (Figure 49). DQM should be used two clocks prior to the Write command to prevent bus contention. The Precharge to bank n will begin when the Write to bank m is registered.*
16. *For a Write with auto precharge interrupted by a Read (with or without auto precharge), the Read to bank m will interrupt the Write on bank n when registered, with the data-out appearing CAS latency later (Figure 50). The Precharge to bank n will begin after t_{WR} is met, where t_{WR} begins when the Read to bank m is registered. The last valid Write bank n will be data-in registered one clock prior to the Read to bank m.*
17. *For a Write with auto precharge interrupted by a Write (with or without auto precharge), the Write to bank m will interrupt the Write on bank n when registered. The Precharge to bank n will begin after t_{WR} is met, where t_{WR} begins when the Write to bank m is registered (Figure 51). The last valid Write to bank n will be data registered one clock to the Write to bank m.*

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on V_{DD}/V_{DDQ} Supply Relative to V_{SS} . . . . . -0.35V to +2.8V
Voltage on Inputs, NC or I/O Pins Relative to VSS . . . . . -0.35V to +2.8V
Operating Temperature T_A (Extended) . . . . . -25°C to +85°C
Storage Temperature (plastic) . . . . . -55°C to +150°C

Table 36. DC Electrical Characteristics and Operating Conditions

Parameter	Symbol	-75		-I0		Units	Notes
		Min	Max	Min	Max		
Supply Voltage	V_{DD}	1.7	1.95	1.7	1.9	V	
I/O Supply Voltage	V_{DDQ}	1.7	1.95	1.7	1.9		
Input High Voltage: Logic 1; All inputs	V_{IH}	0.8 x V_{DDQ}	V_{DD} + 0.3	0.8 x V_{DDQ}	V_{DD} + 0.3		4
Input Low Voltage: Logic 0; All inputs	V_{IL}	-0.3	+0.3	-0.3	+0.3		4
Output High Voltage: All inputs	V_{OH}	0.9 x V_{DDQ}	—	0.9 x V_{DDQ}	—		
Output Low Voltage: All inputs	V_{OL}	—	0.2	—	0.2		
Input Leakage Current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-1.0	1.0	-1.0	1.0	µA	
Output Leakage Current: DQ disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	I_{OZ}	-1.5	1.5	-1.5	1.5	µA	

Notes:

1. *All voltages referenced to V_{SS}. V_{DD} = V_{DDQ} = +1.8V ±0.1V.*
2. *The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-25°C ≤ T_A ≤ +85°C for standard parts; -40°C ≤ T_A ≤ +85°C for IT parts) is ensured.*
3. *An initial pause of 100µs is required after power up, followed by two Auto Refresh commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two Auto Refresh command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.*
4. *V_{IH} overshoot: $V_{IH\ (MAX)}$ = V_{DDQ} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{IL\ (MIN)}$ = -2V for a pulse width ≤ 3ns.*

Table 37. AC Electrical Characteristics and Operating Conditions

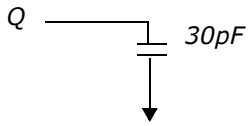
Parameter	Symbol	Min	Max	Units	Notes
Input High Voltage: Logic 1; All inputs	V_{IH}	1.4	—	V	
Input Low Voltage: Logic 0; All inputs	V_{IL}	—	+0.4	V	

Table 38. Electrical Characteristics and Recommended AC Operating Conditions

AC Characteristics			-75		-10		Units	Notes
Parameter		Symbol	Min	Max	Min	Max		
Access time from CLK (pos. edge)	CL=3	t_{AC} (3)		5.4		7	ns	27
	CL=2	t_{AC} (2)		6		8		
Address hold time		t_{AH}	1		1			
Address setup time		t_{AS}	2.5		2.5			
CLK high-level width		t_{CH}	2.5		3			
CLK low-level width		t_{CL}	2.5		3			
Clock cycle time	CL=3	t_{CK} (3)	7.5	100	9.6	100		6
	CL=2	t_{CK} (2)	10	100	12	100		6
CKE hold time		t_{CKH}	1		1			
CKE setup time		t_{CKS}	2.5		2.5			
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	1		1			
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	2.5		2.5			
Data-in hold time		t_{DH}	1		1			
Data-in setup time		t_{DS}	2.5		2.5			
Data-out high-impedance time	CL=3	t_{HZ} (3)		5.4		7		7
	CL=2	t_{HZ} (2)		6		8		7
Data-out low-impedance time		t_{LZ}	1		1			
Data-out hold time (load)		t_{OH}	3		2.5			
Data-out hold time (no load)		t_{OHN}	1.8		1.8			8
Active to Precharge command		t_{RAS}	45	120,000	50	120,000		
Active to Active command period		t_{RC}	80		100			
Active to Read or Write delay		t_{RCD}	22.5		20			
Refresh period (4,096 rows)		t_{REF}		64		64	ms	
Auto Refresh period		t_{RFC}	80		100		ns	
Precharge command period		t_{RP}	22.5		20			
Active bank a to Active bank b command		t_{RRD}	15		20			
Transition time		t_T	0.3	1.2	0.3	1.2		9
Write recovery time		t_{WR} (a)	1 CLK + 7.5 ns		1 CLK + 5ns		—	10
		t_{WR} (m)	15		15		ns	11
Exit Self Refresh to Active command		t_{XSR}	80		100			12

Notes:

1. *The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-25°C ≤ T_A ≤ +85°C for standard parts; -40°C ≤ T_A ≤ +85°C for IT parts) is ensured.*
2. *An initial pause of 100µs is required after power up, followed by two Auto Refresh commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two Auto Refresh command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.*
3. *In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.*
4. *Outputs measured for 1.8V at 0.9V with equivalent load:*



5. *AC timing and IDD tests have V_{IL} and V_{IH}, with timing referenced to $V_{IH}/2$ = crossover point. If the input transition time is longer than $t_{T\ (MAX)}$, then the timing is referenced at $V_{IL\ (MAX)}$ and $V_{IH\ (MIN)}$ and no longer at the $V_{IH}/2$ crossover point.*
6. *The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (Read, Write, including t_{WR}, and Precharge commands). CKE may be used to reduce the data rate*
7. *t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going High-Z.*
8. *Parameter guaranteed by design.*
9. *AC characteristics assume t_T = 1ns.*
10. *Auto precharge mode only. May not exceed limit set for precharge mode.*
11. *Precharge mode only.*
12. *CLK must be toggled a minimum of two times during this period.*

Table 39. AC Functional Characteristics

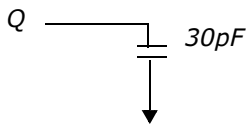
Parameter		Symbol	-75 & -I0	Units	Notes
Read/Write command to Read/Write command		t_{CCD}	1	t_{CK}	7
CKE to clock disable or power-down entry mode		t_{CKED}	1		8
CKE to clock enable or power-down exit setup mode		t_{PED}	1		8
DQM to input data delay		t_{DQD}	0		7
DQM to data mask during Writes		t_{DQM}	0		7
DQM to data high-impedance during Reads		t_{DQZ}	2		7
Write command to input data delay		t_{DWD}	0		7
Data-in to Active command		t_{DAL}	5		9, 10
Data-in to Precharge command		t_{DPL}	2		11, 10
Last data-in to burst Stop command		t_{BDL}	1		7
Last data-in to new Read/Write command		t_{CDL}	1		7
Last data-in to Precharge command		t_{RDL}	2		11, 10
Load Mode Register command to Active or Refresh command		t_{MRD}	2		12
Data-out to high-impedance from Precharge command	CL = 3	t_{ROH} (3)	3		7
	CL = 2	t_{ROH} (2)	2		7

Notes:

1. *The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-25°C ≤ T_A ≤ +85°C for standard parts; -40°C ≤ T_A ≤ +85°C for IT parts) is ensured.*
2. *An initial pause of 100µs is required after power up, followed by two Auto Refresh commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS}*

and V_{SSQ} must be at same potential.) The two Auto Refresh command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.

3. *AC characteristics assume t_T = 1ns.*
4. *In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.*
5. *Outputs measured for 1.8V at 0.9V with equivalent load:*



6. *AC timing and I_{DD} tests have V_{IL} and V_{IH}, with timing referenced to VIH/2 = crossover point. If the input transition time is longer than $t_{T\ (MAX)}$, then the timing is referenced at $V_{IL\ (MAX)}$ and $V_{IH\ (MIN)}$ and no longer at the V_{IH}/2 crossover point.*
7. *Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.*
8. *Timing actually specified by t_{CKS}; clock(s) specified as a reference only at minimum cycle rate.*
9. *Timing actually specified by t_{WR} plus t_{RP}; clock(s) specified as a reference only at minimum cycle rate.*
10. *Based on t_{CK} = 9.6ns for -10.*
11. *Timing actually specified by t_{WR}.*
12. *JEDEC and PC100 specify three clocks.*

Table 40. IDD Specifications and Conditions

Parameter/Condition		Symbol	-75 Max	-I0 Max	Units	Notes
Operating Current: Active Mode; Burst = 2; Read or Write; $t_{RC} = t_{RC\ (MIN)}$		I_{DD1}	50	50	mA	6, 7, 8, 9
Standby Current: Power-Down Mode; All banks idle; CKE = Low		I_{DD2}	220	150	µA	9
Standby Current: Active Mode; CKE = High; CS# = High; All banks active after t_{RCD} met; No accesses in progress		I_{DD3}	5	30	mA	6, 12, 8, 9
Operating Current: Burst Mode; Continuous burst; Read or Write; All banks active		I_{DD4}	50	80		6, 7, 8, 9
Auto Refresh Current CKE = High; CS# = High	$t_{RC} = t_{RFC\ (MIN)}$	I_{DD5}	105	120		6, 12, 7, 8, 9, 10
	t_{RFC} = 15.625µs	I_{DD6}	3	2		
Deep Power Down		I_{ZZ}	10	10	µA	11

Notes:

1. *All voltages referenced to V_{SS}. $V_{DD} = V_{DDQ}$ = +1.8V ±0.1V.*
2. *The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-25°C ≤ T_A ≤ +85°C for standard parts; -40°C ≤ T_A ≤ +85°C for IT parts) is ensured.*
3. *An initial pause of 100µs is required after power up, followed by two Auto Refresh commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS}*

and V_{SSQ} must be at same potential.) The two Auto Refresh command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.

4. *AC timing and I_{DD} tests have V_{IL} and V_{IH}, with timing referenced to VIH/2 = crossover point. If the input transition time is longer than $t_{T\ (MAX)}$, then the timing is referenced at $V_{IL\ (MAX)}$ and $V_{IH\ (MIN)}$ and no longer at the V_{IH}/2 crossover point.*
5. *I_{DD} specifications are tested after the device is properly initialized.*
6. *I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.*
7. *The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.*
8. *Address transitions average one transition every two clocks.*
9. *For -10, CL = 3 and t_{CK} = 9.6ns.*
10. *CKE is High during refresh command period $t_{RFC\ (MIN)}$ else CKE is Low. The I_{DD6} limit is actually a nominal value and does not result in a fail value.*
11. *Deep power down current is a nominal value at 25°C. The parameter is not tested.*

Table 4I. I_{DD7} — Self Refresh Current Options

Temperature Compensated Self Refresh Parameter/Condition	Max Temperature	-75	-I0	Units	Notes
Self Refresh Current: CKE < 0.2V – 4 Banks Open	85°C	220	200	µA	2
	70°C	175	160		
	45°C	150	140		
	15°C	125	120		
Self Refresh Current: CKE < 0.2V – 2 Banks Open	85°C	160	160		
	70°C	125	130		
	45°C	125	120		
	15°C	85	110		
Self Refresh Current: CKE < 0.2V – 1 Bank Open	85°C	130	130		
	70°C	105	120		
	45°C	90	110		
	15°C	75	100		
Self Refresh Current: CKE < 0.2V – 1/2 Bank Open	85°C	TBD	120		
	70°C	TBD	110		
	45°C	TBD	100		
	15°C	TBD	90		
Self Refresh Current: CKE < 0.2V – 1/4 Bank Open	85°C	TBD	115		
	70°C	TBD	105		
	45°C	TBD	95		
	15°C	TBD	90		

Notes:

1. *V_{DD} = V_{DDQ} = +1.8V ±0.1V.*
2. *Enables on-chip refresh and address counters.*

Table 42. Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input Capacitance: CLK	C_{I1}	1.5	4.0	pF	229
Input Capacitance: All other input-only pins	C_{I2}	1.5	4.0	pF	3
Input/Output Capacitance: DQ	C_{IO}	3.0	6.0	pF	4

Notes:

1. *This parameter is sampled. V_{DD}, V_{DDQ} = +1.8V; TA = 25°C; pin under test biased at 1.4V. f = 1 MHz.*
2. *PC100 specifies a maximum of 4pF.*
3. *PC100 specifies a maximum of 5pF.*
4. *PC100 specifies a maximum of 6.5pF*

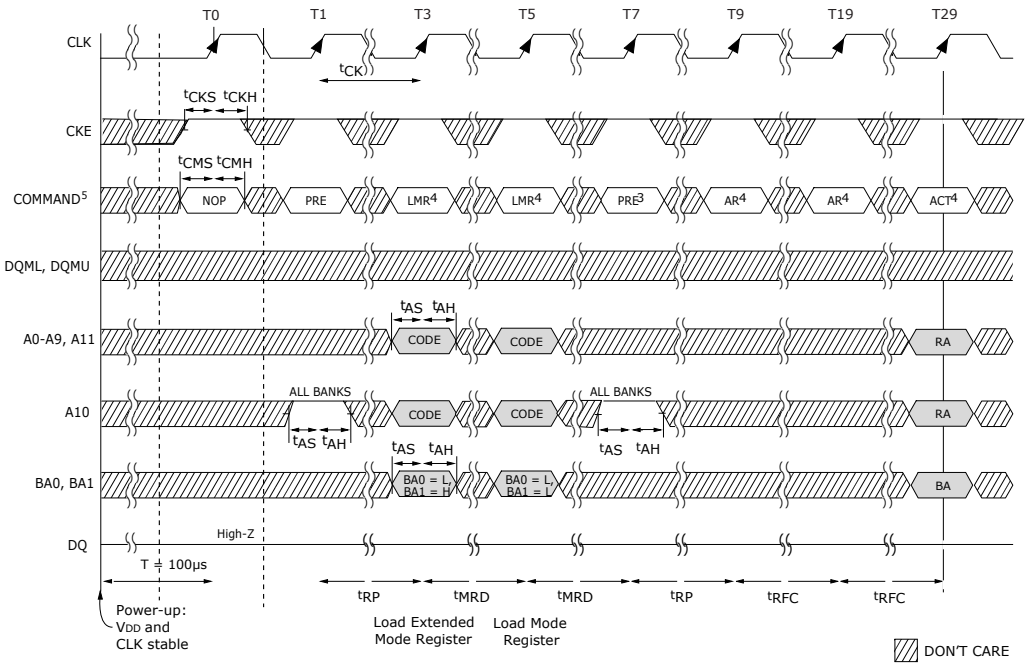


Figure 52. Initialize and Load Mode Register

Notes:

1. *The two Auto Refresh commands at T9 and T19 may be applied before either Load Mode Register (LMR) command.*
2. *PRE = Precharge command, LMR = Load Mode Register command, AR = Auto Refresh command, ACT = Active command, RA = Row Address, BA = Bank Address.*
3. *Optional refresh command.*
4. *The Load Mode Register for both MR/EMR and 2 Auto Refresh commands can be in any order. However, all must occur prior to an Active command.*
5. *Device timing is -10 with 104 MHz clock.*

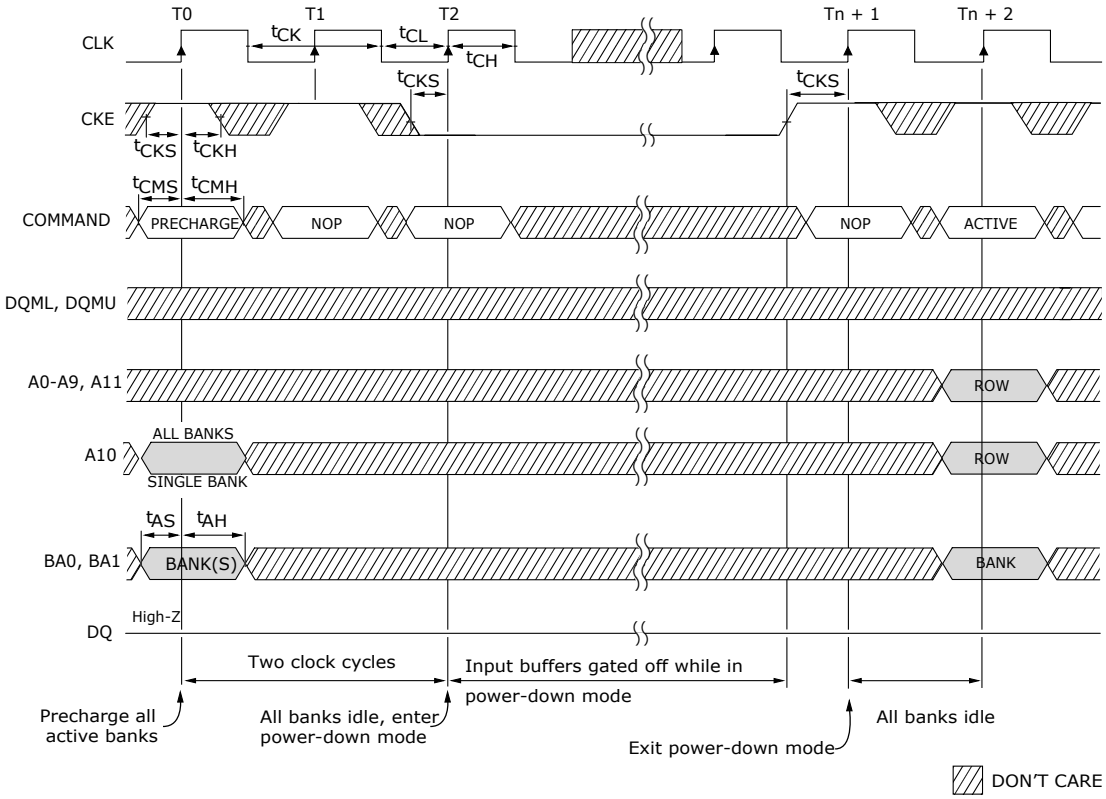


Figure 53. Power Down Mode

Note: *Violating refresh requirements during power-down may result in a loss of data.*

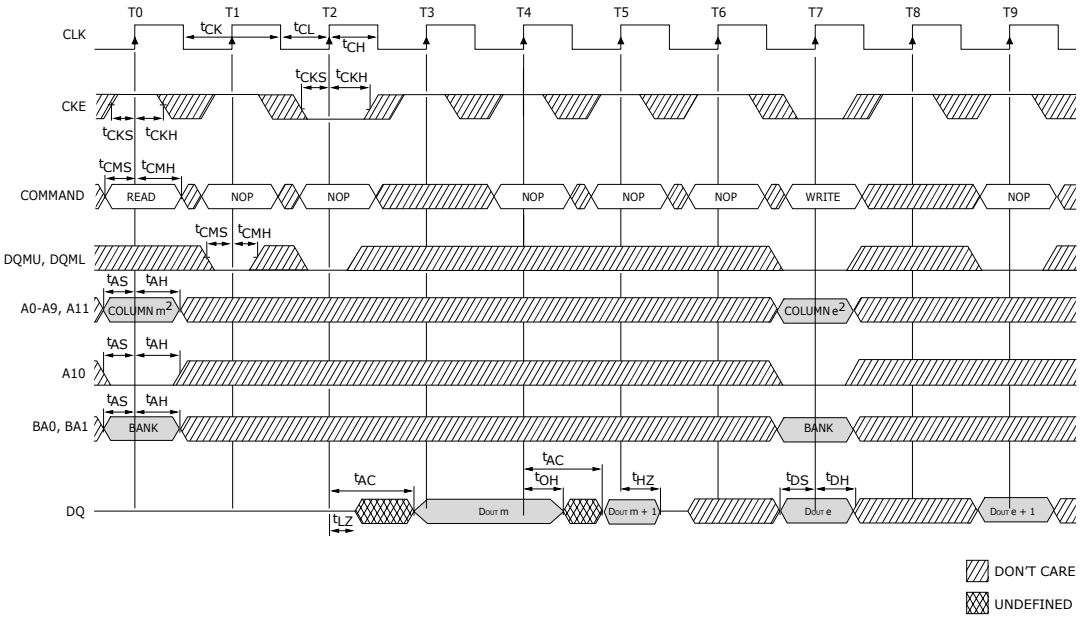


Figure 54. Clock Suspend Mode

Notes:

1. *For this example, the burst length = 2, the CAS latency = 3, and auto precharge is disabled.*
2. *A9 and A11 = "Don't Care."*

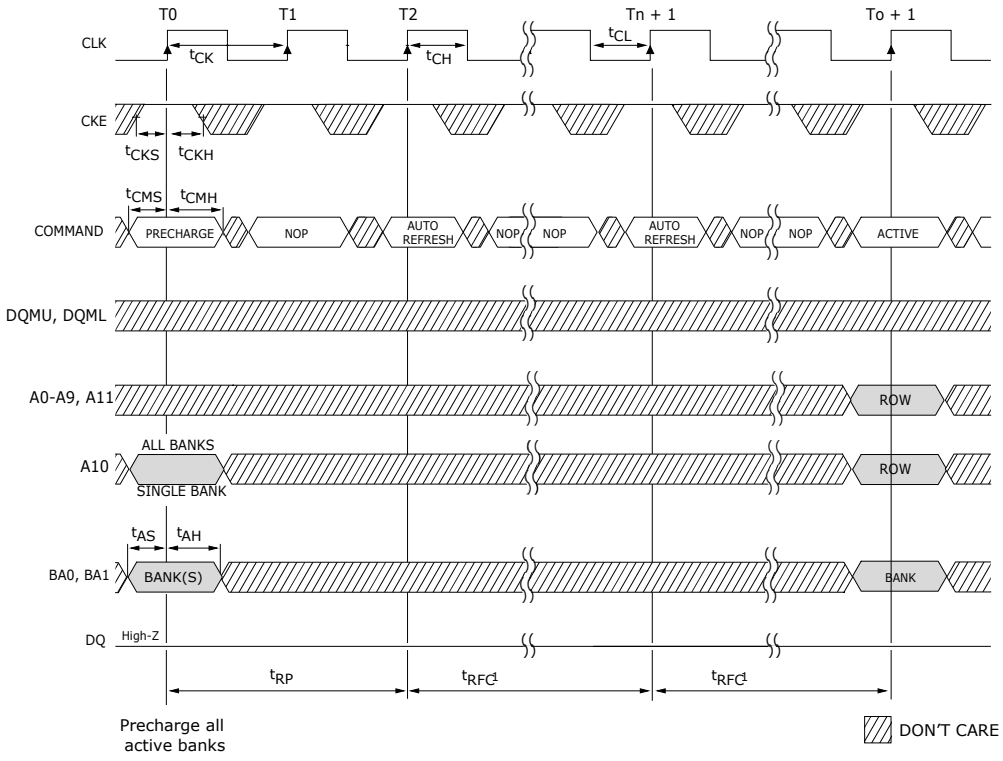


Figure 55. Auto Refresh Mode

Note: *Each Auto Refresh command performs a refresh cycle. Back-to-back commands are not required.*

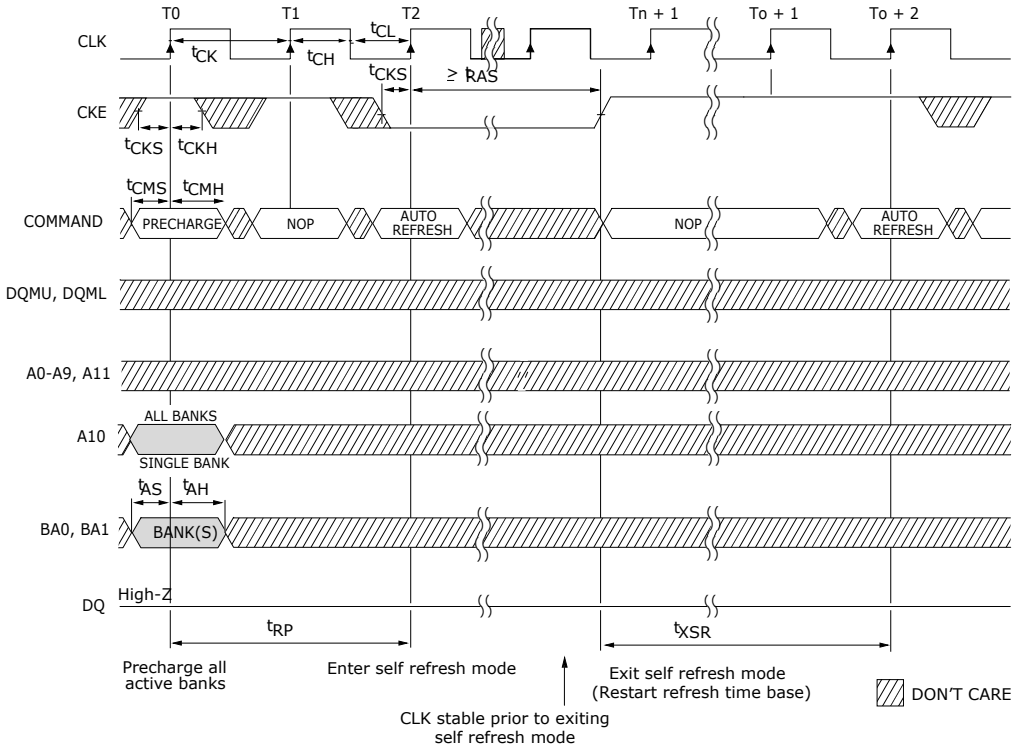


Figure 56. Self Refresh Mode

Note: *Each Auto Refresh command performs a refresh cycle. Back-to-back commands are not required.*

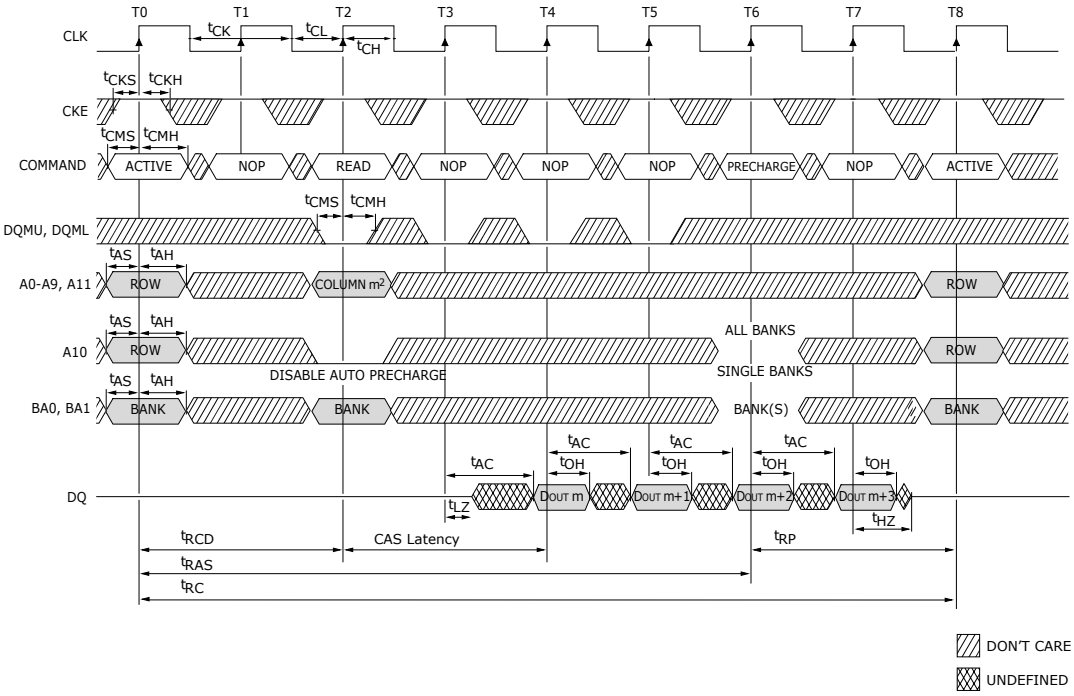


Figure 57. Read - Without Auto Precharge

Notes:

1. *For this example, the burst length = 4, the CAS latency = 2, and the Read burst is followed by a "manual" Precharge.*
2. *A9 and A11 = "Don't Care."*

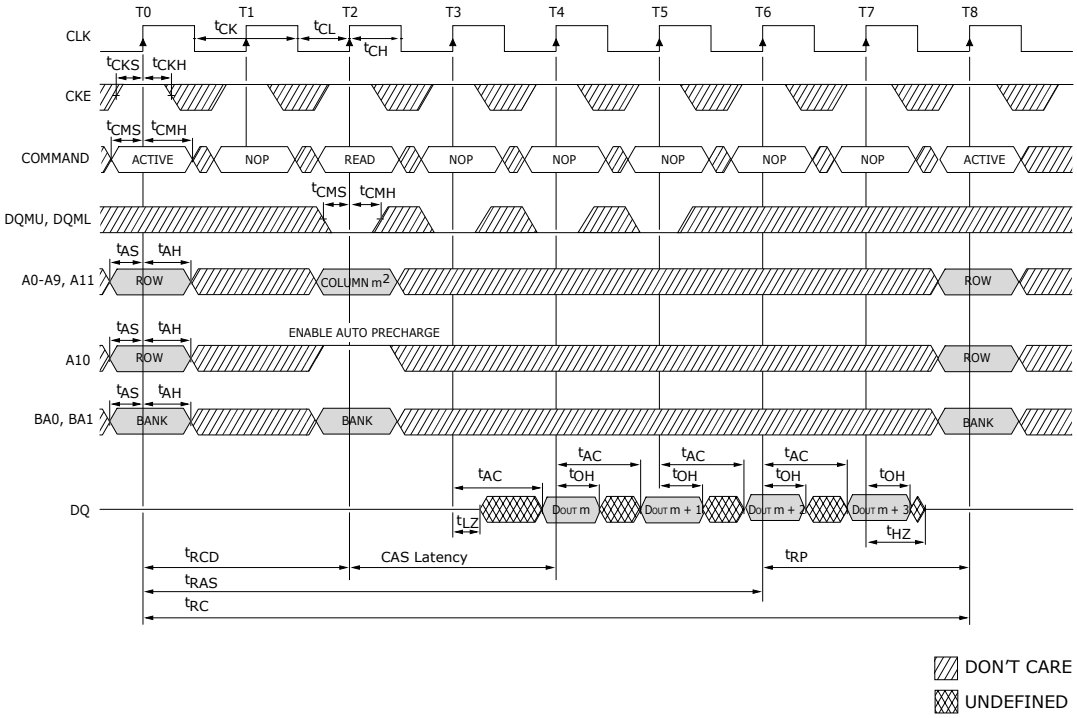


Figure 58. Read - With Auto Precharge

Notes:

1. *For this example, the burst length = 4, the CAS latency = 2.*
2. *A9 and A11 = "Don't Care."*

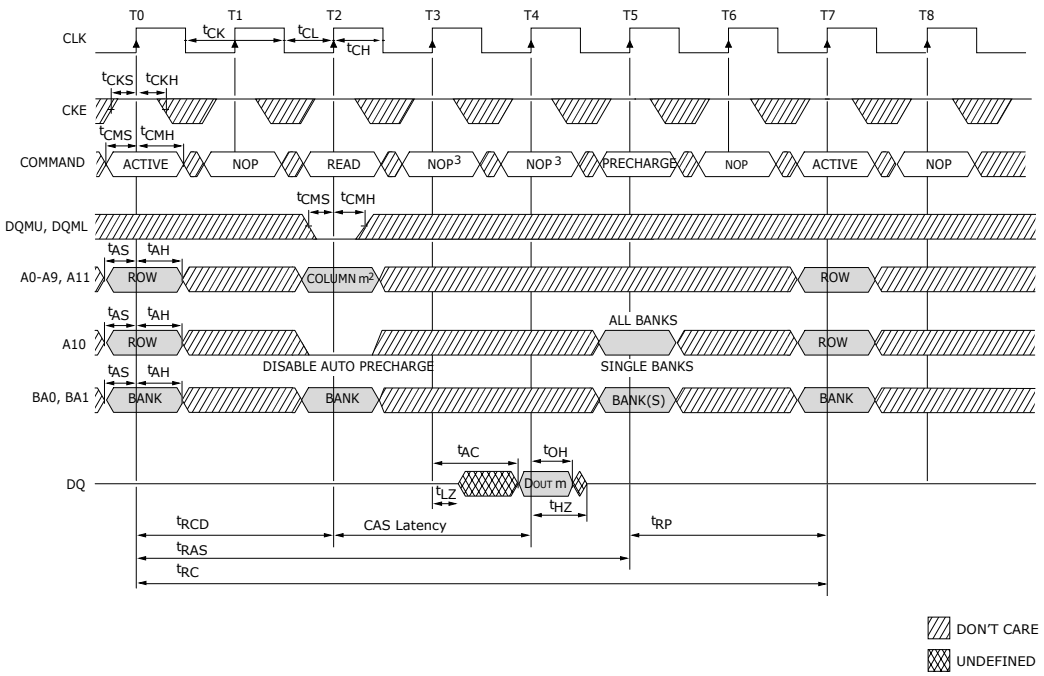


Figure 59. Single Read - Without Auto Precharge

Notes:

1. *For this example, the burst length = 4, the CAS latency = 2, and the Read burst is followed by a "manual" Precharge.*
2. *A9 and A11 = "Don't Care."*
3. *Precharge command not allowed or t_{RAS} would be violated.*

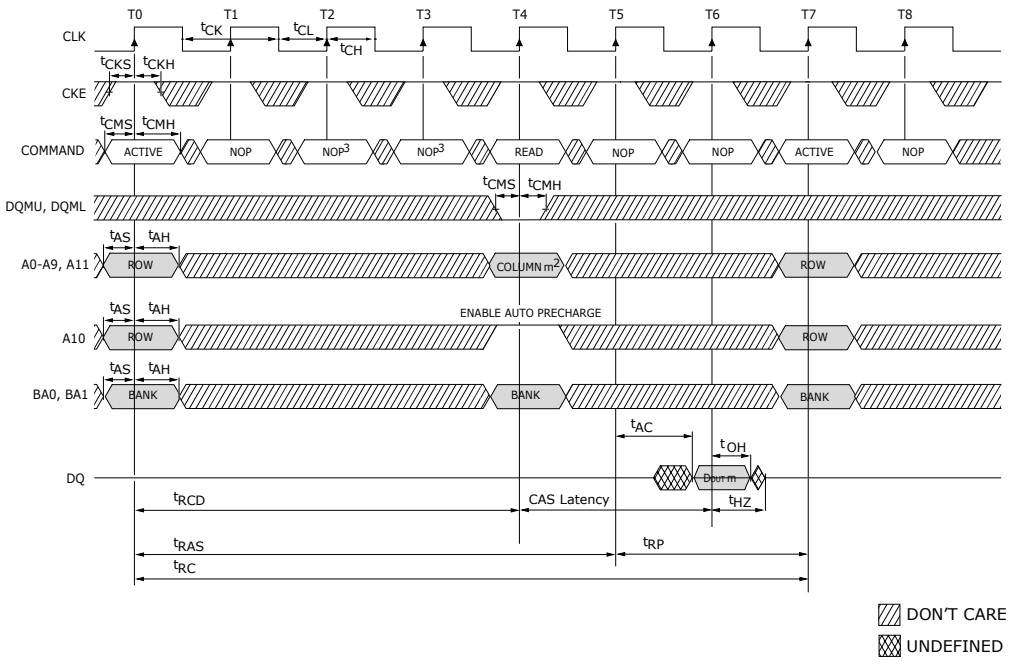


Figure 60. Single Read - With Auto Precharge

Notes:

1. *For this example, the burst length = 4, the CAS latency = 2, and the Read burst is followed by a "manual" Precharge.*
2. *A9 and A11 = "Don't Care."*
3. *Precharge command not allowed or t_{RAS} would be violated.*

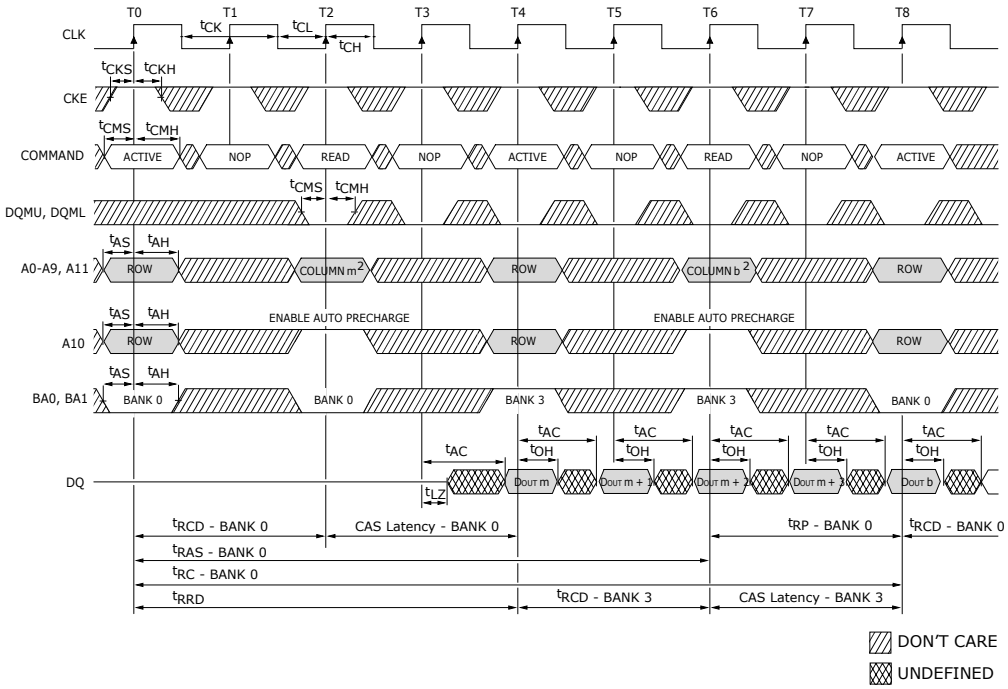


Figure 61. Alternating Bank Read Accesses

Notes:

1. *For this example, the burst length = 4, the CAS latency = 2.*
2. *A9 and A11 = "Don't Care."*

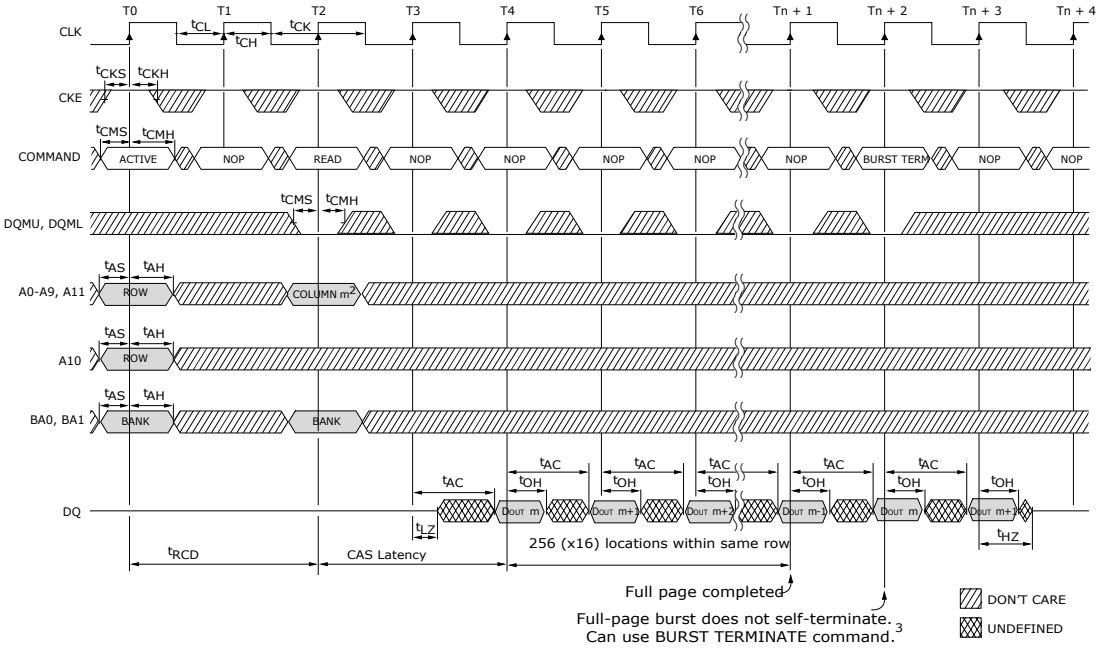


Figure 62. Read - Full-Page Burst

Notes:

1. *For this example, the CAS latency = 2.*
2. *A9 and A11 = "Don't Care."*
3. *Page left open; no t_{RP}.*

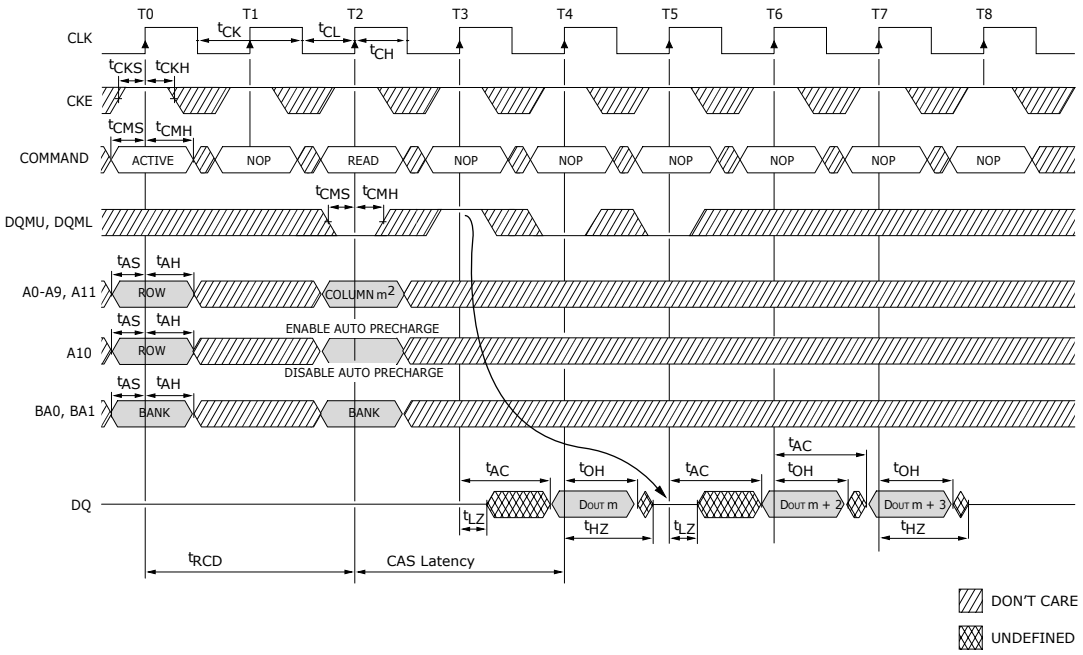


Figure 63. Read - DQM Operation

Notes:

1. *For this example, the CAS latency = 2.*
2. *A9 and A11 = "Don't Care."*

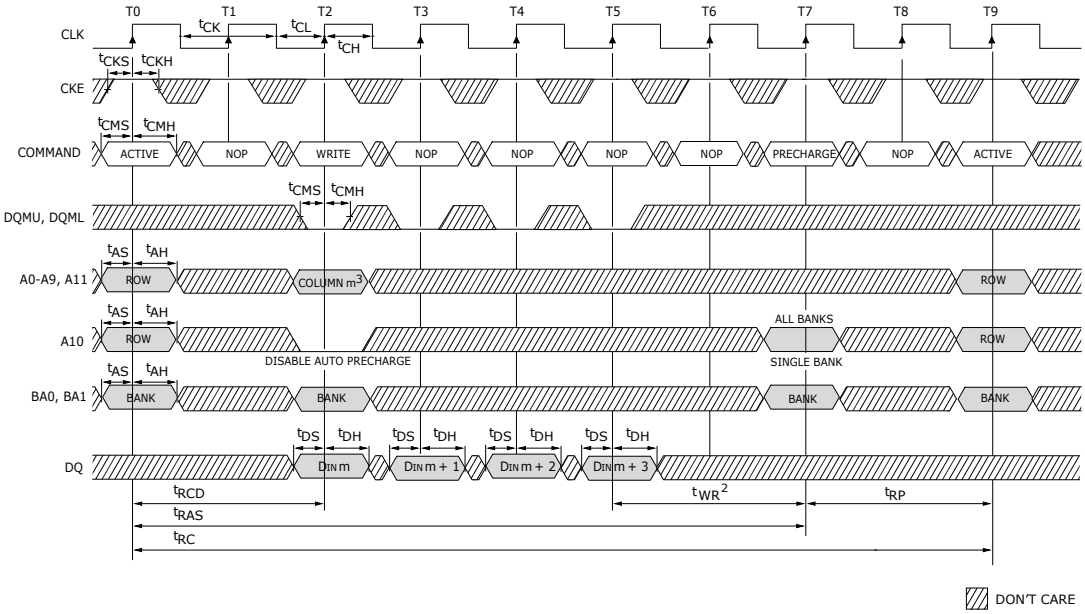


Figure 64. Write - Without Auto Precharge

Notes:

1. *For this example, the burst length = 4, and the Write burst is followed by a "manual" Precharge.*
2. *15ns is required between <DIN m + 3> and the Precharge command, regardless of frequency.*
3. *A9 and A11 = "Don't Care."*

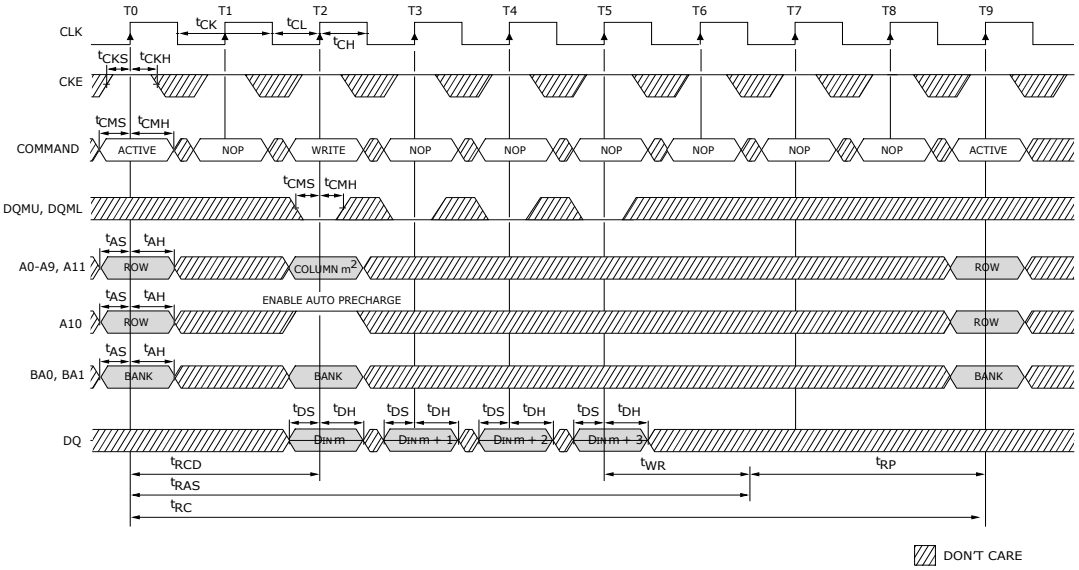


Figure 65. Write - With Auto Precharge

Notes:

1. *For this example, the burst length = 4.*
2. *A9 and A11 = "Don't Care."*

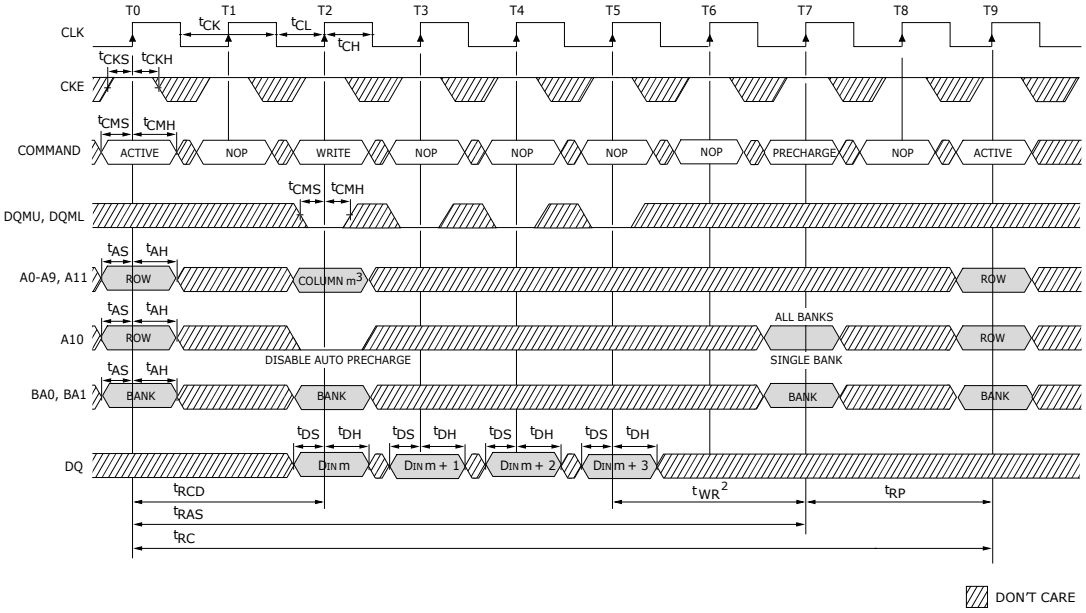


Figure 66. Single Write - Without Auto Precharge

Notes:

1. *For this example, the burst length = 1, and the Write burst is followed by a "manual" Precharge.*
2. *15ns is required between <DIN m> and the Precharge command, regardless of frequency.*
3. *A9 and A11 = "Don't Care."*
4. *Precharge command not allowed else t_{RAS} would be violated.*

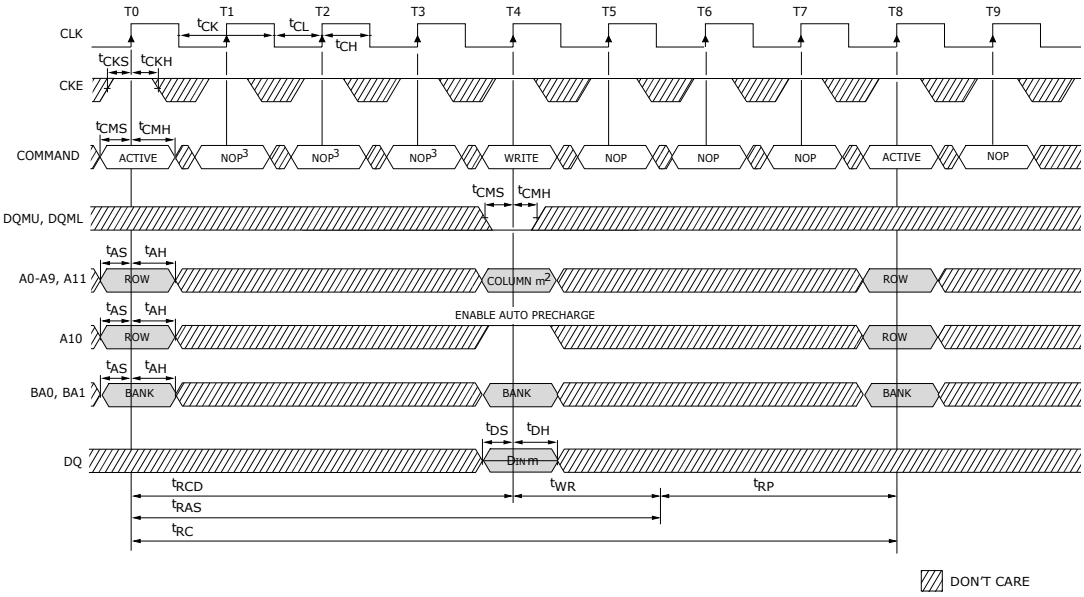


Figure 67. Single Write with Auto Precharge

Notes:

1. *For this example, the burst length = 1, and the Write burst is followed by a "manual" Precharge.*
2. *15ns is required between <DIN m> and the Precharge command, regardless of frequency.*
3. *A9 and A11 = "Don't Care."*
4. *Write command not allowed else t_{RAS} would be violated.*

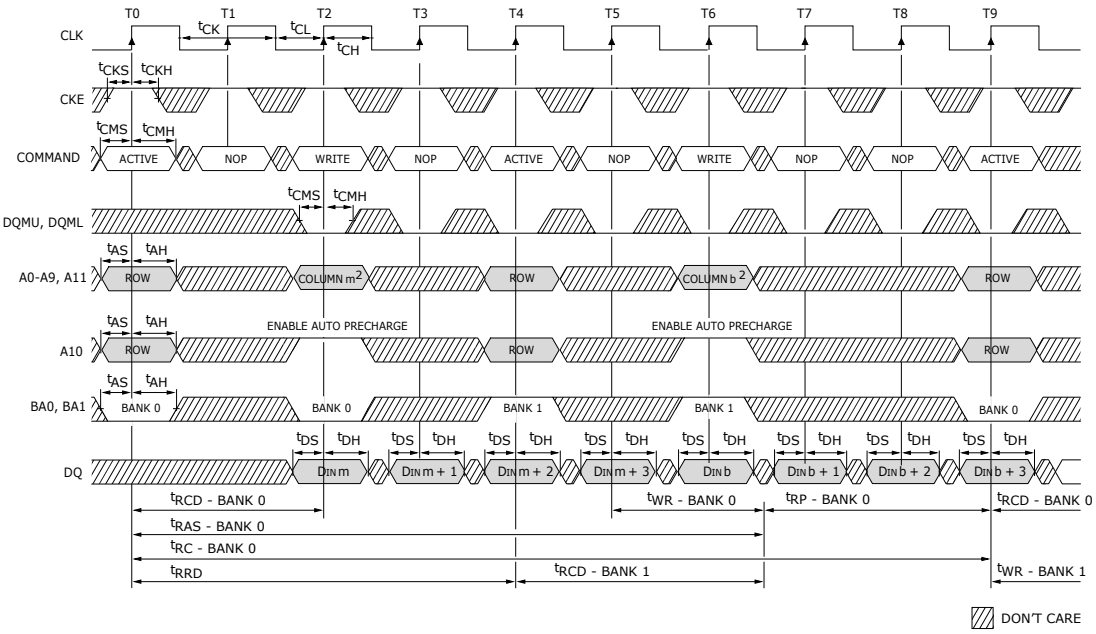


Figure 68. Alternating Bank Write Accesses

Notes:

1. *For this example, the burst length = 4.*
2. *A9 and A11 = "Don't Care."*

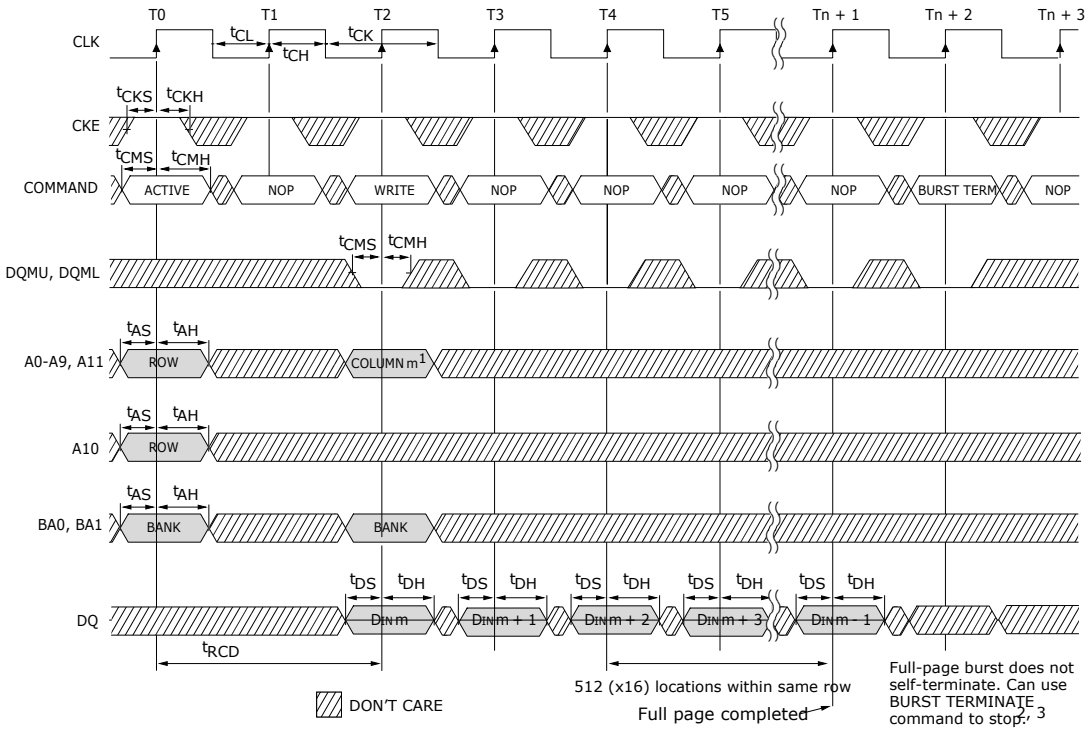


Figure 69. Write - Full Page Burst

Notes:

1. *A9 and A11 = "Don't Care."*
2. *t_{WR} must be satisfied prior to Precharge command.*
3. *Page left open; no t_{RP}.*

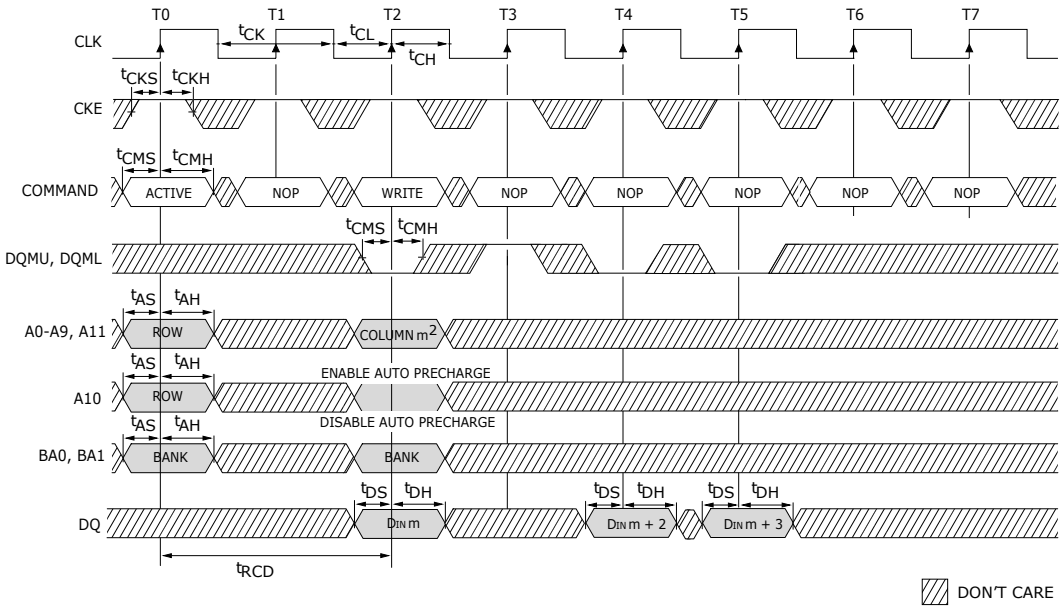


Figure 70. Write - DQM Operation

Notes:

1. *For this example, the burst length = 4.*
2. *A9 and A11 = "Don't Care."*

SDRAM Revision Summary

Revision A0 (August 8, 2004)

Initial Release

Revision AI (April I, 2005)

Cas Latency section updated

Bank/Row Activation section updated

Revision A2 (April 25, 2005)

Added 133 MHz speed grade option

S99KS256N MirrorBit™ Flash Family

256 Megabit (16 Mb x 16-bit), CMOS 1.8 Volt-only Data Storage, Multiplexed, Burst Mode Flash Memory

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

- **Single 1.8 volt read, program and erase (1.70 to 1.95 volt)**
- **VersatileIO™ Feature**
  - Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{CCQ} pin
  - 1.8 V compatible I/O signals
- **Multiplexed Data and Address for reduced I/O count**
  - A15–A0 multiplexed as DQ15–DQ0
  - Addresses are latched by AVD# control input when CE# low
- **Read access times at 80/66 MHz**
  - Burst access times of 9/11 ns at industrial temperature range
  - 80 ns asynchronous random access time
  - 80 ns synchronous random access time
- **Burst length**
  - Continuous linear burst
  - 8/16/32 word linear burst with wrap around
  - 8/16/32 word linear burst without wrap around
- **Secured Silicon Sector region**
  - 256 words accessible through a command sequence, 128 words for the Factory Secured Silicon Sector and 128 words for the Customer Secured Silicon Sector.
- **Power dissipation (typical values, 8 bits switching, C_L = 30 pF) @80 MHz**
  - Continuous Burst Mode Read: 35 mA
  - Program/Erase: 19 mA
  - Standby mode: 20 µA
- **Sector Architecture**
  - Four 16 K word sectors in upper-most address range
  - Two-hundred-fifty-five 64 Kword sectors
  - Sixteen Memory Arrays
- **High Performance**
  - Typical word programming time of 40 µs
  - Typical effective word programming time of 9.4 µs utilizing a 32-Word Write Buffer at Vcc Level
  - Typical effective word programming time of 6 µs utilizing a 32-Word Write Buffer at V_{PP} Level
  - Typical sector erase time of 350 ms for 16 Kword sectors and 800 ms sector erase time for 64 Kword sectors

Security features

- **Dynamic Sector Protection**
  - A command sector protection method to lock combinations of individual sectors to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Hardware Sector Protection**
  - WP# protects the two highest sectors
  - All sectors locked when $V_{PP} = V_{IL}$
- **Handshaking feature**
  - Provides host system with minimum possible latency by monitoring RDY
- **Software command set compatible with JEDEC 42.4 standards**
  - Backwards compatible with Am29F and Am29LV families
- **Manufactured on 110 nm MirrorBit™ process technology**
- **Cycling endurance: 100,000 cycles per sector typical**
- **Data retention: 20 years typical**
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Program Suspend/Resume**
  - Suspends a programming operation to read data from a sector other than the one being programmed, then resume the programming operation
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

General Description

The S99KS256N is a 256 Mb, 1.8 Volt-only, Burst Mode Flash memory device, is organized as 16,777,216 words of 16 bits each. This device uses a single V_{CC} of 1.70 to 1.95 V to read, program, and erase the memory array. A 9.0-volt V_{PP} can be used for faster program performance if desired. This device can also be programmed in standard EPROM programmers.

This device is offered at the following speeds:

Clock Speed	Burst Access (ns)	Synch. Initial Access (ns)	Asynch. Initial Access (ns)	Output Loading
80 MHz	9	80	80	30 pF
66 MHz	11.0	80	80	

The device operates within the temperature range of −25 °C to +85 °C, and are offered in Very Thin FBGA packages.

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{CCQ} pin.

The device uses Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the device additionally requires Ready (RDY) and Clock (CLK). This implementation allows easy interface with minimal glue logic to microprocessors/microcontrollers for high performance read operations.

The device offers complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bit** DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers three types of data protection at the sector level. **Dynamic Sector Protection** provides in-system, command-enabled protection of any combination of sectors using a single power supply at V_{CC}. When at V_{IL}, **WP#** locks the highest two sectors. Finally, when V_{PP} is at V_{IL}, all sectors are locked.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster program times by requiring only two write cycles to program data instead of four. Additionally, **Write Buffer Programming** is available on this device. This feature provides superior programming performance by grouping locations being programmed.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm - an internal algorithm that automatically preprograms the array (if it is not already fully programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The **Program Suspend/Program Resume** feature enables the user to put program on hold to read data from any sector that is not selected for programming. If a read is needed from the Dynamic Protection area after an program suspend, then the user must use the proper command sequence to enter and exit this region. The program suspend/resume functionality is also available when programming in erase suspend (1 level depth only).

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Dynamic Protection area after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a memory array program or erase operation is complete by using the device status bit DQ7 (Data# Polling), DQ6/DQ2 (toggle bits), DQ5 (exceeded timing limit), DQ3 (sector erase start timeout state indicator), and DQ1 (write to buffer abort). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. **The device is fully erased when shipped from the factory**.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers two types of data protection at the sector level. When at V_{IL}, **WP#** locks the two outermost boot sectors at the top of memory.

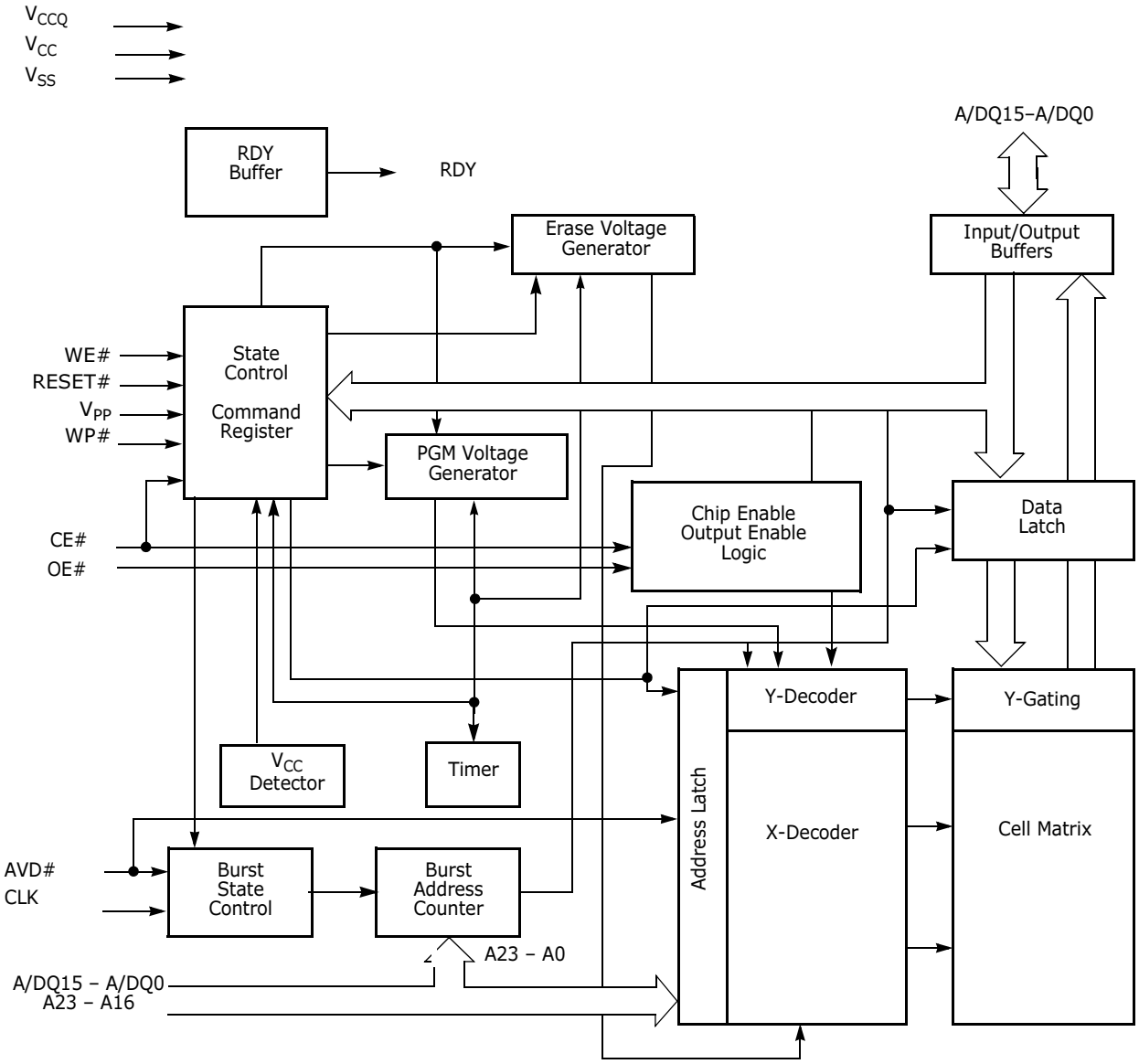
When the V_{PP} pin = V_{IL}, the entire flash memory array is protected.

Spansion LLC Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector. The data is programmed using hot electron injection.

Product Selector Guide

Description	S99KS256N	
Burst Frequency	**80 MHz**	**66 MHz**
Max Initial Synchronous Access Time, ns (T_{IACC})	80	80
Max Burst Access Time, ns (T_{BACC})	9	11.0
Max Asynchronous Access Time, ns (T_{ACC})	80	80
Max CE# Access Time, ns (T_{CE})		
Max OE# Access Time, ns (T_{OE})	9	11.0

Block Diagram

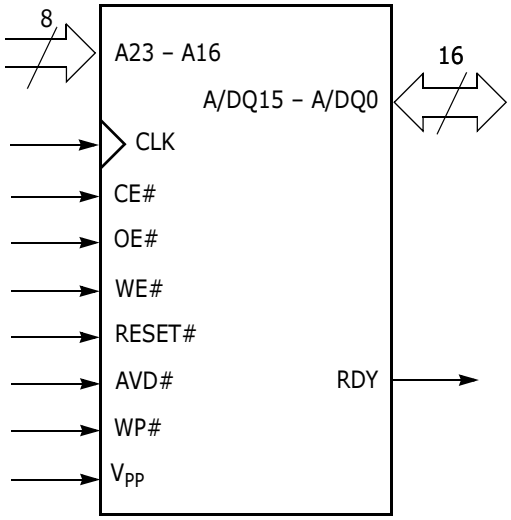


Note: *A15 – A0 are multiplexed with DQ15 – DQ0.*

Input/Output Descriptions

A23–A16	=	Address Inputs
A/DQ15–A/DQ0	=	Multiplexed Address/Data input/output
CE#	=	Chip Enable Input. Asynchronous relative to CLK for the Burst mode.
OE#	=	Output Enable Input. Asynchronous relative to CLK for the Burst mode.
WE#	=	Write Enable Input.
V_{CC}	=	Device Power Supply (1.70 V–1.95 V).
V_{CCQ}	=	Input/Output Power Supply (1.70 V–1.95 V).
V_{SS}	=	Ground
V_{SSQ}	=	Input/Output Ground
NC	=	No Connect; not connected internally
RDY	=	Ready output; indicates the status of the Burst read. V_{OL}= data invalid. V_{OH} = data valid.
CLK	=	The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
AVD#	=	Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15 – A0 are multiplexed, address bits A23 – A16 are address only). V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs
RESET#	=	Hardware reset input. V_{IL}= device resets and returns to reading array data
WP#	=	Hardware write protect input. V_{IL} = disables writes to SA257–258. Should be at V_{IH} for all other conditions.
V_{PP}	=	At 9 V, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions.

Logic Symbol



Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 43 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 43. Device Bus Operations

Operation	CE#	OE#	WE#	A23 –16	A/DQ15 – 0	RESET#	CLK	AVD#
Asynchronous Read	L	L	H	Addr In	I/O	H	L	⌐¯¬
Write	L	H	L	Addr In	I/O	H	H/L	⌐¯¬
Standby (CE#)	H	X	X	X	HIGH Z	H	H/L	X
Hardware Reset	X	X	X	X	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	H	H	Addr In	Addr In	H	⌐	⌐¯¬
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	X	Burst Data Out	H	⌐	H
Terminate current Burst read cycle	H	X	H	X	HIGH Z	H	⌐	X
Terminate current Burst read cycle via RESET#	X	X	H	X	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	H	H	X	I/O	H	⌐	⌐¯¬

Legend: *L = Logic 0, H = Logic 1, X = Don't Care.*

VersatileIO™ (V_{IO}) Control

The VersatileIO (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{CCQ} pin.

Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must assert a valid address on A23 – A16 and A/DQ15 – A/DQ0 while AVD# and CE# are at V_{IL}. WE# should remain at V_{IH}. Note that CLK must remain at V_{IL} during asynchronous read operations. The rising edge of AVD# latches the address, after which the system can drive OE# to V_{IL}. The data appears on A/DQ15–A/DQ0 (see Figure 82). Since the memory array is divided into regions, each regions remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

Requirements for Synchronous (Burst) Read Operation

The device is capable of seven different burst read modes: continuous burst read; 8-, 16-, and 32-word linear burst reads with wrap around; and 8-, 16-, and 32-word linear burst reads without wrap around.

Continuous Burst

When the device first powers up, it is enabled for asynchronous read operation. The device is automatically enabled for burst mode and addresses are latched on the first rising edge of CLK input, while AVD# is held low for one clock cycle.

Prior to activating the clock signal, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst session. The system would then write the Set Configuration Register command sequence.

The initial word is output t_{IACC} after the rising edge of the first CLK cycle. Subsequent words are output t_{BACC} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. **Note that the device has a fixed internal address boundary that occurs every 128 words, starting at address 00007Fh. The transition from the highest address 7FFFFFh to 000000h is also a boundary crossing**. During a boundary crossing, there is a no additional latency between the valid read at address 00007F and the valid read at address 000080 (or between addresses offset from these values by the same multiple of 128 words) for frequencies equal to or lower than 66 Mhz. For frequencies higher than 66 Mhz, there is a latency of 1 cycle.

During the time the device is outputting data with the starting burst address not divisible by four, additional waits are required. The RDY output indicates this condition to the system by deasserting.

Tables 44 – 47 show the address latency as a function of variable wait states.

Table 44. Address Latency for 7, 6 and 5 Wait States

Word										
0	7, 6, and 5 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	**1 ws**	D4	D5	D6	D7	D8
2		D2	D3	**1 ws**	**1 ws**	D4	D5	D6	D7	D8
3		D3	**1 ws**	**1 ws**	**1 ws**	D4	D5	D6	D7	D8

Table 45. Address Latency for 4 Wait States

Word										
0	4 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	**1 ws**	D4	D5	D6	D7	D8	D9
3		D3	**1 ws**	**1 ws**	D4	D5	D6	D7	D8	D9

Table 46. Address Latency for 3 Wait States

Word										
0	3 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	**1 ws**	D4	D5	D6	D7	D8	D9	D10

Table 47. Address Latency for 2 Wait States

Word										
0	2 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	D4	D5	D6	D7	D8	D9	D10	D11

Tables 48 – 51 show the address/boundary crossing latency for variable wait state if a boundary crossing occurs during initial access.

Table 48. Address/Boundary Crossing Latency for 7, 6, and 5 Wait States

Word										
0	7, 6, and 5 ws	D0	D1	D2	D3	**1 ws**	D4	D5	D6	D7
1		D1	D2	D3	**1 ws**	**1 ws**	D4	D5	D6	D7
2		D2	D3	**1 ws**	**1 ws**	**1 ws**	D4	D5	D6	D7
3		D3	**1 ws**	**1 ws**	**1 ws**	**1 ws**	D4	D5	D6	D7

Table 49. Address/Boundary Crossing Latency for 4 Wait States

Word										
0	4 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	**1 ws**	D4	D5	D6	D7	D8
2		D2	D3	**1 ws**	**1 ws**	D4	D5	D6	D7	D8
3		D3	**1 ws**	**1 ws**	**1 ws**	D4	D5	D6	D7	D8

Table 50. Address/Boundary Crossing Latency for 3 Wait States

Word										
0	3 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	**1 ws**	D4	D5	D6	D7	D8	D9
3		D3	**1 ws**	**1 ws**	D4	D5	D6	D7	D8	D9

Table 5I. Address/Boundary Crossing Latency for 2 Wait States

Word										
0	2 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	**1 ws**	D4	D5	D6	D7	D8	D9	D10

The device continues to output continuous, sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system asserts CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 43. The reset command does *not* terminate the burst read operation.

If the host system crosses a 128 word line boundary while reading in burst mode, and the device is not programming or erasing, no additional latency occurs as described above. If the host system crosses the region boundary while the device is programming or erasing, the device provides asynchronous read status information. The clock is ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

8-, 16-, and 32-Word Linear Burst with Wrap Around

These three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 52.)

Table 52. Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h, 18-1Fh...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh, 30-3Fh...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh, 60-7Fh...

As an example: if the starting address in the 8-word mode is 3Ah, and the burst sequence would be 3A-3B-3C-3D-3E-3F-38-39h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wraps back to the first address in the selected address group and terminates the burst read. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 128 words; thus, no wait states are inserted (except during the initial access).**

8-, 16-, and 32-Word Linear Burst without Wrap Around

In these modes, a fixed number of words (predefined as 8, 16, or 32 words) are read from consecutive addresses starting with the initial word, which is written to the device. When the address is at the end of the group address range (see Table 52), the burst read operation stops and the RDY output goes low. There is no group limitation and is different from the Linear Burst with Wrap Around.

As an example, for 8-word length Burst Read, if the starting address written to the device is 3A, the burst sequence would be 3A-3B-3C-3D-3E-3F-40-41h, and the read operation is terminated after all eight words. The 16-word and 32-word modes would operate in a similar fashion and continuously read to the predefined 16 or 32 words accordingly. **Note: In this burst read mode, the address pointer may cross the boundary that occurs every 128 words.**

Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after AVD# is driven active before data is available. Upon power up, the device defaults to the maximum of seven total cycles. The total number of wait states is programmable from two to seven cycles. For further details, see Set Configuration Register Command Sequence.

Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, burst length, RDY configuration, and synchronous mode active.

Handshaking Feature

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the configuration register to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

Writing Commands/Command Sequences

The device has inputs/outputs that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 56 – 59 indicates the address space that each sector occupies. The device address space is divided into multiple regions. A "Memory Region" is the address bits required to uniquely select a region. Similarly, a "sector address" is the address bits required to uniquely select a sector.

See the table, CMOS Compatible, (in DC Characteristics) for write mode current specifications. AC Characteristics contains timing specification tables and timing diagrams for write operations.

Accelerated Program and Erase Operations

The device offers accelerated program and erase operation through the V_{PP} function. V_{PP} is primarily intended to allow faster manufacturing throughput at the factory and not to be used in system operations.

If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program and erase operations. The system can then use the abbreviated Embedded Programming command and Write Buffer Load command sequence provided by the Unlock Bypass mode. Note that if a "Write-to-Buffer-Abort Reset" is required while in Unlock Bypass mode, the **full 3-cycle RESET command sequence must be used to reset the device**. Removing V_{HH} from the V_{PP} input, upon completion of the embedded program or erase operation, returns the device to normal operation. Note that sectors must be unlocked prior to raising V_{PP} to V_{HH}. *Note that the V_{PP} pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the V_{PP} pin must not be left floating or unconnected; inconsistent behavior of the device may result*.

When at V_{IL}, V_{PP} locks all sectors. V_{PP} should be at V_{IH} for all other conditions.

Write Buffer Programming Operation

Write Buffer Programming allows the system to write a maximum of **32** words in one programming operation. This results in a faster effective word programming time than the standard "word" programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming occurs. At this point, the system writes the number of "**word locations minus 1**" that are loaded into the page buffer at the Sector Address in which programming occurs. This tells the device how many write buffer addresses load with data and when to expect the "Program Buffer to Flash" confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts. (NOTE: The number loaded = the number of locations to program minus 1. For example, if the system programs 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the "write-buffer-page" address. All subsequent address/data pairs **must** fall within the "selected-write-buffer-page", and be loaded in sequential order.

The "write-buffer-page" is selected by using the addresses A23 - A5.

The "write-buffer-page" addresses **must be the same for all address/data pairs loaded into the write buffer**. (This means Write Buffer Programming **cannot** be performed across multiple "write-buffer-pages". This also means that Write Buffer Programming **cannot** be performed across multiple sectors. If the system attempts to load programming data outside of the selected "write-buffer-page", the operation ABORTS.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer. Write buffer locations must be loaded in sequential order.

Note that if a Write Buffer address location is loaded multiple times, the "address/data pair" counter **is decremented for every data load operation**. Also, the **last data loaded** at a location before the "Program Buffer to Flash" confirm command is programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements **for each data load operation**, **NOT for each unique write-buffer-address location**.

Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" command at the Sector Address. Any other address/data write combinations abort the Write Buffer Programming operation. The device then "goes busy." The Data Bar polling techniques should be used while monitoring the **last address location loaded into the write buffer**. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then data bar poll at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer "embedded" programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device returns to READ mode.

The Write Buffer Programming Sequence can be ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the "Number of Locations to Program" step.
- Write to an address in a sector different than the one specified during the "Write-Buffer-Load" command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the "Starting Address" during the "write buffer data loading" stage of the operation.

- Write data other than the "Confirm Command" after the specified number of "data load" cycles.

The ABORT condition is indicated by DQ1 = 1, DQ7 = DATA# (for the "last address location loaded"), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A "Write-to-Buffer-Abort reset" command sequence is required when using the Write-Buffer-Programming features in Unlock Bypass mode. **Note: The Secured Silicon sector and autoselect are unavailable when a program operation is in progress**.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed. Write buffer programming is allowed in any sequence of memory (or address) locations. This flash device is capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. However, programming the same word address multiple times without intervening erases requires a modified programming method. Please contact your local Spansion™ representative for details.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output from the internal register (which is separate from the memory array) on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. The autoselect codes can also be accessed in-system.

When verifying sector protection, the sector address must appear on the appropriate highest order address bits. The remaining address bits are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0. The autoselect codes can also be accessed in-system through the command register. The command sequence is illustrated in Table 62. *Note that if a Region Address (RA) on address bits A23, A22, A21, and A20 for the KS256N, is asserted during the third write cycle of the autoselect command, the host system can read autoselect data from that region and then immediately read array data from the other region, without exiting the autoselect mode.*

To access the autoselect codes, the host system must issue the autoselect command via the command register, as shown in Table 62.

Sector Protection and Unprotection

This security feature provides an additional level of protection to all sectors against inadvertent program or erase operations.

The advanced sector protection feature disables both programming and erase operations in any sector while the advanced sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented using either of the two methods

- Hardware method
- Software method

Dynamic Sector Protection is achieved by using the software method while the sector protection with WP# pin is achieved by using the hardware method.

Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

- Dynamic Sector Protection

A software enabled command sector protection method that replaces the old 12 V controlled protection method.

- WP# Hardware Protection

A write protect pin (WP#) can prevent program or erase operations in the outermost sectors.The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Dynamic Sector Protection

Dynamic Protection Bit (DYB)

DYB is a security feature used to protect individual sectors from being programmed or erased inadvertently. It is a volatile protection bit and is assigned to each sector. Upon power-up or a hardware reset, the contents of all DYBs are set (programmed to "0"). Each DYB can be individually modified through the DYB Set Command or the DYB Clear Command.

The Protection Status for a particular sector is determined by the status of the DYB relative to that sector. The DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Set or Clear command sequences, the DYBs are set (programmed to "0") or cleared (erased to "1"), thus placing each sector in the protected or unprotected state respectively. These states are the so-called Dynamic Locked or Unlocked states due to the fact that they can switch back and forth between the protected and unprotected states. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs may be set (programmed to "0") or cleared (erased to "1") as often as needed.

When the parts are first shipped, and upon power up or reset, the DYBs are set. (programmed to "0").

If there is a need to protect some of the sectors, a simple DYB Set command sequence is all that is necessary. The DYB Set or Clear command for the dynamic sectors signify protected or unprotected state of the sectors respectively. Note that the DYB bits have the same function when V_{PP} = V_{HH} as the DYB bits do when V_{PP} = V_{IH}.

The DYB controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program or erase command to a protected sector enables status polling and returns to read mode without having modified the contents of the protected sector.

The programming of the DYB for a given sector can be verified by writing individual status read commands DYB Status to the device.

Hardware Data Protection Mode

The device offers two types of data protection at the sector level:

- When WP# is at V_{IL}, the two outermost sectors at the top are locked (device specific).
- When V_{PP} is at V_{IL}, all sectors are locked. SA257 and SA258 are locked (S99KS256N)

The write protect pin (WP#) adds a final level of hardware program and erase protection to the boot sectors. The boot sectors are the two sectors containing the highest set of addresses in this top-boot-configured device. For the none boot option, the WP# hardware feature is not available. **When this pin is low it is not possible to change the contents of these top sectors.** These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the two outermost sectors. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the "top" boot sectors. If the system asserts V_{IH} on the WP# pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

WP# Boot Sector Protection

The WP# signal is latched at a specific time in the embedded program or erase sequence. To prevent a write to the top two sectors, WP# must be asserted (WP#=V_{IL}) on the last write cycle of the embedded sequence (i.e., 4th write cycle in embedded program, 6th write cycle in embedded erase).

If selecting multiple sectors for erasure: The WP# protection status is latched only on the 6th write cycle of the embedded sector erase command sequence when the first sector is selected. If additional sectors are selected for erasure, they are subject to the WP# status that was latched on the 6th write cycle of the command sequence.

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when VCC is greater than VLKO.

Write Pulse "Glitch" Protection

Noise pulses of less than t_{WEP} on WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up

Lock Register

The Lock Register consists of 3 bits. Each of these bits are non-volatile and read-only. DQ15-DQ3 are reserved and are undefined.

Table 53. Lock Register

DQ15 – 1	DQ0
Undefined	Secured Silicon Sector Protection Bit

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC}. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enters this mode when addresses and clock remain stable for t_{ACC} + 20 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}, the standby current is greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

See the AC Characteristics tables for RESET# parameters and to Figure 83 for the timing diagram.

V_{CC} Power-up and Power-down Sequencing

The device imposes no restrictions on V_{CC} power-up or power-down sequencing. Asserting RESET# to V_{IL} is required during the entire V_{CC} power sequence until the respective supplies reach their operating voltages. Once V_{CC} attains its operating voltage, de-assertion of RESET# to V_{IH} is permitted.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 words in length. All reads outside of the 256 word address range return non-valid data. The Factory Indicator Bit (DQ7) is used to indicate whether or not the Factory Secured Silicon Sector is locked when shipped from the factory. The Customer Indicator Bit (DQ6) is used to indicate whether or not the Customer Secured Silicon Sector is locked when shipped from the factory. The Factory Secured Silicon bits are permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN and customer code once the product is shipped to the field.

Spansion offers the device with a Factory Secured Silicon Sector that is locked and a Customer Secured Silicon Sector that is either locked or is lockable. The Factory Secured Silicon Sector is always protected when shipped from the factory, and has the Factory Indicator Bit (DQ7) permanently set to a "1". The Customer Secured Silicon Sector is shipped unprotected, allowing customers to utilize that sector in any manner they choose. Once the Customer Secured Silicon Sector area is protected, the Customer Indicator Bit is permanently set to "1."

The system accesses the Secured Silicon Sector through a command sequence (see Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence on page 172). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by sector SA0 of the memory array. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. While Secured Silicon Sector access is enabled, Memory Array read access, program operations, and erase operations to all sectors other than SA0 are also available. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

Factory Locked: Factor Secured Silicon Sector Programmed and Protected At the Factory

In a factory sector locked device, the Factory Secured Silicon Sector is protected when the device is shipped from the factory. The Factory Secured Silicon Sector cannot be modified in any way. The device is pre programmed with both a random number and a secure ESN. The Factory Secured Silicon Sector is located at addresses 000000h–00007Fh.

The device is available pre programmed with one of the following:

- A random, secure ESN only within the Factor Secured Silicon Sector
- Customer code within the Customer Secured Silicon Sector through the Spansion™ programming services
- Both a random, secure ESN and customer code through the Spansion™ programming services.

Table 54. Secured Silicon Sector Addresses

Sector	Sector Size	Address Range
Customer	128 words	000080h-0000FFh
Factory	128 words	000000h-00007Fh

Customers may opt to have their code programmed by Spansion through the Spansion™ programming services. Spansion programs the customer's code, with or without the random ESN. The device is then shipped from the Spansion factory with the Factory Secured Silicon Sector and Customer Secured Silicon Sector permanently locked. Contact a Spansion representative for details on using Spansion programming services.

Customer Secured Silicon Sector

If the security feature is not required, the Customer Secured Silicon Sector can be treated as an additional Flash memory space. The Customer Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (V_{PP}) and unlock bypass functions are not available when programming the Customer Secured Silicon Sector, but reading the first region through the last region is available. The Customer Secured Silicon Sector is located at addresses 000080h–0000FFh.

The Customer Secured Silicon Sector area can be protected by writing the Secured Silicon Sector Protection Bit Lock command sequence.

Once the Customer Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing SA0 in the memory array.

The Customer Secured Silicon Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the Customer Secured Silicon Sector area and none of the bits in the Customer Secured Silicon Sector memory space can be modified in any way.

Table 55. Sector Address Table, S99KS256N

Memory Region	Sector Count	Sector Size (KB)	Sector/ Sector Range	Address Range
0	16	128	SA0 – SA15	000000h – FEFFFFh
1	16	128	SA16 – SA31	100000h – 1FFFFFh
2	16	128	SA32 – SA47	200000h – 2FFFFFh
3	16	128	SA48 – SA63	300000h – 3FFFFFh
4	16	128	SA64 – SA79	400000h – 4FFFFFh
5	16	128	SA80 – SA95	500000h – 5FFFFFh
6	16	128	SA96 – SA111	600000h – 6FFFFFh
7	16	128	SA112 – SA127	700000h – 7FFFFFh
8	16	128	SA128 – SA143	800000h – 8FFFFFh
9	16	128	SA144 – SA159	900000h – 9FFFFFh
10	16	128	SA160 – SA175	A00000h – AFFFFFh
11	16	128	SA176 – SA191	B00000h – BFFFFFh
12	16	128	SA192 – SA207	C00000h – CFFFFFh
13	16	128	SA208 – SA223	D00000h – DFFFFFh
14	15	128	SA224 – SA239	E00000h – EFFFFFh
15	15	128	SA240 – SA254	F00000h – FEFFFFh
	4	32	SA255 – SA258	FF0000h – FFFFFFh

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 62 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the rising edge of AVD#. All data is latched on the rising edge of WE#. See AC Characteristics for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each region is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding region enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands on page 177 for more information.

After the device accepts a Program Suspend command, the corresponding region enters the program-suspend-read mode, after which the system can read data from any non-program-suspended sector within the same region.

The system *must* issue the reset command to return a region to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the region is in the autoselect mode.

For more information, also see VersatileIO™ (V_{IO}) Control on page 154 and Requirements for Synchronous (Burst) Read Operation on page 154 in Device Bus Operations. The Asynchronous Read on page 197 and Synchronous/Burst Read on page 195 tables provide the read parameters, and Figure 81 and Figure 82 show the timing diagrams.

Set Configuration Register Command Sequence

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, RDY configuration, and synchronous mode active. The configuration register must be set before the device enters burst mode.

The configuration register is loaded with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be D0h and address bits should be 555h. During the fourth cycle, the configuration code should be entered onto the data bus with the address bus set to address 000h. Once the data has been programmed into the configuration register, a software reset command is required to set the device into the correct state. The device powers up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

Read Configuration Register Command Sequence

The configuration register can be read with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C6h and address bits should be 555h. During the fourth cycle, the configuration code should be read out of the data bus with the address bus set to address 000h. Once the data has been read from the configuration register, a software reset command is required to set the device into the correct set mode.

Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations.

Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before the data is available. This value is determined by the input frequency of the device. **Configuration Bit CR13 – CR11** determine the setting (see Table 56).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 56. Programmable Wait State Settings

CR13	CR12	CR11	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7 (default)
1	1	0	Reserved
1	1	1	Reserved

Notes:

1. *Upon power-up or hardware reset, the default setting is seven wait states.*
2. *RDY defaults to being active with data when the Wait State Setting is set to a total initial access cycle of 2.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset sets the wait state to the default setting.

Programmable Wait State

The host system should set **CR13-CR11** to 101/100/011 for a clock frequency of 80 / 66 MHz for the system/device to execute at maximum speed.

Table 57 describes the typical number of clock cycles (wait states) for various conditions.

Table 57. Wait States for Handshaking

Conditions at Address	Typical No. of Clock Cycles after AVD# Low	
	80 MHz	66 MHz
Initial address (V_{CCQ} = 1.8 V)	7	6

Handshaking

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on the clock frequency.

The autoselect function allows the host system to determine whether the flash device is enabled for handshaking.

Burst Length Configuration

The device supports four different read modes: continuous mode, and 8, 16, and 32 word linear with or without wrap-around modes. A continuous sequence (default) begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear read with wrap around begins on the starting address written to the device and then advances to the next 8 word boundary. The address pointer then returns to the 1st word after the previous eight word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 58 shows the **CR2-CR0** and settings for the four read modes.

Table 58. Burst Length Configuration

Burst Modes	Address Bits		
	CR2	CR1	CR0
Continuous	0	0	0
8-word linear	0	1	0
16-word linear	0	1	1
32-word linear	1	0	0

Notes:

1. *Upon power-up or hardware reset the default setting is continuous.*
2. *All other conditions are reserved.*

Burst Wrap Around

By default, the device performs burst wrap around with **CR3** set to a '1.' Changing the **CR3** to a '0' disables burst wrap around.

RDY Configuration

By default, the device is set so that the RDY pin outputs V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. **CR8** determines this setting; "1" for RDY active (default) with data, "0" for RDY active one clock cycle before valid data.

RDY Polarity

By default, the RDY pin always indicates that the device is ready to handle a new transaction with **CR10** set to a '1'. In this case, the RDY pin is active high. Changing the **CR10** to a '0' sets the RDY pin to be active low. In this case, the RDY pin always indicates that the device is ready to handle a new transaction when low.

Configuration Register

Table 59 shows the address bits that determine the configuration register settings for various device functions.

Table 59. Configuration Register

CR Bit	Function	Settings (Binary)
CR15	Reserved	0 = Default
CR14	Reserved	0 = Default
CR13	Programmable Wait State	000 = Data is valid on the 2nd active CLK edge after AVD# transition to V_{IH} 001 = Data is valid on the 3rd active CLK edge after AVD# transition to V_{IH} 010 = Data is valid on the 4th active CLK edge after AVD# transition to V_{IH} 011 = Data is valid on the 5th active CLK edge after AVD# transition to V_{IH} 100 = Data is valid on the 6th active CLK edge after AVD# transition to V_{IH} 101 = Data is valid on the 7th active CLK edge after AVD# transition to V_{IH} (default) 110 = Reserved 111 = Reserved
CR12		
CR11		
CR10	RDY Polarity	0 = RDY signal is active low 1 = RDY signal is active high (default)
CR9	Reserved	1 = Default
CR8	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
CR7	Reserved	1 = Default
CR6		
CR5	Reserved	0 = Default
CR4		
CR3	Burst Wrap Around	0 = No Wrap Around Burst 1 = Wrap Around Burst (default)
CR2	Burst Length	000 = Continuous (default) 010 = 8-Word Linear Burst 011 = 16-Word Linear Burst 100 = 32-Word Linear Burst (All other bit settings are reserved)
CR1		
CR0		

Note: *Device is in the default state upon power-up or hardware reset.*

Reset Command

Writing the reset command resets the regions to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the region to which the system was writing to the read mode. **Once erasure begins, however, the device ignores reset commands until the operation is complete**.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the region to which the system was writing to the read mode. If the program command sequence is written to a region that is in the Erase Suspend mode, writing the reset command returns that region to the erase-suspend-read mode. **Once programming begins, however, the device ignores reset commands until the operation is complete**.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a region entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that region to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the regions to the read mode (or erase-suspend-read mode if that region was in Erase Suspend).

Note: If DQ1 goes high during a Write Buffer Programming operation, the system must write the "Write to Buffer Abort Reset" command sequence to RESET the device to reading array data. The standard RESET command does not work. See Table 62 for details on this command sequence.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 62 shows the address and data requirements. The autoselect command sequence may be written to an address within a region that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other region. Autoselect does not support burst mode.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the region address and the autoselect command. The region then enters the autoselect mode. The system may read at any address within the same region any number of times without initiating another autoselect command sequence. Table 60 describes the address requirements for the various autoselect functions, and the resulting data. RA represents the region address. The device ID is read in three cycles. During this time, other regions are still available to read the data from the memory.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the region was previously in Erase Suspend).

Table 60. Device ID

Description	Address	Read Data
		256N
Manufacturer ID	(RA) + 00h	0001h
Device ID, Word 1	(RA) + 01h	2D7E
Device ID, Word 2	(RA) + 0Eh	2D2F
Device ID, Word 3	(RA) + 0Fh	2D00
Revision ID	(RA) + 03h	TBD
Sector Block Lock/Unlock	(SA) = 02h	0001 - Locked 0000 - Unlocked
Indicator Bits	(RA) + 07h	DQ15 - DQ8 = Reserved DQ7 - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ6 - Customer Lock Bit 1 = Locked, 0 = Not Locked DQ5 Handshake Bit 1 = Reserved 0 = Standard Handshake DQ4 & DQ3 - WP# Protections Boot Code 01 = WP# Protects only the Top Boot Sectors DQ2-DQ0 = Reserved

Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 62 shows the address and data requirements for both command sequences.

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program faster than the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That region then enters the unlock bypass mode.

During the unlock bypass mode only the command is valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the region address and the data 90h. The second cycle need only contain the data 00h. The region then returns to the read mode.

Program Command Sequence

Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 62 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that region then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. See Write Operation Status on page 183 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that region has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may causes that region to set DQ5 = 1 (change-up condition). However, a succeeding read shows that the data is still "0." Only erase operations can convert a "0" to a "1."

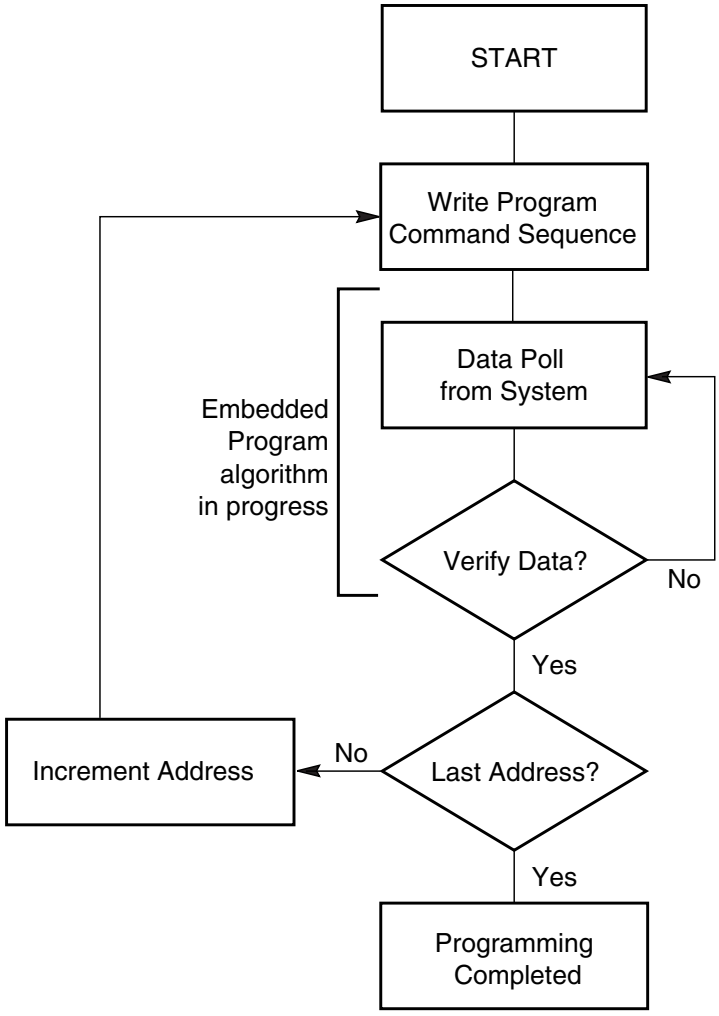
Program Command Sequence (Unlock Bypass Mode)

Once the device enters the unlock bypass mode, then a two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 62 shows the requirements for the unlock bypass command sequences.

Accelerated Program

The device offers accelerated program operations through the V_{PP} input. When the system asserts V_{PP} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the V_{PP} input to accelerate the operation.

Figure 71 illustrates the algorithm for the program operation. See the Erase/Program Operations table in AC Characteristics for parameters, and Figure 84 for timing diagrams.



Note: *See Table 62 for program command sequence*

Figure 7I. Program Operation

Write Buffer Programming Command Sequence

Write Buffer Programming Sequence allows for faster programming as compared to the standard Program Command Sequence. See Table 61 for the program command sequence.

Table 61. Write Buffer Command Sequence

Sequence	Address	Data	Comment
Unlock Command 1	555	00AA	Not required in the Unlock Bypass mode
Unlock Command 2	2AA	0055	Same as above
Write Buffer Load	Starting Address	0025h	
Specify the Number of Program Locations	Starting Address	Word Count	Number of locations to program minus 1
Load 1st data word	Starting Address	Program Data	All addresses must be within write-buffer-page boundaries, but do not have to be loaded in any order
Load next data word	Write Buffer Location	Program Data	Same as above
...	...	...	Same as above
Load last data word	Write Buffer Location	Program Data	Same as above
Write Buffer Program Confirm	Sector Address	0029h	This command must follow the last write buffer location loaded, or the operation ABORTS
Device goes busy			
Status monitoring through DQ pins (Perform Data Bar Polling on the **Last Loaded Address**)			

Note: *Write buffer addresses must be loaded in sequential order.*

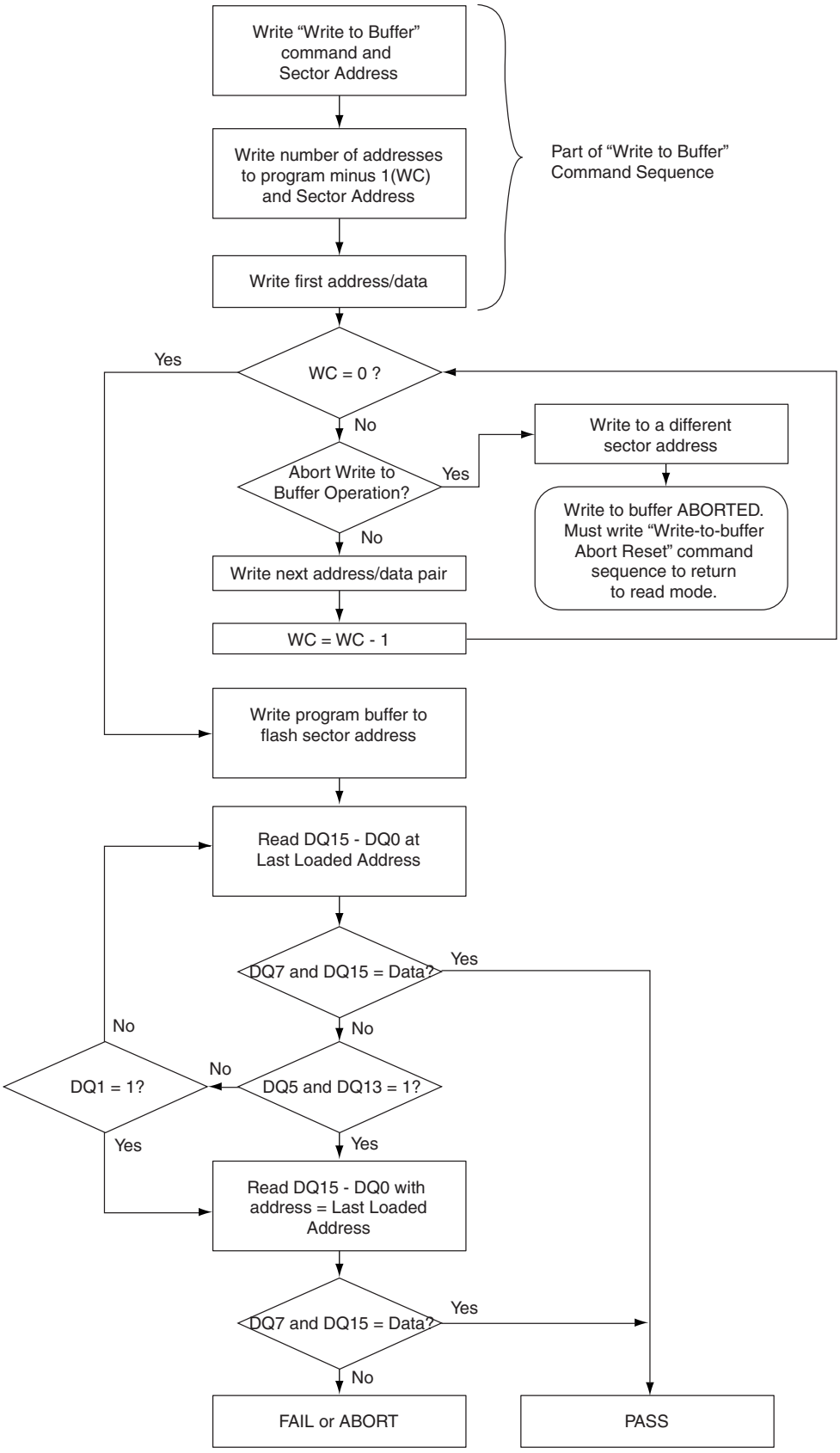


Figure 72. Write Buffer Programming Operation

Chip Erase Command Sequence

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 62 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that region returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. See Write Operation Status on page 183 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that region has returned to reading array data, to ensure data integrity.

Sector Erase Command Sequence

Sector Erase Command Sequence

Sector erase in normal mode is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 62 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than t_{SEA}, sector erase accept, occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than t_{SEA}. Any sector erase address and command following the exceeded time-out may or may not be accepted. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that region to the read mode.**

The system can monitor DQ3 to determine if the sector erase timer has timed out (see DQ3: Sector Erase Start Timeout State Indicator on page 188). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the region returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing regions. The system can determine the status of the erase operation by reading DQ7 or DQ6/ DQ2 in the erasing region. See Write Operation Status on page 183 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that region has returned to reading array data, to ensure data integrity.

Accelerated Sector Erase

The device offers accelerated sector erase operation through the V_{PP} function. This method of erasing sectors is faster than the standard sector erase command sequence. **The accelerated sector erase function must not be used more than 100 times per sector.** In addition, accelerated sector erase should be performed at room temperature (30°C +-10°C).

The following procedure is used to perform accelerated sector erase:

1. Sectors to be erased must be DYB cleared. All sectors that remain locked are not erased.
2. Apply 9 V to the V_{PP} input. This voltage must be applied at least 1 µs before completing step 3.
3. Issue the standard chip erase command.
4. Monitor status bits DQ2/DQ6 or DQ7 to determine when erasure is complete, just as in the standard erase operation. See Write Operation Status on page 183 for further details.
5. Lower V_{PP} from 9 V to V_{CC}.

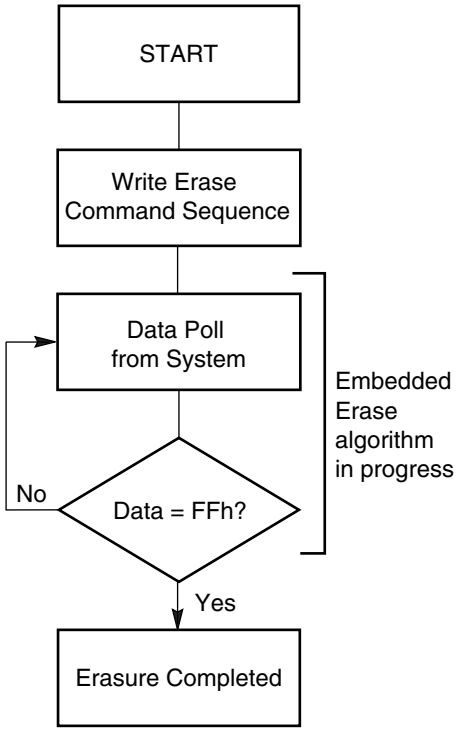


Figure 73. Erase Operation

Note: *See DQ3: Sector Erase Start Timeout State Indicator on page 188 for information.*

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, program data to, any sector not selected for erasure. The system may also lock or unlock any sector while the erase operation is suspended. **The system must not write the sector lock/unlock command to sectors selected for erasure.** The region address is required when writing this command. This command is valid only during the sector erase operation, including the minimum t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of t_{ESL}, erase suspend latency, to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the region enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) The system may also lock or unlock any sector while in the erase-suspend-read mode. Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See Write Operation Status on page 183 for information on these status bits.

After an erase-suspended program operation is complete, the region returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. See Autoselect Command Sequence for details.

To resume the sector erase operation, the system must write the Erase Resume command. The region address of the erase-suspended region is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt a embedded programming operation or a "Write to Buffer" programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL}, program suspend latency, and updates the status bits. Addresses are defined when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One Time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence on page 171 for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are "don't care") to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

Lock Register Command Set Definitions

The Lock Register Command Set permits the user to read the Lock Register.

The Lock Register Command Set Entry command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Lock Register Command Set Entry** command disables reads and writes for Region 0. Reads from other regions excluding Region 0 are allowed.

- Lock Register Read Command
- Lock Register Exit Command

The **Lock Register Command Set Exit** command **must** be issued after the execution of the commands to reset the device to read mode, and re-enables reads and writes for Region 0.

Volatile Sector Protection Command Set

The Volatile Sector Protection Command Set permits the user to set the Dynamic Protection Bit (DYB), clear the Dynamic Protection Bit (DYB), and read the logic state of the Dynamic Protection Bit (DYB).

The **Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Volatile Sector Protection Command Set Entry** command disables reads and writes for the region selected with the command. Reads for other regions excluding the selected region are allowed.

- DYB Set Command
- DYB Clear Command
- DYB Status Read Command

The DYB Set/Clear command is used to set or clear a DYB for a given sector. The high order address bits (A23 – A14) are issued at the same time as the code 00h or 01h on DQ7 – DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time. The DYBs are set at power-up or hardware reset.

The programming state of the DYB for a given sector can be verified by writing a DYB Status Read Command to the device.

Note: The region entered during entry is the active region. Take for example the active region is RA0. Any reads in RA0 results in status reads of the DYB bit. If the user wants to set (programmed to "0") in a different region other than the active region, for example RA5, then the active region switches from RA0 to RA5. Reading in RA5 results in status read of the bit whereas reading in RA0 results in true data.

The **Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Volatile Sector Protection Command Set Exit** command re-enables reads and writes for the region selected.

Table 62. Command Definitions (Sheet I of 2)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (7)		1	RA	RD												
Reset (8)		1	XXX	F0												
Autoselect (9)	Manufacturer ID	4	555	AA	2AA	55	(MR) 555	90	(MR) X00	0001						
	Device ID	6	555	AA	2AA	55	(MR) 555	90	(MR) X01	(Note 10)	(MR) X0E	(Note 10)	(MR) X0F	(Note 10)		
	Indicator Bits (11)	4	555	AA	2AA	55	(MR) 555	90	(MR) X0D	(Note 11)						
	Revision ID	4	555	AA	2AA	55	(MR) 555	90	(MR) X03							
Unlock Bypass	Mode Entry	3	555	AA	2AA	55	555	20								
	Program (12)	2	XXX	A0	PA	PD										
	Reset (13)	2	MR	90	XXX	00										
Program		4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer (17)		6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD		
Program Buffer to Flash		1	SA	29												
Write to Buffer Abort Reset (18)		3	555	AA	2AA	55	555	F0								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend / Program Suspend (14)		1	MR	B0												
Erase Resume / Program Resume (15)		1	MR	30												
Set Config. Register (25)		4	555	AA	2AA	55	555	D0	X00	CR						
Read Configuration Register		4	555	AA	2AA	55	555	C6	X00	CR						
Lock Register Command Set Definitions																
Lock	Lock Register Command Set Entry	3	555	AA	2AA	55	555	40								
	Lock Register Bits Read	1	(MR0) 00	data												
	Lock Register Command Set Exit (21)	2	XX	90	XX	00										
Secured Silicon Sector Command Definitions																
Secured Silicon Sector	Secured Silicon Sector Entry (19)	3	555	AA	2AA	55	555	88								
	Secured Silicon Sector Program	2	XX	A0	00	data										
	Secured Silicon Sector Read	1	00	data												
	Secured Silicon Sector Exit (21)	4	555	AA	2AA	55	555	90	XX	00						

Table 62. Command Definitions (Sheet 2 of 2)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Volatile Sector Protection Command Set Definitions																
DYB	Volatile Sector Protection Command Set Entry (19)	3	555	AA	2AA	55	(MR) 555	E0								
	DYB Set	2	XX	A0	(MR) SA	00										
	DYB Clear	2	XX	A0	(MR) SA	01										
	DYB Status Read	1	(MR) SA	RD(0)												
	Volatile Sector Protection Command Set Exit (23)	2	XX	90	XX	00										

Legend:

X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.
PD(0) = Secured Silicon Sector Lock Bit. PD(0), or bit[0].
SA = Address of the sector to be verified (in autoselect mode) or erased. SA includes MR. Address bits A23–A13 uniquely select any sector.
MR = Address of the memory region that is being switched to autoselect mode, is in bypass mode, or is being erased.
CR = Configuration Register set by data bits D15-D0.
RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0, if unprotected, DQ0 = 1.
RD(1) = DQ1 protection indicator bit. If protected, DQ1 = 0, if unprotected, DQ1 = 1.
RD(2) = DQ2 protection indicator bit. If protected, DQ2 = 0, if unprotected, DQ2 = 1.
RD(4) = DQ4 protection indicator bit. If protected, DQ4 = 0, if unprotected, DQ4 = 1.
WBL = Write Buffer Location. Address must be within the same write buffer page as PA.
WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 43 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A23–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence can place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when the region is reading array data.*
8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a region is in the autoselect mode, or if DQ5 goes high (while the region is providing status information).*
9. *The fourth cycle of the autoselect command sequence is a read cycle. The system must read device IDs across the 4th, 5th, and 6th cycles, The system must provide the region address. See Autoselect Command Sequence for more information.*
10. *See Table 60 for description of bus operations.*
11. *See Autoselect Command Sequence.*
12. *The Unlock Bypass command sequence is required prior to this command sequence.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the region is in the unlock bypass mode.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the region address.*
15. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the region address.*
16. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
17. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.*
18. *Command sequence resets device for next command after write-to-buffer operation.*
19. *Entry commands are needed to enter a specific mode to enable instructions only available within that mode.*
20. *Write Buffer Programming can be initiated after Unlock Bypass Entry.*

21. The Exit command must be issued to reset the device into read mode. Otherwise the device hangs.
22. Note: Autoselect, OTP, Unlock Bypass Mode and all ASP modes cannot be nested with each other.
23. Only A7 –A0 (lower address bits) are used
24. A23 – A0 (all address bits) are used.
25. Requires the RESET# command to configure the configuration register.

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 64 and the following sections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a region is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. **Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page returns false status information.**

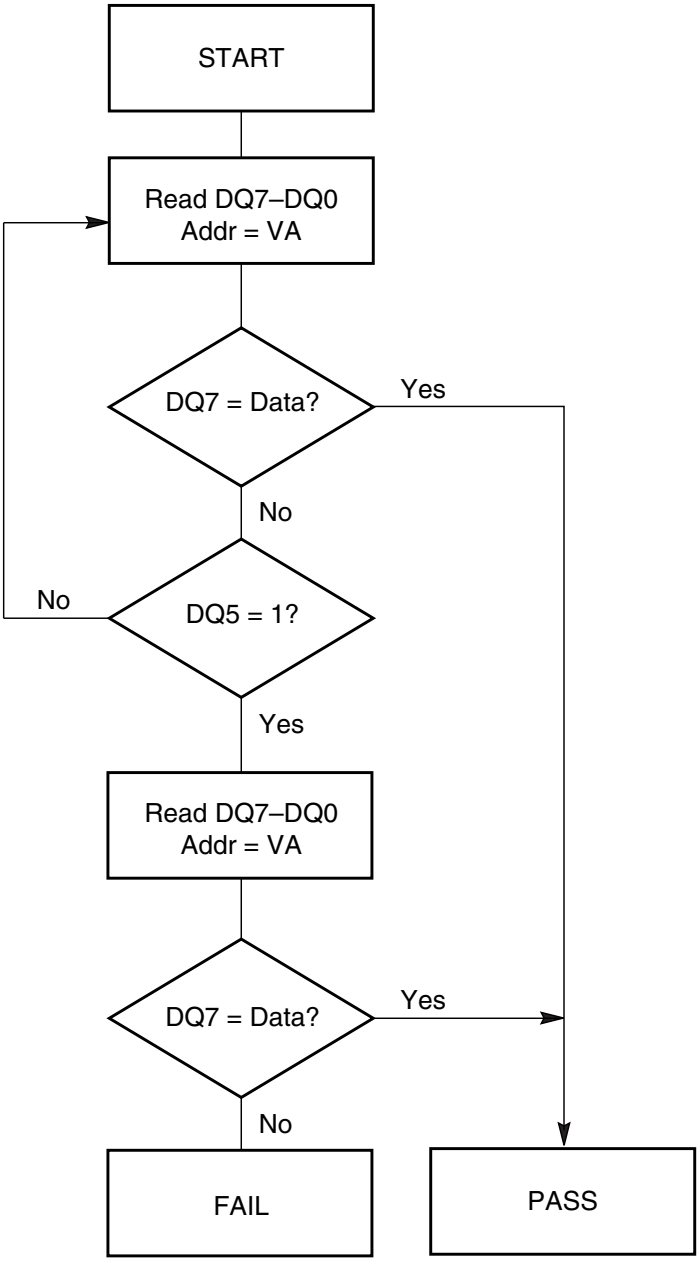
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately t_{PSP}, then that region returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the region enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{ASP}, then the region returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6–DQ0 may be still invalid. Valid data on DQ7–DQ0 appears on successive read cycles.

Table 64 shows the outputs for Data# Polling on DQ7. Figure 74 shows the Data# Polling algorithm. Figure 87 in AC Characteristics shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5*

Figure 74. Data# Polling Algorithm

RDY: Ready

The RDY pin is a dedicated status output that indicates valid output data on A/DQ15–A/DQ0 during burst (synchronous) reads. When RDY is asserted (RDY = V_{OH}), the output data is valid and can be read. When RDY is de-asserted (RDY = V_{OL}), the system should wait until RDY is re-asserted before expecting the next word of data.

In synchronous (burst) mode with CE# = OE# = V_{IL}, RDY is de-asserted under the following conditions: during the initial access; after crossing the internal boundary between addresses 7Eh and 7Fh (and addresses offset from these by a multiple of 64). The RDY pin also switches during status reads when a clock signal drives the CLK input. In addition, RDY = V_{OH} when CE# = V_{IL} and OE# = V_{IH}, and RDY is Hi-Z when CE# = V_{IH}.

In asynchronous (non-burst) mode, the RDY pin does not indicate valid or invalid output data. Instead, RDY = V_{OH} when CE# = V_{IL}, and RDY is Hi-Z when CE# = V_{IH}.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same region, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase timeout.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. Note that OE# must be low during toggle bit status reads. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{ASP}, all sectors protected toggle time, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately t_{PSP} after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

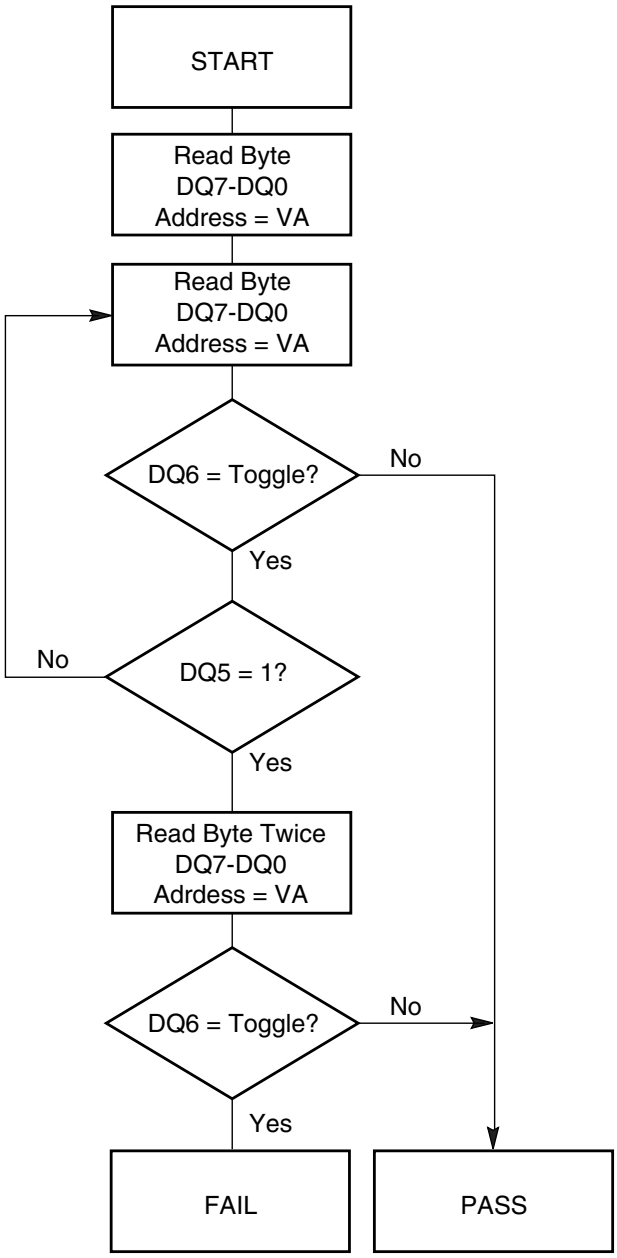
See the following for additional information: (toggle bit flowchart), DQ6: Toggle Bit I (description), Figure 88 (toggle bit timing diagram), and Table 63 (compares DQ2 and DQ6).

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. Note that OE# must be low during toggle bit status reads. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 64 to compare outputs for DQ2 and DQ6.

See the following for additional information: (toggle bit flowchart), DQ6: Toggle Bit I (description), Figure 88 (toggle bit timing diagram), and Table 63 (compares DQ2 and DQ6).



Note:

The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See DQ6: Toggle Bit I and DQ2: Toggle Bit IIfor more information

Figure 75. Toggle Bit Algorithm

Table 63. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see DQ5: Exceeded Timing Limits). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a region was previously in the erase-suspend-program mode).

DQ3: Sector Erase Start Timeout State Indicator

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. Also, see Sector Erase Command Sequence on page 176.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device accepts additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 64 shows the status of DQ3 relative to the other status bits.

DQ1: Write to Buffer Abort

DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a '1'. The system must issue the Write to Buffer Abort Reset command sequence to return the device to reading array data. See Write Buffer Programming Operation on page 159 for more details.

Table 64. Write Operation Status

Status			DQ7 (Note 3)	DQ6	DQ5 (Note 2)	DQ3	DQ2 (Note 3)	DQ1 (Note 5)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A
Program Suspend Mode (Note 4)	Reading within Program Suspended Sector		Valid data for all address except the address being programed, which returns invalid data					
	Reading within Non-Program Suspended Sector		Data					
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	N/A
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	Data
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	N/A
Write to Buffer (Note 6)	BUSY State		DQ7#	Toggle	0	N/A	N/A	0
	Exceeded Timing Limits		DQ7#	Toggle	1	N/A	N/A	0
	ABORT State		DQ7#	Toggle	0	N/A	N/A	1

Notes:

1. *Status information must be read from the same sector where the write operation is being performed.*
2. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See DQ5: Exceeded Timing Limits for more information.*
3. *DQ7 and DQ2 require a valid address when reading status information. See DQ7: Data# Polling and DQ2: Toggle Bit II for further details.*
4. *Data are invalid for addresses in a Program Suspended sector.*
5. *DQ1 indicates the Write to Buffer ABORT status during Write Buffer Programming operations.*
6. *The data-bar polling algorithm should be used for Write Buffer Programming operations. Note that DQ7# during Write Buffer Programming indicates the data-bar for DQ7 data* ***for the LAST LOADED WRITE-BUFFER ADDRESS location****.*

Absolute Maximum Ratings

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground, All Inputs and I/Os except V_{PP} (Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V

V_{CC} (Note 1) . . . . . –0.5 V to +2.5 V

V_{PP} (Note 2) . . . . . –0.5 V to + 9.5 V

Output Short Circuit Current (Note 3). . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, input at I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns during voltage transitions inputs might overshooot to V_{CC} +0.5 V for periods up to 20 ns. See Figure 76. Maximum DC voltage on output and I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 77.*
2. *Minimum DC input voltage on V_{PP} is –0.5 V. During voltage transitions, V_{PP} may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 76. Maximum DC input voltage on V_{PP} is +9.5 V which may overshoot to +10.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

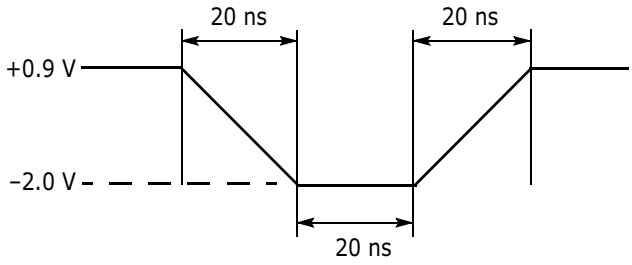


Figure 76. Maximum Negative Overshoot Waveform

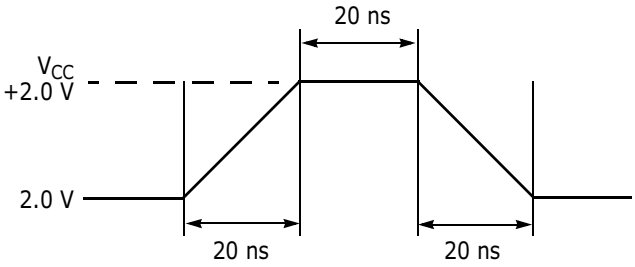


Figure 77. Maximum Positive Overshoot Waveform

Operating Ranges

Ambient Temperature (T_A) . . . . . –25°C to +85°C

Ambient Temperature (T_A) during Accelerated Sector Erase . . . . . +20°C to +40°C

V_{CC} Supply Voltages

V_{CC} min . . . . . +1.70 V

V_{CC} max . . . . . +1.95 V

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

DC Characteristics

CMOS Compatible

Parameter	Description	Test Conditions (Note 1)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{CCB}	V_{CC} Active Burst Read Current (Note 5)	CE# = V_{IL}, OE# = V_{IL}, burst length = 8	80 MHz		26	36	mA
			66 MHz		24	33	
		CE# = V_{IL}, OE# = V_{IL}, burst length = 16	80 MHZ		26	38	mA
			66 MHz		24	35	
		CE# = V_{IL}, OE# = V_{IL}, burst length = 32	80 MHZ		28	40	mA
			66 MHz		26	37	
		CE# = V_{IL}, OE# = V_{IL}, burst length = continuous	80 MHZ		30	42	mA
			66 MHz		28	39	
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 2)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		15	18	mA
			1 MHz		3	4	mA
I_{CC2}	V_{CC} Active Write Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}, $V_{PP} = V_{IH}$			19	52.5	mA
I_{CC3}	V_{CC} Standby Current (Note 4)	CE# = V_{IH}, RESET# = V_{IH} (Note 8)			20	70	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL} (Note 8)			80	150	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IL} (Note 8)			50	60	mA
I_{CC6}	V_{CC} Sleep Current	CE# = V_{IL}, OE# = V_{IH}			20	70	µA
I_{PPW}	Accelerated Program Current (Note 6)	V_{PP} = 9 V			20	30	mA
I_{PPE}	Accelerated Erase Current (Note 6)	V_{PP} = 9 V			20	30	mA
V_{IL}	Input Low Voltage			–0.5		0.4	V
V_{IH}	Input High Voltage			V_{IO} – 0.4		V_{IO} + 0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{IO} – 0.1			V
V_{ID}	Voltage for Accelerated Program			8.5		9.5	V
V_{LKO}	Low V_{CC}, Lock-out Voltage			1.0		1.4	V

Notes:

1. *Maximum I_{CC} spnts2ecifications are tested with $V_{CC} = V_{CC}$max.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 20 ns. Typical sleep mode current is equal to I_{CC3}.*
5. *Specifications assume 8 I/Os switching and continuous burst length.*
6. *Not 100% tested. V_{PP} is not a power supply pin.*
7. *While measuring Output Leakage Current, CE# should be at V_{IH}.*
8. *$V_{IH} = V_{CC}$ ± -0.2 V and V_{IL} > -0.1V.*

Test Conditions

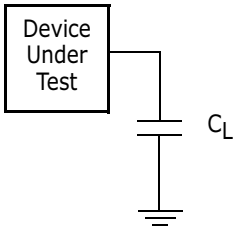
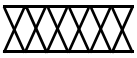
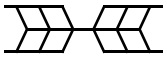


Figure 78. Test Setup

Table 65. Test Specifications

Test Condition	All Speeds	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	2.5 @ 80 MHz, 3 @ 66 MHz	ns
Input Pulse Levels	0.0–V_{CC}	V
Input timing measurement reference levels	V_{IO} / 2	V
Output timing measurement reference levels	V_{IO} / 2	V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Switching Waveforms

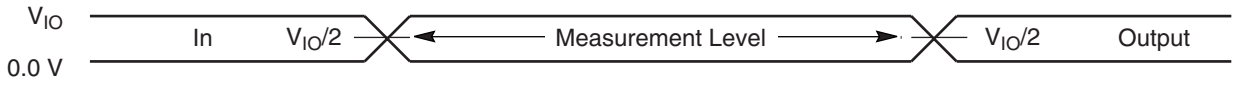


Table 66. Input Waveforms and Measurement Levels

AC Characteristics

V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	1	ms

Notes:

1. *V_{CC} >+ V_{CCQ} - 100mV and VCC ramp rate is >1V/100µs*
2. *VCC ramp rate <1V/100µs, Hardware Reset is required*

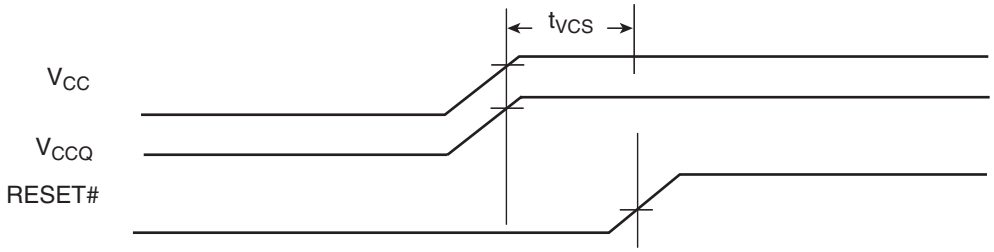


Figure 79. V_{CC} Power-up Diagram CLK Characterization

Parameter	Description		80 MHz	66 MHz	Unit
f_{CLK}	CLK Frequency	Max	80	66	MHz
t_{CLK}	CLK Period	Min	12.5	15.0	ns
t_{CH}	CLK High Time	Min	5	6.1	ns
t_{CL}	CLK Low Time				
t_{CR} (Note)	CLK Rise Time	Max	2.5	3	ns
t_{CF} (Note)	CLK Fall Time				

Note: *Not 100% tested.*

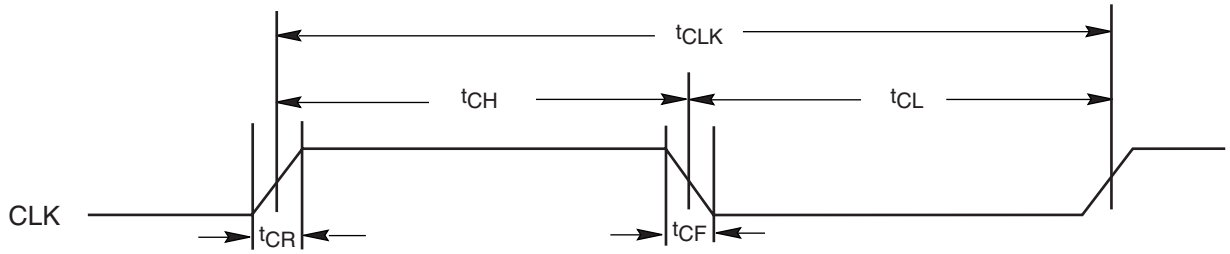


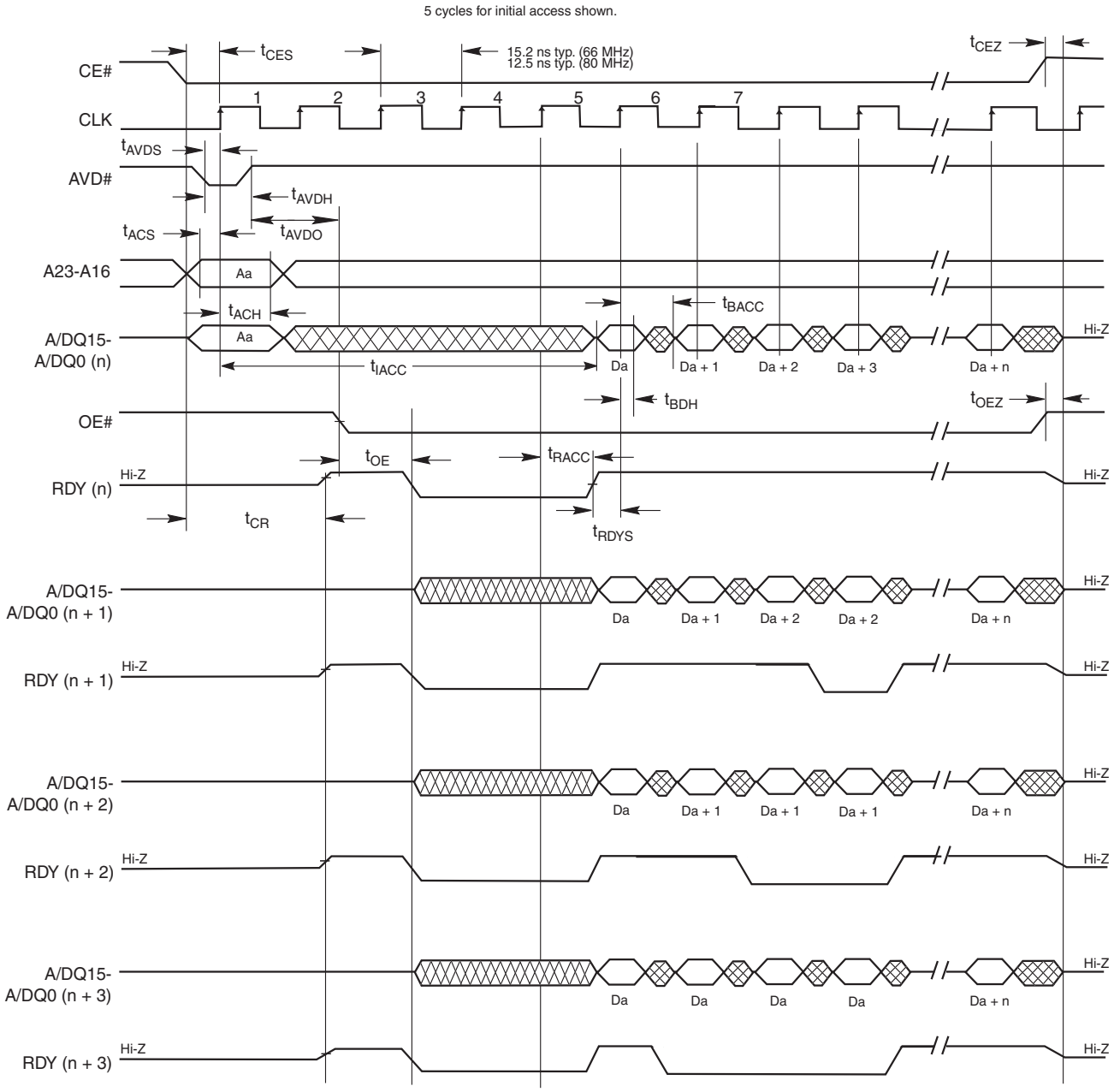
Figure 80. CLK Characterization

AC Characteristics

Synchronous/Burst Read

Parameter		Description		80 MHz	66 MHz	Unit
JEDEC	Standard					
	t_{IACC}	Initial Access Time	Max	80		ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	9	11.0	ns
	t_{AVDS}	AVD# Setup Time to CLK	Min	4	4	ns
	t_{AVDH}	AVD# Hold Time from CLK	Min	6	6	ns
	t_{AVDO}	AVD# High to OE# Low	Min	0		ns
	t_{ACS}	Address Setup Time to CLK	Min	4	4	ns
	t_{ACH}	Address Hold Time from CLK	Min	6	6	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	3	3	ns
	t_{OE}	Output Enable to Data, or RDY Valid	Max	9	11.0	ns
	t_{CEZ}	Chip Enable to High Z (Note)	Max	8	10	ns
	t_{OEZ}	Output Enable to High Z (Note)	Max	8	10	ns
	t_{CES}	CE# Setup Time to CLK	Min	4		ns
	t_{RDYS}	RDY Setup Time to CLK	Min	3.5	4	ns
	t_{RACC}	Ready access time from CLK	Max	9	11.0	ns

Note: *Not 100% tested.*



Notes:

1. *Figure shows total number of clock set to five.*
2. *If any burst address occurs at "address + 1," "address + 2," or "address +3," additional clock delays are inserted, and are indicated by RDY.*

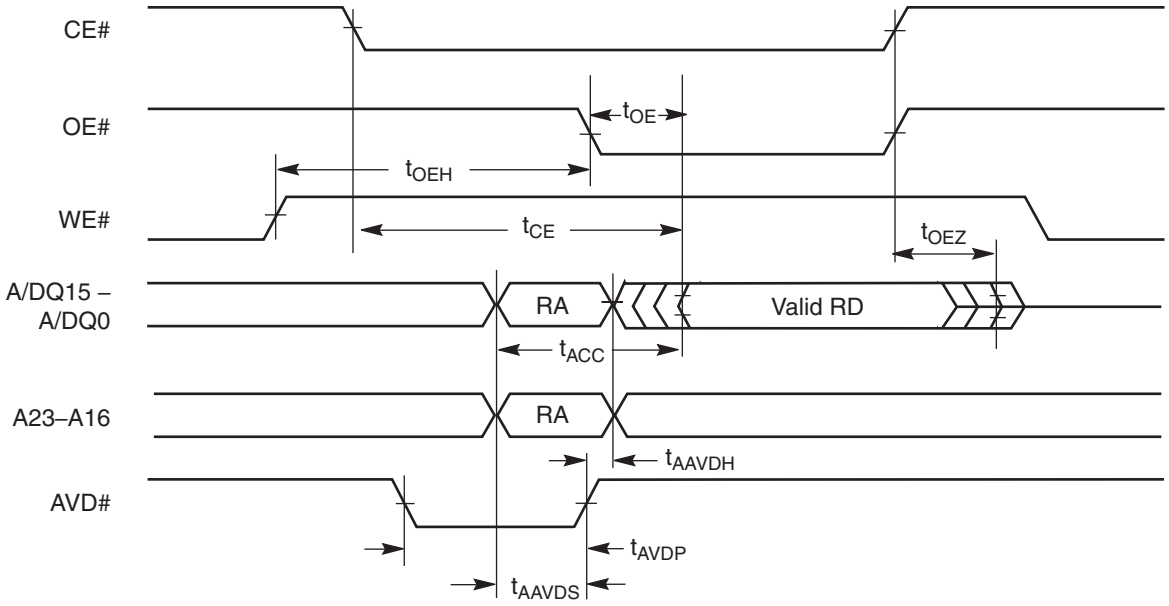
Figure 8I. Burst Mode Read

AC Characteristics

Asynchronous Read

Parameter		Description			80 MHz	66 MHz	Unit
JEDEC	Standard						
	t_{CE}	Access Time from CE# Low		Max	80		ns
	t_{ACC}	Asynchronous Access Time		Max	80		ns
	t_{AVDP}	AVD# Low Time		Min	8		ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	4	4	ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	6	6	ns
	t_{OE}	Output Enable to Output Valid		Max	9	11.0	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	10		ns
	t_{OEZ}	Output Enable to High Z (Note)		Max	10		ns

Note: *Not 100% tested.*



Note: *RA = Read Address, RD = Read Data.*

Figure 82. Asynchronous Mode Read

AC Characteristics

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	
JEDEC	Std				Unit
	t_{RP}	RESET# Pulse Width	Min	200	ns
	t_{RH}	Reset High Time Before Read	Min	10	µs

Note: *Not 100% tested.*

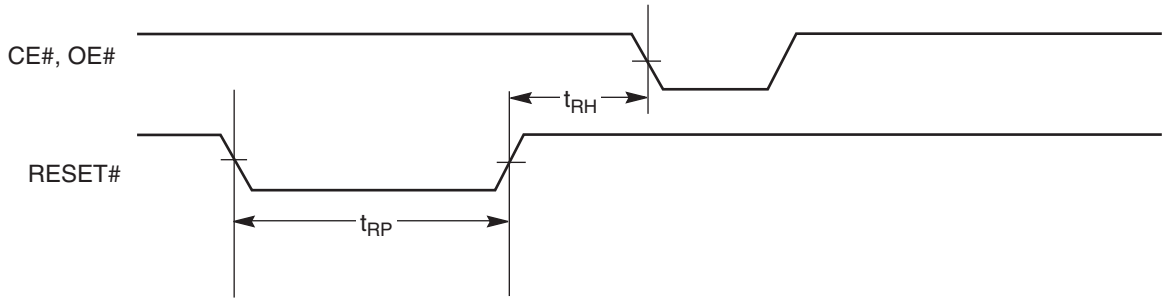


Figure 83. Reset Timings

AC Characteristics

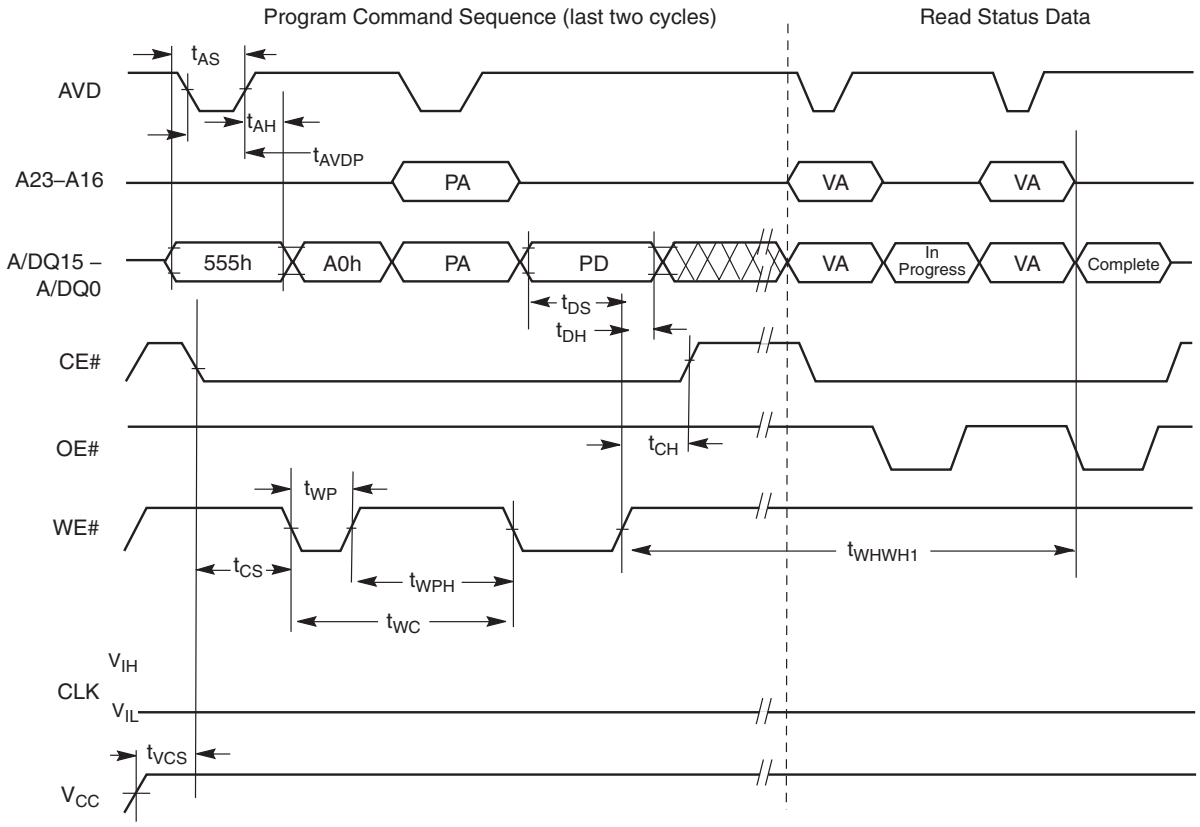
Erase/Program Operations

Parameter		Description		80 MHz	66 MHz	Unit
JEDEC	Standard					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	45	45	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	5		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	9		ns
	t_{AVDP}	AVD# Low Time	Min	8		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	20	25	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write	Typ	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Typ	4	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Typ	0		ns
t_{WLWH}	t_{WP}/t_{WRL}	Write Pulse Width	Typ	30		ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Typ	20		ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0		ns
	t_{VPP}	V_{PP} Rise and Fall Time	Min	500		ns
	t_{VPS}	V_{PP} Setup Time (During Accelerated Programming)	Min	1		µs
	t_{VCS}	V_{CC} Setup Time	Min	50		µs
	t_{SEA}	Sector Erase Accept Time-out	Max	50		µs
	t_{ESL}	Erase Suspend Latency	Max	35		µs
	t_{PSL}	Program Suspend Latency	Max	35		µs
	t_{PSP}	Toggle Time During Programming Within a Protected Sector	Typ	1		µs
	t_{ASP}	Toggle Time During Sector Protection	Typ	100		µs
	t_{WEP}	Noise Pulse Margin on WE#	Max	3		ns

Notes:

1. *Not 100% tested.*
2. *See Erase and Programming Performance for more information.*
3. *Does not include the preprogramming time.*

AC Characteristics

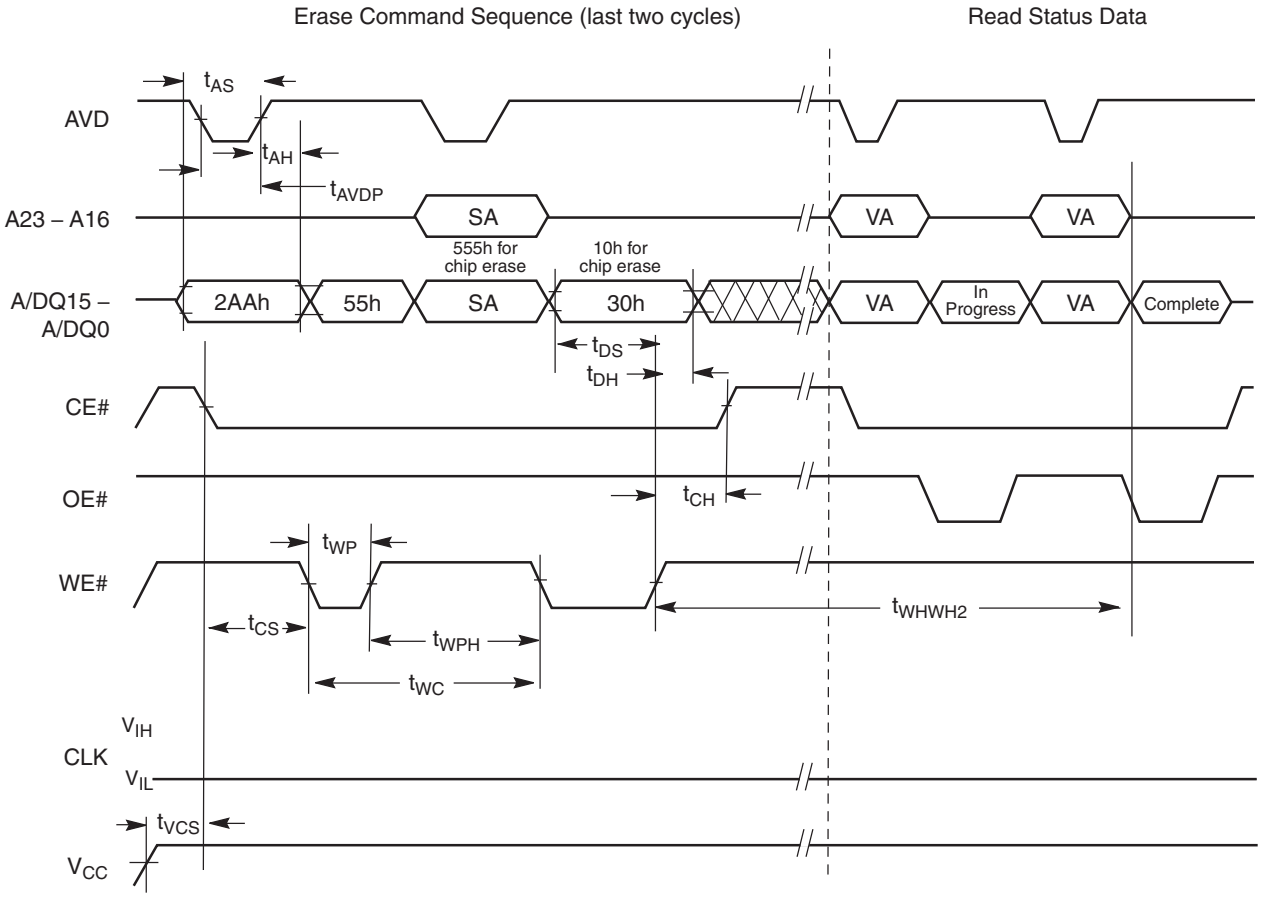


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A23 – A16 are don't care during command sequence unlock cycles.*

Figure 84. Program Operation Timings

AC Characteristics

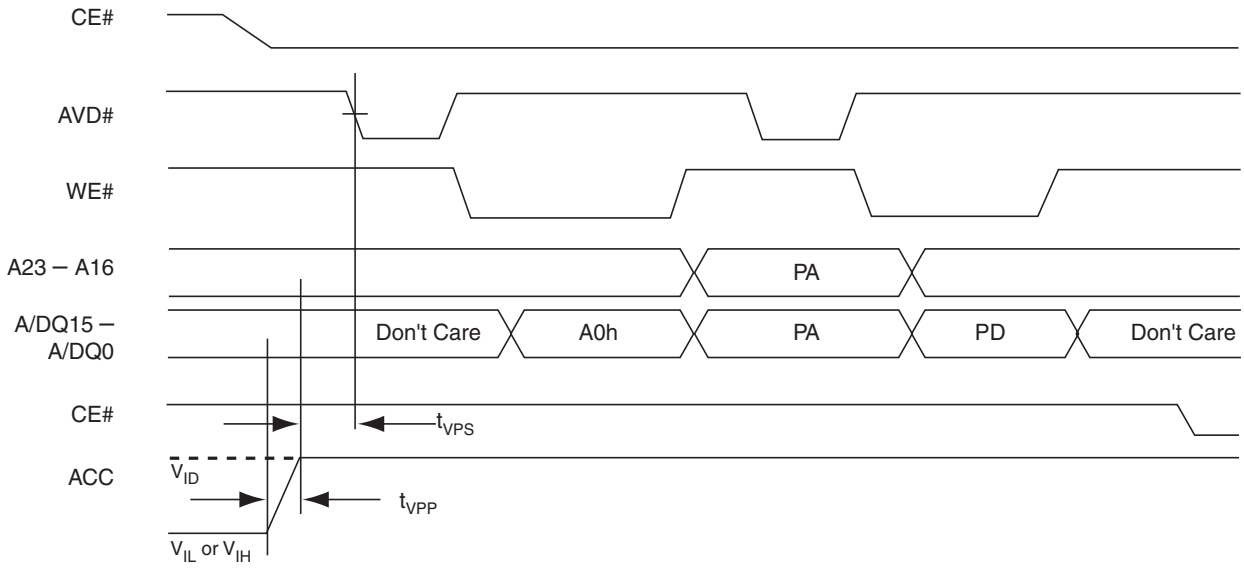


Notes:

1. *SA is the sector address for Sector Erase.*
2. *Address bits A23 – A16 are don't cares during unlock cycles in the command sequence.*

Figure 85. Chip/Sector Erase Operations

AC Characteristics

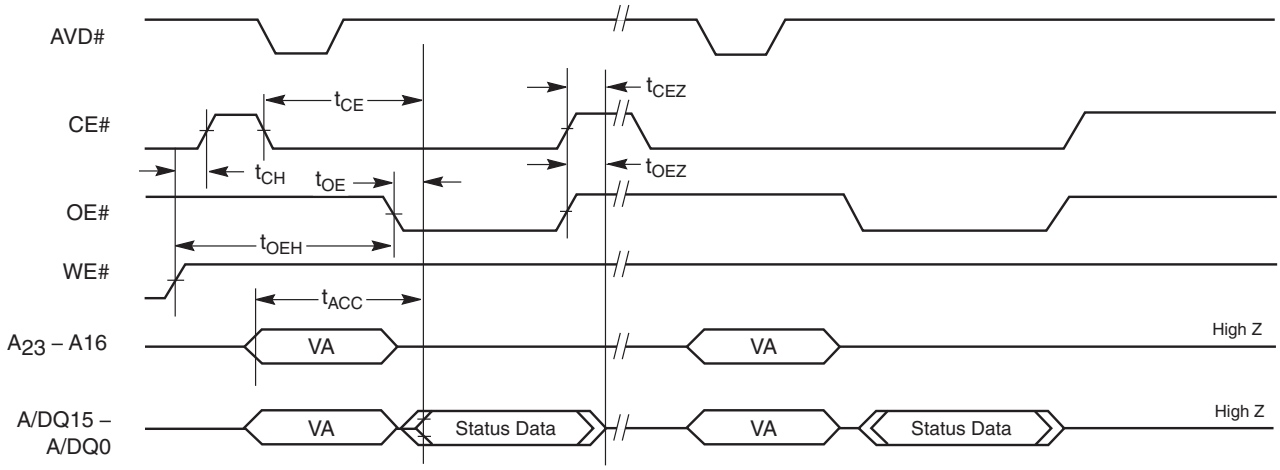


Notes:

1. *V_{PP} can be left high for subsequent programming pulses.*
2. *Use setup and hold times from conventional program operation.*

Figure 86. Accelerated Unlock Bypass Programming Timing

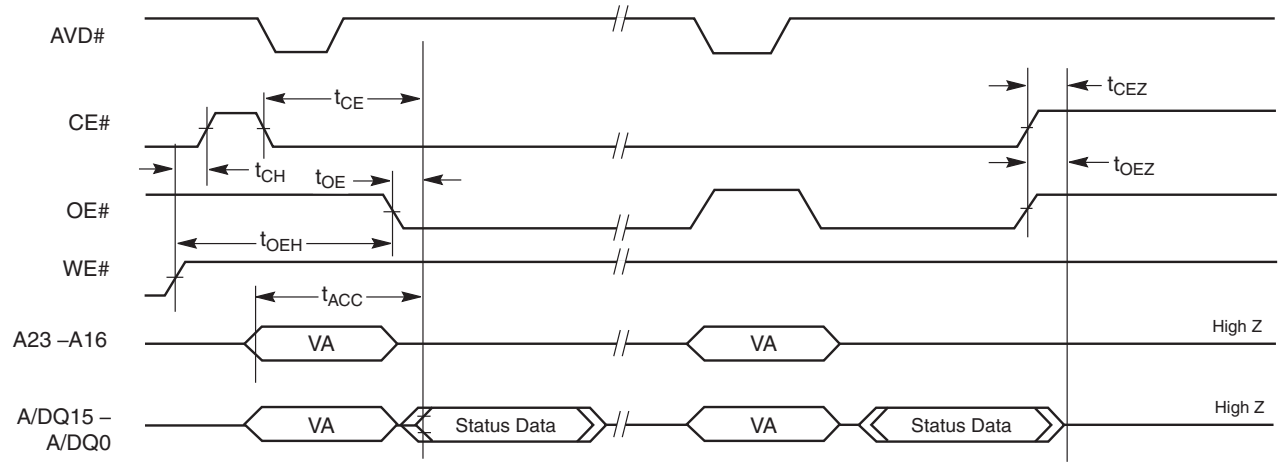
AC Characteristics



Notes:

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling outputs true data.*

Figure 87. Data# Polling Timings (During Embedded Algorithm)

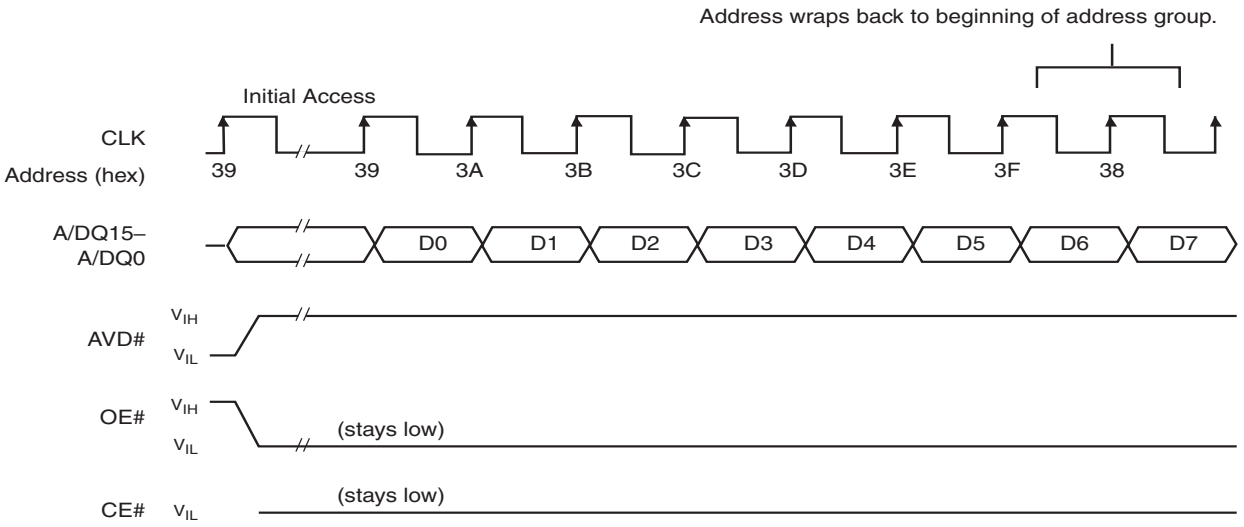


Notes:

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits stop toggling.*

Figure 88. Toggle Bit Timings (During Embedded Algorithm)

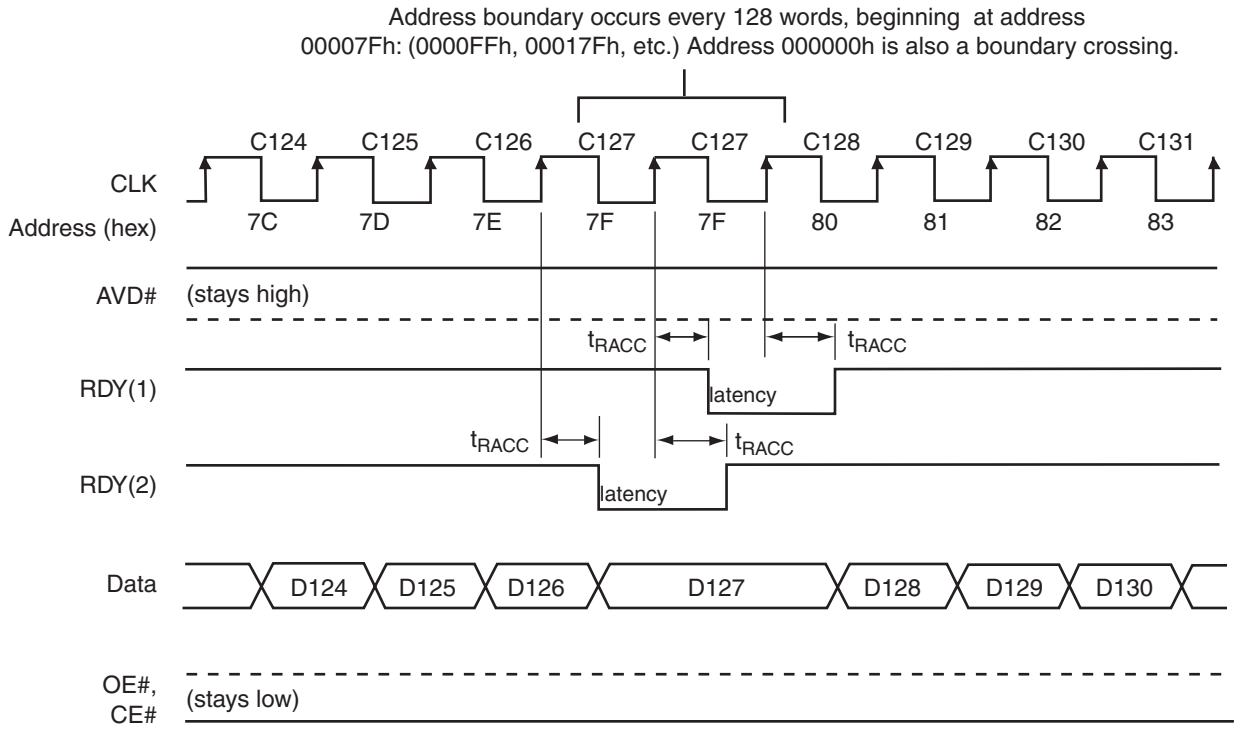
AC Characteristics



Notes:

1. *8-word linear burst mode shown. 16- and 32-word linear burst read modes behave similarly.*
2. *D0 represents the first word of the linear burst.*

Figure 89. 8-, 16-, and 32-Word Linear Burst Address Wrap Around

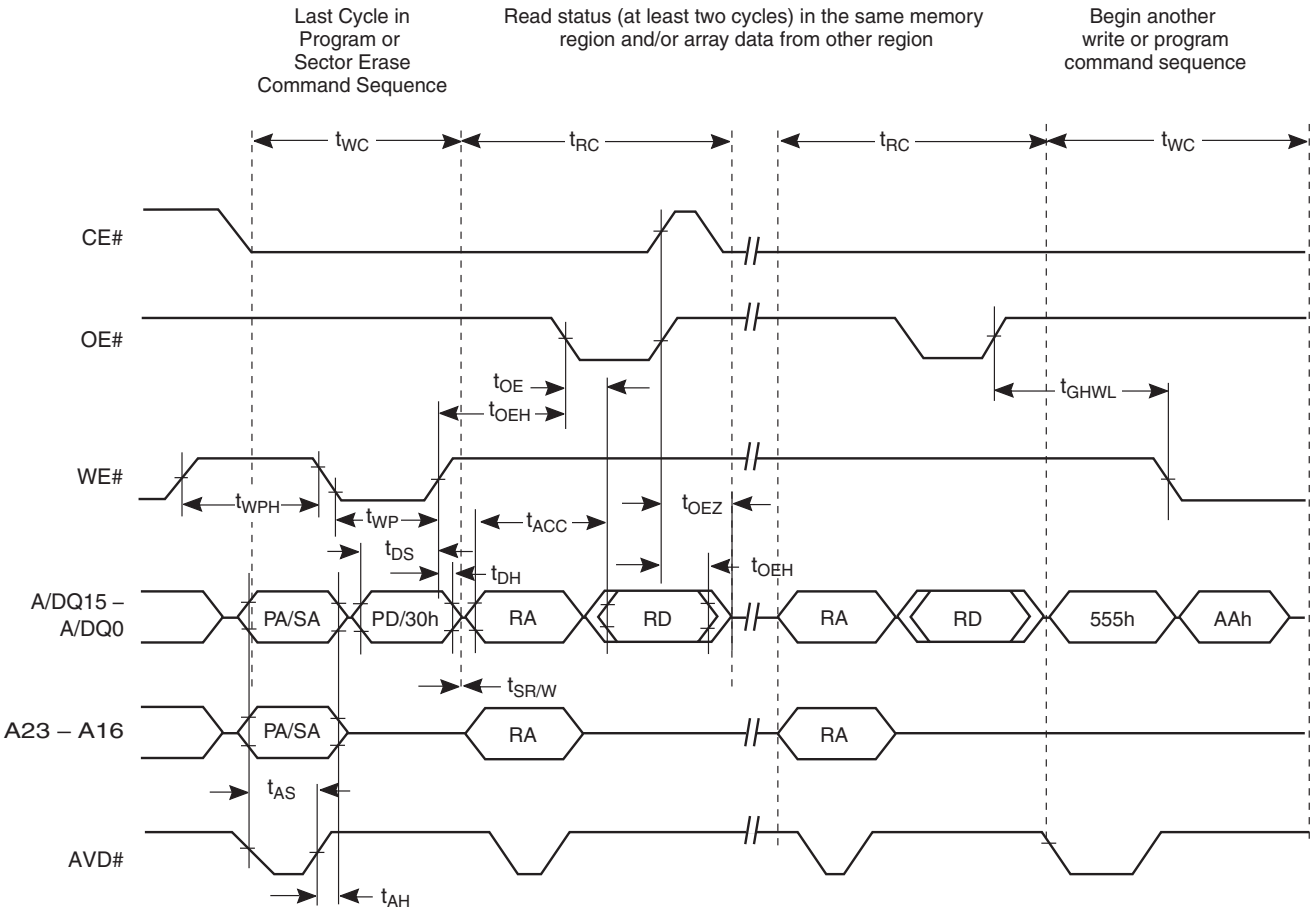


Notes:

1. *Cxx indicates the clock that triggers data Dxx on the outputs; for example, C60 triggers D60.*
2. *At frequencies less than or equal to 66 Mhz, there is no latency.*

Figure 90. Latency with Boundary Crossing

AC Characteristics



Note: *Breakpoints in waveforms indicate the status of the program or erase operation is being checked. The system should read the status twice to ensure valid information.*

Figure 91. Back-to-Back Read/Write Cycle Timings

Erase and Programming Performance

Parameter			Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	64 Kword	V_{CC}	0.8	3.5	s	Excludes 00h programming prior to erasure (Note 5)
	16 Kword	V_{CC}	<0.35	2		
Chip Erase Time		V_{CC}	154	308	s	
		V_{PP}	131	262		
Single Word Programming Time		V_{CC}	40	400	µs	
		V_{PP}	24	240		
Effective Word Programming Tim utilizing Program Write Buffer		V_{CC}	9.4	94	µs	
		V_{PP}	6	60		
Total 32-Word Buffer Programming Time		V_{CC}	300	3000	µs	
		V_{PP}	192	1920		
Chip Programming Time (Note 4)		V_{CC}	157.3	314.6	s	Excludes system level overhead (Note 6)
		V_{PP}	100.7	201.3		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 10,000 cycles typical. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.70 V, 100,000 cycles.*
3. *Effective write buffer specification is based upon a 32-word write buffer operation.*
4. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
5. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
6. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 62 for further information on command definitions.*

Device History

Device	Revision	Extended Code (Hex)	Major Reason(s) for Change
KS256N	ES1	TBD	Initial release.

S99KS-N Revision Summary

Revision A0 (December l4, 2004)

Initial Release. (Publication S99KS256N_00)

Revision Al (April 28, 2005)

Global

Deleted 54 MHz speed option. Changed ACC to V_{PP}. The document publication number has been changed to S99KS256N_M1. The previous revision was S99KS256N_00, Revision A0.

Distinctive Characteristics

High Performance bullet: Changed typical sector erase time for 64 Kword sectors from 600 to 800 ms.

Autoselect Command Sequence

Changed device ID data as follows:

Word	Previous Revision	This Revision
Word 1	2E7E	2D73
Word 2	2E2C	2D2F
Word 3	2E01	2D00

DC Characteristics table

Changed maximum specification on I_{CC3} and I_{CC6} from 40 µA to 70 µA.

Erase and Programming Performance

Changed typical sector erase time for 64 Kword sectors from 600 to 800 ms.

Device History

Added section.

MCP Revision Summary

Revision A0 (December 24, 2004)

Initial release.

Revision AI (May 2, 2005)

Global

Removed 54 MHz options.

Revision A2 (September 23, 2005)

Ordering Information

Updated the Package Type options

Valid Combinations table

Updated to include new Lead (Pb)-free options