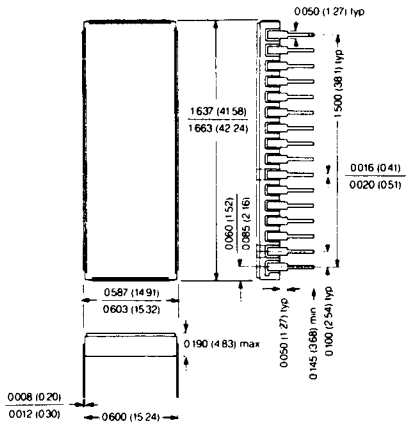
47kHz, 16-bit Self-calibrating Sampling A/D Converter

FEATURES

- **Self-Calibrating A/D Provides True 16-Bit Performance**
- **47kHz Sampling Rate with Inherent T/H Function**
- **16-Bit No-Missing-Codes Guaranteed Over Full Operating Temperature Range**
- **Complete - Contains:**
  - **T/H Function**
  - **Analog Input Buffer**
  - **Reference**
  - **μP Interface**
  - **Full 16-Bit Parallel Output**
  - **Output Bus Driver**
- **±1LSB Integral Linearity**
- **88dB SNR, −98dB Harmonics**
- **785mW Maximum Power Consumption**
- **Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S Model)**
- **MIL-PRF-38534 Screening Optional**

32-PIN SIDE-BRAZED DIP



DESCRIPTION

The MN6450 is a complete 16-bit sampling A/D converter capable of converting analog signals into digital words at a 47kHz rate. Each device contains an inherent sampling function, analog input buffer amplifier, reference, microprocessor interface and a 16-bit-wide parallel data bus driver.

The inherent sampling function associated with the A/D converter's architecture allows changing input signals (up to 12kHz) to be digitized without the need for an external T/H amplifier. Self-calibration accounts for the device's ±0.0015%FSR integral linearity and 16-bit no-missing-code performance. In addition to static performance characteristics, the MN6450 is also specified for dynamic applications with frequency domain specifications including 88dB signal-to-noise ratio and -98dB harmonics.

The MN6450 is packaged in a small 32-pin, hermetically sealed, double-wide, side-brazed DIP package. Designers can select from four electrical grades (J, K, and S) and two operating temperature ranges (0°C to +70°C and −55°C to +125°C). In addition, S models are available environmentally stress screened or fully compliant with MIL-PRF-38534.

APPLICATIONS

Test and Measurement	Weights and Measures
P.C.-Based Data Acquisition	Robotics and Motion Control
Geophysical/Seismic	Fire and Control Systems
Systems ATE	Analyzers

MN6450 47kHz 16-Bit SELF-CALIBRATING SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	–55°C to +125°C
Specified Temperature Range	
MN6450J, K	0°C to +70°C
MN6450S	–55°C to +125°C
Storage Temperature Range	–65°C to 150°C
+15V Supply (+V_{CC}, Pin 17)	0 to +16.5 Volts
–15V Supply (-V_{CC}, Pin 20)	0 to -16.5 Volts
+5V Supply (+V_{DD}, Pin 32)	–0.3 to +6 Volts
Digital Inputs (Pins 18, 19, 25, 26, 27, 28, 29)	–0.3 to +V_{DD} + 0.3V
Analog Inputs: 5V (Pin 22)	±V_{CC}
10V (Pin 21)	±V_{CC}

ORDERING INFORMANTION

PART NUMBER — MN6450S/B CH

Select suffix J, K, or S for desired performance and specified temperature range.

Add "/B" to "S" models for Environmental Stress Screening.

Add "CH" to "S/B" models for 100% screening according to MIL-PRF-38534

DESIGN SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V unless otherwise specified) (Note 10)

ANALOG INPUTS		MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges:	5V Input		0 to +5		Volts
			–5 to +5		Volts
	10V Input		0 to +10		Volts
			–10 to +10		Volts
Input Impedance:	5V Input		5		kΩ
	10V Input		10		kΩ
DIGITAL INPUTS					
Logic Levels:	Logic "1"	+2.0			Volts
	Logic "0"			+0.8	Volts
Logic Currents:	Logic "1" (V_{IH} = +2.4V)			±10	µA
	Logic "0" (V_{IL} = +0.4V)			±10	µA
DIGITAL OUTPUTS					
Logic Levels (Note 12):	Logic "1" (I_{OH} = –6.0mA)	+3.9			Volts
	Logic "0" (I_{OL} = +6.0mA)			+0.26	Volts
Logic Levels (Note 13):	Logic "1" (I_{OH} = 40µA)	+2.4			Volts
	Logic "0" (I_{OL} = 1.6mA)			+0.4	Volts
3-State Leakage Current				±10	µA
INTERNAL REFERENCE					
Reference Output:	Voltage (Note 11)	+4.45	+4.5	+4.55	Volts
	Drift		±3	±10	ppm/°C
POWER SUPPLY REQUIREMENTS					
Power Supply Range:	±V_{CC} Supply	±11.4	±15	±16.5	Volts
	+V_{DD} Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection:	+V_{CC} Supply		±.0001	±.001	%FS/%VS
	–V_{CC} Supply		±.0001	±.001	%FS/%VS
	+V_{DD} Supply		±.0001	±.001	%FS/%VS
Current Drains:	+V_{CC} Supply		+5	+13	mA
	–V_{CC} Supply		–20	–31	mA
	+V_{DD} Supply		+14	+25	mA
Power Consumption			445	785	mW

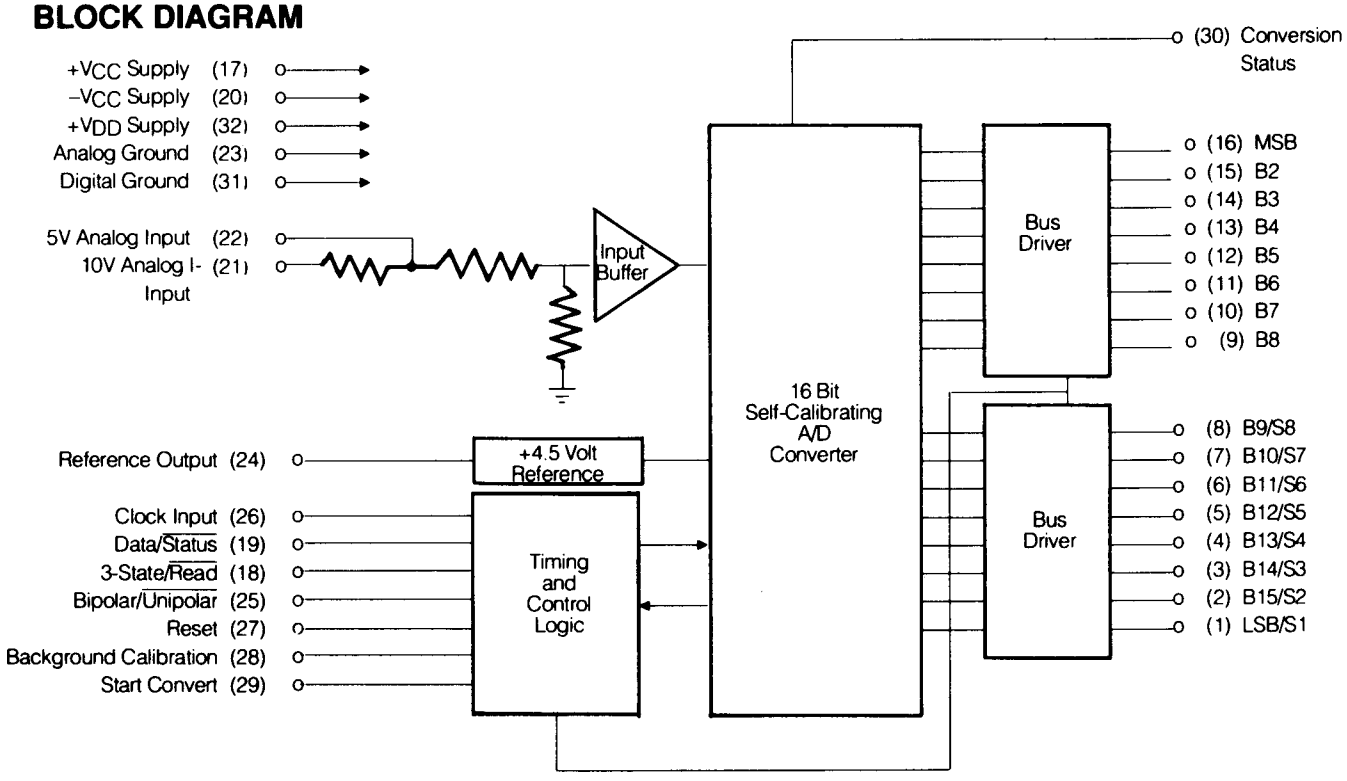
SPECIFICATION NOTES:

1. External Master Clock frequency set to 4MHz and background calibration disabled.
2. Specification listed applies after calibration at any temperature within the specified temperature range.
3. Specification listed applies over the specified temperature range after initial calibration at 25°C.
4. Specification listed applies after calibration at 25°C.
5. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6450 on a unipolar range.
6. Bipolar zero error is defined as the difference between the ideal and actual input voltage at which the digital output changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN6450 on a bipolar range.
7. Full scale absolute accuracy error includes offset, gain linearity, noise and all other errors. Full scale absolute accuracy specifications apply at postive full scale for unipolar input ranges and at both positive and negative full scales for bipolar input ranges. Full scale absolute accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0001 to 0000 0000 0000 0000 transition for bipolar input ranges.
8. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full scale analog input sine wave (0dB) at the specified frequencies.
9. This parameter represents the peak-to-peak non-fundamental component (harmonic or spurious, inband or out-of-band) in the output spectrum.
10. External Master Clock frequency set to 4MHz.
11. Reference output is to be bypassed to Analog Ground with a 10µF capacitor in parallel with an 0.1µF capacitor. Reference must not be used for applications circuits without buffering.
12. For all digital outputs except Conversion Status.
13. Specification for Conversion Status Only.

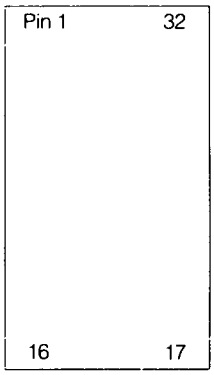
PERFORMANCE SPECIFICATIONS (Typical at +25°C, ±V_{CC}=±15V, +V_{DD}=+5V unless otherwise indicated)(Note 1)

STATIC CHARACTERISTICS	MN6450J	MN6450K	MN6450S	UNITS
Integral Linearity Error (Max) (Note2) Integral Linearity Error (Max) (Note 3)	±0.0015 ±0.0022	±0.0015 ±0.0015	±0.0015 ±0.0022	%FSR %FSR
Minimum Resolution for Which No Missing Codes is Guaranteed (Note 3)	16	16	16	Bits
Unipolar Offset Error (Notes 4, 5) Initial (Maximum) Drift (Maximum)	 ±0.03 ±4	 ±0.02 ±2.5	 ±0.03 ±4	 %FSR ppm of FSR/°C
Bipolar Zero Error (Notes 4, 6) Initial (Maximum) Drift (Maximum)	 ±0.03 ±4	 ±0.02 ±2.5	 ±0.03 ±4	 %FSR ppm of FSR/°C
Full Scale Accuracy Error s (Notes 4, 7) Initial (Maximum) Drift (Maximum)	 ±0.1 ±15	 ±.05 ±10	 ±0.1 ±15	 %FSR ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Minimum Guaranteed Sampling Rate Maximum A/D Conversion Time	47 16.25	47 16.25	47 16.25	kHz µsec
Signal-to-Noise Ratio (Notes 3, 8): Initial (+25°C): 1kHz Full Scale Input 12kHz Full Scale Input T_{min} to T_{max}: 1kHz Full Scale Input 12kHz Full Scale Input	 85 81 83 79	 88 84 85 82	 85 81 83 79	 dB dB dB dB
Harmonics and Spurious Noise (Notes 3,9): Initial (+25°C): 1kHz Full Scale Input 12kHz Full Scale Input T_{min} to T_{max}: 1kHz Full Scale Input 12kHz Full Scale Input	 –96 –90 –94 –88	 –98 –92 –96 –90	 –96 –90 –94 –88	 dB dB dB dB

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Bit 16 (LSB)
2 Bit 15
3 Bit 14
4 Bit 13
5 Bit 12
6 Bit 11
7 Bit 10
8 Bit 9
9 Bit 8
10 Bit 7
11 Bit 6
12 Bit 5
13 Bit 4
14 Bit 3
15 Bit 2
16 Bit 1 (MSB)

32 +5V Supply (+V_{DD})
31 Digital Ground
30 Conversion Status
29 Start Convert
28 Background Calibration
27 Reset
26 Clock Input
25 Bipolar/Unipolar
24 Reference Output
23 Analog Ground
22 5V Analog Input
21 10V Analog Input
20 −15V Supply (−V_{CC})
19 Data/Status
18 3-State/Read
17 +15V Supply (+V_{CC})

APPLICATION INFORMATION

DESCRIPTION OF OPERATION – The MN6450 is a 16-bit, Sampling A/D converter containing an inherent, user-transparent T/H function and features self-calibration and microprocessor interface logic. Self-calibration and the inherent T/H function enable the MN6450 to accurately sample and digitize dynamically changing analog input signals at a 47kHz throughput rate.

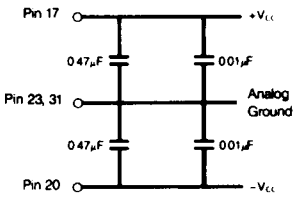
The MN6450 is designed to operate from standard ±12 or ±15V and +5V power supplies and an internal or externally generated Master Clock. After initial power-up, the device must be reset by bringing Reset (pin 27) high for a minimum of 100nsec. Bringing Reset high clears the internal logic circuitry while returning Reset low initiates a full calibration cycle. Full calibration cycles require 1,441,020 Master Clock cycles (360.255msec with an externally applied 4MHz Master Clock). Conversion Status (pin 30) is high during calibration and returns low when calibration is complete.

After calibration, conversions can be initiated by the falling edge of Start Convert (pin 29). The signal applied to Start Convert must remain low for one Master Clock cycle plus 50nsec. This translates to 300nsec with the use of an external 4MHz clock. Start Convert must remain high prior to the end of the conversion cycle (65 clock cycles, 16.25µsec with a 4MHz external clock) to allow sufficient acquisition of the next analog signal to be converted.

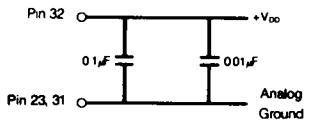
With the conversion complete, digital output data and device status information can be read using various combinations of the digital input control lines. Parallel data is available in a single 16-bit-wide word and is read by bringing 3-State/Read low. Output data lines are returned to the high-impedance state by bringing 3-State/Read high.

POWER SUPPLIES AND LAYOUT – The MN6450 is powered from standard +12/15V (pin 17), −12/15V (pin 20), and +5V (pin 32) supplies. The analog ground (pin 23) and digital ground (pin 31) pins are not connected together internal to the device to minimize analog and digital circuit interaction. The analog ground connection is used as a signal reference point, therefore it should be used as the system analog reference point. Care should be taken to reduce the system noise to a level below the MN6450's high-resolution conversion capability.

It is recommended, for most applications, that the power supplies to the MN6450 be decoupled in the following manner. The +12/15V and −12/15V supplies should be bypassed with a 0.01µF capacitor in parallel with a 0.47µF capacitor to analog ground. The +5V supply, which powers both analog and digital circuits, should be bypassed with a 0.1µF capacitor in parallel with a 0.01µF capacitor to analog ground. System noise characteristics will actually dictate the optimum combination of bypass capacitors.



Power Supply Decoupling



DEVICE CALIBRATION – The MN6450 features two user-controlled self-calibration modes of operation. Self-calibration insures optimum performance at any temperature and at any time throughout the lifetime of the device. Self-calibration also eliminates the need for additional external circuits to maintain operation of the device within specification.

The first mode of calibration is called reset, and its initiation is controlled via the Reset input (pin 27). The device must be reset after the application of power, and can be repeated at the user's option at any time thereafter to compensate for changes in temperature, etc. The required initial reset is initiated by bringing Reset (pin 27) high for a minimum of 100nsec. When Reset is brought high, all internal calibration logic is cleared. When reset is returned low, a single full calibration cycle lasting 1,441,020 master clock cycles begins (360.225msec with a 4MHz external master clock applied). During reset, the Conversion Status

output (pin 30) will be in a high state, and will fall low upon the completion of the calibration cycle.

The reset mode of calibration can be initiated either by hardware using a power-up reset circuit or by software in microprocessor controlled applications.

In the second mode of operation, calibration can be interleaved with the conversion process. In this mode of calibration the conversion cycle is extended by 20 master clock cycles to accommodate a portion of the calibration process. This mode of calibration is called Background Calibration and is initiated by bringing Background Calibration (pin 28) and 3-State/Read (pin 18) both low. This mode differs from Reset in that a fraction of the calibration process is accomplished at the end of each conversion. After 72,051 conversions, the calibration cycle is complete. Except for the increase in conversion time (and a proportionate decrease in throughput), the background calibration mode is transparent to the user.

MASTER CLOCK – The MN6450 operates from a master clock that can be supplied externally or generated internally depending upon the signal applied to Clock Input (pin 26). A logic low on this pin will activate the 2MHz minimum internal clock. Optionally, the user can supply a TTL or CMOS system clock with a maximum frequency of 4MHz (100kHz minimum) to the clock input. All device timing characteristics scale to the master clock frequency. The internal oscillator exhibits relatively high jitter when compared to crystal oscillators, which may have an adverse affect on performance in some sampling applications.

INITIATING CONVERSIONS – A falling edge on the start convert input will set the device into the hold mode and initiate a conversion cycle. The start convert signal must remain low for a minimum of one master clock cycle plus 50nsec (300nsec total for applications using an applied 4MHz external clock). It must return high before the minimum conversion time of 65 clock cycles (16.25µsec with an applied 4MHz external clock) to allow for sufficient time to acquire the next sample to be digitized.

T/H ACQUISITION – The MN6450 is a sampling A/D converter, therefore it requires a finite amount of time to accurately acquire an analog input signal before performing an A/D conversion. At the end of a conversion cycle, signalled by the falling of Conversion Status (pin 30), the device automatically enters the acquisition mode and begins to track the analog input signal. A minimum of six master clock cycles plus 2.25µsec (3.75µsec with an applied 4MHz external clock) is required to acquire the input signal. When driving the MN6450 from a high impedance, it may be necessary to extend the amount of time allowed for the increase in the input settling time constant.

The MN6450's acquisition circuitry operates from a delayed and divided down internal clock frequency of 1/4 times the Master Clock. If sampling is not synchronized to this internal clock, a sample will be synchronously taken but may not be converted until up to four master clock cycles later (1µsec with an applied 4MHz Master Clock). In other words, when Start Convert is brought low asynchronously with respect to the generated internal master clock a maximum of four clock cycles could pass before Conversion Status returns high and the conversion begins. This asynchronous uncertainty in effect adds these four master clock cycles plus 235nsec of internal clock delay (1.235µsec with applied 4MHz Master Clock) to the conversion time.

When operating the MN6450 in an asynchronous application, the conversion cycle will require 69 master clock cycles plus 235nsec while signal acquisition requires six master clock cycles plus 2.25µsec for a total of 75 master clock cycles plus 2.485µsec (21.325µsec with applied 4MHz Master Clock). This corresponds to a maximum throughput rate of 47.1kHz. Although the sample is converted asynchronously, it is important to note for DSP applications that the sample itself was taken synchronously with the falling edge of Start Convert.

ANALOG INPUTS – The MN6450 can be operated in four user-selectable input voltage range configurations. They are 0 to +5V, ±5V, 0 to +10V and ±10V. The 5V analog input (pin 22) is used for 5V full scale analog inputs (0 to +5V and ±5V) while the 10V input (pin 21) is used for 10V full scale inputs (0 to 10V and ±10V). Selection of either bipolar or unipolar operation is controlled via digital input control line Bipolar/Unipolar (pin 25). A logic "1" on this pin selects a bipolar transfer function while a logic "0" applied to this pin selects a unipolar transfer function.

The unipolar ranges are digitally represented at the digital outputs in Straight Binary format. An all 0's output correspond to 0V applied at the input to the device. Likewise, an all 1's output corresponds to +FS applied to the device input. Bipolar ranges are digitally represented at the digital outputs in Offset Binary format. All 0's at the digital output corresponds to an analog input of –FS while all 1's at the digital output corresponds to +FS.

The MN6450 contains an analog input buffer amplifier configured to condition the analog input signal for optimum acquisition and conversion performance. Additional signal conditioning circuitry meeting 16-bit performance levels can be used to drive the analog input to the device.

REFERENCE OUTPUT – The MN6450 contains an internal +4.5V precision low-drift reference. This reference voltage appears at Reference Output (pin 24) to allow for the attachment of a 0.1µf capacitor in parallel with a 10µF tantalum capacitor. These capacitors are required to allow the reference to exhibit a low output impedance throughout the frequency range of device operation. The optimum value for these capacitors will vary depending on the Master Clock frequency being used.

It is recommended to not use the Reference Output to drive any additional circuit requirements. If absolutely necessary, the Reference Output can be buffered and used to fulfill additional circuit requirements.

DIGITAL OUTPUTS – The MN6450 supplies converted parallel output data in a 16-bit-wide format. Output data is read by bringing digital input 3-State/Read (pin 18) low after a conversion is complete. Data outputs are returned to the high-impedance state when 3-State/Read is returned high.

In addition to digital output data, device status information can be read via the parallel data output bits. The information present on the the 16-bit output bus is controlled via the Data/Status control line (pin 19). When high (logic 1), converted data is presented on digital output lines.

When low (logic 0), the Status Register can be read on bit 16 through bit 9 (pins 1-8). Output bit 1 through bit 8 remain in a high impedance state (pins 9-16). Status bit pin locations appear in the table labled Parallel Output Pin Description.

PARALLEL OUTPUT PIN DESCRIPTION

PIN #	DATA OUTPUT	STATUS BIT	STATUS INFORMATION
1	LSB	S1	Same as Conversion Status (pin 30).
2	Bit 15	S2	Reserved for factory use.
3	Bit 14	S3	Reserved for factory use.
4	Bit 13	S4	Acquisition Status – when low, indicates that sufficient time has been allowed for input signal acquisition.
5	Bit 12	S5	Reserved for factory use.
6	Bit 11	S6	Tracking—high when device is tracking analog input.
7	Bit 10	S7	Converting–high when device is converting analog input.
8	Bit 9	S8	Calibrating –high when device is calibrating.
9	Bit 8	Hi-Z	
10	Bit 7	Hi-Z	
11	Bit 6	Hi-Z	
12	Bit 5	Hi-Z	
13	Bit 4	Hi-Z	
14	Bit 3	Hi-Z	
15	Bit 2	Hi-Z	
16	MSB	Hi-Z	

PIN DESCRIPTION

POWER SUPPLY CONNECTIONS

Pin Designation	Function
+15V/+12V Supply ($+V_{CC}$, Pin 17)	Positive analog power supply. Devices will operate from nominal +12V or +15V supplies.
–15V/–12V Supply ($-V_{CC}$, Pin 20)	Negative analog power supply. Devices will operate from nominal –12V or –15V supplies.
+5V Supply ($+V_{DD}$, Pin 32)	Positive digital and analog power supply. Device operates from nominal +5V.

ANALOG INPUTS

Pin Designation	Function
10V Analog Input (Pin 21)	When in the Unipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "0"), accepts 0 to +10V analog input signals. When in Bipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "1"), accepts ±10V analog input signals.
5V Analog Input (Pin 22)	When in the Unipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "0"), accepts 0 to +5V analog input signals. When in the Bipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "1"), accepts ±5V analog input signals.

ANALOG OUTPUTS

Pin Designation	Function
Reference Output (Pin 24)	Provides reference voltage of +4.5V to be bypassed to Analog Ground with an external 10µF tantalum capacitor in parallel with an 0.1µF ceramic disk capacitor. Use of this reference in additional circuit applications requires the use of an external, low-input current buffer amplifier.

DIGITAL OUTPUTS

Pin Designation	Function
Parallel Data Outputs (Pins 1-16)	Output data is presented in a 16-bit parallel format and is 3-State controlled via the 3-State/$\overline{\text{Read}}$ input. In addition to output data, the device's status register may be read back on pin 1 through pin 8. Data Output is controlled by 3-State/$\overline{\text{Read}}$ and is dependent on Data/$\overline{\text{Status}}$.
Conversion Status (Pin 30)	Indicates A/D Converter status. When high (Logic "1"), the A/D is busy in a conversion or calibration cycle. Returns high on first read cycle or the beginning of new conversion cycle.

DIGITAL INPUTS

Pin Designation	Function
Clock Input (Pin 26)	Connect external Master Clock signal (TTL or CMOS level @ 4MHz maximum) or tie to digital ground to activate the internal clock.
Data/$\overline{\text{Status}}$ (Pin 19)	Selects the type of information presented to digital output pins 1-8 during the read operation. When high (Logic "1"), converted output data is presented to parallel output pins 1-16, when low (Logic "0"), status register is presented to digital outputs (Pins 1-8).
3-State/$\overline{\text{Read}}$ (Pin 18)	Selects state of digital data output pins 1-16. When high (Logic "1"), data is disabled and parallel output bits are in high-impedance state. When low (Logic "0"), converted data (Data/Status pin 19=Logic "1") or status information (Data/Status, pin19=Logic "0") is presented to output pins 1-8. Converted output data is presented in one 16-bit word. Additionally, falling edges latch the state of Background Calibration.

Pin Designation	Function
Bipolar/$\overline{\text{Unipolar}}$ (Pin 25)	Selects either unipolar or bipolar operation. When high (Logic "1"), the analog input range is bipolar (–Full Scale to + Full Scale). When low (Logic "0"), the analog input range is unipolar (0V to +Full Scale). The analog input voltage pins selects the desired full scale range.
Reset (Pin 27)	Controls the device clear and calibration cycle initiation. When brought high, the internal logic is cleared. When returned low (after being high for 100nsec minimum) a full device calibration cycle is initiated.
Background Calibration (Pin 28)	Controls the device active calibration mode. When latched low by the falling edge of 3-State/$\overline{\text{Read}}$, the device interleaves conversions and calibration cycles. Full calibration cycle extends over 72,051 conversions at the expense of extended conversion time.
Start Convert (Pin 29)	The falling edge of Start Convert initiates the conversion cycle. Start Convert must remain low for at least one Master Clock cycle plus 50nsec.

DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGES	MSB LSB
+F.S.	+F.S.	1111 1111 1111 1111
+F.S.–3/2LSB	+F.S.–3/2LSB	1111 1111 1111 111Ø*
+1/2F.S.+1/2LSB	+1/2LSB	1000 0000 0000 000Ø*
+1/2F.S.–1/2LSB	–1/2LSB	ØØØØ ØØØØ ØØØØ ØØØØ*
+1/2F.S.–3/2LSB	–3/2LSB	0111 1111 1111 111Ø*
+1/2LSB	–F.S.+1/2LSB	0000 0000 0000 000Ø*
0	–F.S.	0000 0000 0000 0000

CODING NOTES:

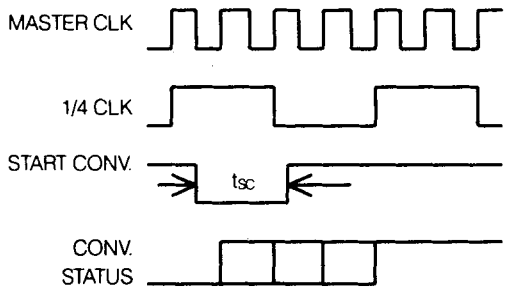
1. For 5 Volt FSR, 1LSB for 16 Bits =76.3µV.
2. For 10 Volt FSR, 1LSB for 16 Bits =152.6µV.
3. For 20 Volt FSR, 1LSB for 16 Bits =305.6µV.
4. For unipolar ranges, the coding is straight binary.
5. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transition indicated. Ideally, with the MN6450 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

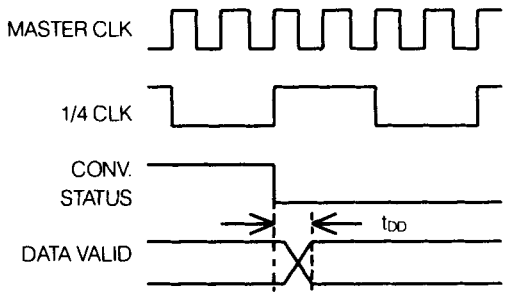
INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE			
	0 to +5V	0 to +10V	±5V	±10V
Connect Pin 22 to	Analog Input	Open	Analog Input	Open
Connect Pin 21 to	Open	Analog Input	Open	Analog Input
Connect Pin 25 to Logic	"0"	"0"	"1"	"1"

INITIATING A CONVERSION:



END OF CONVERSION:



NOTES:

1. 1/4 CLK is shown for reference only. It is generated internally by the device and is used to synchronize all other signals. It is not available as an output.
2. The uncertainty at the rising edge of CONVERSION STATUS is due to the unknown phase relation between START CONV. and 1/4 CLK. CONVERSION STATUS will go high on the first rising edge of 1/4 CLK which occurs after START CONVERT has been recognized as a low. This delay is a maximum of 4 MASTER CLK cycles.
3. The width of CONVERSION STATUS="1" will always be a maximum of 65 MASTER CLK cycles plus 235 nsec regardless of the uncertainty at the rising edge.
4. Although CONVERSION STATUS may not go high for up to 4 MASTER CLK cycles after START CONVERT goes low, the analog input will be held at the value present when START CONVERT goes low.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}, $\pm V_{CC}$, = ± 15V, $+V_{DD}$ = +5V, CL=50pF)

PARAMETER	MIN	TYP	MAX	UNITS
Master Clock Frequency (f_{CLK}) Internal External	 2 0.1		 4	 MHz MHz
Start Convert Pulse Width (t_{SC})	$1/f_{CLK}$ +0.05		t_C	µsec
Conversion Time	$65/f_{CLK}$		$69/f_{CLK}$ +0.235	µsec
Acquisition Time			$6/f_{CLK}$ +2.25	µsec
Throughput Time Asynchronous Sampling			$75/f_{CLK}$ +2.485	µsec
Set Up Times Background Calibration, Data/$\overline{\text{Status}}$ to 3-State/$\overline{\text{Read}}$ Low	20	10		nsec
Hold Times 3-State/Read High to Background Calibration, Data/$\overline{\text{Status}}$ Invalid	50	30		nsec
Data Delay Time (t_{DD})		40	100	nsec
Data Access Time 3-State/$\overline{\text{Read}}$ Low to Data Valid		80	150	nsec
Output Float Delay 3-State/$\overline{\text{Read}}$ High to Output High Z		80	150	nsec