AH215 / ECP100G

1 Watt, High Gain HBT Amplifier *Product Information*

Product Features

- 400 – 2300 MHz
- +31.5 dBm P1dB
- +46 dBm Output IP3
- 18 dB Gain @ 900 MHz
- Single Positive Supply (+5 V)
- Lead-free/green/RoHS-compliant SOIC-8 SMT Pkg.

Applications

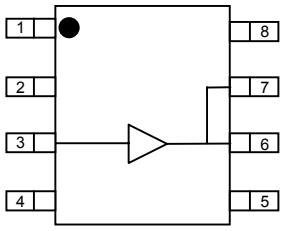
- Final stage amplifiers for Repeaters
- Mobile Infrastructure
- Defense / Homeland Security

Product Description

The AH215 / ECP100 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve superior performance for various narrowband-tuned application circuits with up to +46 dBm OIP3 and +31.5 dBm of compressed 1-dB power. The part is housed in a lead-free/green/RoHS-compliant SOIC-8 package. All devices are 100% RF and DC tested.

The product is targeted for use as driver amplifier for various current and next generation wireless technologies such as GPRS, GSM, CDMA, W-CDMA, and UMTS, where high linearity and high power is required. The internal active bias allows the AH215 / ECP100 to maintain high linearity over temperature and operate directly off a +5 V supply.

Functional Diagram



Function	Pin No.
Vref	1
Input	3
Output	6, 7
Vbias	8
GND	Backside Paddle
N/C or GND	2, 4, 5

Specifications (1)

Parameters	Units	Min	Typ	Max
Operational Bandwidth	MHz	400		2300
Test Frequency	MHz		2140	
Gain	dB	10	11	
Input Return Loss	dB		18	
Output Return Loss	dB		8	
Output P1dB	dBm	+29	+31.5	
Output IP3 (2)	dBm	+43.8	+45	
Noise Figure	dB		6.3	
IS-95 Channel Power @ -45 dBc ACPR, 1960MHz	dBm		+25.5	
W-CDMA Channel Power @ -45 dBc ACPR, 2140 MHz	dBm		+23	
Operating Current Range , Icc (3)	mA	400	450	500
Device Voltage, Vcc	V		5	

1. Test conditions unless otherwise noted: 25ºC, +5V Vsupply, 2140 MHz, in tuned application circuit.
2. 3OIP measured with two tones at an output power of +15 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
3. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8. It is expected that the current can increase by an additional 90 mA at P1dB. Pin 1 is used as a reference voltage for the internal biasing circuitry. It is expected that Pin 1 will pull 10.8 mA of current when used with a series bias resistor of R1=51 Ω. (ie. total device current typically will be 461 mA.)

Typical Performance (4)

Parameters	Units	Typical		
Frequency	MHz	900	1960	2140
S21 – Gain	dB	18	12	11
S11	dB	-13	-11	-18
S22	dB	-7	-10	-8
Output P1dB	dBm	+31	+32	+31.5
Output IP3	dBm	+46	+46	+45
IS-95A Channel Power @ -45 dBc ACPR	dBm	+25.5	+25.5	
W-CDMA Channel Power @ -45 dBc ACPR	dBm			+23
Noise Figure	dB	7.0	5.5	6.2
Supply Bias		+5 V @ 450 mA		

4. Typical parameters reflect performance in a tuned application circuit at +25° C.

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-65 to +150 °C
RF Input Power (continuous)	+26 dBm
Device Voltage	+8 V
Device Current	900 mA
Device Power	5 W
Junction Temperature	+250 °C

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

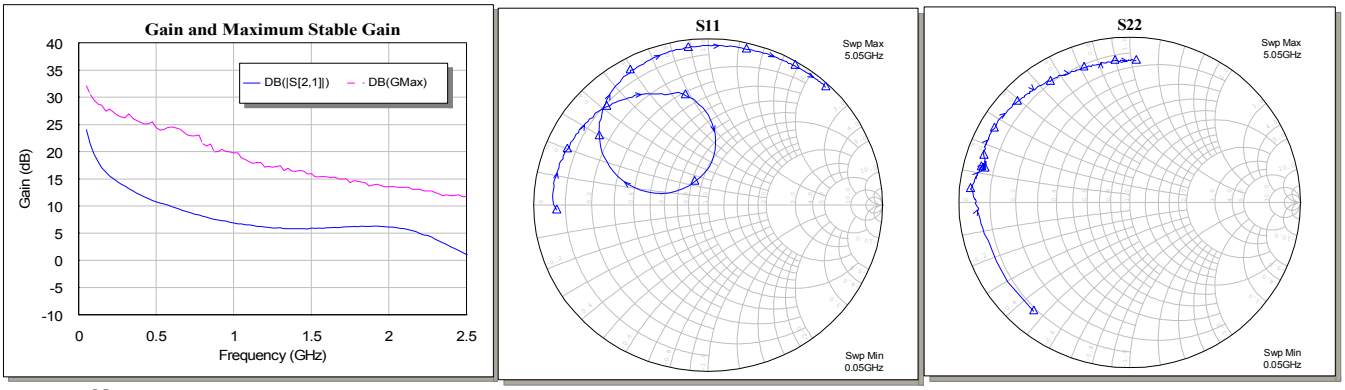
Part No.	Description
AH215-S8*	1 Watt, High Linearity InGaP HBT Amplifier (lead-tin SOIC-8 Pkg)
ECP100G*	1 Watt, High Linearity InGaP HBT Amplifier (lead-tin SOIC-8 Pkg)
AH215-S8G	1 Watt, High Linearity InGaP HBT Amplifier (lead-free/green/RoHS-compliant SOIC-8 Pkg)
AH215-S8PCB900	900 MHz Evaluation Board
AH215-S8PCB1960	1960 MHz Evaluation Board
AH215-S8PCB2140	2140 MHz Evaluation Board

* This package is being phased out in favor of the green package type which is backwards compatible for existing designs. Refer to Product Change Notification WJPCN06MAY05TC1 on the WJ website.

Specifications and information are subject to change without notice.

Typical Device Data

S-Parameters (V_{cc} = +5 V, I_{cc} = 450 mA, T = 25°C, calibrated to device leads)

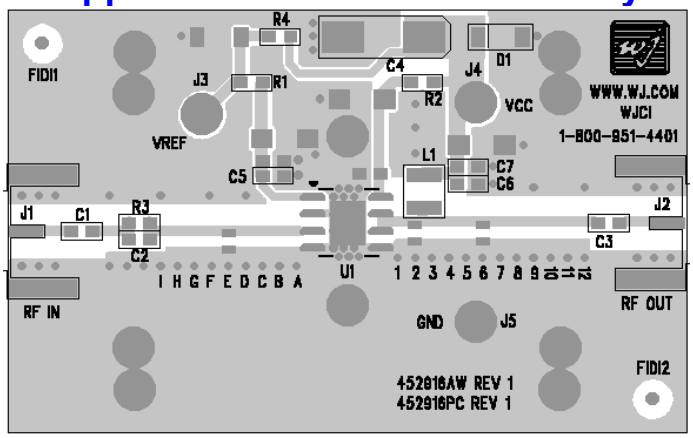


Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line. The impedance loss plots are shown from 0.05 – 5.05 GHz, with markers placed in 0.5 GHz increments.

S-Parameters (V_{cc} = +5 V, I_{cc} = 450 mA, T = 25°C, unmatched 50 ohm system, calibrated to device leads)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-1.23	-177.95	24.07	122.55	-40.25	17.32	-1.26	-130.4
100	-1.01	178.17	19.55	116.55	-39.49	10.63	-1.33	-155.43
200	-1.01	172.63	15.55	112.97	-40.13	15.98	-1.17	-169.92
400	-1.03	163.72	12.03	98.68	-38.83	10.31	-0.93	179.61
600	-1.21	155.20	9.86	85.80	-39.30	-4.249	-0.66	173.43
800	-1.34	146.17	8.11	73.18	-37.70	-2.398	-0.83	168.67
1000	-1.52	136.69	6.92	61.43	-37.73	-16.27	-0.95	166.34
1200	-2.00	126.65	6.13	49.60	-37.14	-14.34	-1.05	165.13
1400	-2.65	115.04	5.80	37.55	-36.23	-28.50	-1.04	164.55
1600	-3.86	97.52	6.01	21.48	-36.45	-46.08	-1.11	166.24
1800	-6.72	86.05	6.17	1.700	-34.63	-68.99	-1.10	164.44
2000	-14.09	94.99	6.15	-23.83	-35.91	-100.68	-1.00	162.35
2200	-9.98	166.89	4.98	-52.92	-36.75	-147.66	-0.77	158.42
2400	-4.27	157.68	2.52	-80.08	-39.10	171.86	-0.79	154.12
2600	-2.13	142.95	-0.42	-100.8	-37.80	123.26	-0.81	149.03
2800	-1.24	130.88	-3.40	-116.44	-38.58	89.55	-0.84	144.09
3000	-0.82	120.68	-6.09	-128.99	-39.37	67.22	-0.92	138.4

Application Circuit PC Board Layout



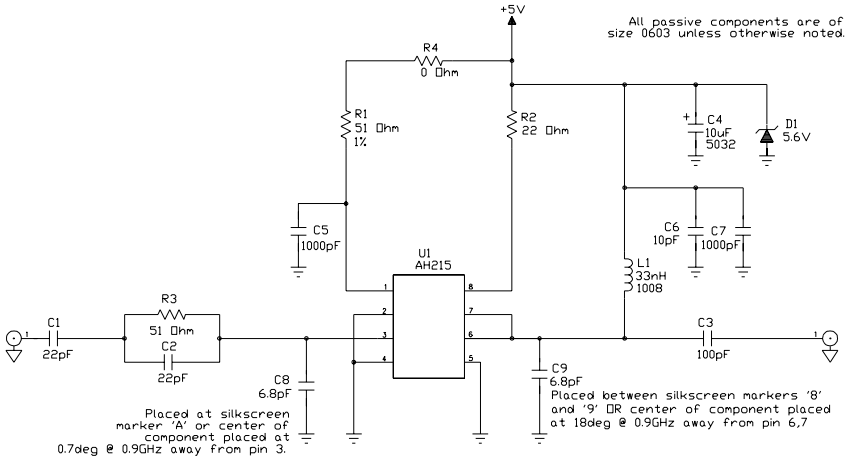
Circuit Board Material: Top RF layer is .014" Getek, 4 total layers (0.062" thick) for mechanical rigidity
1 oz copper, Microstrip line details: width = .026", spacing = .026"
The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050" increments.

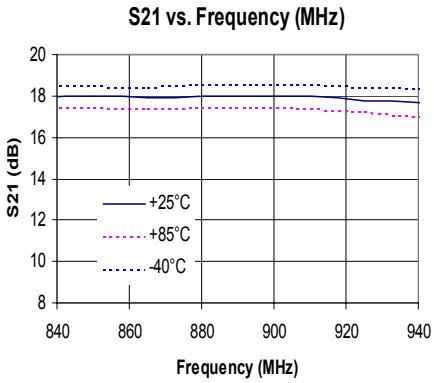
900 MHz Application Circuit (AH215-S8PCB900)

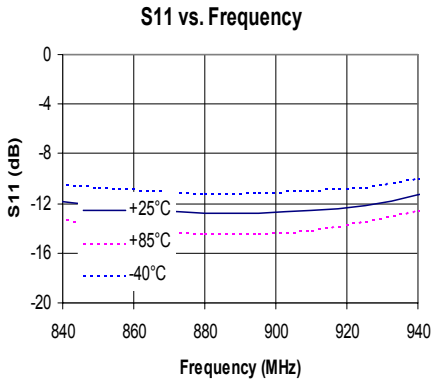
Typical RF Performance at 25°C

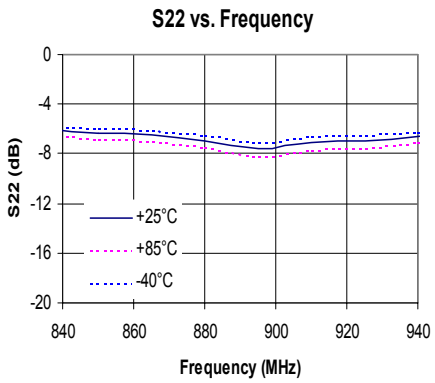
Frequency	900 MHz
S21 – Gain	18 dB
S11 – Input Return Loss	-13 dB
S22 – Output Return Loss	-7.0 dB
Output P1dB	+31 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+46 dBm
Channel Power (@-45 dBc ACPR, IS-95 9 channels fwd)	+25.5 dBm
Noise Figure	7.0 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

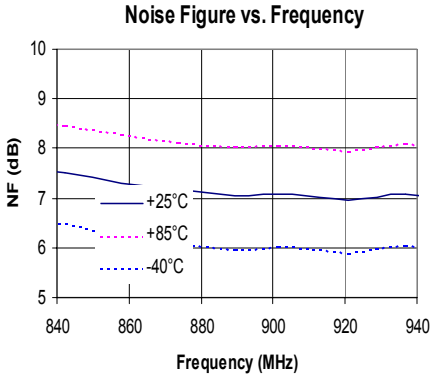
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8.

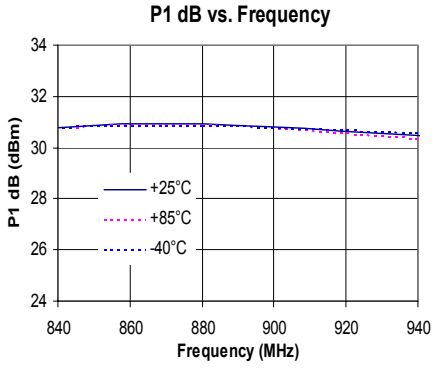


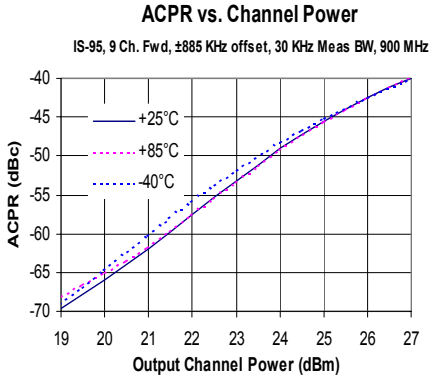


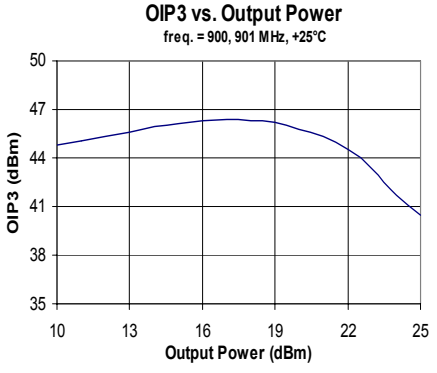


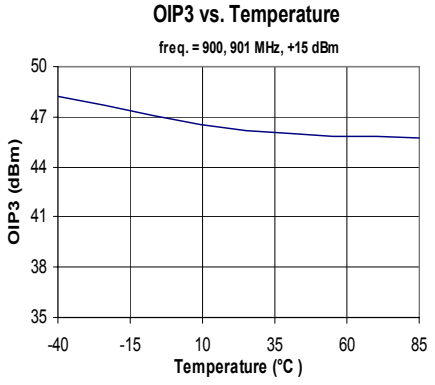


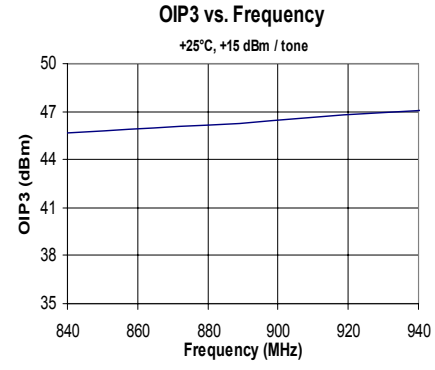












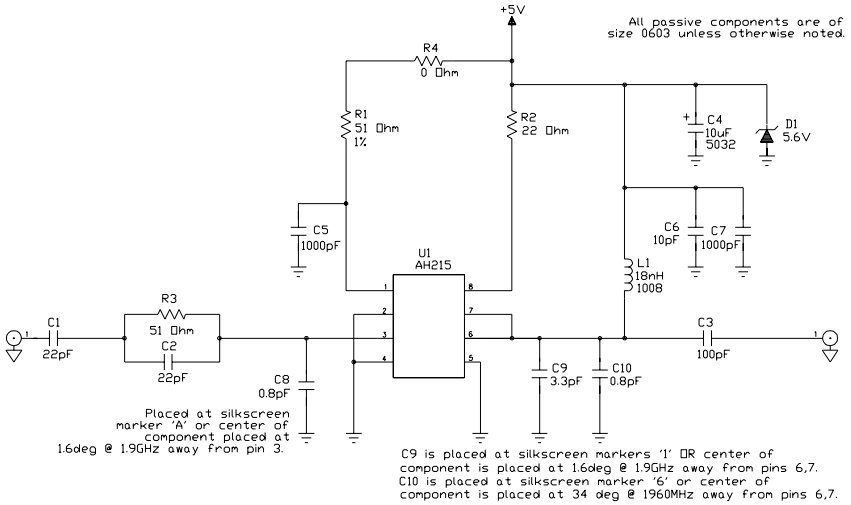
Specifications and information are subject to change without notice.

1960 MHz Application Circuit (AH215-S8PCB1960)

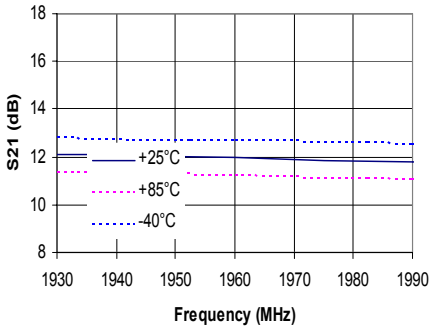
Typical RF Performance at 25°C

Frequency	1960 MHz
S21 – Gain	12 dB
S11 – Input Return Loss	-11 dB
S22 – Output Return Loss	-10 dB
Output P1dB	+32 dBm
Output IP3 (+17 dBm / tone, 1 MHz spacing)	+46 dBm
Channel Power (@-45 dBc ACPR, IS-95 9 channels fwd)	+25.5 dBm
Noise Figure	5.5 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

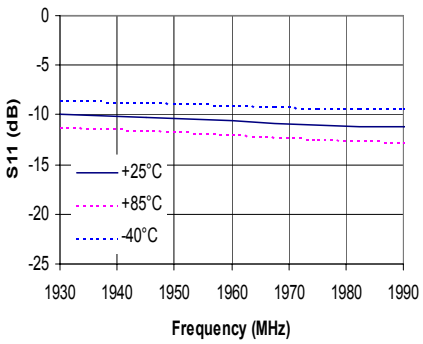
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8.



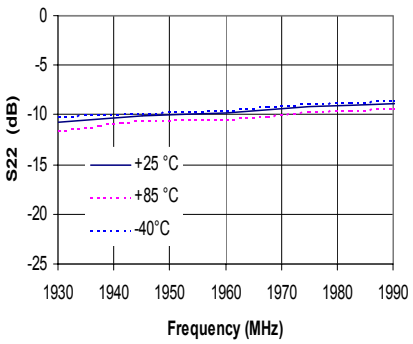
S21 vs. Frequency



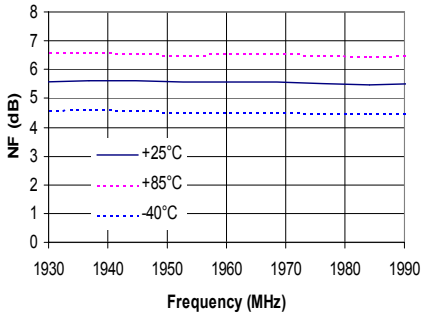
S11 vs. Frequency



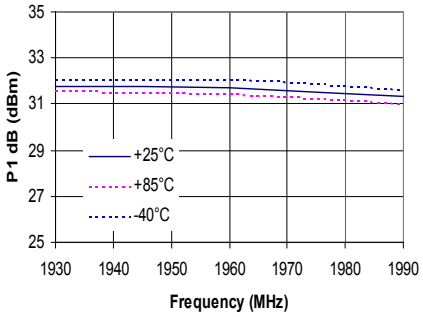
S22 vs. Frequency



Noise Figure vs. Frequency

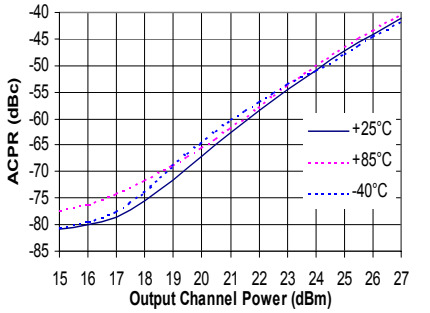


P1 dB vs. Frequency



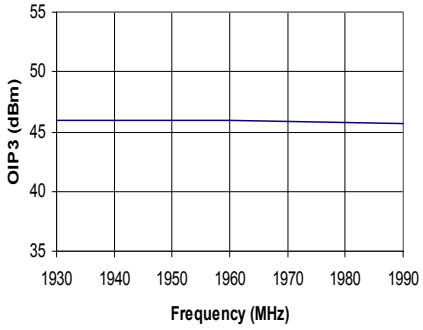
ACPR vs. Channel Power

IS-95, 9 Ch. Fwd. ±885 KHz offset, 30 KHz Meas BW, 1960 MHz



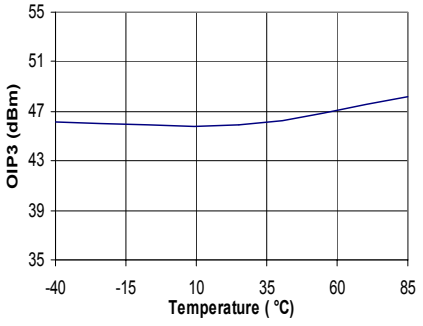
OIP3 vs. Frequency

+25°C, 15 dBm / tone



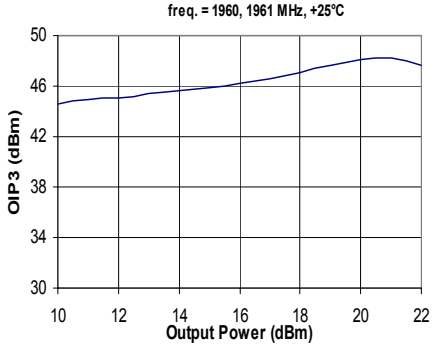
OIP3 vs. Temperature

freq. = 1960, 1961 MHz, +15 dBm



OIP3 vs. Output Power

freq. = 1960, 1961 MHz, +25°C

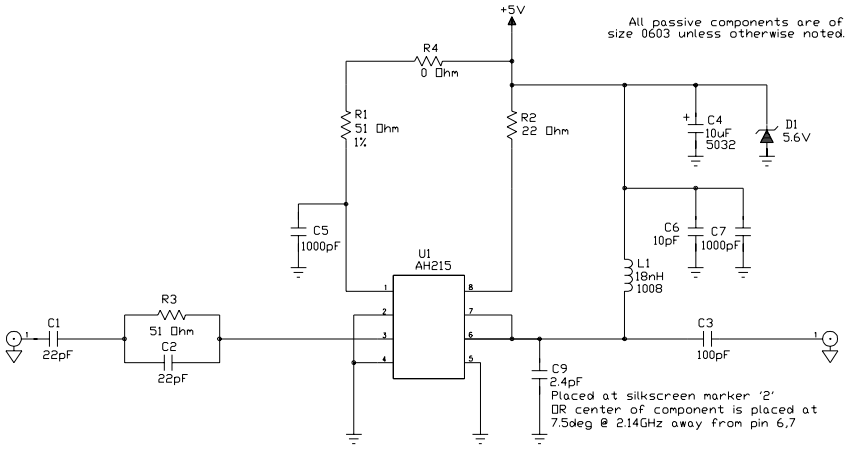


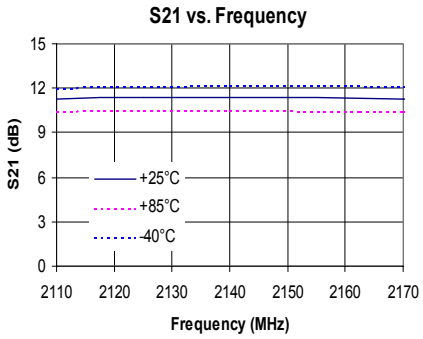
2140 MHz Application Circuit (AH215-S8PCB2140)

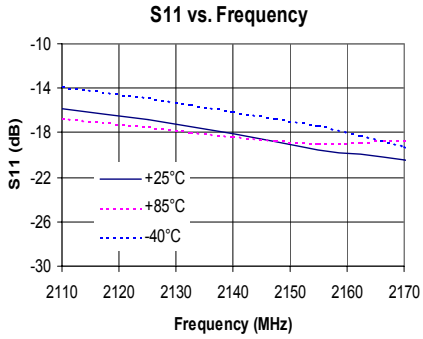
Typical RF Performance at 25°C

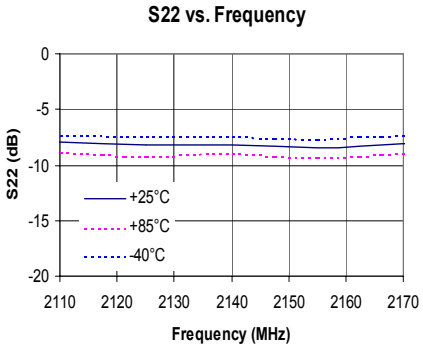
Frequency	2140 MHz
S21 – Gain	11 dB
S11 – Input Return Loss	-18 dB
S22 – Output Return Loss	-8.0 dB
Output P1dB	+31.5 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+45 dBm
Channel Power (@-45 dBc ACPR, IS-95 9 channels fwd)	+23 dBm
Noise Figure	6.2 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

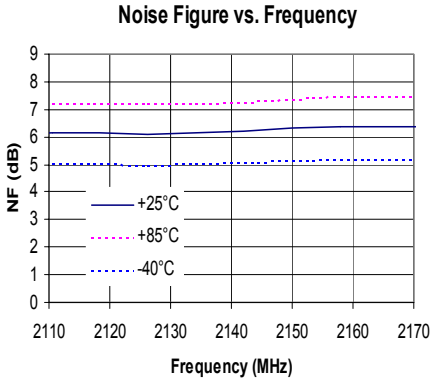
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8.

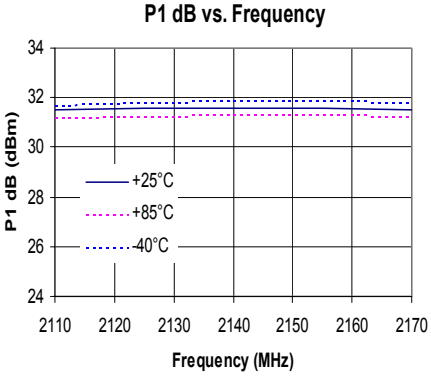


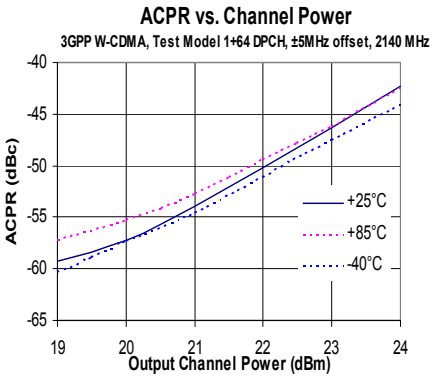


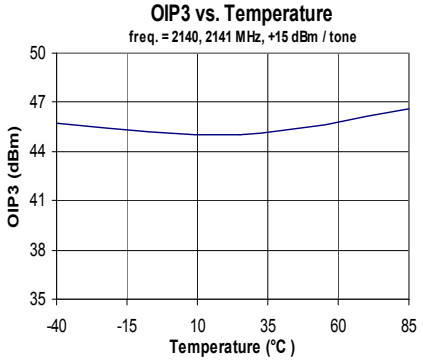


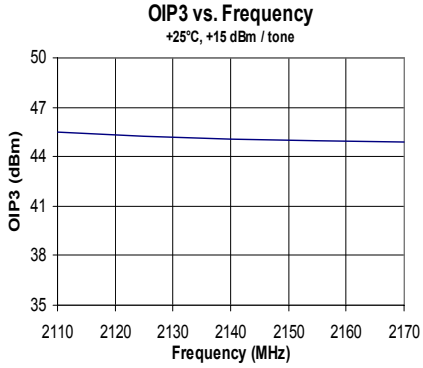


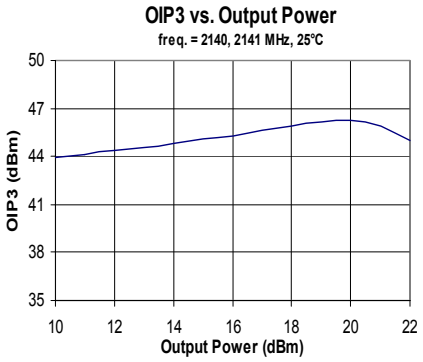










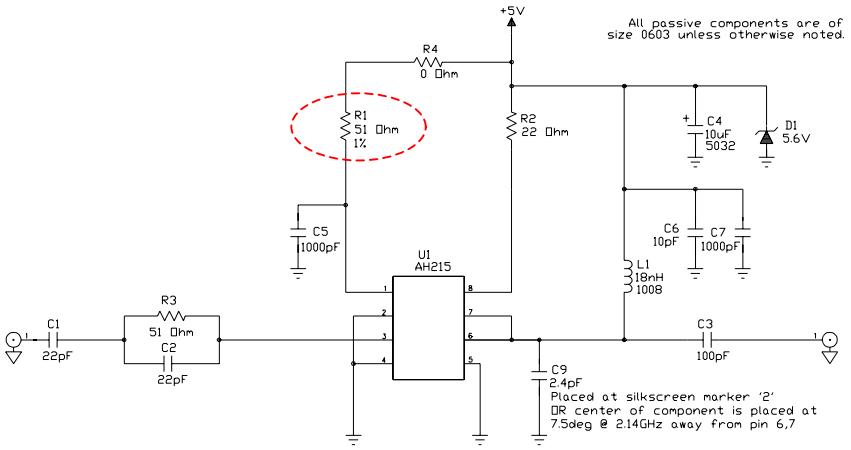


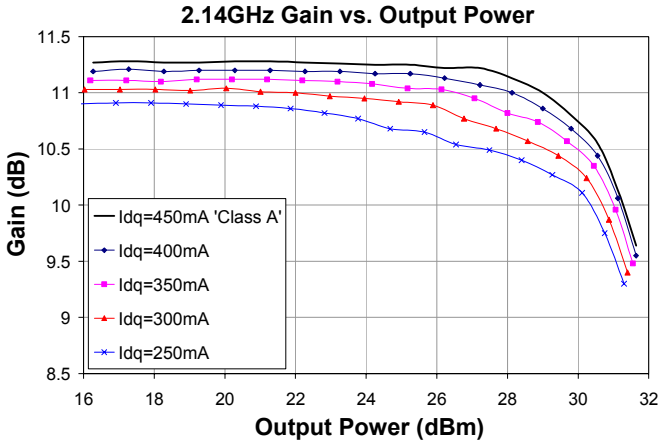
Application Note: Reduced Bias Configurations

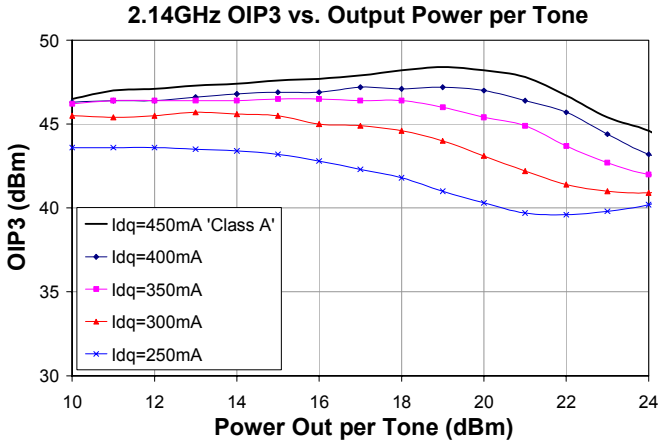
The AH215 / ECP100 can be configured to be operated with lower bias current by varying the bias-adjust resistor – R1. The recommended circuit configurations shown previously in this datasheet have the device operating in Class A operation. Lowering the current has little effect on the gain, OIP3, and P1dB performance of the device, but will slightly lower the ACLR/ACPR performance of the device as shown below. An example of the measured data below represents the AH215 / ECP100 measured and configured for 2.14 GHz applications. It is expected that variation of the bias current for other frequency applications will produce similar performance results.

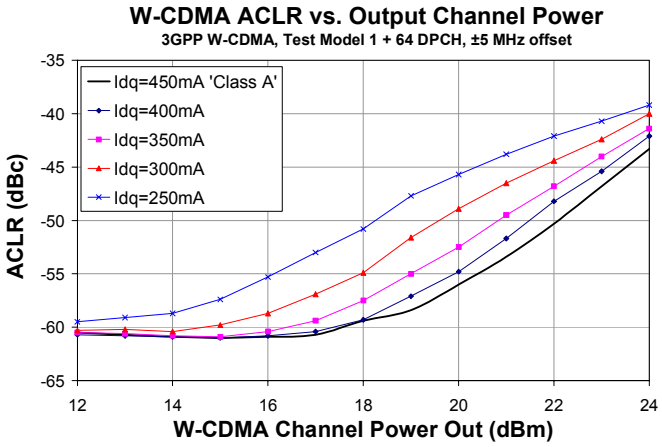
AH215-PCB2140 Performance Data

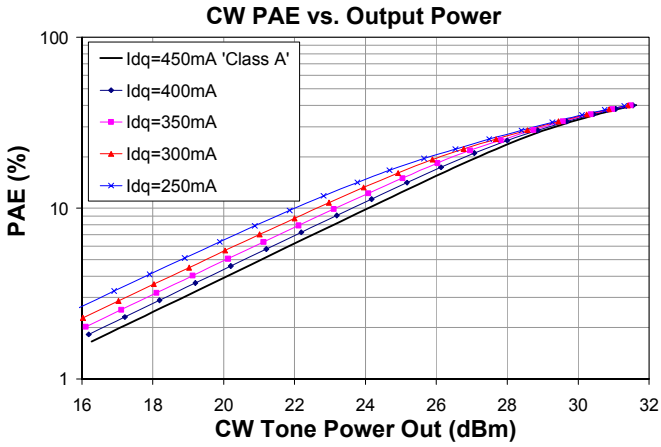
R1 (ohms)	Icq (mA)	Pdiss (W)	P1dB (dBm)	OIP3 (dBm)
51	450	2.25	+31.0	+47.1
68	400	2.00	+30.9	+46.4
100	350	1.75	+30.8	+46.4
130	300	1.50	+30.6	+45.5
180	250	1.25	+30.5	+43.6







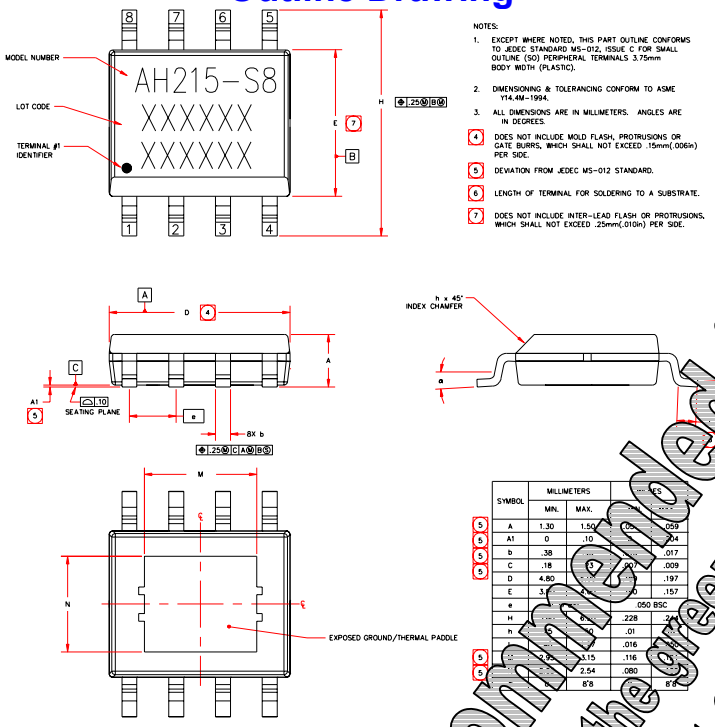




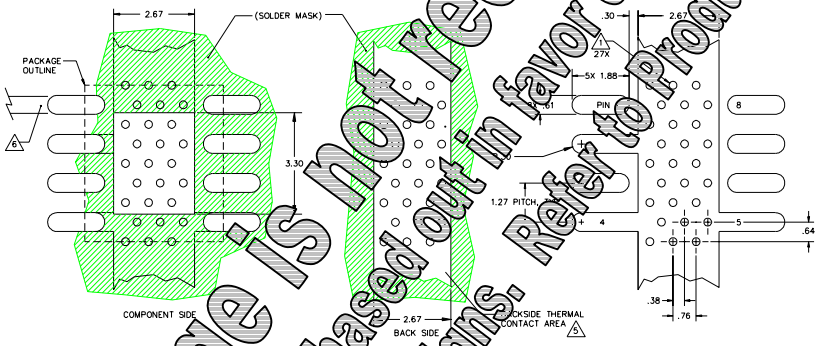
AH215-S8 (SOIC-8 Package) Mechanical Information

This package may contain lead-bearing materials. The plating material on the leads is SnPb.

Outline Drawing



Land Pattern



Product Marking

The component will be marked with an "AH215-S8" designator and an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution: ESD sensitive device.

ESD Rating: Class 1B
Value: Passes /500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating: Level 3 at +235° C convection reflow
Standard: JEDEC Standard J-STD-020

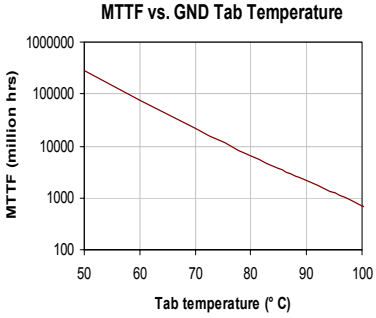
Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85° C
Thermal Resistance [1] Rth	45° C / W
Junction Temperature [2] Tjc	139° C

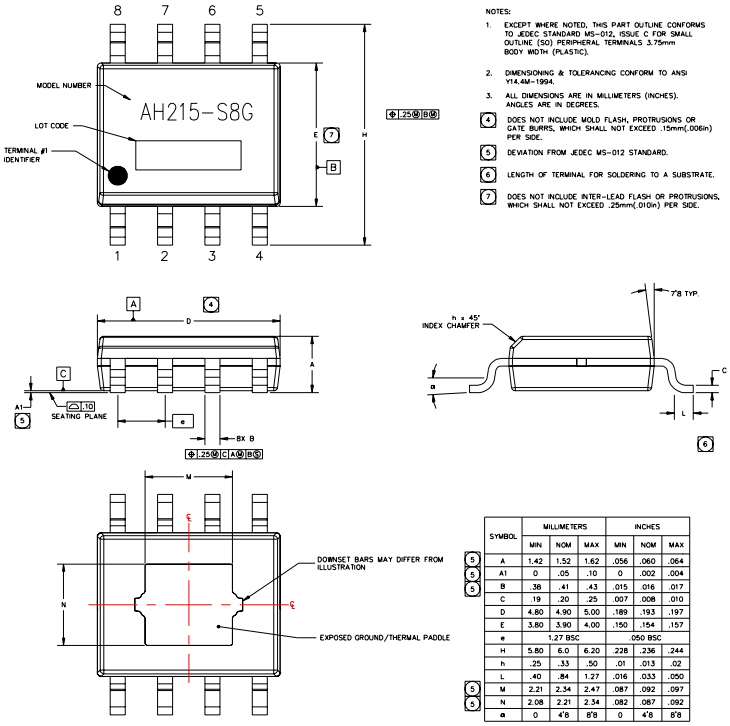
Notes:
1. The thermal resistance is referenced from the junction-to-case at a case temperature of 85° C. Tjc is a function of the voltage across pins 6 and 7 and the current applied to pins 6, 7, and 8 and can be calculated by:
   Tjc = Tcase + Rth * Vcc * Icc
2. This corresponds to typical biasing condition of +5V, 450 mA at an 85° C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 247° C.



AH215-S8G (Lead-Free Package) Mechanical Information

This package is lead-free/green/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260°C reflow temperature) and lead (maximum 245°C reflow temperature) soldering processes.

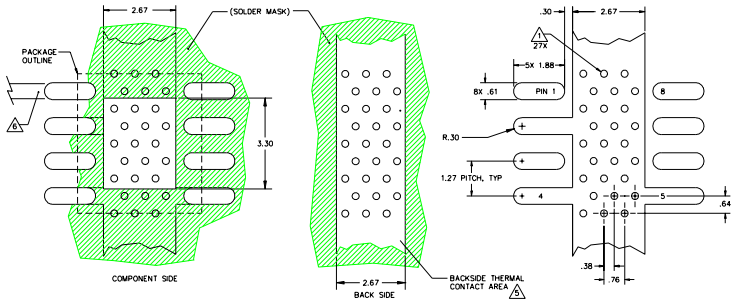
Outline Drawing



NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e		1.27 BSC			.050 BSC	
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°8	8°8	0	4°8	8°8

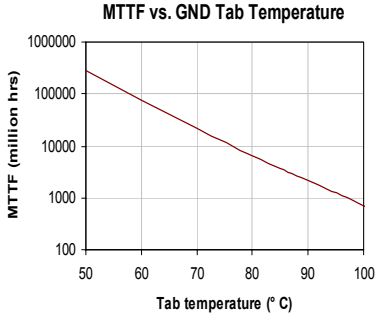
Mounting Configuration / Land Pattern



Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85° C
Thermal Resistance (1), Rth	33° C / W
Junction Temperature (2), Tjc	159° C

Notes:
1. The thermal resistance is referenced from the junction-to-case at a case temperature of 85° C. Tjc is a function of the voltage at pins 6 and 7 and the current applied to pins 6, 7, and 8 and can be calculated by:
   Tjc = Tcase + Rth * Vcc * Icc
2. This corresponds to the typical biasing condition of +5V, 450 mA at an 85° C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 247° C.



Product Marking

The component will be marked with an "AH215-S8G" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes /500V to <1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 2 at +260° C convection reflow
Standard:	JEDEC Standard J-STD-020

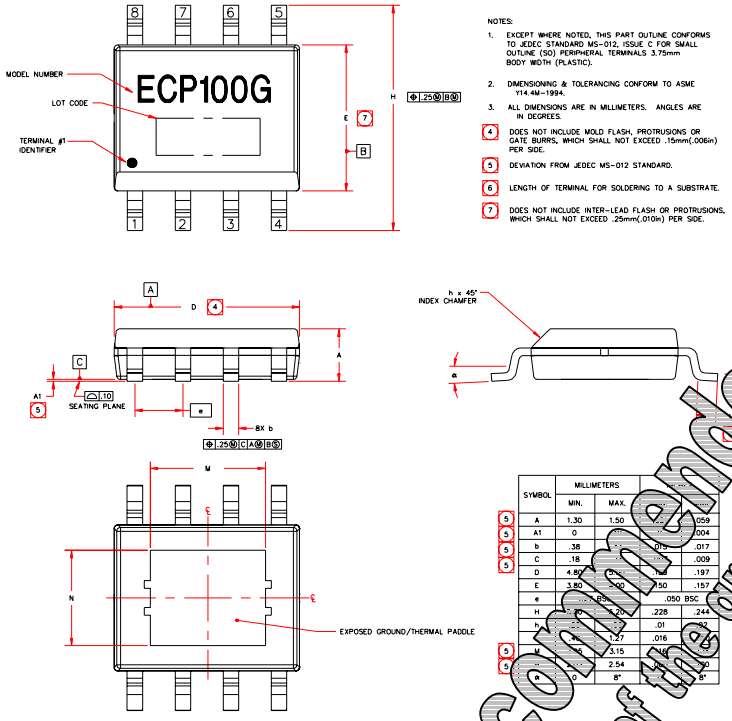
Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.

ECP100G (SOIC-8 Package) Mechanical Information

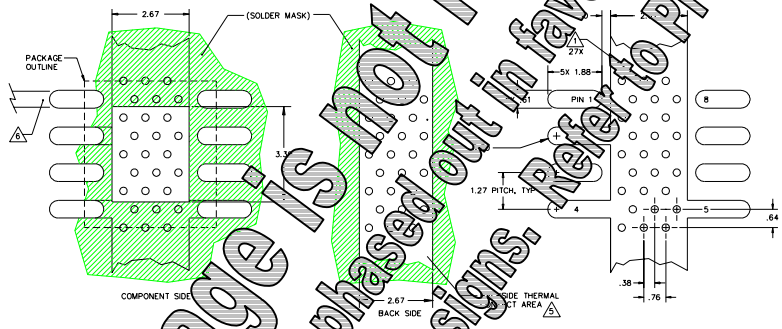
This package may contain lead-bearing materials. The plating material on the leads is SnPb.

Outline Drawing



SYMBOL	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	1.30	1.50	.051	.059
A1	0	[illegible]	.000	.004
b	.38	[illegible]	.015	.017
C	.18	[illegible]	[illegible]	.009
D	4.85	[illegible]	[illegible]	.197
E	3.80	[illegible]	.150	.157
e	BSC		.050 BSC	
H	[illegible]	[illegible]	.228	.244
h	[illegible]	[illegible]	.01	[illegible]
L	[illegible]	1.27	.016	[illegible]
M	[illegible]	3.15	[illegible]	[illegible]
N	[illegible]	2.54	[illegible]	.100
α	0°	8°	0°	8°

Land Pattern

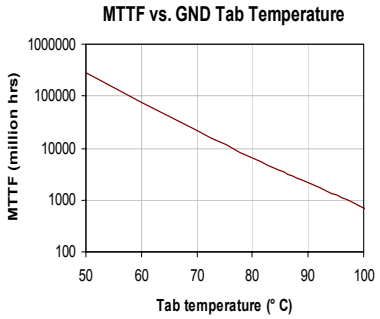


Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40° C to +85° C
Thermal Resistance, Rth (2)	38° C/W
Junction Temperature, Tjc (1)	253° C

Notes:

1. The thermal resistance is referenced from the junction-to-case at a case temperature of +85° C. Tjc is a function of the voltage at pins 5 and 7 and the current fed to pins 5, 6, 7, and 8. Tjc can be calculated by:
   Tjc = Tcase + Rth * (Vd * Icc)
2. This corresponds to the typical biasing condition of +5V, 95 mA at a +85° C case temperature. A maximum MTTF of 1 million hours is achieved for junction temperatures below 247° C.



Product Marking

The component will be marked with an "ECP100G" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the Application Note section.

ESD / MSL Information

Caution: ESD sensitive device.

ESD Rating: Class 1B
Value: Passes between 500 and 1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating: Level 3 at +235° C convection reflow
Standard: JEDEC Standard J-STD-020

Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.