74VCX16245

Low-Voltage 1.8/2.5/3.3V 16-Bit Transceiver

With 3.6 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

The 74VCX16245 is an advanced performance, non−inverting 16−bit transceiver. It is designed for very high−speed, very low−power operation in 1.8 V, 2.5 V or 3.3 V systems.

When operating at 2.5 V (or 1.8 V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3 V busses. It is guaranteed to be over−voltage tolerant to 3.6 V.

The VCX16245 is designed with byte control. It can be operated as two separate octals, or with the controls tied together, as a 16−bit wide function. The Transmit/Receive (T/$\overline{R}$n) inputs determine the direction of data flow through the bi−directional transceiver. Transmit (active−HIGH) enables data from A ports to B ports; Receive (active−LOW) enables data from B to A ports. The Output Enable inputs ($\overline{OEn}$), when HIGH, disable both A and B ports by placing them in a HIGH Z condition.

Features

- Designed for Low Voltage Operation: V_{CC} = 1.65−3.6 V
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 2.5 ns max for 3.0 to 3.6 V
  3.0 ns max for 2.3 to 2.7 V
  6.0 ns max for 1.65 to 1.95 V
- Static Drive: ±24 mA Drive at 3.0 V
  ±18 mA Drive at 2.3 V
  ±6 mA Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±250 mA @ 125°C
- ESD Performance: Human Body Model >2000 V;
  Machine Model >200 V
- Pb−Free Package is Available*

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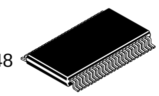
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TSSOP−48
DT SUFFIX
CASE 1201

MARKING DIAGRAM

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A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
74VCX16245DT	TSSOP	39 / Rail
74VCX16245DTR	TSSOP	2500/Tape & Reel
74VCX16245DTRG	TSSOP (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

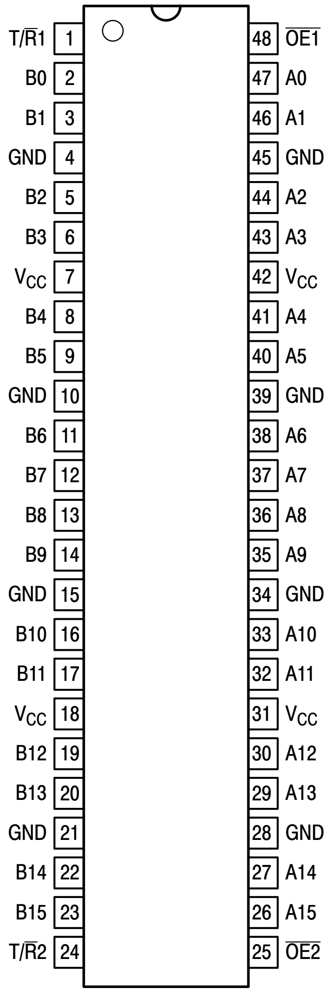


Figure 1. 48−Lead Pinout
(Top View)

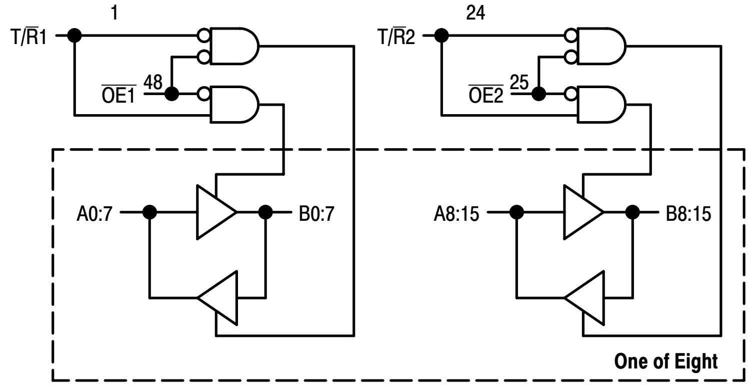


Figure 2. Logic Diagram

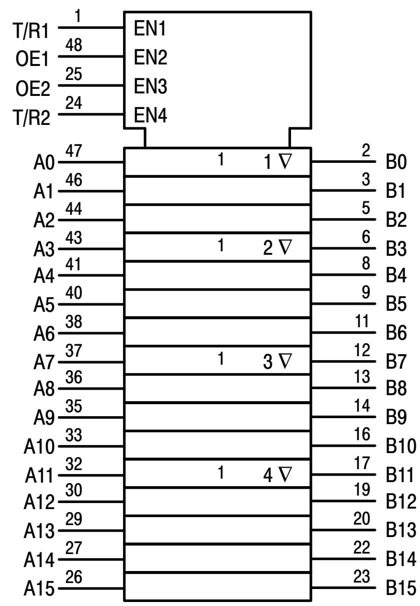


Figure 3. IEC Logic Diagram

PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
T/$\overline{R}$n	Transmit/Receive Inputs
A0−A15	Side A Inputs or 3−State Outputs
B0−B15	Side B Inputs or 3−State Outputs

Inputs		Outputs	Inputs		Outputs
$\overline{OE1}$	T/$\overline{R1}$		$\overline{OE2}$	T/$\overline{R2}$	
L	L	Bus B0:7 Data to Bus A0:7	L	L	Bus B8:15 Data to Bus A8:15
L	H	Bus A0:7 Data to Bus B0:7	L	H	Bus A8:15 Data to Bus B8:15
H	X	High Z State on A0:7, B0:7	H	X	High Z State on A8:15, B8:15

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level and Transitions Are Acceptable

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +4.6$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +4.6$	Output in 3−State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$	Note 1.; Outputs Active	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute−maximum−rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	1.65 1.2	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	−0.3		3.6	V
V_O	Output Voltage (Active State) (3−State)	0 0		V_{CC} 3.6	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V − 3.6V			−24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V − 3.6V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.3V − 2.7V			−18	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.3V − 2.7V			18	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 1.65 − 1.95V			−6	mA
I_{OL}	LOW Level Output Current, V_{CC} = 1.65 − 1.95V			6	mA
T_A	Operating Free−Air Temperature	−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$ Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 2.)	$1.65V \le V_{CC} < 2.3V$	0.65 x V_{CC}		V
		$2.3V \le V_{CC} \le 2.7V$	1.6		
		$2.7V < V_{CC} \le 3.6V$	2.0		
V_{IL}	LOW Level Input Voltage (Note 2.)	$1.65V \le V_{CC} < 2.3V$		0.35 x V_{CC}	V
		$2.3V \le V_{CC} \le 2.7V$		0.7	
		$2.7V < V_{CC} \le 3.6V$		0.8	
V_{OH}	HIGH Level Output Voltage	$1.65V \le V_{CC} \le 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		$V_{CC} = 1.65V$; $I_{OH} = -6mA$	1.25		
		$V_{CC} = 2.3V$; $I_{OH} = -6mA$	2.0		
		$V_{CC} = 2.3V$; $I_{OH} = -12mA$	1.8		
		$V_{CC} = 2.3V$; $I_{OH} = -18mA$	1.7		
		$V_{CC} = 2.7V$; $I_{OH} = -12mA$	2.2		
		$V_{CC} = 3.0V$; $I_{OH} = -18mA$	2.4		
		$V_{CC} = 3.0V$; $I_{OH} = -24mA$	2.2		
V_{OL}	LOW Level Output Voltage	$1.65V \le V_{CC} \le 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		$V_{CC} = 1.65V$; $I_{OL} = 6mA$		0.3	
		$V_{CC} = 2.3V$; $I_{OL} = 12mA$		0.4	
		$V_{CC} = 2.3V$; $I_{OL} = 18mA$		0.6	
		$V_{CC} = 2.7V$; $I_{OL} = 12mA$		0.4	
		$V_{CC} = 3.0V$; $I_{OL} = 18mA$		0.4	
		$V_{CC} = 3.0V$; $I_{OL} = 24mA$		0.55	
I_I	Input Leakage Current	$1.65V \le V_{CC} \le 3.6V$; $0V \le V_I \le 3.6V$		±5.0	μA
I_{OZ}	3−State Output Current	$1.65V \le V_{CC} \le 3.6V$; $0V \le V_O \le 3.6V$; $V_I = V_{IH}$ or V_{IL}		±10	μA
I_{OFF}	Power−Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 3.6V$		10	μA
I_{CC}	Quiescent Supply Current (Note 3.)	$1.65V \le V_{CC} \le 3.6V$; V_I = GND or V_{CC}		20	μA
		$1.65V \le V_{CC} \le 3.6V$; $3.6V \le V_I$, $V_O \le 3.6V$		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7V < V_{CC} \le 3.6V$; $V_{IH} = V_{CC} - 0.6V$		750	μA

2. These values of V_I are used to test DC electrical characteristics only.
3. Outputs disabled or 3−state only.

AC CHARACTERISTICS (Note 4.; $t_R = t_F = 2.0ns$; $C_L = 30pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits $T_A = -40°C$ to $+85°C$ $V_{CC} = 3.0V$ to $3.6V$ Min	Max	$V_{CC} = 2.3V$ to $2.7V$ Min	Max	$V_{CC} = 1.65$ to1.95V Min	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	0.8 0.8	2.5 2.5	1.0 1.0	3.0 3.0	1.5 1.5	6.0 6.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	0.8 0.8	3.8 3.8	1.0 1.0	4.9 4.9	1.5 1.5	9.3 9.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	0.8 0.8	3.7 3.7	1.0 1.0	4.2 4.2	1.5 1.5	7.6 7.6	ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 5.)			0.5 0.5		0.5 0.5		0.75 0.75	ns

4. For C_L = 50pF, add approximately 300ps to the AC maximum specification.
5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25°C$ Typ	Unit
V_{OLP}	Dynamic LOW Peak Voltage (Note 6.)	V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	0.25	V
		V_{CC} = 2.5V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	0.6	
		V_{CC} = 3.3V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	0.8	
V_{OLV}	Dynamic LOW Valley Voltage (Note 6.)	V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	−0.25	V
		V_{CC} = 2.5V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	−0.6	
		V_{CC} = 3.3V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	−0.8	
V_{OHV}	Dynamic HIGH Valley Voltage (Note 7.)	V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.5	V
		V_{CC} = 2.5V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.9	
		V_{CC} = 3.3V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	2.2	

6. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.
7. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the HIGH state.

CAPACITIVE CHARACTERISTICS

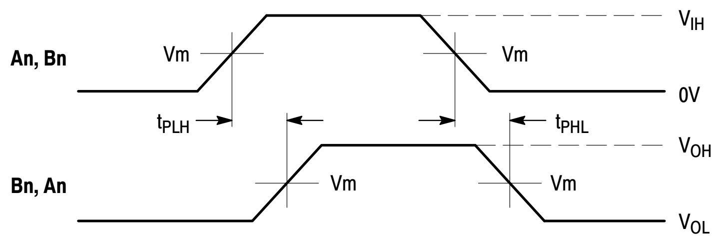
Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	Note 8.	6	pF
C_{OUT}	Output Capacitance	Note 8.	7	pF
C_{PD}	Power Dissipation Capacitance	Note 8., 10MHz	20	pF

8. V_{CC} = 1.8, 2.5 or 3.3V; V_I = 0V or V_{CC}.

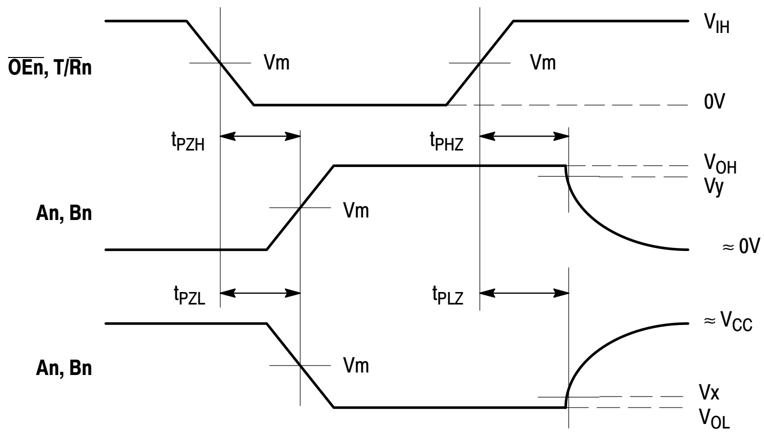
AC CHARACTERISTICS ($t_R = t_F$ = 2.0ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits T_A = −40°C to +85°C V_{CC} = 3.0V to 3.6V Min	Max	V_{CC} = 2.7V Min	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	3	1.0 1.0	3.0 3.0		3.6 3.6	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	4	1.0 1.0	4.4 4.4		5.4 5.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	4	1.0 1.0	4.1 4.1		4.6 4.6	ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 9.)			0.5 0.5		0.5 0.5	ns

9. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.



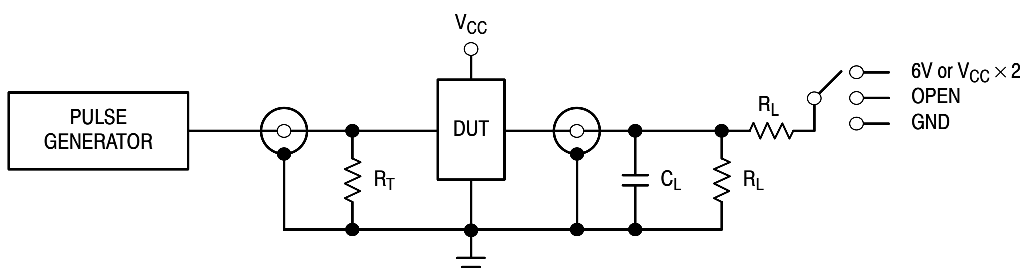
WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.0ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.0ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 4. AC Waveforms

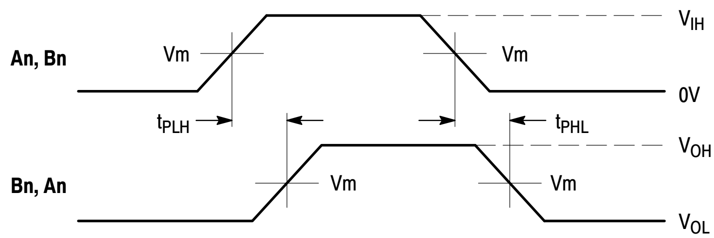
Symbol	V_{CC} 3.3V ±0.3V	V_{CC} 2.5V ±0.2V	V_{CC} 1.8V ±0.15V
V_{IH}	2.7V	V_{CC}	V_{CC}
V_m	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_x	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V



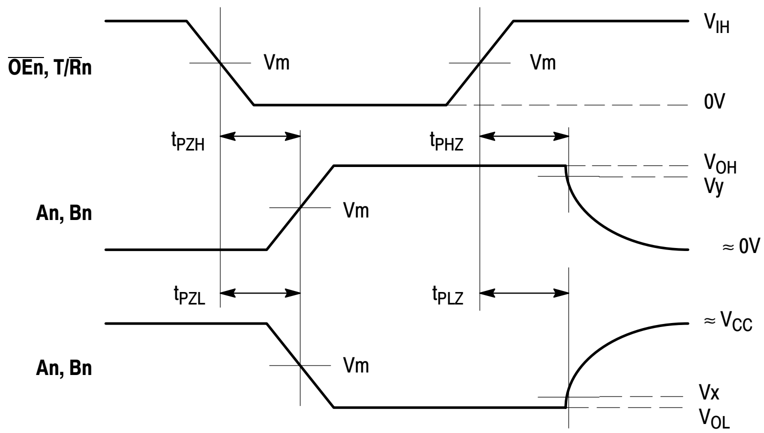
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ±0.3V; V_{CC}× 2 at V_{CC} = 2.5 ±0.2V; 1.8V ±0.15V
t_{PZH}, t_{PHZ}	GND

C_L = 30pF or equivalent (Includes jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 5. Test Circuit



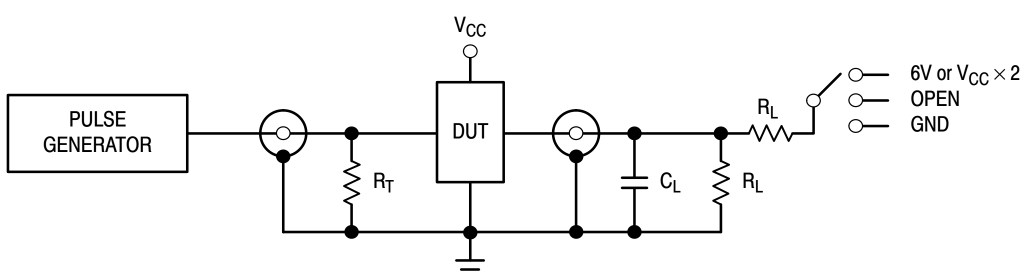
WAVEFORM 3 – PROPAGATION DELAYS
$t_R = t_F = 2.0ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 4 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.0ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 6. AC Waveforms

Symbol	V_{CC} 3.3V ±0.3V	V_{CC} 2.7V
V_{IH}	2.7V	2.7V
V_m	1.5V	1.5V
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V



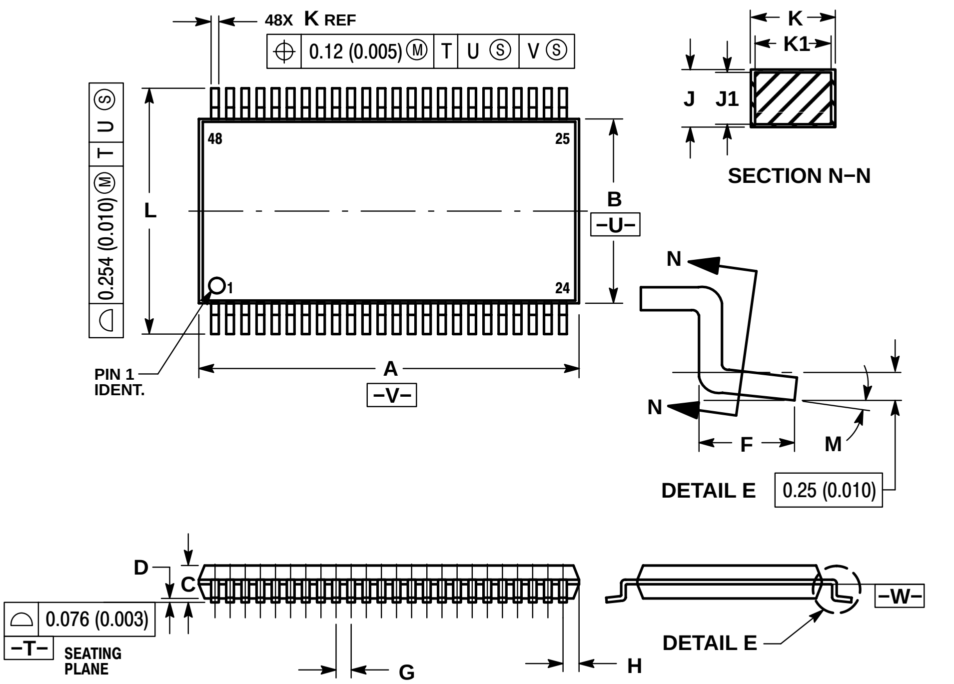
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ±0.3V; $V_{CC} \times 2$ at V_{CC} = 2.5 ±0.2V; 1.8 ±0.15V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 7. Test Circuit

PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	−−−	1.10	−−−	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	−−−	0.015	−−−
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

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