



2GB – 2x128Mx64 DDR2 SDRAM UNBUFFERED

FEATURES

- 200-pin, dual in-line memory module (SO-DIMM)
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- Adjustable data-output drive strength
- On-die termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Dual Rank
- RoHS compliant
- JEDEC Package option
 - 200 Pin (SO-DIMM)
 - PCB – 30.00mm (1.181") TYP.

DESCRIPTION

The WV3HG2128M64EEU is a 2x128Mx64 Double Data Rate DDR2 SDRAM high density SO-DIMM. This memory module consists of sixteen 128Mx8 bit with 8 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 200-pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-tRCD-tRP	3-3-3	4-4-4	5-5-5	6-6-6

* Consult factory for availability



PIN CONFIGURATION

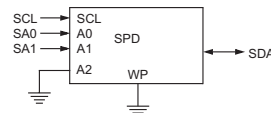
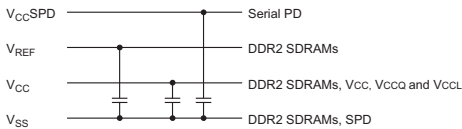
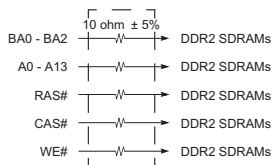
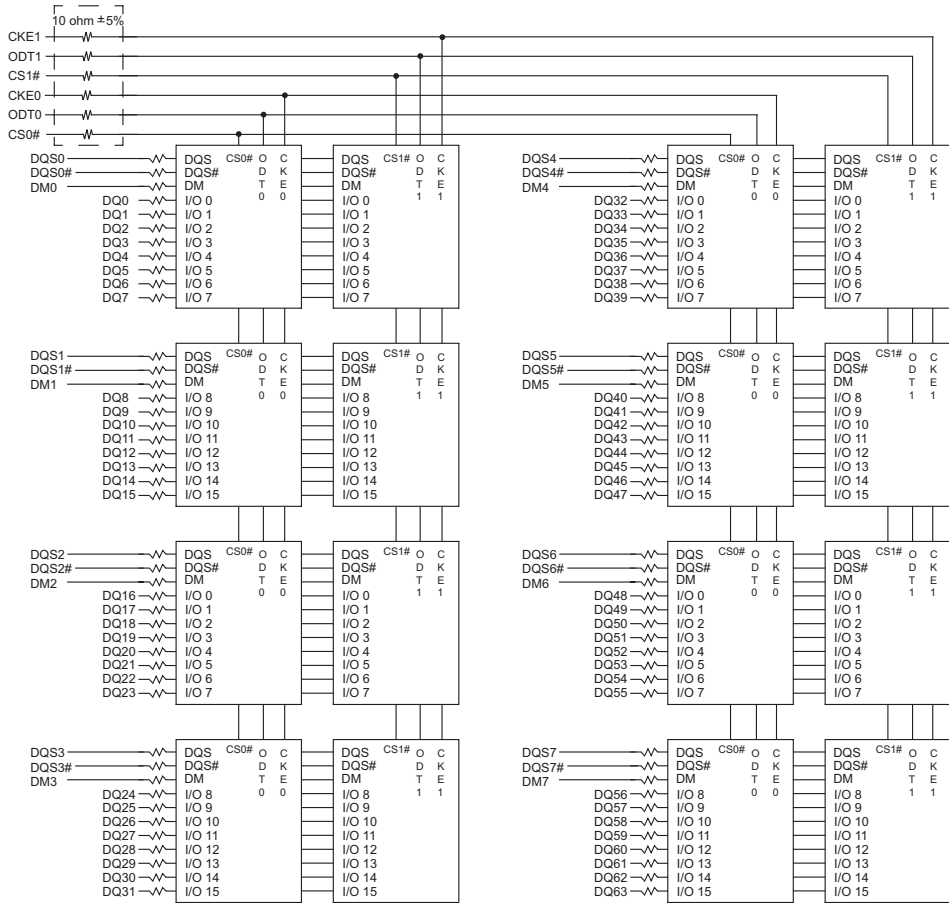
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	51	DQS2	101	A1	151	DQ42
2	Vss	52	DM2	102	A0	152	DQ46
3	Vss	53	Vss	103	Vcc	153	DQ43
4	DQ4	54	Vss	104	Vcc	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	Vss
6	DQ5	56	DQ22	106	BA1	156	Vss
7	DQ1	57	DQ19	107	BA0	157	DQ48
8	Vss	58	DQ23	108	RAS#	158	DQ52
9	Vss	59	Vss	109	WE#	159	DQ49
10	DM0	60	Vss	110	CS0#	160	DQ53
11	DQS0#	61	DQ24	111	Vcc	161	Vss
12	Vss	62	DQ28	112	Vcc	162	Vss
13	DQS0	63	DQ25	113	CAS#	163	NC
14	DQ6	64	DQ29	114	ODT0	164	CK1
15	Vss	65	Vss	115	CS1#	165	Vss
16	DQ7	66	Vss	116	A13	166	CK1#
17	DQ2	67	DM3	117	Vcc	167	DQS6#
18	Vss	68	DQS3#	118	Vcc	168	Vss
19	DQ3	69	NC	119	ODT1	169	DQS6
20	DQ12	70	DQS3	120	NC	170	DM6
21	Vss	71	Vss	121	Vss	171	Vss
22	DQ13	72	Vss	122	Vss	172	Vss
23	DQ8	73	DQ26	123	DQ32	173	DQ50
24	Vss	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51
26	DM1	76	DQ31	126	DQ37	176	DQ55
27	Vss	77	Vss	127	Vss	177	Vss
28	Vss	78	Vss	128	Vss	178	Vss
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	Vcc	131	DQS4	181	DQ57
32	CK0#	82	Vcc	132	Vss	182	DQ61
33	Vss	83	NC	133	Vss	183	Vss
34	Vss	84	NC	134	DQ38	184	Vss
35	DQ10	85	BA2	135	DQ34	185	DM7
36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	Vcc	137	DQ35	187	Vss
38	DQ15	88	Vcc	138	Vss	188	DQS7
39	Vss	89	A12	139	Vss	189	DQ58
40	Vss	90	A11	140	DQ44	190	Vss
41	Vss	91	A9	141	DQ40	191	DQ59
42	Vss	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	Vss
44	DQ20	94	A6	144	Vss	194	DQ63
45	DQ17	95	Vcc	145	Vss	195	SDA
46	DQ21	96	Vcc	146	DQS5#	196	Vss
47	Vss	97	A5	147	DM5	197	SCL
48	Vss	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	Vss	199	VCCSPD
50	NC	100	A2	150	Vss	200	SA1

PIN NAMES

Pin Name	Function
CK0,CK1	Clock Inputs, positive line
CK0#, CK1#	Clock Inputs, negative line
CKE0, CKE1	Clock Enables
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CS0#, CS1#	Chip Selects
A0-A13	Address Inputs
A10/AP	Address Input/Auto precharge
BA0 - BA2	SDRAM Bank Address
ODT0,ODT1	On-die termination control
SCL	Serial Presence Detect (SPD) Clock Input
SDA	SPD Data Input/Output
SA0, SA1	SPD address
DQ0-DQ63	Data Input/Output
DM0-DM7	Data Masks
DQS0-DQS7	Data strobes
DQS0#-DQS7#	Data strobes complement
Vcc	Core and I/O Power
Vss	Ground
VREF	Input/Output Reference
VccSPD	SPD Power
NC	Spare pins, No connect



FUNCTIONAL BLOCK DIAGRAM



* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0#	8 DDR2 SDRAMs
*CK1/CK1#	8 DDR2 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Notes :

1. All resistor values are 22 ohms ± 5% unless otherwise specified
2. BAx, Ax, RAS#, CAS#, WE# resistors : 3.0 Ohms ±5%.



DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	V _{CC}	1.7	1.8	1.9	V	
I/O Reference Voltage	V _{REF}	0.49 x V _{CC}	0.50 x V _{CC}	0.51 x V _{CC}	V	1
I/O Termination Voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	2

Notes:

- V_{REF} is expected to equal V_{CC2} of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-1.0	2.3	V	
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5	2.3	V	
T _{STG}	Storage Temperature	-55	100	°C	
I _L	Input leakage current; Any input 0V<V _{IN} <V _{CC} ; V _{REF} input 0V<V _{IN} <0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-80	80	µA
		CS#, CKE	-40	40	µA
		CK, CK#	-40	40	µA
		DM	-10	10	µA
I _{oz}	Output leakage current; 0V<V _{IN} <V _{CC} ; DQs and ODT are disable				
		DQ, DQS, DQS#	-10	10	µA
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level	-32	32	µA	

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	C _{IN1}	20	36	pF
Input Capacitance (CKE0, CKE1), (ODT0, ODT1)	C _{IN2}	12	20	pF
Input Capacitance (CS0#, CS1#)	C _{IN3}	12	20	pF
Input Capacitance (CK0, CK0#, CK1, CK1#)	C _{IN4}	12	20	pF
Input Capacitance (DM0 ~ DM7), (DQS0 ~ DQS7)	C _{IN5} (667)*	9	11	pF
	C _{IN5} (533 & 400)	9	12	pF
Input Capacitance (DQ0 ~ DQ63)	C _{OUT1} (667)*	9	11	pF
	C _{OUT1} (533 & 400)	9	12	pF

* 800Mb/s = TBD



OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0° to 85°	°C	1, 2

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDED JESD51.2
2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

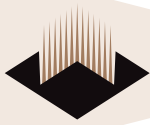
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V _{IH} (DC)	V _{REF} + 0.125	V _{CC} + 0.300	V
Input Low (Logic 0) Voltage	V _{IL} (DC)	-0.300	V _{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V _{IH} (DC)	V _{REF} + 0.250	-	V
Input Low (Logic 1) Voltage DDR2-667	V _{IH} (DC)	V _{REF} + 0.200	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V _{IL} (DC)	-	V _{REF} - 0.250	V
Input Low (Logic 0) Voltage DDR2-667, DDR2-800 TBD	V _{IL} (DC)	-	V _{REF} - 0.200	V



Icc SPECIFICATION

Symbol	Proposed Conditions	806	665	534	403	Units	
I _{CC0} *	Operating one bank active-precharge; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	816	776	736	mA	
I _{CC1} *	Operating one bank active-read-precharge; I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W}	TBD	896	856	816	mA	
I _{CC2P} **	Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	192	192	192	mA	
I _{CC2Q} **	Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	140	560	560	mA	
I _{CC2N} **	Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING	TBD	720	640	640	mA	
I _{CC3P} **	Active power-down current; All banks open; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	480	400	400	mA
		Slow PDN Exit MRS(12) = 1	TBD	192	192	192	mA
I _{CC3N} **	Active standby current; All banks open; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RAS} min(I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	800	720	720	mA	
I _{CC4W} *	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RAS} max(I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1,336	1,136	1,016	mA	
I _{CC4R} *	Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RAS} max(I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W}	TBD	1,336	1,136	1,016	mA	
I _{CC5} **	Burst auto refresh current; t _{CK} = t _{CK} (I _{CC}); Refresh command at every t _{RFC} (I _{CC}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	3,520	3,440	3,360	mA	
I _{CC6} **	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	160	160	160	mA
I _{CC7} *	Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = t _{RC} D(I _{CC})-1*t _{CK} (I _{CC}); t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RRD} = t _{RRD} (I _{CC}), t _{RCD} = 1*t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	TBD	2,496	2,336	2,176	mA	

Icc specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Note:

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.



AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS			806		665		534		403		UNIT	
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock	Clock cycle time	CL = 6	t _{CK (6)}	TBD	TBD						ps	
		CL = 5	t _{CK (5)}	TBD	TBD	3,000	8,000				ps	
		CL = 4	t _{CK (4)}	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	t _{CK (3)}	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width	t _{CH}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
	CK low-level width	t _{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
	Half clock period	t _{HP}	TBD	TBD	MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		ps	
Clock jitter	t _{JIT}	TBD	TBD	-125	125	-125	125	-125	125	ps		
Data	DQ output access time from CK/CK#	t _{AC}	TBD	TBD	-450	+450	-500	+500	-600	+600	ps	
	Data-out high-impedance window from CK/CK#	t _{HZ}	TBD	TBD		t _{AC} MAX		t _{AC} MAX		t _{AC} MAX	ps	
	Data-out low-impedance window from CK/CK#	t _{LZ}	TBD	TBD	t _{AC} MIN	t _{AC} MAX	t _{AC} MIN	t _{AC} MAX	t _{AC} MIN	t _{AC} MAX	ps	
	DQ and DM input setup time relative to DQS	t _{DS}	TBD	TBD	100		100		150		ps	
	DQ and DM input hold time relative to DQS	t _{DH}	TBD	TBD	225		225		275		ps	
	DQ and DM input pulse width (for each input)	t _{DLPW}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	Data hold skew factor	t _{QHS}	TBD	TBD		340		400		450	ps	
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access	t _{QH}	TBD	TBD	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ps	
	Data valid output window (DVW)	t _{DVW}	TBD	TBD	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns	
Data Strobe	DQS input high pulse width	t _{DQSH}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	DQS input low pulse width	t _{DQSL}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	DQS output access time from CK/CK#	t _{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps	
	DQS falling edge to CK rising ... setup time	t _{DSS}	TBD	TBD	0.2		0.2		0.2		t _{CK}	
	DQS falling edge from CK rising ... hold time	t _{DSH}	TBD	TBD	0.2		0.2		0.2		t _{CK}	
	DQS...DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}	TBD	TBD		240		300		350	ps	
	DQS read preamble	t _{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	
	DQS read postamble	t _{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
	DQS write preamble setup time	t _{WPRES}	TBD	TBD	0		0		0		ps	
	DQS write preamble	t _{WPRE}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	DQS write postamble	t _{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
	Write command to first DQS latching transition	t _{DQSS}	TBD	TBD	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t _{CK}	
	Address and control	Address and control input pulse width for each input	t _{IPW}	TBD	TBD	0.6		0.6		0.6		t _{CK}
Address and control input setup time		t _{IS}	TBD	TBD	200		250		350		ps	
Address and control input hold time		t _{IH}	TBD	TBD	275		375		475		ps	
Address and control input hold time		t _{ICD}	TBD	TBD	2		2		2		t _{CK}	

AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

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AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			800		665		534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t _{RC}	TBD	TBD	55		60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t _{RCD}	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t _{FAW}	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t _{RAS}	TBD	TBD	45	70,000	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t _{RTP}	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t _{WR}	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t _{DAL}	TBD	TBD	t _{WR} + t _{RP}		t _{WR} + t _{RP}		t _{WR} + t _{RP}		ns
	Internal WRITE to READ command delay	t _{WTR}	TBD	TBD	7.5		7.5		10		ns
	PRECHARGE command period	t _{RP}	TBD	TBD	15		15		15		ns
	PRECHARGE ALL command period	t _{RPA}	TBD	TBD	t _{RP} +t _{CK}		t _{RP} +t _{CK}		t _{RP} +t _{CK}		ns
	LOAD MODE command cycle time	t _{MRD}	TBD	TBD	2		2		2		tck
CKE low to CK,CK# uncertainty	t _{DELAY}	TBD	TBD	t _{IS} + t _{CK} + t _{IH}		t _{IS} + t _{CK} + t _{IH}		t _{IS} + t _{CK} + t _{IH}		ns	
Self Refresh	REFRESH to Active of Refresh to Refresh command interval	t _{RFC}	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t _{REFI}	TBD	TBD		7.8		7.8		7.8	μs
	Exit self refresh to non-READ command	t _{XSNR}	TBD	TBD	t _{RFC} (MIN) + 10		t _{RFC} (MIN) + 10		t _{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t _{XSRD}	TBD	TBD	200		200		200		tck
	Exit self refresh timing reference	t _{ISXR}	TBD	TBD	t _{IS}		t _{IS}		t _{IS}		ps
ODT	ODT turn-on delay	t _{AOND}	TBD	TBD	2	2	2	2	2	2	tck
	ODT turn-on	t _{AON}	TBD	TBD	t _{AC} (MIN)	t _{AC} (MAX) + 1000	t _{AC} (MIN)	t _{AC} (MAX) + 1000	t _{AC} (MIN)	t _{AC} (MAX) + 1000	ps
	ODT turn-off delay	t _{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	tck
	ODT turn-off	t _{AOF}	TBD	TBD	t _{AC} (MIN)	t _{AC} (MAX) + 600	t _{AC} (MIN)	t _{AC} (MAX) + 600	t _{AC} (MIN)	t _{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t _{AONPD}	TBD	TBD	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t _{AOFFPD}	TBD	TBD	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t _{ANPD}	TBD	TBD	3		3		3		tck
	ODT power-down exit latency	t _{AXPD}	TBD	TBD	8		8		8		tck
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}	TBD	TBD	2		2		2		tck
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}	TBD	TBD	7 - AL		6 - AL		6 - AL		tck
	A Exit precharge power-down to any non-READ command.	t _{XP}	TBD	TBD	2		2		2		tck
	CKE minimum high/low time	t _{CKE}	TBD	TBD	3		3		3		tck

AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.



ORDERING INFORMATION FOR D4

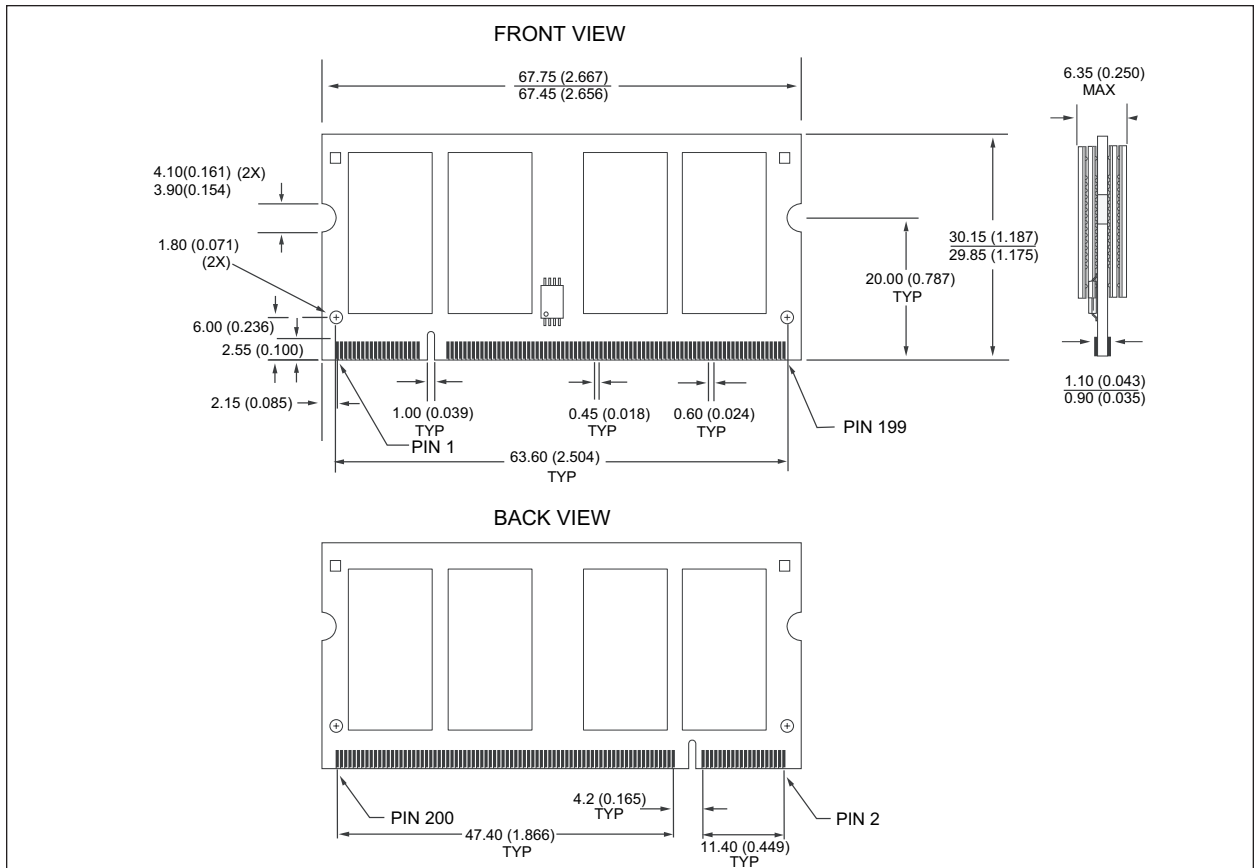
Part Number	Clock Speed	CAS Latency	t _{RC} D	t _{RP}	Height**
WV3HG2128M64EEU806D4xG*	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG2128M64EEU665D4xG*	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG2128M64EEU534D4xG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG2128M64EEU403D4xG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

* Consult factory for availability

NOTES:

- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

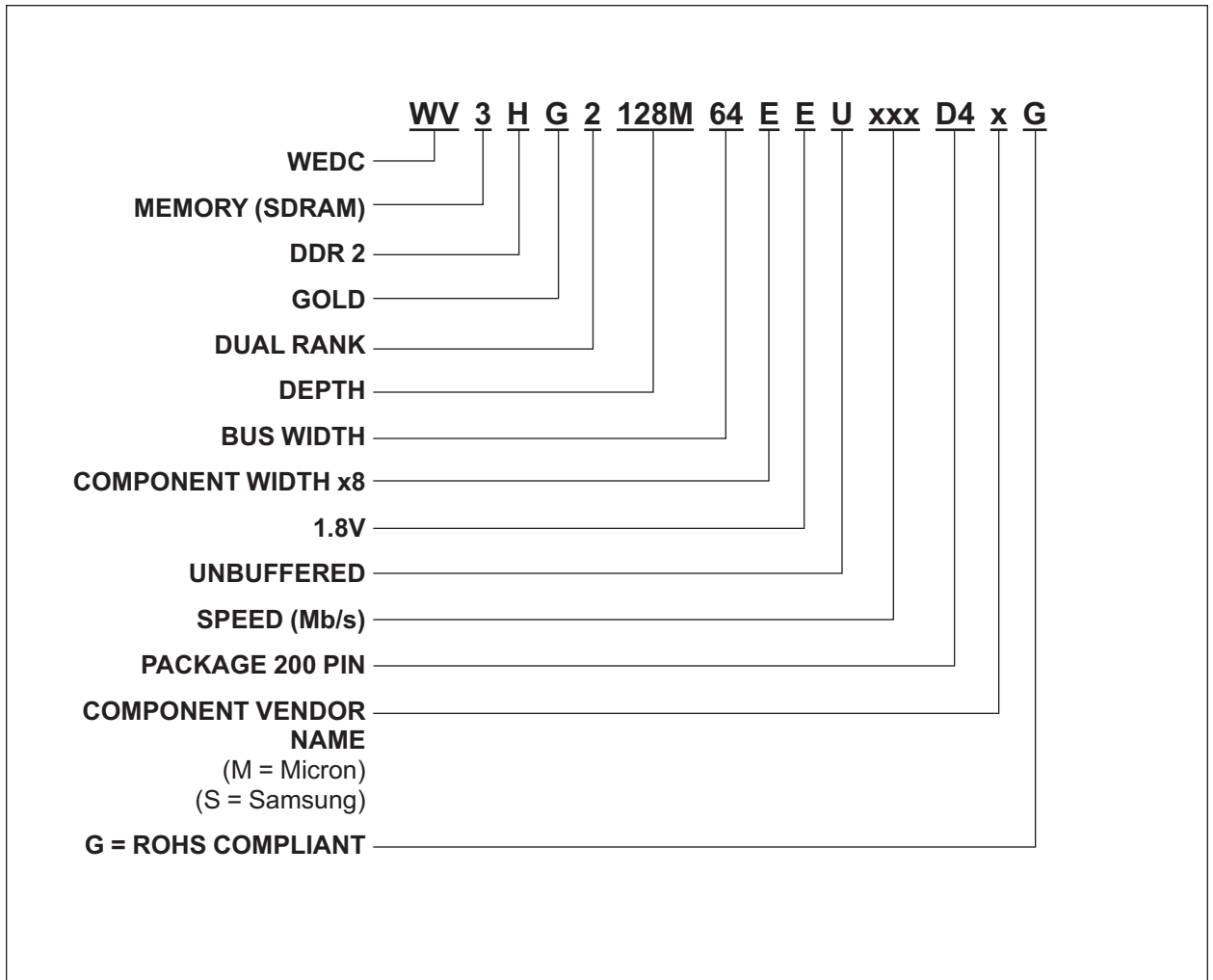
PACKAGE DIMENSIONS FOR D4



** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

2GB – 2x128Mx64 DDR2 SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	February 2006	Advanced