# 512MB – 64Mx64 DDR SDRAM UNBUFFERED

## FEATURES

- Double-data-rate architecture
- PC2700 @ CL 2.5
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input.
- Auto and self refresh, (8K/64ms refresh)
- Serial presence detect with EEPROM
- Power supply:
  - $V_{CC} = V_{CCQ} = +2.5V \pm 0.2V$
- 184 pin DIMM package
  - D3 PCB height: 28.58mm (1.125")

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

## DESCRIPTION

The WV3EG64M64ETSU is a 64Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM components. The module consists of eight 64Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change without notice.

### OPERATING FREQUENCIES

| | DDR333 @CL=2.5 |
|---|---|
| Clock Speed | 166MHz |
| CL-$t_{RCD}$-$t_{RP}$ | 2.5-3-3 |

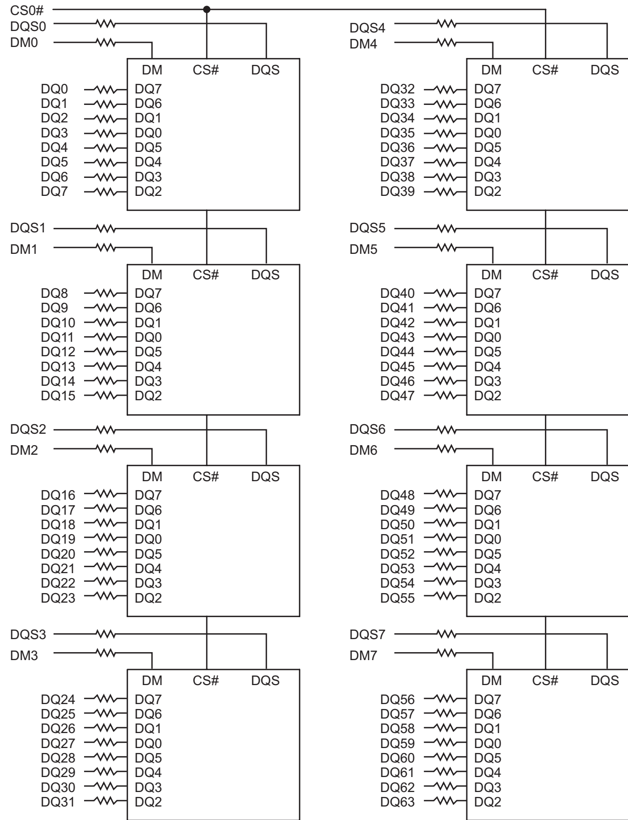
## PIN CONFIGURATION

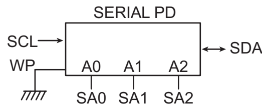
| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|---|---|---|---|---|---|---|---|
| 1 | $V_{REF}$ | 47 | NC | 93 | $V_{SS}$ | 139 | $V_{SS}$ |
| 2 | DQ0 | 48 | A0 | 94 | DQ4 | 140 | NC |
| 3 | $V_{SS}$ | 49 | NC | 95 | DQ5 | 141 | A10 |
| 4 | DQ1 | 50 | $V_{SS}$ | 96 | $V_{CCQ}$ | 142 | NC |
| 5 | DQS0 | 51 | NC | 97 | DM0 | 143 | $V_{CCQ}$ |
| 6 | DQ2 | 52 | BA1 | 98 | DQ6 | 144 | NC |
| 7 | $V_{CC}$ | 53 | DQ32 | 99 | DQ7 | 145 | $V_{SS}$ |
| 8 | DQ3 | 54 | $V_{CCQ}$ | 100 | $V_{SS}$ | 146 | DQ36 |
| 9 | NC | 55 | DQ33 | 101 | NC | 147 | DQ37 |
| 10 | NC | 56 | DQS4 | 102 | NC | 148 | $V_{CC}$ |
| 11 | $V_{SS}$ | 57 | DQ34 | 103 | NC | 149 | DM4 |
| 12 | DQ8 | 58 | $V_{SS}$ | 104 | $V_{CCQ}$ | 150 | DQ38 |
| 13 | DQ9 | 59 | BA0 | 105 | DQ12 | 151 | DQ39 |
| 14 | DQS1 | 60 | DQ35 | 106 | DQ13 | 152 | $V_{SS}$ |
| 15 | $V_{CCQ}$ | 61 | DQ40 | 107 | DM1 | 153 | DQ44 |
| 16 | CK1 | 62 | $V_{CCQ}$ | 108 | $V_{CC}$ | 154 | RAS# |
| 17 | CK1# | 63 | WE# | 109 | DQ14 | 155 | DQ45 |
| 18 | $V_{SS}$ | 64 | DQ41 | 110 | DQ15 | 156 | $V_{CCQ}$ |
| 19 | DQ10 | 65 | CAS# | 111 | NC | 157 | CS0# |
| 20 | DQ11 | 66 | $V_{SS}$ | 112 | $V_{CCQ}$ | 158 | NC |
| 21 | CKE0 | 67 | DQS5 | 113 | NC | 159 | DM5 |
| 22 | $V_{CCQ}$ | 68 | DQ42 | 114 | DQ20 | 160 | $V_{SS}$ |
| 23 | DQ16 | 69 | DQ43 | 115 | A12 | 161 | DQ46 |
| 24 | DQ17 | 70 | $V_{CC}$ | 116 | $V_{SS}$ | 162 | DQ47 |
| 25 | DQS2 | 71 | NC | 117 | DQ21 | 163 | NC |
| 26 | $V_{SS}$ | 72 | DQ48 | 118 | A11 | 164 | $V_{CCQ}$ |
| 27 | A9 | 73 | DQ49 | 119 | DM2 | 165 | DQ52 |
| 28 | DQ18 | 74 | $V_{SS}$ | 120 | $V_{CC}$ | 166 | DQ53 |
| 29 | A7 | 75 | CK2# | 121 | DQ22 | 167 | NC |
| 30 | $V_{CCQ}$ | 76 | CK2 | 122 | A8 | 168 | $V_{CC}$ |
| 31 | DQ19 | 77 | $V_{CCQ}$ | 123 | DQ23 | 169 | DM6 |
| 32 | A5 | 78 | DQS6 | 124 | $V_{SS}$ | 170 | DQ54 |
| 33 | DQ24 | 79 | DQ50 | 125 | A6 | 171 | DQ55 |
| 34 | $V_{SS}$ | 80 | DQ51 | 126 | DQ28 | 172 | $V_{CCQ}$ |
| 35 | DQ25 | 81 | $V_{SS}$ | 127 | DQ29 | 173 | NC |
| 36 | DQS3 | 82 | $V_{CCID}$ | 128 | $V_{CCQ}$ | 174 | DQ60 |
| 37 | A4 | 83 | DQ56 | 129 | DM3 | 175 | DQ61 |
| 38 | $V_{CC}$ | 84 | DQ57 | 130 | A3 | 176 | $V_{SS}$ |
| 39 | DQ26 | 85 | $V_{CC}$ | 131 | DQ30 | 177 | DM7 |
| 40 | DQ27 | 86 | DQS7 | 132 | $V_{SS}$ | 178 | DQ62 |
| 41 | A2 | 87 | DQ58 | 133 | DQ31 | 179 | DQ63 |
| 42 | $V_{SS}$ | 88 | DQ59 | 134 | NC | 180 | $V_{CCQ}$ |
| 43 | A1 | 89 | $V_{SS}$ | 135 | NC | 181 | SA0 |
| 44 | NC | 90 | NC | 136 | $V_{CCQ}$ | 182 | SA1 |
| 45 | NC | 91 | SDA | 137 | CK0 | 183 | SA2 |
| 46 | $V_{CC}$ | 92 | SCL | 138 | CK0# | 184 | $V_{CCSPD}$ |

## PIN NAMES

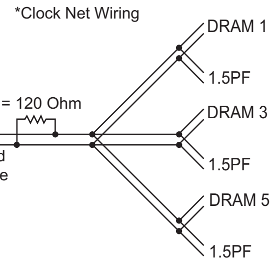
| | |
|---|---|
| A0-A12 | Address input (Multiplexed) |
| BA0-BA1 | Bank Select Address |
| DQ0-DQ63 | Data Input/Output |
| DQS0-DQS7 | Data Strobe Input/Output |
| CK0, CK1, CK2 | Clock Input |
| CK0#, CK1#, CK2# | Clock Input |
| CKE0 | Clock Enable input |
| CS0# | Chip Select Input |
| RAS# | Row Address Strobe |
| CAS# | Column Address Strobe |
| WE# | Write Enable |
| DM0-DM7 | Data-in-mask |
| $V_{CC}$ | Power Supply |
| $V_{CCQ}$ | Power Supply for DQS |
| $V_{SS}$ | Ground |
| $V_{REF}$ | Power Supply for Reference |
| $V_{CCSPD}$ | Serial EEPROM Power Supply |
| SDA | Serial data I/O |
| SCL | Serial clock |
| SA0-SA2 | Address in EEPROM |
| $V_{CCID}$ | $V_{CC}$ Indentification Flag |
| NC | No Connect |

## FUNCTIONAL BLOCK DIAGRAM

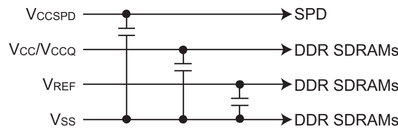



| Clock Wiring | |
|---|---|
| Clock Input | DDR SDRAMs |
| CK0, CK0#<br>CK1, CK1#<br>CK2, CK2# | 2 DDR SDRAMs<br>3 DDR SDRAMs<br>3 DDR SDRAMs |




| | | |
|---|---|---|
| BA0-BA1 | → | BA0-BA1: DDR SDRAMs |
| A0-A12 | → | A0-A12: DDR SDRAMs |
| RAS# | → | RAS#: DDR SDRAMs |
| CAS# | → | CAS#: DDR SDRAMs |
| CKE0 | → | CKE: DDR SDRAMs |
| WE# | → | WE#: DDR SDRAMs |




NOTE: All datalines are terminated through a 22 ohm series resistor.

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS# relationships must be maintained as shown.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.5 to 3.6 | V |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$ | -1.0 to 3.6 | V |
| Voltage on $V_{CCQ}$ supply relative to $V_{SS}$ | $V_{CCQ}$ | -1.0 to 3.6 | V |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |
| Operating Temperature | $T_A$ | 0 to +70 | °C |
| Power Dissipation | $P_D$ | 8 | W |
| Short Circuit Current | $I_{OS}$ | 50 | mA |

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

## DC CHARACTERISTICS

0°C ≤ $T_A$ ≤ 70°C, $V_{CC}$ = $V_{CCQ}$ = 2.5V ± 0.2V

| Parameter | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage DDR266/DDR333 (nominal $V_{CC}$ of 2.5V) | | $V_{CC}$ | 2.3 | 2.7 | | |
| I/O Supply voltage DDR266/DDR333 (nominal $V_{CC}$ of 2.5V) | | $V_{CCQ}$ | 2.3 | 2.7 | V | |
| I/O Reference voltage | | $V_{REF}$ | 0.49*$V_{CCQ}$ | 0.51*$V_{CCQ}$ | V | 1 |
| I/O Termination voltage | | $V_{TT}$ | $V_{REF}$-0.04 | $V_{REF}$+0.04 | V | 2 |
| Input logic high voltage | | $V_{IH}$(DC) | $V_{REF}$+0.15 | $V_{CCQ}$+0.30 | V | |
| Input logic low voltage | | $V_{IL}$(DC) | -0.3 | $V_{REF}$-0.15 | V | |
| Input voltage level, CK and CK# | | $V_{IN}$(DC) | -0.3 | $V_{CCQ}$+0.30 | V | |
| Input differential voltage, CK and CK# | | $V_{ID}$(DC) | 0.36 | $V_{CCQ}$+0.60 | V | 3 |
| Input crossing point voltage, CK and CK# | | $V_{IX}$(DC) | 0.3 | $V_{CCQ}$+0.60 | V | |
| Input leakage current | Addr, CAS#, RAS#, WE# | $I_I$ | -16 | 16 | uA | |
| | CS#, CKE | | -16 | 16 | uA | |
| | CK, CK# | | -6 | 6 | uA | |
| | DM | | -2 | 2 | uA | |
| Output leakage current | | $I_{OZ}$ | -5 | 5 | uA | |
| Output high current (normal strengh); $V_{OUT}$ = V +0.84V | | $I_{OH}$ | -16.8 | — | mA | |
| Output high current (normal strengh); $V_{OUT}$ = $V_{TT}$ -0.84V | | $I_{OL}$ | 16.8 | — | mA | |
| Output high current (half strengh); $V_{OUT}$ = $V_{TT}$ +0.45V | | $I_{OH}$ | -9 | — | mA | |
| Output high current (half strengh); $V_{OUT}$ = $V_{TT}$ -0.45V | | $I_{OL}$ | 9 | — | mA | |

NOTES:

1. $V_{REF}$ is expected to be equal to 0.5*$V_{CCQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on $V_{REF}$ may not exceed ±2% of the DC value
2. $V_{TT}$ is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors, is expected to be set equal to $V_{REF}$, and must track variations in the DC level of $V_{REF}$
3. $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on CK#.

## CAPACITANCE

$T_A$ = 25°C, f = 1MHz, $V_{CC}$ = $V_{CCQ}$ = 2.5V

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Capacitance (A0-A12, BA0-BA1, RAS#, CAS#, WE#) | $C_{IN1}$ | 20 | 28 | pF |
| Input Capacitance (CKE0) | $C_{IN2}$ | 20 | 28 | pF |
| Input Capacitance (CS0#) | $C_{IN3}$ | 20 | 28 | pF |
| Input Capacitance (CK0 to CK2, CK0# to CK2#) | $C_{IN4}$ | 10 | 13 | pF |
| Input Capacitance (DM0-DM7) | $C_{IN5}$ | 8 | 9 | pF |
| Data and DQS input/output capacitance (DQ0-DQ63) | $C_{OUT1}$ | 8 | 9 | pF |

## $I_{DD}$ SPECIFICATIONS AND TEST CONDITIONS

0°C ≤ $T_A$ ≤ 70°C, $V_{CC}$ = $V_{CCQ}$ = 2.5V ± 0.2V
Includes DDR SDRAM component only

| Parameter | Symbol | Conditions | DDR333 @ CL = 2.5 | Unit |
|---|---|---|---|---|
| Operating current | $I_{DD0}$* | One device bank active; Active-Precharge; $t_{RC}$ = $t_{RC(MIN)}$; $t_{CK}$ = $t_{CK(MIN)}$; DQ, DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles | 1000 | mA |
| Operating current | $I_{DD1}$* | One device bank; Active-Read-Precharge; BL = 4; $t_{RC}$ = $t_{RC(MIN)}$; $t_{CK}$ = $t_{CK(MIN)}$; $I_{OUT}$ = 0mA; Address and control inputs change once per clock cycle | 1200 | mA |
| Percharge power-down standby current | $I_{DD2P}$** | All device banks are idle; Power-down mode; $t_{CK}$ = $t_{CK(MIN)}$; CKE = LOW | 40 | mA |
| Idle standby current | $I_{DD2F}$** | CS# = HIGH; All device banks are idle; $t_{CK}$ = $t_{CK(MIN)}$; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN}$ = $V_{REF}$ for DQ, DQS and DM | 240 | mA |
| Active power-down standby current | $I_{DD3P}$** | One device bank active; Power-down mode; $t_{CK}$ = $t_{CK(MIN)}$; CKE = LOW | 240 | mA |
| Active standby current | $I_{DD3N}$** | CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC}$ = $t_{RAS(MAX)}$; $t_{CK}$ = $t_{CK(MIN)}$; DQ, DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle | 400 | mA |
| Operating current | $I_{DD4R}$* | Burst = 2; Reads; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; $t_{CK}$ = $t_{CK(MIN)}$; $I_{OUT}$ = 0mA | 1440 | mA |
| Operating current | $I_{DD4W}$* | Burst = 2; Writes; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; $t_{CK}$ = $t_{CK(MIN)}$; DQ, DM and DQS inputs change twice per clock cycle | 1480 | mA |
| Auto refresh current | $I_{DD5}$** | $t_{RC}$ = $t_{RFC(MIN)}$ | 2000 | mA |
| Self refresh current | $I_{DD6}$** | CKE < 0.2V | 40 | mA |
| Orerating current | $I_{DD7}$* | Four device bank interleaving Reads Burst = 4 with auto precharge; $t_{RC}$ = $t_{RFC(MIN)}$; $t_{CK}$ = $t_{CK(MIN)}$; Address and control inputs change only during Active READ, or WRITE commands | 3120 | mA |

Note: These specifications apply to modules built with Samsung components only.
* Value calculated as one module rank in this operation condition and other module rank in $I_{DD2P}$ (CKE low) mode.
** Value calculated as all module ranks in this operation condition.

## DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

| Parameter | | Symbol | 335 | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Row cycle time | | $t_{RC}$ | 60 | | ns |
| Refresh row cycle time | | $t_{RFC}$ | 72 | | ns |
| Row active time | | $t_{RAS}$ | 42 | 70K | ns |
| RAS to CAS delay | | $t_{RCD}$ | 18 | | ns |
| Row precharge time | | $t_{RP}$ | 18 | | ns |
| Row active to Row active delay | | $t_{RRD}$ | 12 | | ns |
| Write recovery time | | $t_{WR}$ | 15 | | ns |
| Last data into Read command | | $t_{WTR}$ | 1 | | $t_{CK}$ |
| Clock cycle time | CL = 2.5 | $t_{CK}$ | 6 | 12 | ns |
| Clock high level width | | $t_{CH}$ | 0.45 | 0.55 | $t_{CK}$ |
| Clock low level width | | $t_{CL}$ | 0.45 | 0.55 | $t_{CK}$ |
| DQS-out access time from CK/CK | | $t_{DQSCK}$ | -0.6 | +0.6 | ns |
| Output data access time from CK/CK | | $t_{AC}$ | -0.7 | +0.7 | ns |
| Data strobe edge to ouput data edge | | $t_{DQSQ}$ | — | 0.45 | ns |
| Read Preamble | | $t_{RPRE}$ | 0.9 | 1.1 | $t_{CK}$ |
| Read Postamble | | $t_{RPST}$ | 0.4 | 0.6 | $t_{CK}$ |
| CK to valid DQS-in | | $t_{DQSS}$ | 0.75 | 1.25 | $t_{CK}$ |
| DQS-in setup time | | $t_{WPRES}$ | 0 | | ns |
| DQS-in hold time | | $t_{WPRE}$ | 0.25 | | $t_{CK}$ |
| DQS falling edge to CK rising-setup time | | $t_{DSS}$ | 0.2 | | $t_{CK}$ |
| DQS falling edge from CK rising-hold time | | $t_{DSH}$ | 0.2 | | $t_{CK}$ |
| DQS-in high level width | | $t_{DQSH}$ | 0.35 | | $t_{CK}$ |
| DQS-in low level width | | $t_{DQSL}$ | 0.35 | | $t_{CK}$ |
| Address and Control Input setup time (fast) | | $t_{IS}$ | 0.75 | | ns |
| Address and Control Input hold time (fast) | | $t_{IH}$ | 0.75 | | ns |
| Address and Control Input setup time (slow) | | $t_{ISF}$ | 0.8 | | ns |
| Address and Control Input hold time (slow) | | $t_{IHF}$ | 0.8 | | ns |
| Data-out high impedence time from CK/CK | | $t_{HZS}$ | -0.7 | +0.7 | ns |
| Data-out low impedence time from CK/CK | | $t_{LZS}$ | -0.7 | +0.7 | ns |
| Output Slew Rate Matching Ratio (rise to fall) | | $t_{SLMR}$ | 0.67 | 1.5 | |

Note: These specifications apply to modules built with Samsung components only.

## DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (continued)

| Parameter | Symbol | 335 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Mode register set cycle time | $t_{MRD}$ | 12 | | ns |
| DQ & DM setup time to DQS | $t_{DS}$ | 0.45 | | ns |
| DQ & DM hold time to DQS | $t_{DH}$ | 0.45 | | ns |
| Control & Address input pulse width | $t_{IPW}$ | 2.2 | | ns |
| DQ & DM input pulse width | $t_{DIPW}$ | 1.75 | | ns |
| Exit self refresh to non-Read command | $t_{XSNR}$ | 75 | | ns |
| Exit self refresh to read command | $t_{XSRD}$ | 200 | | $t_{CK}$ |
| Refresh interval time | $t_{REFI}$ | | 7.8 | us |
| Output DQS valid window | $t_{QH}$ | $t_{HP}$-$t_{QHS}$ | — | ns |
| Clock half period | $t_{HP}$ | $t_{CLmin}$ or $t_{CHmin}$ | — | ns |
| Data hold skew factor | $t_{QHS}$ | | 0.55 | ns |
| DQS write postamble time | $t_{WPST}$ | 0.4 | 0.6 | ns |
| Active to Read with Auto precharge command | $t_{RAP}$ | 18 | | |
| Autoprecharge write recovery + Precharge time | $t_{DAL}$ | ($t_{WR}$/$t_{CK}$) + ($t_{RP}$/$t_{CK}$) | | $t_{CK}$ |

## AC OPERATING TEST CONDITIONS

$V_{CC}$ = 2.5V, $V_{CCQ}$ = 2.5V, 0°C ≤ $T_A$ ≤ 70°C

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | $V_{IH(AC)}$ | $V_{REF}$ +0.31 | | V | 1 |
| Input Low (Logic 0) Voltage | $V_{IL(AC)}$ | | $V_{REF}$ -0.31 | V | 1 |
| Input Differential Voltage, CK and CK# inputs | $V_{ID(AC)}$ | 0.7 | $V_{CCQ}$+0.6 | V | |
| Input Crossing Point Voltage, CK and CK# inputs | $V_{IX(AC)}$ | 0.5*$V_{CCQ}$-0.2 | 0.5*$V_{CCQ}$+0.2 | V | |

NOTES:

1. $V_{IH}$ overshoot: $V_{IH}$ = $V_{CCQ}$ +1.5V for a pulse width < 3ns and the pulse can not be greater than 1/3 of the cycle rate.
   $V_{IL}$ undershoot: $V_{IL}$ = -1.5V for a pulse width < 3ns and the pulse can not be greater than 1/3 of the cycle rate.

## ORDERING INFORMATION FOR D3

| Part Number | Speed | CAS Latency | $t_{RCD}$ | $t_{RP}$ | Height* | Temperature |
|---|---|---|---|---|---|---|
| WV3EG64M64ETSU335D3xG | 166MHz/333Mb/s | 2.5 | 3 | 3 | 28.58 (1.125") | 0°C to 70°C |

NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

## PACKAGE DIMENSIONS FOR D3

133.35 ±0.15
(5.25 ±0.006)
128.95
(5.077")
4.00
(0.158 (2x))
17.80
(0.70)
10.00
(0.393)
64.77
(2.550)
2.175
(0.085)
1.80
(0.071)
49.53
(1.95)
1.27 (0.050)
28.58 ±0.15
(1.125 ±0.006)
2.30
(0.10)
(2x)
3.00
(0.118)
(4x)
3.30
(0.130)
MAX
1.27 ±0.10
(0.050 ±0.004)

* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

## PART NUMBERING GUIDE

WV 3 E G 64M 64 E T S U xxx D3 x G

| Field | Meaning |
|---|---|
| WV | WEDC |
| 3 | MEMORY |
| E | DDR |
| G | GOLD |
| 64M | DEPTH |
| 64 | BUS WIDTH |
| E | x8 |
| T | TSOP |
| S | 2.5V |
| U | UNBUFFERED |
| xxx | SPEED (MHz) |
| D3 | PACKAGE 184 PIN |
| x | COMPONENT VENDOR NAME (M = Micron) (S = Samsung) |
| G | G = ROHS COMPLIANT |

## Document Title

512MB – 64Mx64 DDR SDRAM UNBUFFERED

## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev 0 | Created | 7-05 | Advanced |
| Rev 1 | 1.1 Update to DC, $I_{DD}$ and AC specifications<br>1.2 Changed from Advanced to Preliminary | 8-05 | Preliminary |