512K x 32 SSRAM / 1M x 64 SDRAM
EXTERNAL MEMORY SOLUTION FOR LUCENT'S LUCTAPC640 ATM PORT CONTROLLER

FEATURES

- Clock speeds:
  - SSRAM: 100 MHz
  - SDRAM: 100 MHz
- 100% tested to timing requirements of LUCTAPC640's memory interface
- Packaging:
  - 192 pin BGA, 21mm x 21mm
- 3.3V Operating supply voltage
- Direct control interface to both the CRAM and VCRAM ports on the LUCTAPC640
- 62% space savings vs. monolithic solution
- Reduced system inductance and capacitance

DESCRIPTION

The WED9LAPC2C16V8BC is a 3.3V, 512K x 32 Synchronous Pipeline SRAM and a 1M x 64 Synchronous DRAM array packaged in a 21mm x 21mm 192 lead BGA.

The WED9LAPC2C16V8BC provides the memory required for the CRAM (Control Memory) and VCRAM (Virtual Connection Memory) memory ports for Lucent's LUCTAPC640 ATM port controller. When used in conjunction with the WED9LAPC2B16P8BC, which provides memory for the BRAM (Buffer Memory) and PRAM (Pointer Memory) memory ports, the entire memory requirement of the LUCTAPC640 can be met using these 2 BGA devices.

The WED9LAPC2C16V8BC is 100% tested to the timing requirements of the LUCTAPC640's memory interface timing for both Commercial and Industrial temperature ranges.

PIN CONFIGURATION
PINOUT CRAM AND VCRAM MCM -- TOP VIEW

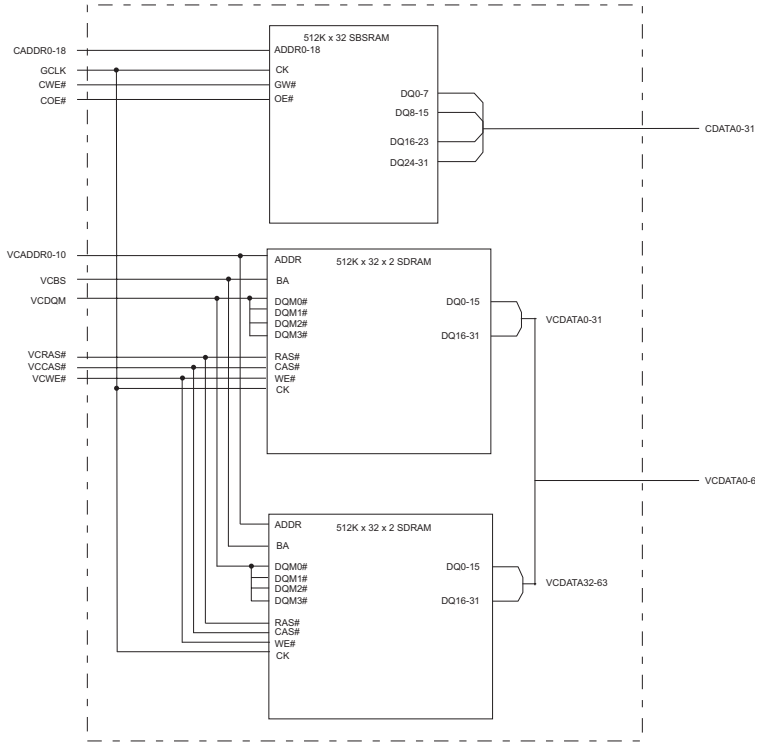
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	CADDR	CADDR	V_{CC}	CDATA	CDATA	V_{SS}	CDATA	CDATA	V_{CC}	CDATA	CDATA	V_{SS}	CDATA	CDATA	V_{CC}	CADDR
B	CWE#	CADDR	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CADDR	CADDR
C	COE#	CADDR	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CDATA	CADDR	CADDR
D	V_{SS}	CADDR	CADDR	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	CADDR	CADDR	CADDR
E	GCK	V_{SS}	NC	V_{CC}									V_{SS}	CADDR	CADDR	CADDR
F	V_{SS}	VCDATA_b	VCDATA_b	V_{CC}									V_{CC}	CADDR0	CADDR1	V_{SS}
G	VCDATA_b	VCDATA_b	VCDATA_b	V_{SS}									V_{CC}	VCDATA_a	VCDATA_a	VCDATA_a
H	VCDATA_b	VCDATA_b	VCDATA_b	V_{SS}									V_{SS}	VCDATA_a	VCDATA_a	VCDATA_a
J	V_{CC}	VCDATA_b	VCDATA_b	V_{SS}									V_{SS}	VCDATA_a	VCDATA_a	V_{CC}
K	VCDATA_b	VCDATA_b	VCDATA_b	V_{CC}									V_{SS}	VCDATA_a	VCDATA_a	VCDATA_a
L	VCDATA_b	VCDATA_b	VCDATA_b	V_{CC}									V_{CC}	VCDATA_a	VCDATA_a	VCDATA_a
M	V_{SS}	VCDATA_b	VCDATA_b	V_{CC}									V_{CC}	VCDATA_a	VCDATA_a	V_{SS}
N	VCDATA_b	VCDATA_b	VCDATA_b	V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{CC}	VCDATA_a	VCDATA_a
P	VCDATA_b	VCDATA_b	VCDATA_b	VCDATA_b	VCDATA_b	V_{SS}	VCADDR0	VCADDR2	VCADDR10	VCADDR6	V_{SS}	VCDATA_a	VCDATA_a	VCDATA_a	VCDATA_a	VCDATA_a
R	V_{CC}	VCDATA_b	VCDATA_b	VCDATA_b	VCBS	VCADDR8	VCADDR1	VCADDR3	VCADDR4	VCADDR7	VCDATA_a	VCDATA_a	VCDATA_a	VCDATA_a	VCDATA_a	V_{CC}
T	VCDATA_b	VCDATA_b	V_{SS}	VCDATA_b	VCDQM	VCCAS#	VCWE#	VCRAS#	VCADDR5	VCADDR9/AP	V_{CC}	VCDATA_a	VCDATA_a	V_{SS}	VCDATA_a	VCDATA_a

PIN CONFIGURATION (CONTINUED)

PIN DESCRIPTION

Symbol	Pin Name	Description
CADDR	CRAM Address	Address pins for the SSRAM that serves as the control RAM (CRAM)
CDATA	CRAM Data	Data I/O pins for the SSRAM control memory (CRAM)
CWE#	CRAM write enable	Write enable control for the SSRAM control memory (CRAM)
COE#	CRAM output enable	Output enable control pin for the SSRAM control memory (CRAM)
VCADDR	VCRAM address	Address pins for the SDRAM memory that serves as the virtual connection memory (VCRAM)
VCDATA	VCRAM data	Data I/O pins for the SDRAM virtual connection memory (VCRAM)
VCBS	VCRAM bank select	Bank address pin for the SDRAM virtual connection memory (VCRAM)
VCDQM	VCRAM DQM	DQM (data mask) pin for the SDRAM virtual conection memory (VCRAM)
VCRAS#	VCRAM row address strobe	RAS# pin for the SDRAM virtual connection memory (VCRAM)
VCCAS#	VCRAM column address strobe	CAS# pin for the SDRAM virtual connection memory (VCRAM)
VCWE#	VCRAM write enable	Write enable pin for the SDRAM virtual connection memory (VCRAM)
GCK	Global clock	Common clock pin for both the CRAM and VCRAM memory arrays
V_{CC}	Power supply	Power supply pins
V_{SS}	Ground	Ground Pins

FIG. 1 BLOCK DIAGRAM 512K X 32 SSRAM / 1M X 64



ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} Relative to V_{SS}	-0.5V to +4.6V
Vin (DQx)	-0.5V to Vcc +0.5V
Storage Temperature (BGA)	-55°C to +125°C
Junction Temperature	+125°C
Short Circuit Output Current	50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 5\%$ unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Supply Voltage (1)	V_{CC}	3.135	3.465	V
Input High Voltage (1,2)	V_{IH}	2.0	V_{CC} +0.3	V
Input Low Voltage (1,2)	V_{IL}	-0.3	0.8	V
Input Leakage Current 0 - V_{IN} - Vcc	I_{LI}	-10	10	µA
Output Leakage (Output Disabled) 0 - V_{IN} - Vcc	I_{LO}	-10	10	µA
CRAM Output High (I_{OH} = -4mA) (1)	V_{OH}	2.4	—	V
CRAM Output Low (I_{OL} = 8mA) (1)	V_{OL}	—	0.4	V
VCRAM Output High (I_{OH} = -2mA) (1)	V_{OH}	2.4	—	V
VCRAM Output Low (I_{OL} = 2mA) (1)	V_{OL}	—	0.4	V

NOTES:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC/2}$
   Undershoot: $V_{IL} \ge -2.0V$ for $t \le t_{KC/2}$

DC ELECTRICAL CHARACTERISTICS

Description	Conditions	Symbol	Typ	Max	Units
Operating Current	CRAM and VCRAM active	I_{CC1}	400	500	mA
Operating Current	CRAM active/VCRAM inactive	I_{CC2}	350	390	mA
Operating Current	CRAM inactive/VCRAM active	I_{CC3}	270	330	mA
Operating Current	CRAM inactive/VCRAM inactive	I_{CC4}	150	180	mA

BGA CAPACITANCE

Description	Conditions	Symbol	Typ	Max	Units
Address Input Capacitance[1]	T_A = 25°C; f = 1MHz	C_I	5	8	pF
Input/Output Capacitance (DQ)[1]	T_A = 25°C; f = 1MHz	C_O	8	10	pF
Control Input Capacitance[1]	T_A = 25°C; f = 1MHz	C_A	5	8	pF
Clock Input Capacitance[1]	T_A = 25°C; f = 1MHz	C_{CK}	4	6	pF

NOTE:
1. This parameter is sampled.

SSRAM AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units
Clock Cycle Time	t_{KHKH}	7.5		ns
Clock HIGH Time	t_{KLKH}	3.0		ns
Clock LOW Time	t_{KHKL}	3.0		ns
Clock to output valid	t_{KHQV}		4.2	ns
Clock to output invalid	t_{KHQX}	1.5		ns
Clock to output in Low-Z	t_{KQLZ}	1.5		ns
Clock to output in High-Z	t_{KQHZ}	1.5	3.5	ns
Output Enable to output valid	t_{OELQV}		4.2	ns
Output Enable to output in Low-Z	t_{OELZ}	0		ns
Output Enable to output in High-Z	t_{OEHZ}		3.5	ns
Address, Control, Data-in Setup Time to Clock	t_S	1.5		ns
Address, Control, Data-in Hold Time to Clock	t_H	0.5		ns

SSRAM OPERATION TRUTH TABLE

Operation	Address Used	CWE#	COE#	CDATA
WRITE Cycle, Begin Burst	External	L	X	D
READ Cycle, Begin Burst	External	H	L	Q
READ Cycle, Begin Burst	External	H	H	High-Z

NOTE:
1. X means “don’t care”, H means logic HIGH. L means logic LOW.
2. All inputs except SSOE# must meet setup and hold times around the rising edge (LOW to HIGH) of SSCLK.
3. For a write operation following a read operation, SSOE# must be HIGH before the input data required setup time plus High-Z time for SSOE# and staying HIGH thoughout the input data hold time.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

FIG. 2 SSRAM READ TIMING

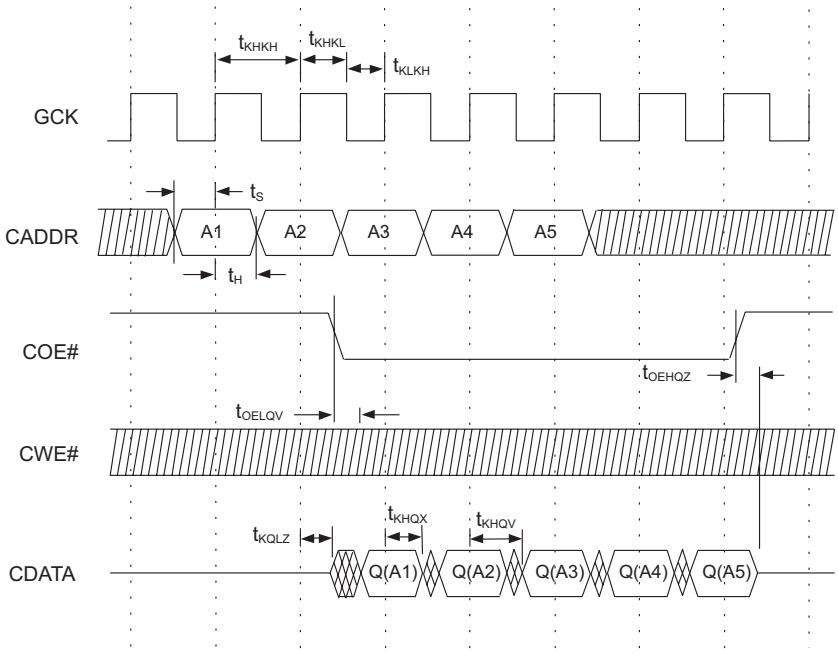
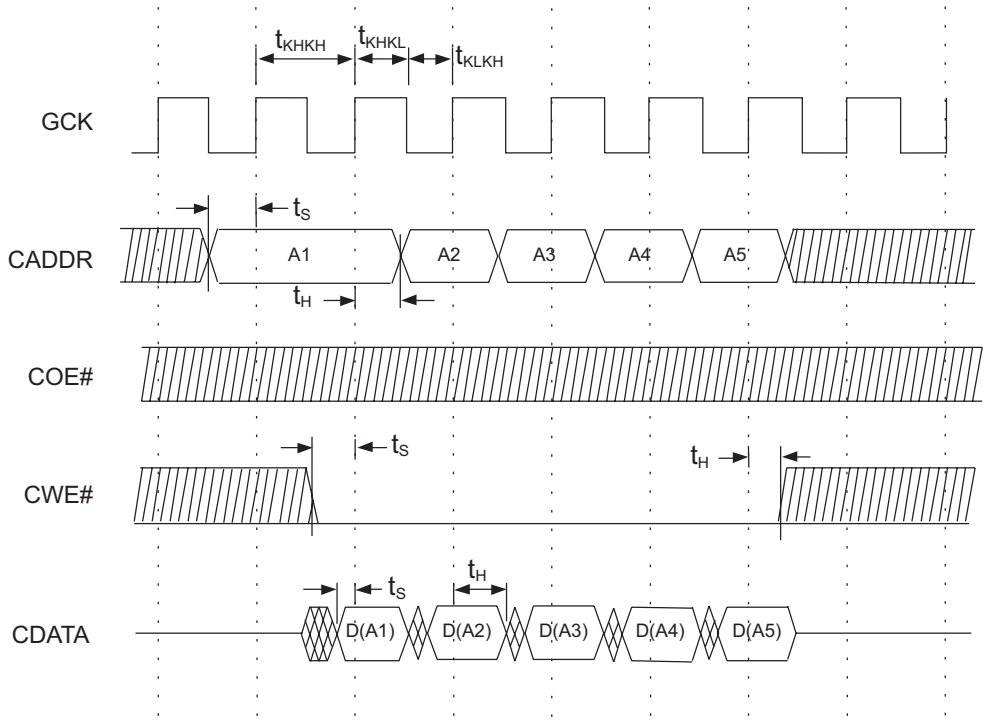


FIG. 3 SSRAM WRITE TIMING



SDRAM AC CHARACTERISTICS

Parameter		Symbol	Min	Max	Units
Clock Cycle Time[1]	CL = 3	t_{CC}	8	1000	ns
	CL = 2	t_{CC}	10	1000	ns
Clock to valid Output delay[1,2]		t_{SAC}		6	ns
Output Data Hold Time[2]		t_{OH}	2.5		ns
Clock HIGH Pulse Width[3]		t_{CH}	3		ns
Clock LOW Pulse Width[3]		t_{CL}	3		ns
Input Setup Time[3]		t_{SS}	2		ns
Input Hold Time[3]		t_{SH}	1		ns
CK to Output Low-Z[2]		t_{SLZ}	1		ns
CK to Output High-Z		t_{SHZ}		6	ns
Row Active to Row Active Delay[4]		t_{RRD}	16		ns
RAS# to CAS# Delay[4]		t_{RCD}	20		ns
Row Precharge Time[4]		t_{RP}	20		ns
Row Active Time[4]		t_{RAS}	48	10,000	ns
Row Cycle Time - Operation[4]		t_{RC}	70		ns
Row Cycle Time - Auto Refresh[4,8]		t_{RFC}	70		ns
Last Data in to New Column Address Delay[5]		t_{CDL}	1		CK
Last Data in to Row Precharge[5]		t_{RDL}	2		CK
Last Data in to Burst Stop[5]		t_{BDL}	1		CK
Column Address to Column Address Delay[6]		t_{CCD}	1		CK
Number of Valid Output Data[7]				2	ea
				1	ea

NOTES:
1. Parameters depend on programmed CAS latency.
2. If clock rise time is longer than 1ns (t_{RISE}/2 -0.5)ns should be added to the parameter.
3. Assumed input rise and fall time = 1ns. If trise of t_{FALL} are longer than 1ns. [(t_{RISE} = t_{FALL})/2] - 1ns should be added to the parameter.
4. The minimum number of clock cycles required is detemined by dividing the minimum time required by the clock cycle time and then rounding up to the next higher integer.
5. Minimum delay is required to complete write.
6. All devices allow every cycle column address changes.
7. In case of row precharge interrupt, auto precharge and read burst stop.
8. A new command may be given t_{RFC} after self-refresh exit.

CLOCK FREQUENCY AND LATENCY PARAMETERS

(Unit = number of clock)

Cycle Time	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	10ns	10ns	10ns
8.0ns	3	9	6	3	2	3	1	1	2
10.0ns	2	7	5	2	2	2	1	1	2

REFRESH CYCLE PARAMETERS

Parameter	Symbol	Min	Max	Units
Refresh Period[1,2]	t_{REF}	—	64	ms

NOTES:
1. 1024 cycles
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.

SDRAM COMMAND TRUTH TABLE

FUNCTION		VCRAS#	VCCAS#	VCWE#	VCDQM#	VCBS	VCADDR	NOTES
Mode Register Set		L	L	L	X	OP CODE		
Auto Refresh (CBR)		L	L	H	X	X	X	
Precharge	Single Bank	L	H	L	X	BA	L	2
	Precharge all Banks	L	H	L	X	X	H	
Bank Activate		L	H	H	X	BA	Row Address	2
Write		H	L	L	X	BA	L	2
Write with Auto Precharge		H	L	L	X	BA	H	2
Read		H	L	L	X	BA	L	2
Read with Auto Precharge		H	L	H	X	BA	H	2
Burst Termination		H	H	L	X	X	X	3
No Operation		H	H	H	X	X	X	
Data Write/Output Disable		X	X	X	L	X	X	4
Data Mask/Output Disable		X	X	X	H	X	X	4

NOTES:

1. All of the SDRAM operations are defined by states of VCWE#, VCRAS#, VCCAS#, and VCDQM# at the positive rising edge of the clock.
2. Bank Select (VCBS), if VCBS = 0 then bank A is selected, if VCBS = 1 then bank B is selected.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS latency.
4. The VCDQM# has two functions for the data DQ Read and Write operations. During a Read cycle, when VCDQM# goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. VCDQM# also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).

SDRAM CURRENT STATE TRUTH TABLE

Current State	Command						Action	Notes
	VCRAS#	VCCAS#	VCWE#	VCBS	VCADDR	Description		
Idle	L	L	L	OP Code		Mode Register Set	Set the Mode Register	1
	L	L	H	X	X	Auto or Self Refresh	Start Auto	1
	L	H	L	X	X	Precharge	No Operation	
	L	H	H	BA	Row Address	Bank Activate	Activate the specified bank and row	
	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	1
	H	H	L	X	X	Burst Termination	No Operation	1
	H	H	H	X	X	No Operation	No Operation	
Row Active	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	Precharge	3
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	1
	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	4,5
	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	4,5
	H	H	L	X	X	Burst Termination	No Operation	
	H	H	H	X	X	No Operation	No Operation	
Read	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	Terminate Burst; Start the Write cycle	5,6
	H	L	H	BA	Column	Read	Terminate Burst; Start a new Read cycle	5,6
	H	H	L	X	X	Burst Termination	Terminate the Burst	
	H	H	H	X	X	No Operation	Continue the Burst	
Write	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	Terminate Burst; Start a new Write cycle	5,6
	H	L	H	BA	Column	Read	Terminate Burst; Start the Read cycle	5,6
	H	H	L	X	X	Burst Termination	Terminate the Burst	
	H	H	H	X	X	No Operation	Continue the Burst	
Read with Auto Precharge	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	ILLEGAL	
	H	L	H	BA	Column	Read	ILLEGAL	
	H	H	L	X	X	Burst Termination	ILLEGAL	
	H	H	H	X	X	No Operation	Continue the Burst	

SDRAM CURRENT STATE TRUTH TABLE (CONT.)

Current State	Command						Action	Notes
	VCRAS#	VCCAS#	VCWE#	VCBS	VCADDR	Description		
Write with Auto Precharge	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	ILLEGAL	
	H	L	H	BA	Column	Read	ILLEGAL	
	H	H	L	X	X	Burst Termination	ILLEGAL	
	H	H	H	X	X	No Operation	Continue the Burst	
Precharging	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	No Operation; Bank(s) idle after t_{RP}	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	20
	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RP}	
	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}	
Row Activating	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	ILLEGAL	2
	H	L	H	BA	Column	Read	ILLEGAL	2
	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{RCD}	
	H	H	H	X	X	No Operation	No Operation; Row active after t_{RCD}	
Write Recovering	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	6
	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	6
	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{DPL}	
	H	H	H	X	X	No Operation	No Operation; Row active after t_{DPL}	
Write Recovering with Auto Precharge	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	ILLEGAL	2,6
	H	L	H	BA	Column	Read	ILLEGAL	2,6
	H	H	L	X	X	Burst Termination	No Operation; Precharge after t_{DPL}	
	H	H	H	X	X	No Operation	No Operation; Precharge after t_{DPL}	

SDRAM CURRENT STATE TRUTH TABLE (CONT.)

Current State	Command						Action	Notes
	VCRAS#	VCCAS#	VCWE#	VCBS	VCADDR	Description		
Refreshing	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	H	L	L	BA	Column	Write	ILLEGAL	
	H	L	H	BA	Column	Read	ILLEGAL	
	H	H	L	X	X	Burst Termination	No Operation; Idle after t_{RC}	
	H	H	H	X	X	No Operation	No Operation; Idle after t_{RC}	
Mode Register Accessing	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	H	L	L	BA	Column	Write	ILLEGAL	
	H	L	H	BA	Column	Read	ILLEGAL	
	H	H	L	X	X	Burst Termination	ILLEGAL	
	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	

Notes:

1. Both Banks must be idle otherwise it is an illegal action.
2. The Current State refers only refers to one of the banks, if VCBS selects this bank then the action is illegal. If VCBS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
3. The minimum and maximum Active time (t_{RAS}) must be satisfied.
4. The VCRAS# to VCCAS# Delay (t_{RCD}) must occur before the command is given.
5. Address VCADDR9/AP is used to determine if the Auto Precharge function is activated.
6. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements. The command is illegal if the minimum bank-to-bank delay time (t_{RRD}) is not satisfied.

FIG. 4 SDRAM SINGLE BIT READ-WRITE-READ CYCLE (SAME PAGE) @CAS LATENCY = 3, BURST LENGTH = 1

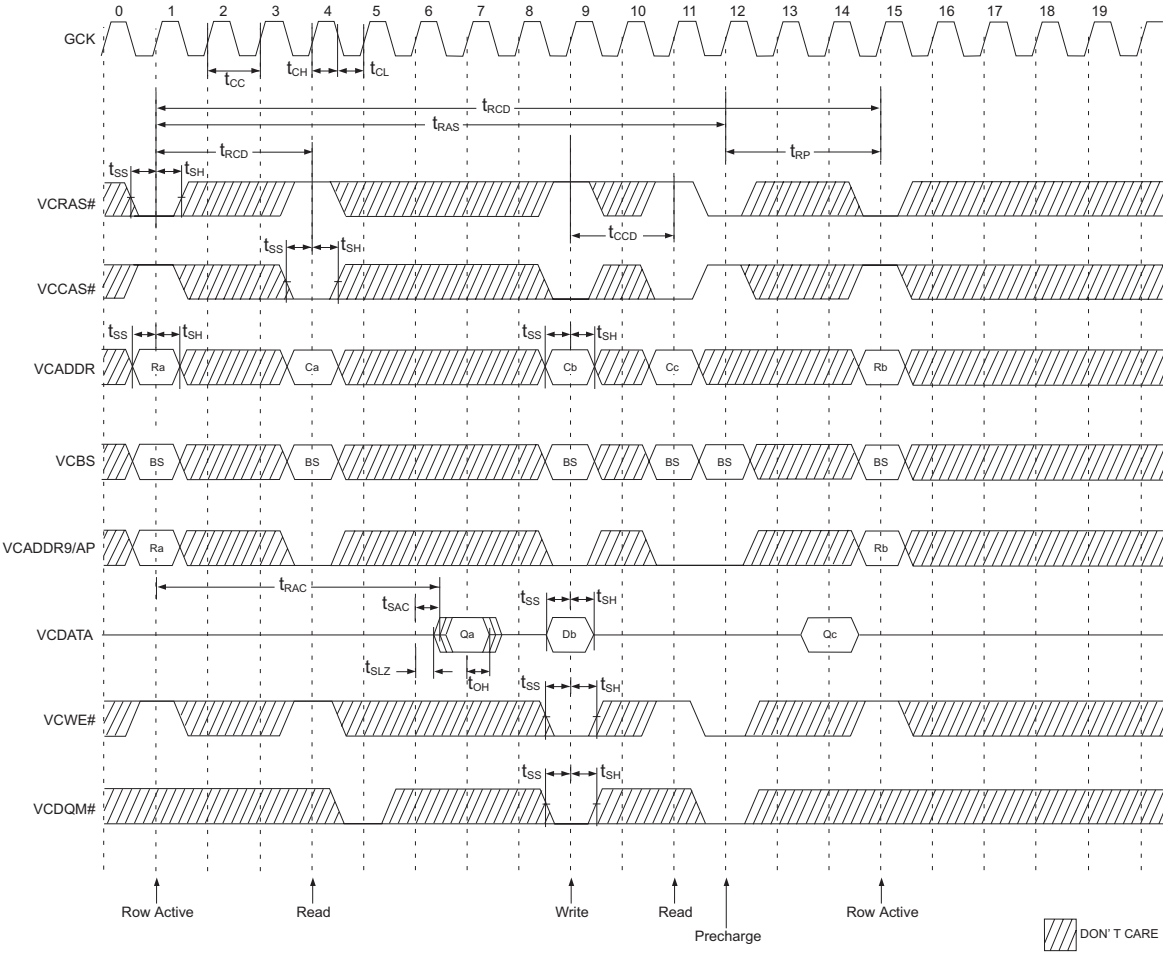


FIG. 5 SDRAM POWER UP SEQUENCE

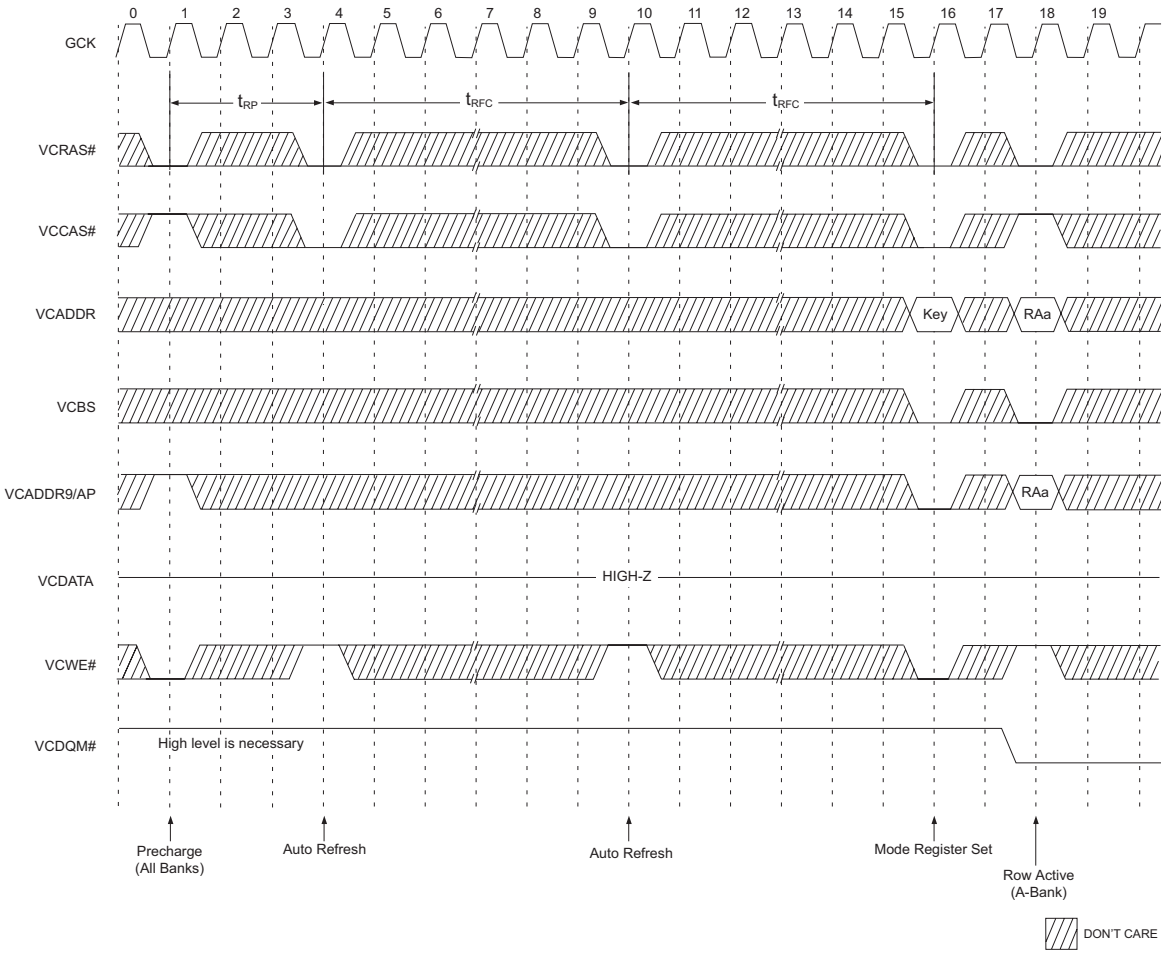
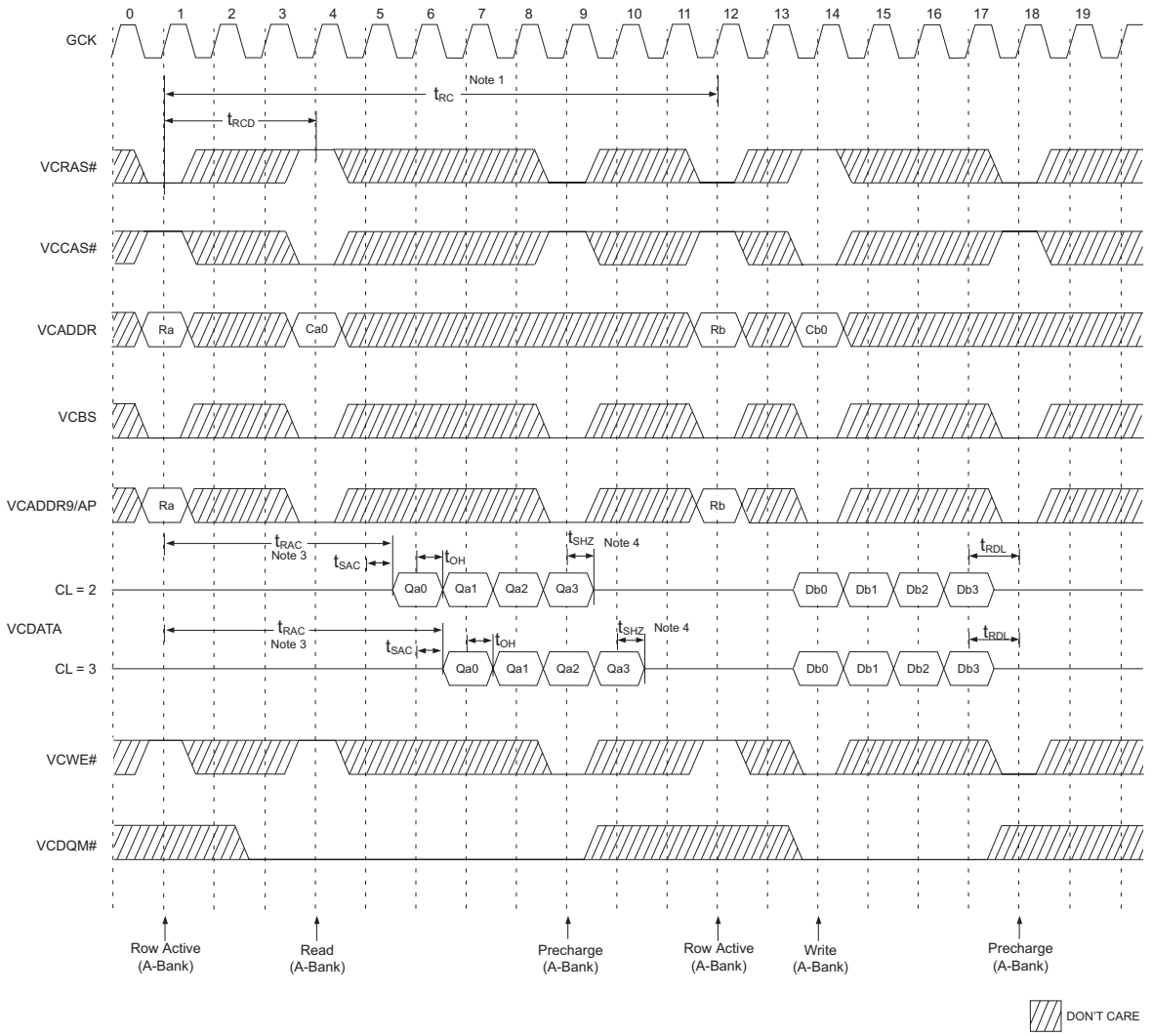


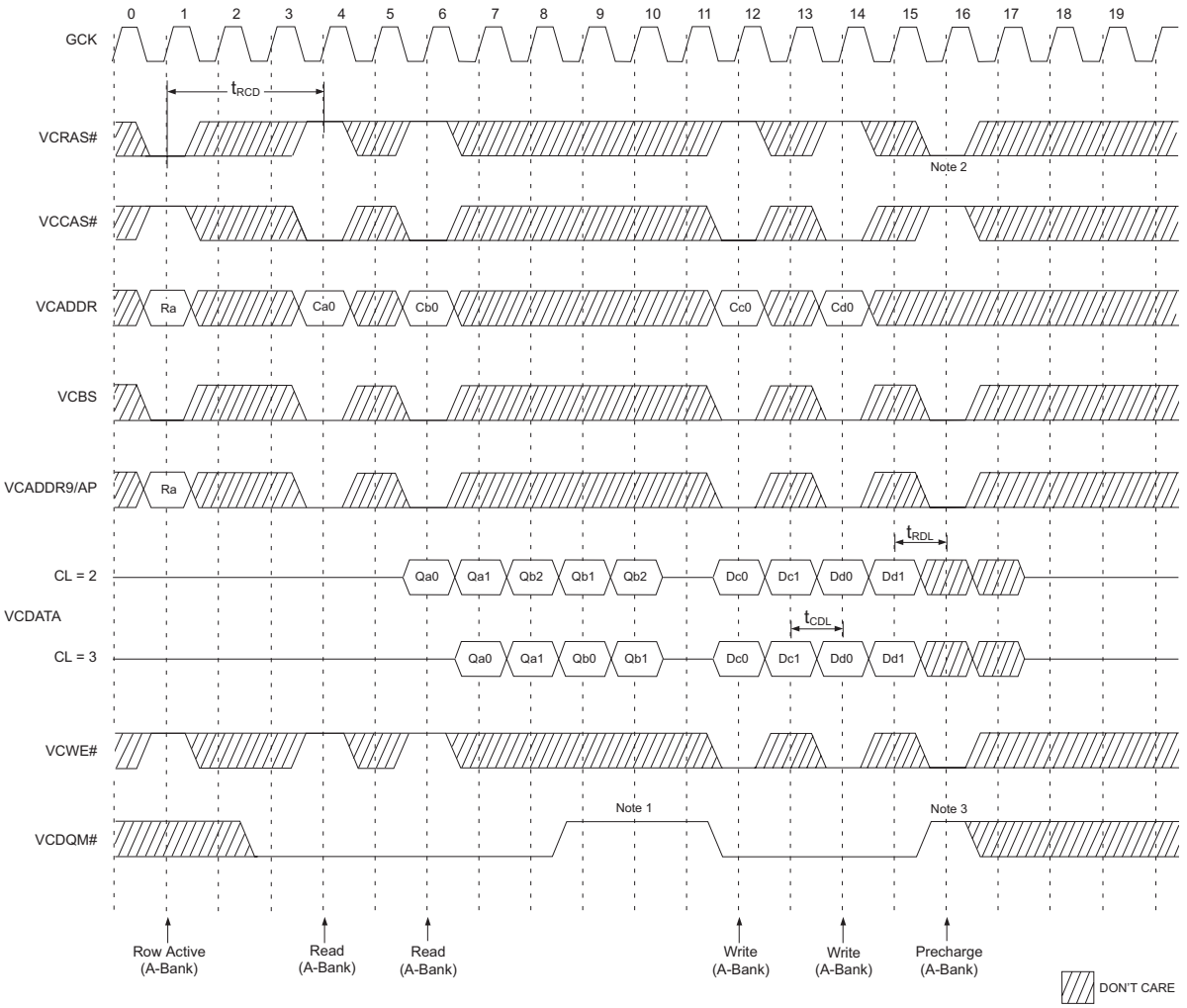
FIG. 6 SDRAM READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



Notes:

1. Minimum row cycle times are required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. (CAS Latency - 1) number of valid output data is available after Row precharge. Last valid output will be Hi-Z (t_{SHZ}) after the clock.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS Latency - 1) + t_{SAC}.
4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

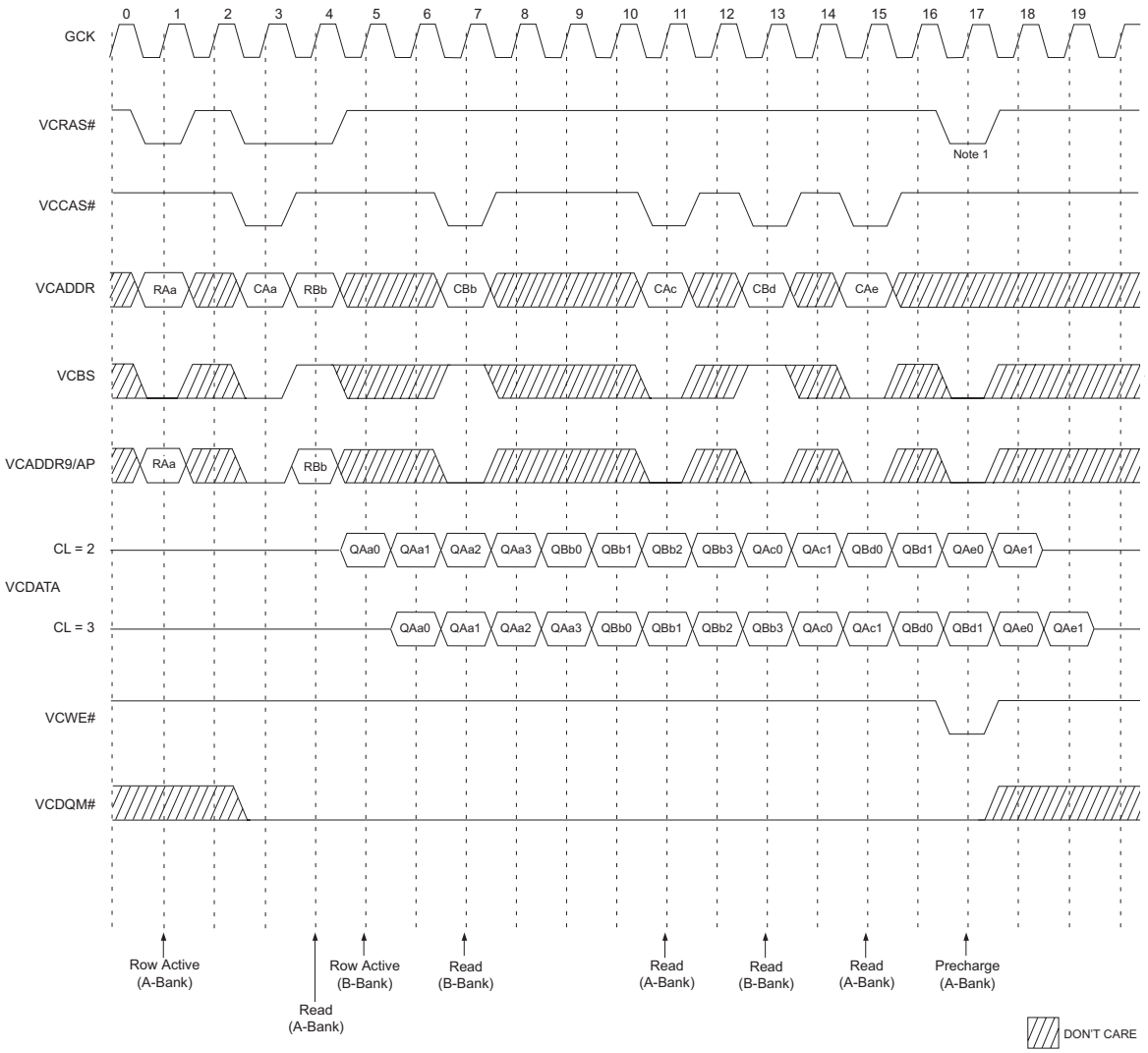
FIG. 7 SDRAM PAGE READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



Notes:

1. To write data before burst read ends. VCDQM# should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge will be written.
3. VCDQM# should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

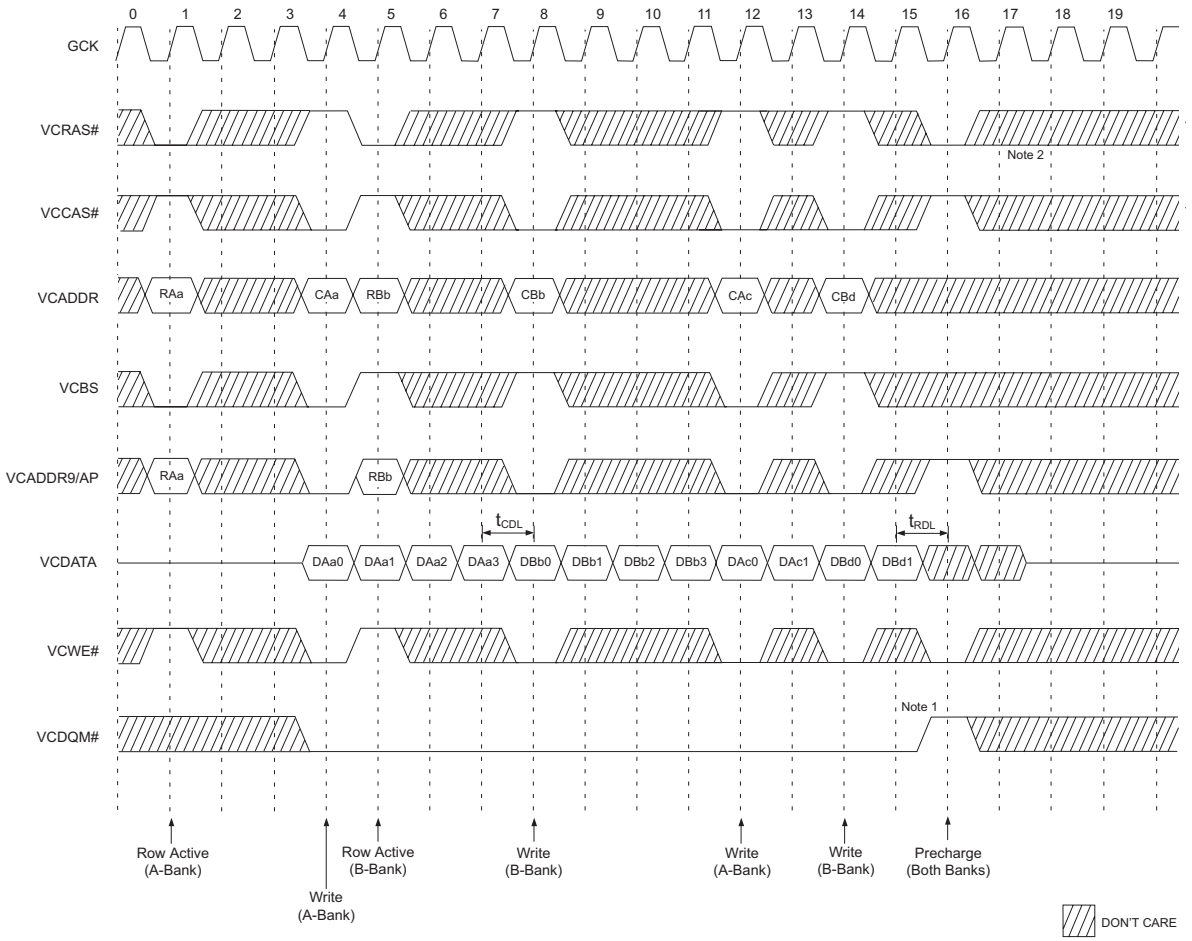
FIG. 8 SDRAM PAGE READ CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



Note:

1. To interrupt a burst read by Row precharge, both the read and the precharge banks must be the same.

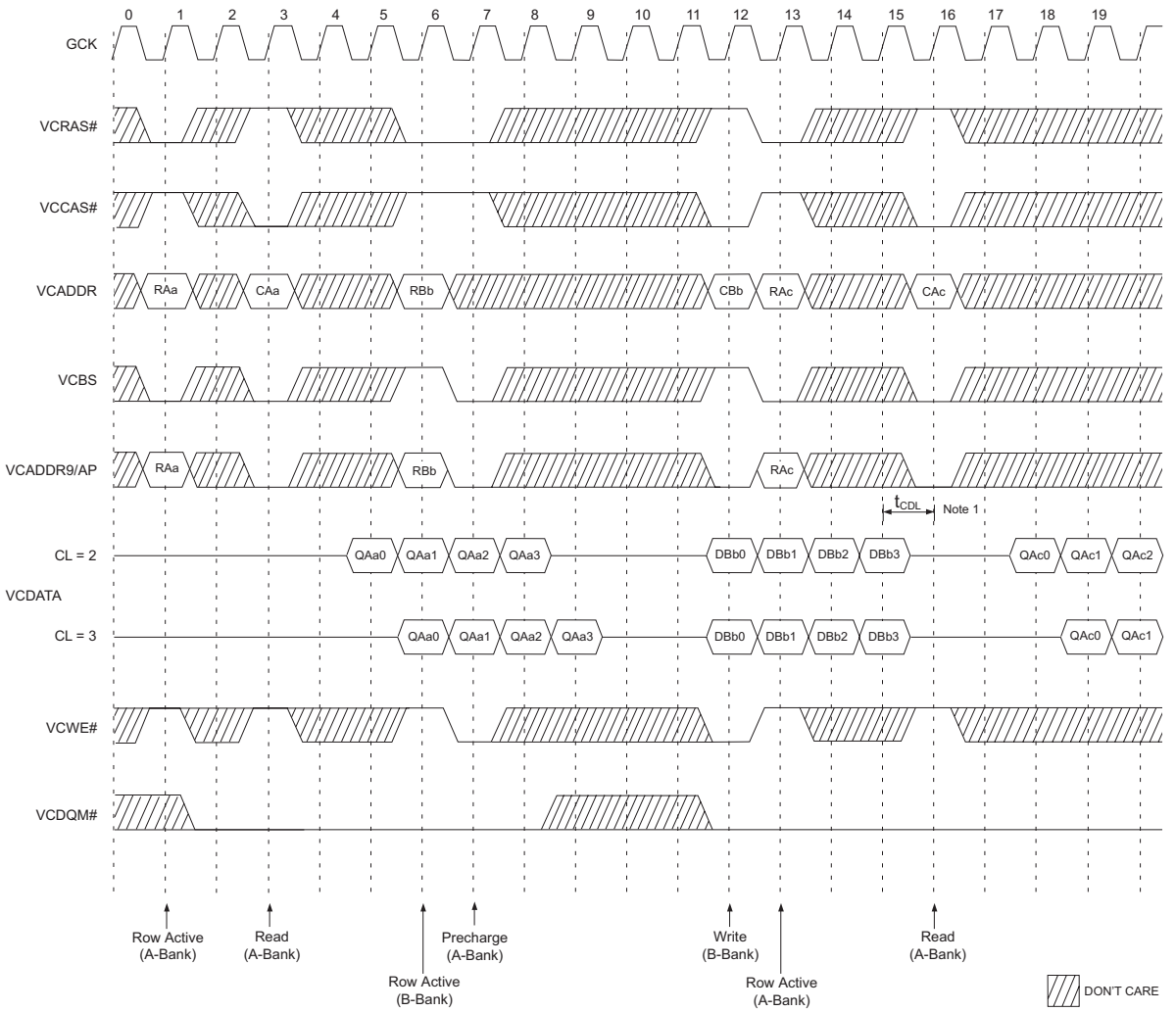
FIG. 9 SDRAM PAGE WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTES:

1. To interrupt burst write by Row precharge, VCDQM# should be asserted to mask invalid input data.
2. To interrupt a burst read by Row precharge, both the read and the precharge banks must be the same.

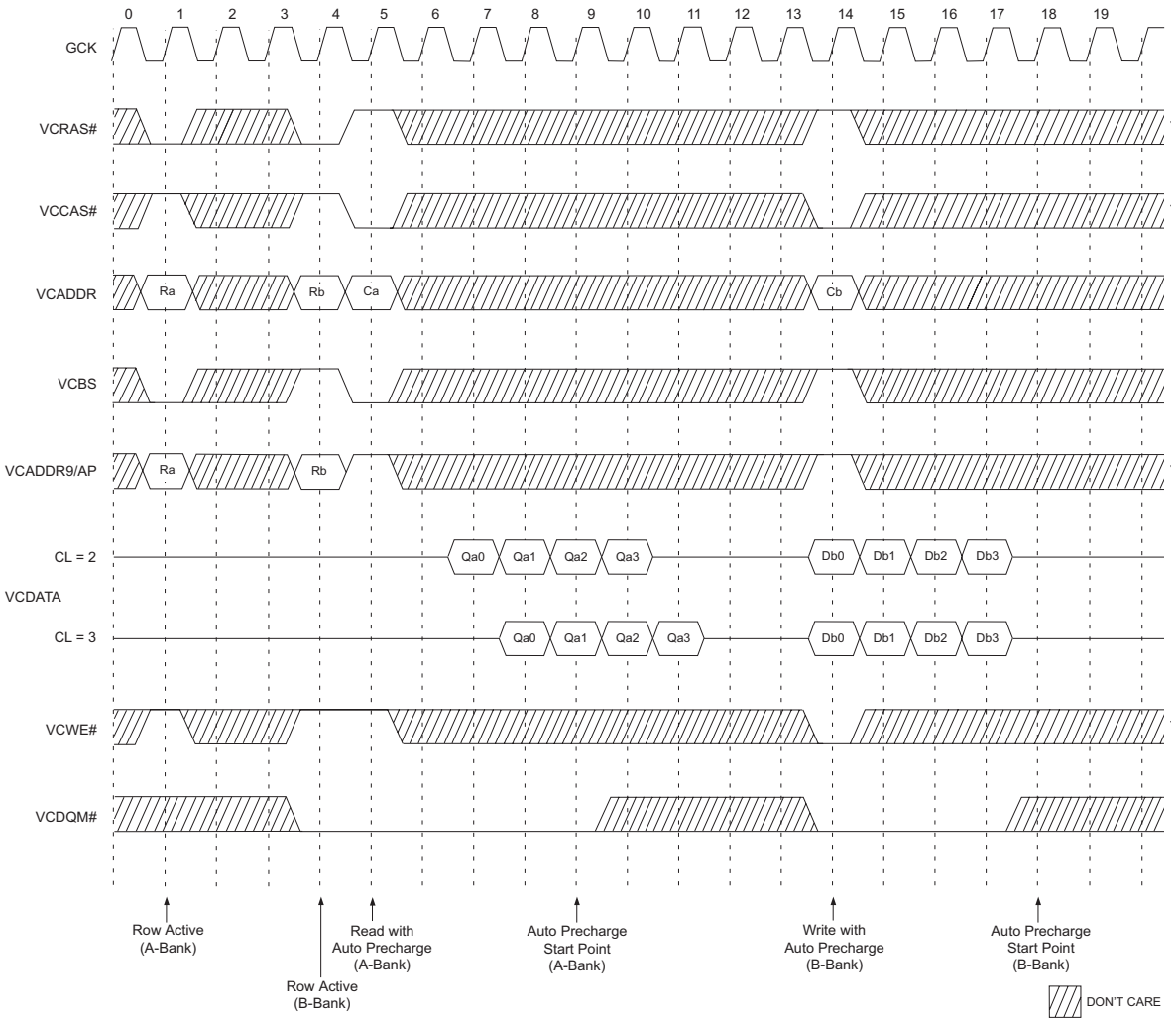
FIG. 10 SDRAM READ & WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



Note:

1. t_{CDL} should be met to complete write.

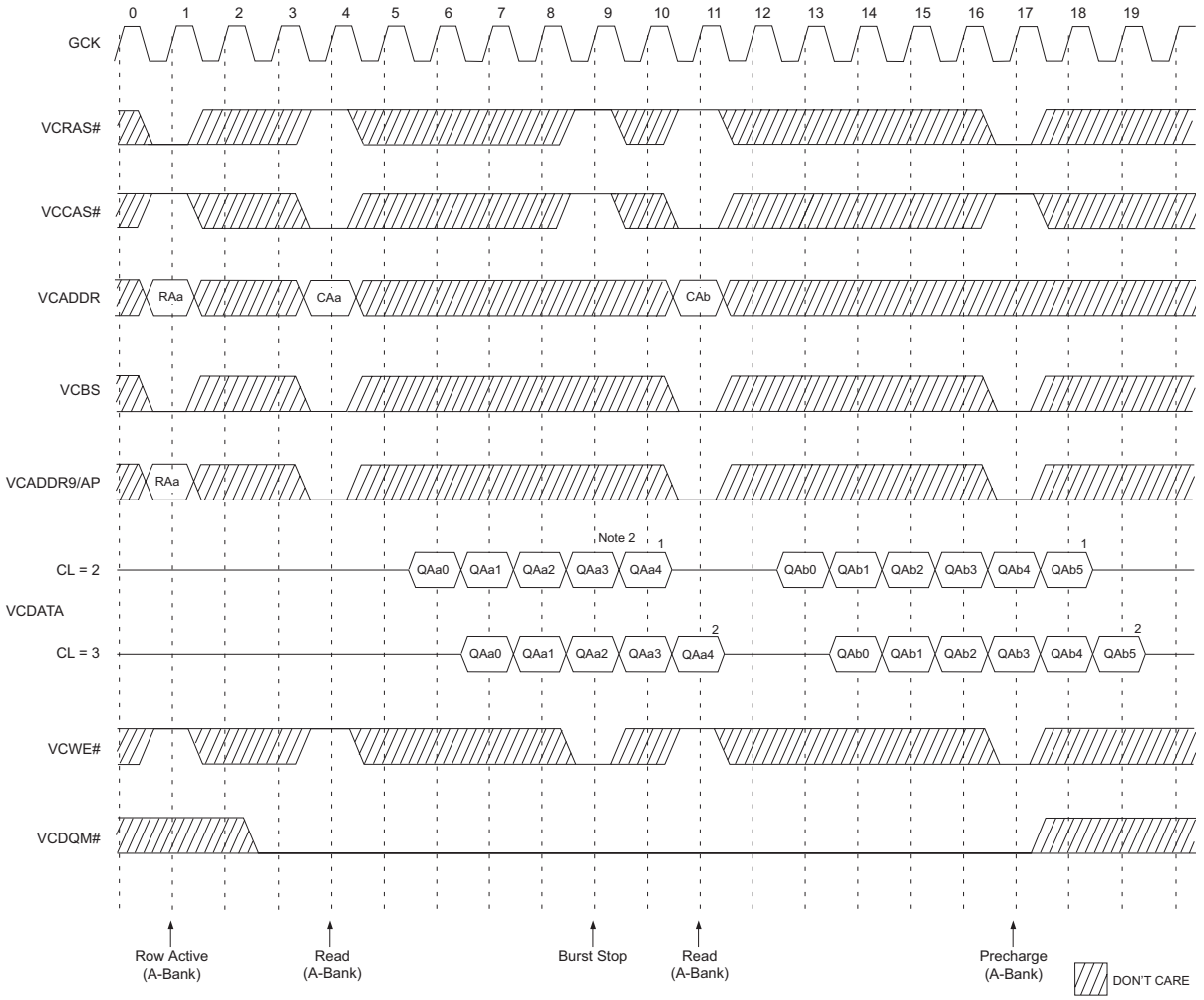
FIG. 11 SDRAM READ & WRITE CYCLE WITH AUTO PRECHARGE @BURST LENGTH = 4



Note:

1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start. (In the case of Burst Length = 1 & 2 and BRSW mode)

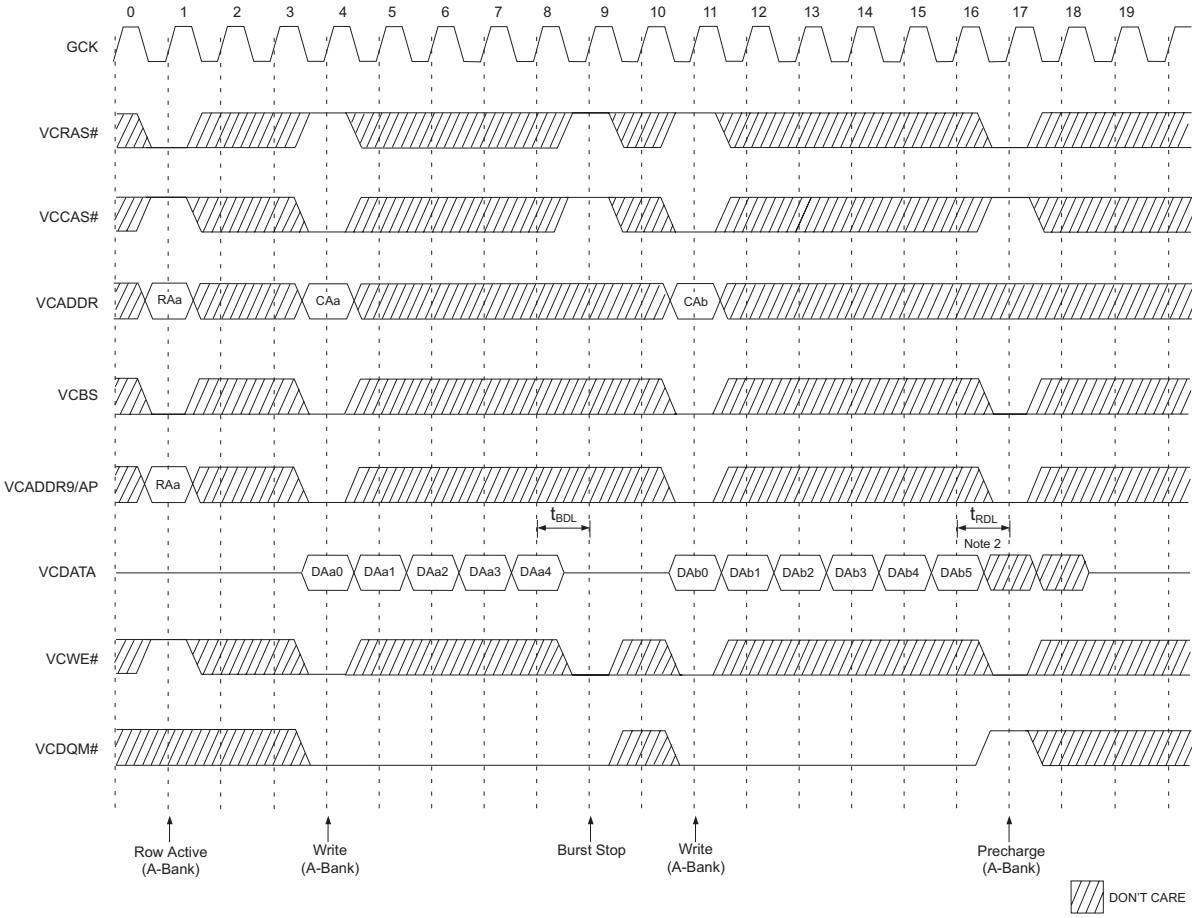
FIG. 12 SDRAM READ INTERRUPTED BY PRECHARGE COMMAND & READ BURST STOP @ BURST LENGTH = FULL PAGE



Notes:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid VCDATAs after burst stop, it is the same as the case of VCRAS# interrupt. Both cases are illustrated in the above timing diagram. See the label 1, 2 on each of them. But at burst write, burst stop and VCRAS# interrupt should be compared carefully. Refer to the timing diagram of "Full page write burst stop cycle."
3. Burst stop is valid at every burst length.

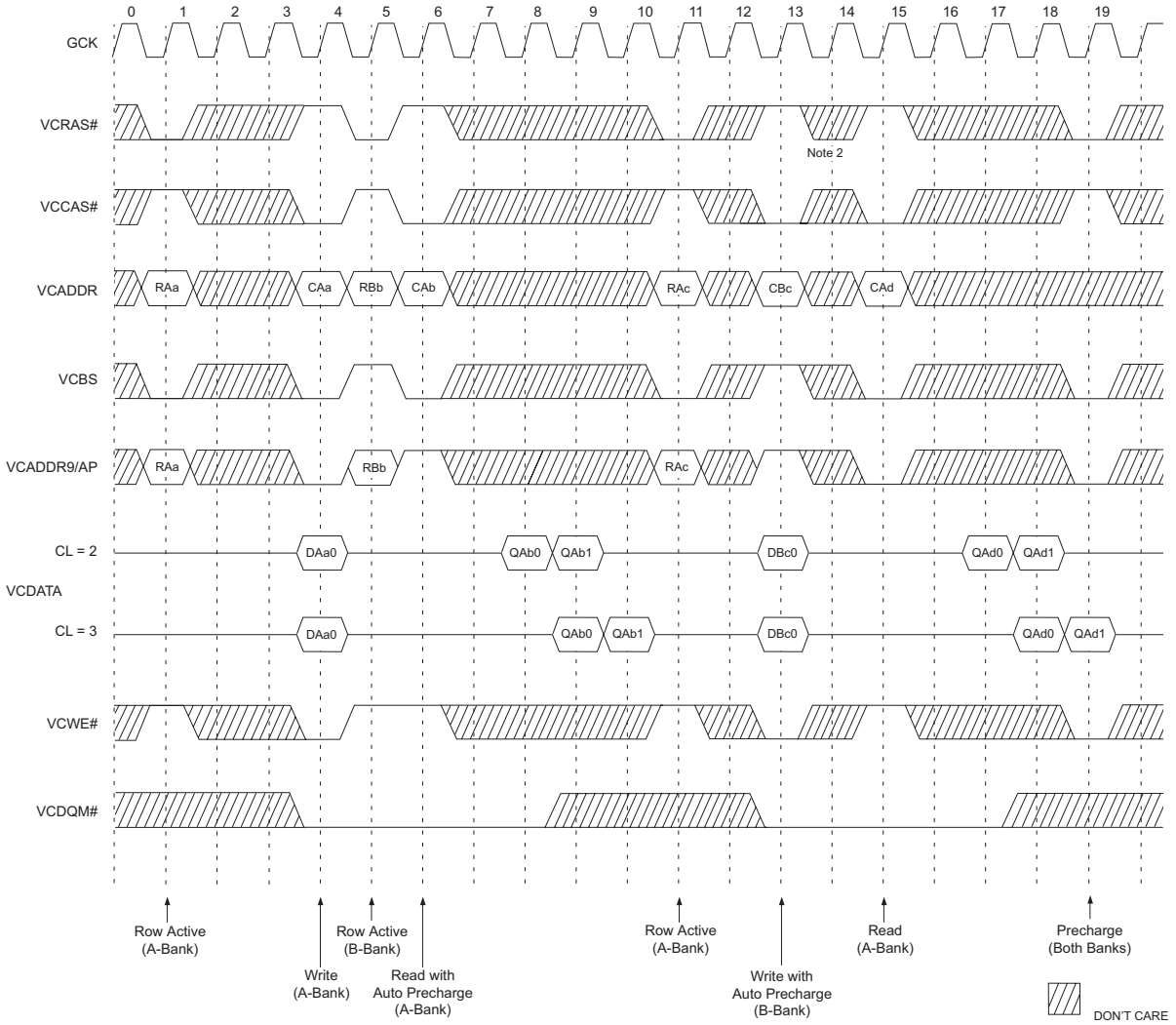
FIG. 13 SDRAM WRITE INTERRUPTED BY PRECHARGE COMMAND & WRITE BURST STOP @ BURST LENGTH = FULL PAGE



Notes:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   VCDQM# at write interrupt by precharge command is needed to prevent invalid write.
   VCDQM# should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

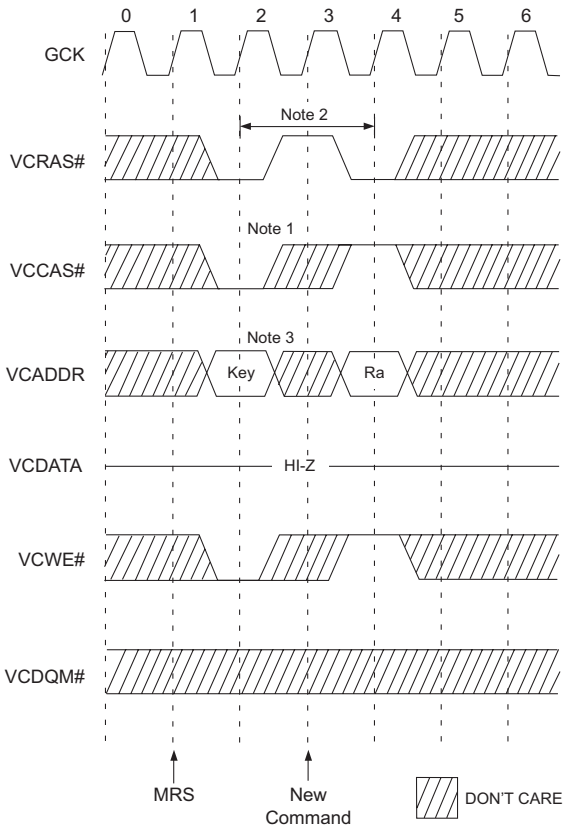
FIG. 14 SDRAM BURST READ SINGLE BIT WRITE CYCLE @ BURST LENGTH = 2



Notes:

1. BRSW modes enabled by setting A9 "High" at MRS (Mode Register Set).
   At the BRSW Mode, the burst length at Write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated. Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

FIG. 15 SDRAM MODE REGISTER SET CYCLE



*Both banks precharge should be completed before Mode Register Set cycle.

NOTES:
MODE REGISTER SET CYCLE

1. VCRAS#, VCCAS# & VCWE# activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new VCRAS# activation.
3. Please refer to Mode Register Set table.

MODE REGISTER FIELD TABLE TO PROGRAM MODES

REGISTER PROGRAMMED WITH MRS

Address	BA0	A9/AP	A8	A10	A7	A6	A5	A4	A3	A2	A1	A2
Function	RFU	RFU	W.B.L.	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A10	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9		Length	1	0	1	Reserved			1	0	1	Reserved	Reserved
0		Burst	1	1	0	Reserved			1	1	0	Reserved	Reserved
1		Single Bit	1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length: x32 (256)

POWER UP SEQUENCE

SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

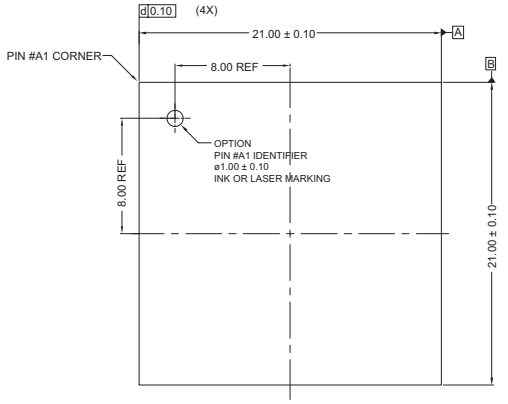
1. Apply power and start clock. Must maintain CKE= “H”,DQM = “H” and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200µs.
3. Issue precharge commandes for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

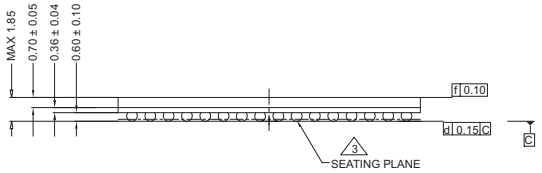
The device is now ready for normal operation.

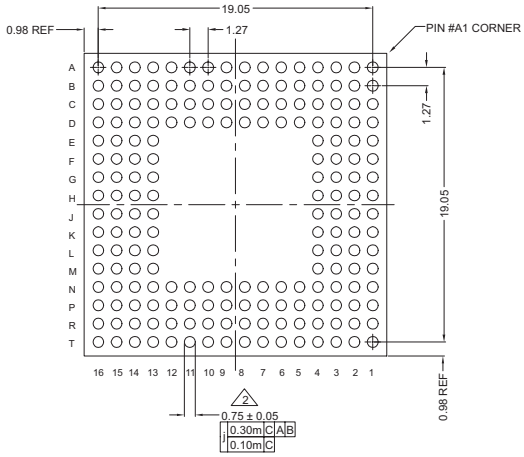
Note:
1. If A8 is high during MRS cycle, “Burst Read Single Bit Write” function will be enabled.
2. RFU (Reserved for future use) shuld stay “0” during MRS cycle.

PACKAGE DESCRIPTION: 192 LEAD BGA 21MM X 21MM



TOP VIEW





BOTTOM VIEW

NOTE

1. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y 14.5M-1994.
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C .
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDIER BALLS.
4. THE SURFACE FINISH OF THE PACKAGE SHALL BE EDM CHARMILLE #24 - #27
5. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ± 0.05
   ANGULAR ± 2º

ORDERING INFORMATION

WED9LAPC2C16V8BC	Commercial Temperature:	0ºC to +70ºC
WED9LAPC2C16V8BI	Industrial Temperature:	-40ºC to +85ºC