6A SINGLE HIGH-SPEED, CMOS POWER MOSFET DRIVER

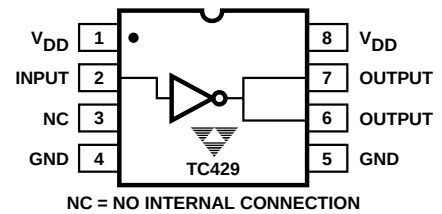
FEATURES

- **High Peak Output Current 6A**
- **Wide Operating Range ..... 7V to 18V**
- **High-Impedance CMOS Logic Input**
- **Logic Input Threshold Independent of Supply Voltage**
- **Low Supply Current**
  - **— With Logic 1 Input ..... 5mA Max**
  - **— With Logic 0 Input ..... 0.5mA Max**
- **Output Voltage Swing Within 25 mV of Ground or V_{DD}**
- **Short Delay Time ..... 75nsec Max**
- **High Capacitive Load Drive Capability**
  - **— t_{RISE}, t_{FALL} = 35nsec Max With C_{LOAD} = 2500pF**

APPLICATIONS

- **Switch-Mode Power Supplies**
- **CCD Drivers**
- **Pulse Transformer Drive**
- **Class D Switching Amplifiers**

PIN CONFIGURATION



NC = NO INTERNAL CONNECTION

NOTE: Duplicate pins must both be connected for proper operation.

GENERAL DESCRIPTION

The TC429 is a high-speed, single CMOS-level translator and driver. Designed specifically to drive highly capacitive power MOSFET gates, the TC429 features 2.5Ω output impedance and 6A peak output current drive.

A 2500pF capacitive load will be driven 18V in 25nsec. Delay time through the device is 60nsec. The rapid switching times with large capacitive loads minimize MOSFET transition power loss.

A TTL/CMOS input logic level is translated into an output voltage swing that equals the supply and will swing to within 25mV of ground or V_{DD}. Input voltage swing may equal the supply. Logic input current is under 10µA, making direct interface to CMOS/bipolar switch-mode power supply controllers easy. Input "speed-up" capacitors are not required.

The CMOS design minimizes quiescent power supply current. With a logic 1 input, power supply current is 5mA maximum and decreases to 0.5mA for logic 0 inputs.

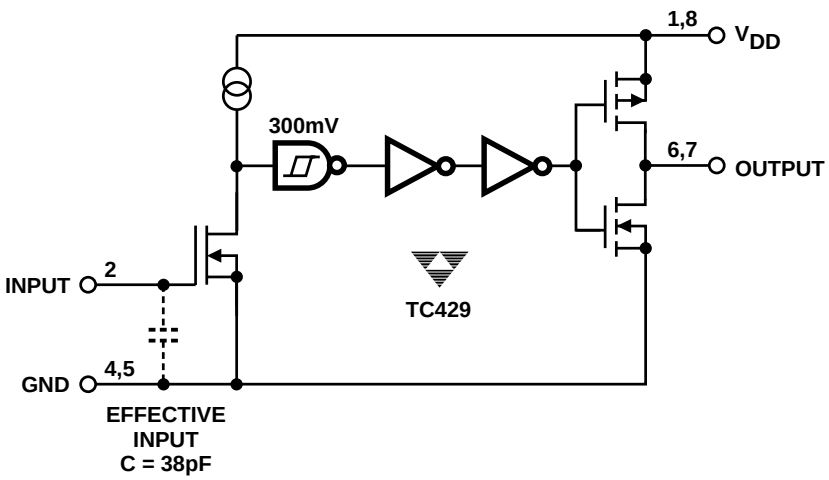
For dual devices, see the TC426/TC427/TC428 data sheet.

For noninverting applications, or applications requiring latch-up protection, see the TC4420/TC4429 data sheet.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC429CPA	8-Pin Plastic DIP	0°C to +70°C
TC429EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC429MJA	8-Pin CerDIP	– 55°C to +125°C

TYPICAL APPLICATION



TC429

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +20V
Input Voltage, Any Terminal ..... V_{DD} +0.3V to GND – 0.3V
Power Dissipation ($T_A \leq 70°C$)
- Plastic DIP 730mW
- CerDIP 800mW

Derating Factors
- Plastic DIP ..... 5.6 mW/°C Above 36°C
- CerDIP ..... 6.4 mW/°C

Operating Temperature Range
- C Version ..... 0°C to +70°C
- I Version ..... – 25°C to +85°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

T_A = +25°C with 7V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0, Low Input Voltage		—	1.3	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{IN} = 0.8V, I_{OUT} = 10mA, V_{DD} = 18V	—	1.8	2.5	Ω
		V_{IN} = 2.4V, I_{OUT} = 10mA, V_{DD} = 18V	—	1.5	2.5	
I_{PK}	Peak Output Current	V_{DD} = 18V (See Figure 3)	—	6	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500pF	—	23	35	nsec
t_F	Fall Time	Figure 1, C_L = 2500pF	—	25	35	nsec
t_{D1}	Delay Time	Figure 1	—	53	75	nsec
t_{D2}	Delay Time	Figure 1	—	60	75	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	3.5	5	mA
		V_{IN} = 0V	—	0.3	0.5	

NOTES: 1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS: Over operating temperature with $7V \le V_{DD} \le 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_{DD}$	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{IN} = 0.8V, I_{OUT} = 10 mA, V_{DD} = 18V	—	—	5	Ω
		V_{IN} = 2.4V, I_{OUT} = 10 mA, V_{DD} = 18V	—	—	5	
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500pF	—	—	70	nsec
t_F	Fall Time	Figure 1, C_L = 2500pF	—	—	70	nsec
t_{D1}	Delay Time	Figure 1	—	—	100	nsec
t_{D2}	Delay Time	Figure 1	—	—	120	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	—	12	mA
		V_{IN} = 0V	—	—	1	

NOTE: 1. Switching times guaranteed by design.

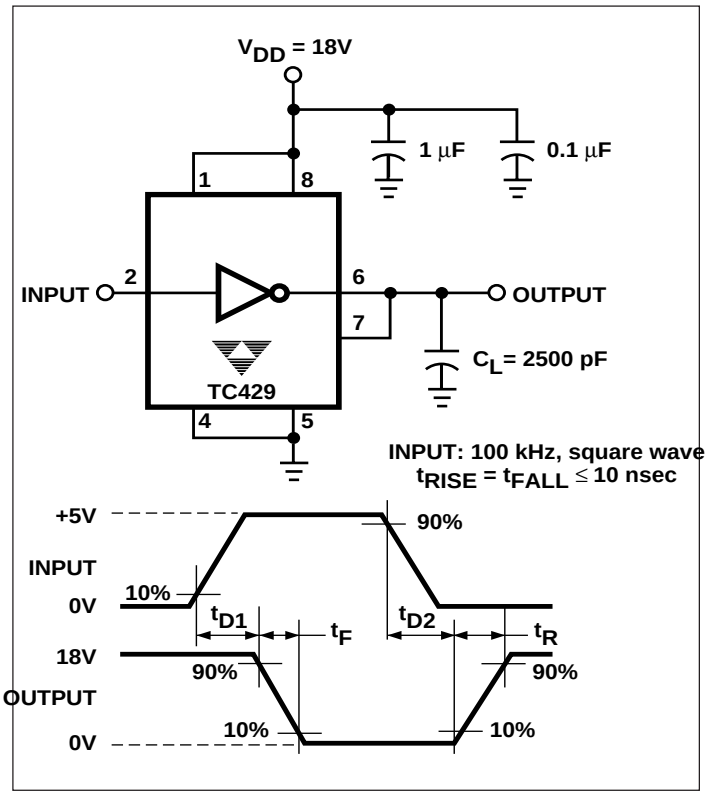
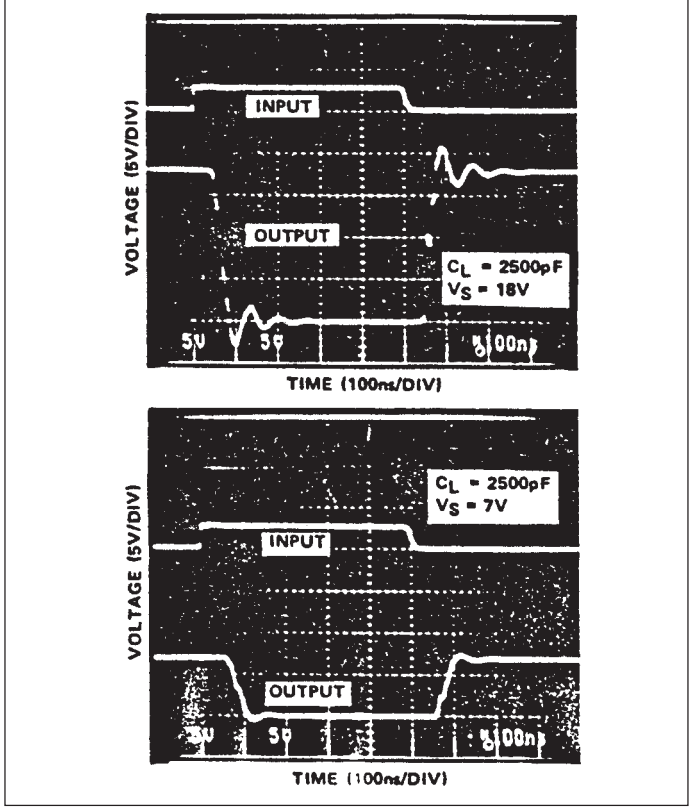


Figure 1. Inverting Driver Switching Time Test Circuit

SWITCHING SPEED



SUPPLY BYPASSING

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500 pF load 18V in 25nsec requires a 1.8A current from the device's power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (<0.5 in.) should be used. A 1 μF film capacitor in parallel with one or two 0.1 μF ceramic disk capacitors normally provides adequate bypassing.

GROUNDING

The high-current capability of the TC429 demands careful PC board layout for best performance. Since the TC429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. The feedback is especially noticeable with slow rise-time inputs, such as those produced by an open-collector output with resistor pull-up. The TC429 input structure includes about 300 mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 2 shows the feedback effect in detail. As the TC429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the TC429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillations may result.

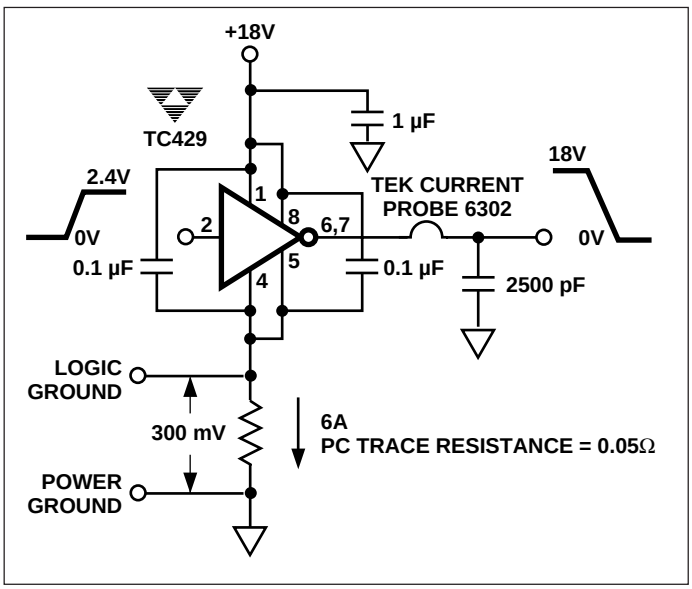


Figure 2. Switching Time Degradation Due to Negative Feedback

To ensure optimum device performance, separate ground traces should be provided for the logic and power connections. Connecting logic ground directly to the TC429 GND pins ensures full logic drive to the input and fast output switching. Both GND pins should be connected to power ground.

INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 3 mA current source load. With a logic "1" input, the maximum quiescent supply current is 5 mA. Logic "0" input level signals reduce quiescent current to 500 μA maximum.

The TC429 input is designed to provide 300 mV of hysteresis, providing clean transitions and minimizing output stage current spiking when changing states. Input voltage levels are approximately 1.5V, making the device TTL compatible over the 7V to 18V operating supply range. Input current is less than 10μA over this range.

The TC429 can be directly driven by TL494, SG1526/1527, SG1524, SE5560 or similar switch-mode power supply integrated circuits. By off-loading the power-driving duties to the TC429, the power supply controller can operate at lower dissipation, improving performance and reliability.

POWER DISSIPATION

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as the 4000 and 74C have outputs that can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The TC429, however, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. Table I lists the maximum operating frequency for several power supply voltages when driving a 2500pF load. More accurate power dissipation figures can be obtained by summing the three power sources.

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operation temperature is easily calculated. The 8-pin CerDIP junction-to-ambient thermal resistance is 150°C/W. At +25°C, the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

(1) Capacitive load dissipation (P_C)
(2) Quiescent power (P_Q)
(3) Transition power (P_T)

The capacitive load-caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

$$P_C = f\ C\ V_S^2,$$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage.

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low-power dissipation mode with only 0.5 mA total current drain. Logic high signals raise the current to 5 mA maximum. The quiescent power dissipation is:

$$P_Q = V_S\ (D\ (I_H) + (1–D)\ I_L),$$

where: I_H = Quiescent current with input high (5 mA max)
I_L = Quiescent current with input low (0.5 mA max)
D = Duty cycle.

Transition power dissipation arises because the output stage N- and P-channel MOS transistors are ON simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

$$P_T = f\ V_S\ (3.3 \times 10^{-9}\ A \cdot Sec).$$

An example shows the relative magnitude for each item.

Example 1:

C = 2500 pF
V_S = 15V
D = 50%
f = 200 kHz
P_D = Package power dissipation = $P_C + P_T + P_Q$
= 113 mW + 10 mW + 41 mW
= 164 mW.

Maximum operating temperature = $T_J – \theta_{JA}\ (P_D)$
= 125°C,

where: T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (150°C/W, CerDIP).

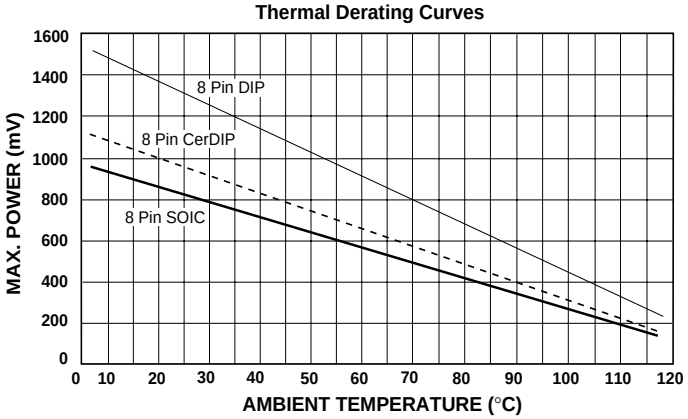
NOTE: Ambient operating temperature should not exceed +85°C for IJA devices or +125°C for MJA devices.

Table 1. Maximum Operating Frequencies

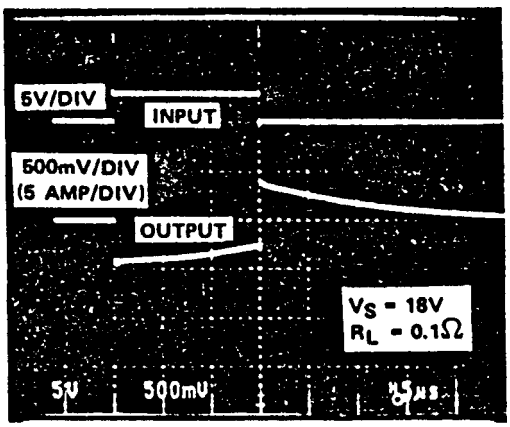
V_S	f_{Max}
18V	500 kHz
15V	700 kHz
10V	1.3 MHz
5V	>2 MHz

CONDITIONS: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = +25°C
3. C_L = 2500 pF

Thermal Derating Curves



Peak Output Current Capability



POWER-ON OSCILLATION

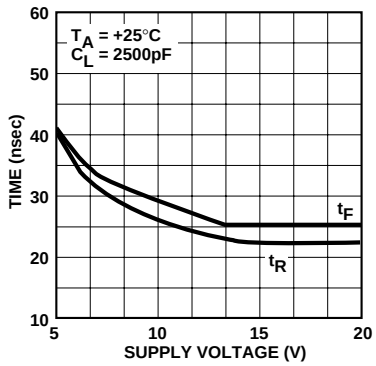
It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

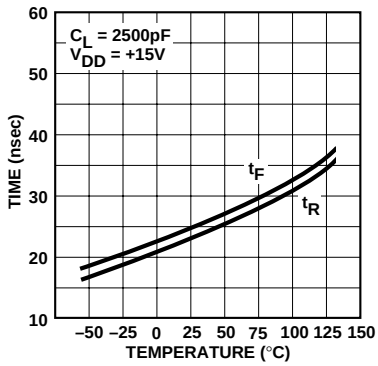
TC429

TYPICAL CHARACTERISTICS

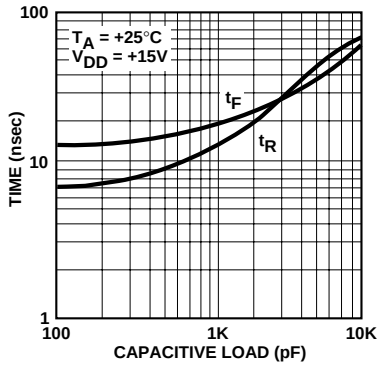
Rise/Fall Times vs. Supply Voltage



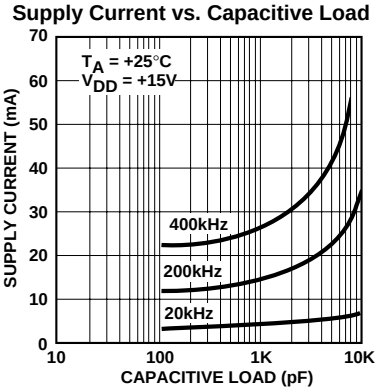
Rise/Fall Times vs. Temperature



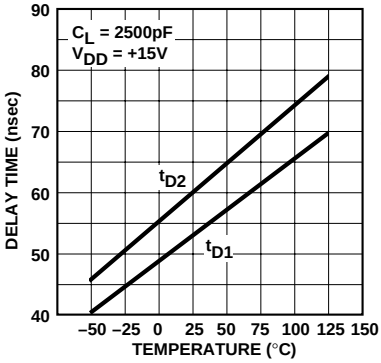
Rise/Fall Times vs. Capacitive Load



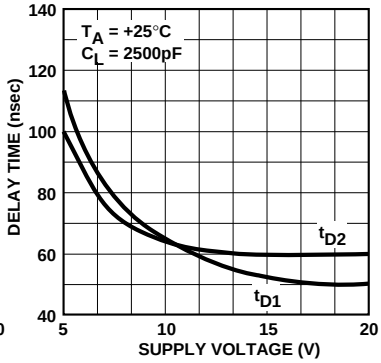
Supply Current vs. Capacitive Load



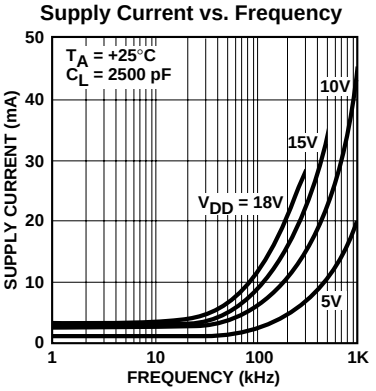
Delay Times vs. Temperature



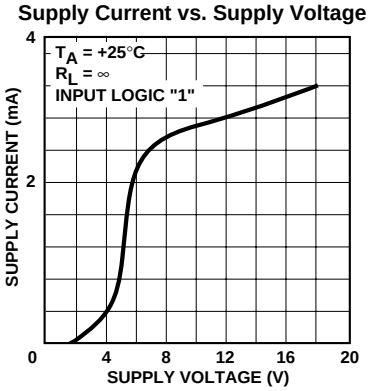
Delay Times vs. Supply Voltage



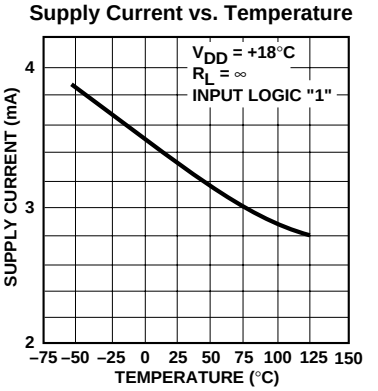
Supply Current vs. Frequency



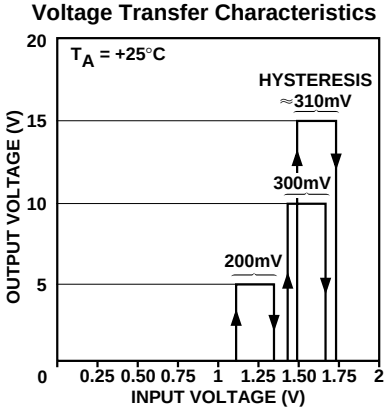
Supply Current vs. Supply Voltage



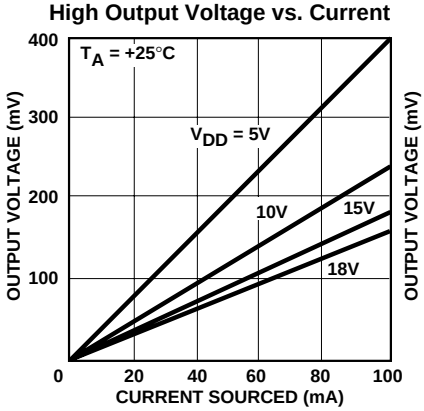
Supply Current vs. Temperature



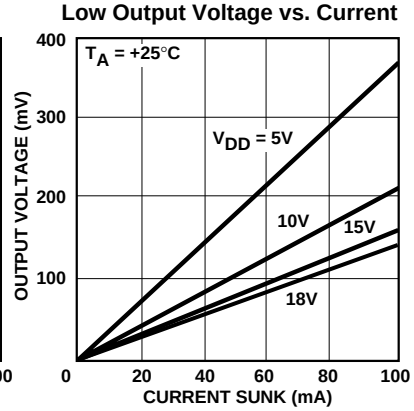
Voltage Transfer Characteristics



High Output Voltage vs. Current



Low Output Voltage vs. Current



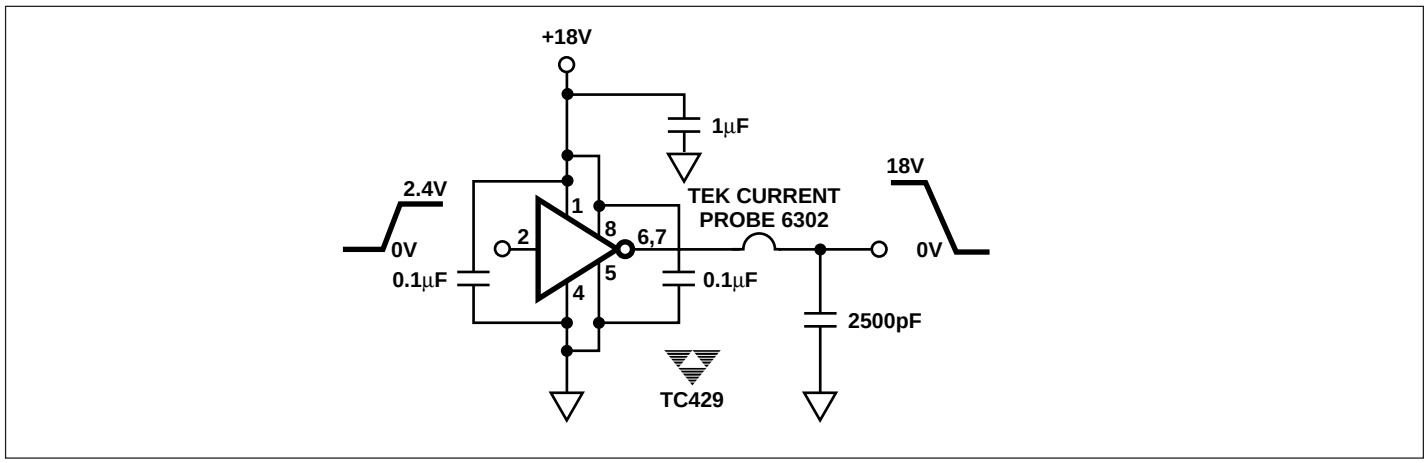


Figure 3. Peak Output Current Test Circuit