

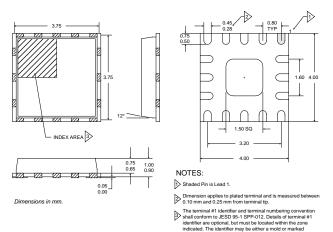
3V CDMA/FM MIXER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

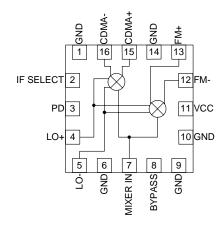
The RF2466 is a receiver dual downconverter designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to downconvert RF signals while providing 14dB gain in CDMA mode and 7dB gain in FM mode. Also, it features IF output selection and power down mode. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. The IC is manufactured on an advanced Silicon Bipolar process.



Package Style: LCC, 16-Pin, 4x4

4 Pins 1 and 9 are fused. 5 Package Warpage: 0.05 max

Optimum Technology Matching® Applied ✓ Si BJT ☐ GaAs HBT ☐ GaAs MESFET ☐ Si Bi-CMOS ☐ SiGe HBT ☐ Si CMOS



Functional Block Diagram

Features

- Dual Mode CDMA/AMPS
- Dual Mode JCDMA/TACS
- Digitally Selectable IF Outputs
- 500MHz to 1100MHz Operation
- Power Down Mode

Ordering Information

RF2466 3V CDMA/FM Mixer

RF2466 PCBA Fully Assembled Evaluation Board

RF Micro Devices, Inc. 7628 Thorndike Road Greensboro, NC 27409, USA Tel (336) 664 1233 Fax (336) 664 0454 http://www.rfmd.com

Rev A7 010717

RF2466

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification		Unit	Condition		
Faranietei	Min.	Тур.	Max.		Condition	
Overall					T=25°C, V _{CC} =3.0V, RF=881MHz, LO=966MHz @ 0dBm, IF1=CDMA, IF2=FM	
RF Frequency Range		200 to 1000		MHz		
LO Frequency Range		500 to 1100		MHz		
IF Frequency Range		0.1 to 250		MHz		
Conversion Gain	12.5	14		dB	IF1, 1kΩ balanced load.	
	5	7		dB	IF2, 870 Ω load.	
Noise Figure		9		dB	IF1 single sideband.	
		10.5		dB	IF2 single sideband	
Input VSWR		<1.5:1			IF1 with external matching	
		<2:1			IF2 with external matching	
Input IP3	+3	+7		dBm	IF1	
	+3	+7		dBm	IF2	
Input P1dB		-7		dBm	IF1	
		-4		dBm	IF2	
MIX IN to IF1, IF2 Rejection		35		dB		
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network	
Output Impedance		>1		kΩ	IF1, balanced, open collector	
		870		Ω	IF2, single ended, with external inductor.	
LO Input						
LO Input Range	-10	-3	0	dBm		
LO IN to RF Input Rejection		20		dB		
LO IN to IF1, IF2 Rejection		15		dB		
LO Input VSWR		<2:1			IF1 with external matching network	
		2.5			IF2 with external matching network	
Power Supply						
Voltage	2.7	3.0	4.0	V		
Current Consumption		16	21	mA	IF1 selected	
		12	16	mA	IF2 selected	
			5	μΑ	ENABLE=0	

6-8 Rev A7 010717

Pin	Function	Description	Interface Schematic
1	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
2	IF SELECT	Control line for IF out select. A logic "low" enables the FM output. A logic "high" enables the CDMA output. The threshold voltage is 1.6V, and the pin draws less than 50μA when selected.	C1 O—ΛΛΛ
3	PD	Power down pin. A logic "low" (<1.6V) turns the part off. A logic "high" (>1.6V) turns the part on. In addition, pin 2 (IF SELECT) should also be taken low during power down.	PD 0
4	LO+	Mixer LO balanced input pin. For single-ended input operation, this pin is used as an input and pin 5 is bypassed to ground.	LO IN-
5	LO-	Same as pin 4 except complementary input.	See pin 4.
6	GND	Ground connection for the mixer. For best performance, keep traces physically short and connect immediately to ground plane.	
7	MIXER IN	Mixer RF input pin. This pin is internally DC-biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	MIX IN O
8	BYPASS	Internal voltage reference. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
9	GND	Same as pin 1.	
10	GND	Same as pin 1.	
11	vcc	Supply voltage for the mixers, bias circuits, and control logic. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	VCC2 BIAS COUT
12	FM-	Same as pin 13, except complimentary output. For typical single ended operation, this pin is connected directly to $V_{\rm CC}$.	See pin 13.
13	FM+	FM IF output pin. This is a balanced output, but is typically used as a single-ended output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC} , sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, is about 870Ω at 85MHz . Because this pin is biased to V_{CC} , a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	1F2+ 1F2- 8.5 pF 2.1 kΩ
14	GND	Same as pin 1.	
15	CDMA+	CDMA IF output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC} , sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 85MHz is higher than $1\mathrm{k}\Omega$, even though the part is designed to drive a $1\mathrm{k}\Omega$ load. Because this pin is biased to V_{CC} , a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	IF1+ GND2 IF1- 1.2 1.2 pF pF
16	CDMA-	Same as pin 15, except complementary output.	See pin 15.

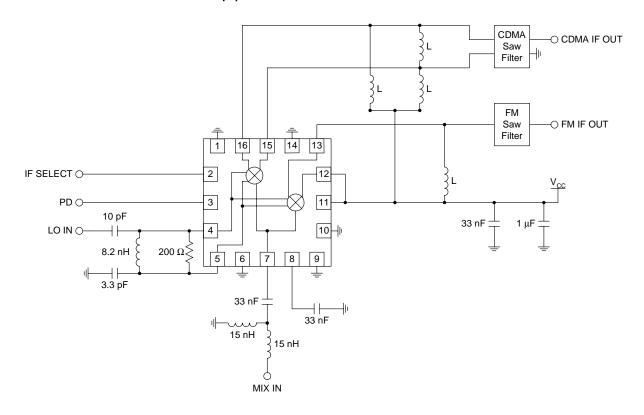
Rev A7 010717 6-9

RF2466

Pin	Function	Description	Interface Schematic
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

6-10 Rev A7 010717

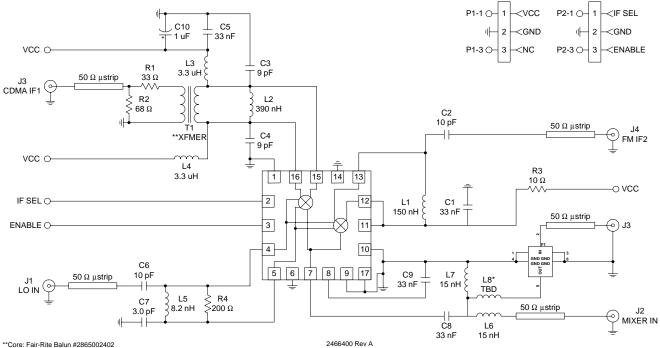
Application Schematic



Rev A7 010717 6-11

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



**Core: Fair-Rite Balun #2865002402

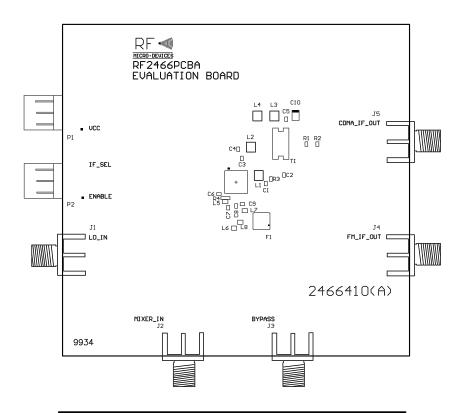
"Core: Fair-Nite Balun #2865002402
L12: 3 turns #30 AWG (Green)
L34: 12 turns #32 AWG (Red)
One turn = one pass through BOTH holes.
Winding starts and finishes on same end of core.
L12 and L34 exit opposite ends of core.
F1: filter

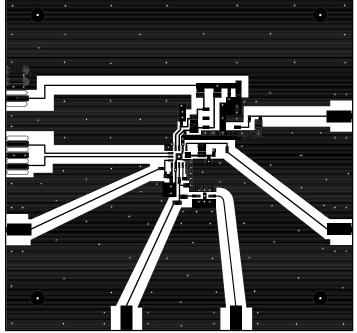
Enable	IF Select	Stage
0	0	Off
0	1	Off
1	0	FM
1	1	CDMA

Rev A7 010717 6-12

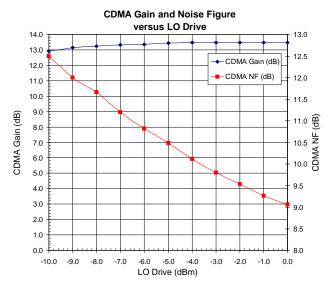
Evaluation Board Layout Board Size 3.070" x 2.928"

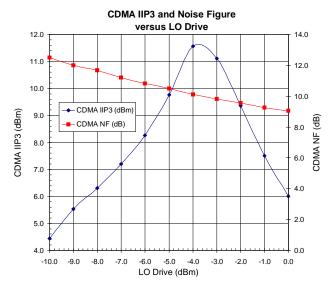
Board Thickness 0.056", Board Material FR-4, Multi-Layer

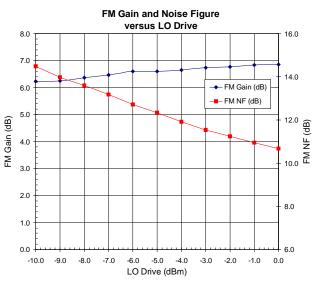


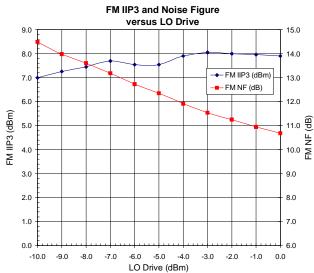


Rev A7 010717 6-13









6-14 Rev A7 010717