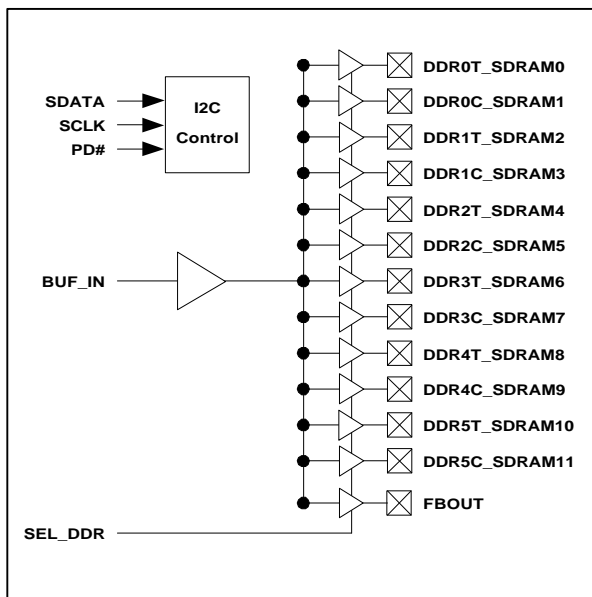


DDR SDRAM Buffer with 2 DDR or 3 SDRAM DIMMS

FEATURES

- Generates 12-output buffers from one input.
- Supports up to 2 DDR DIMMS or 3 SDRAM DIMMS.
- Supports 266MHz DDR SDRAM.
- One additional output for feedback.
- Less than 5ns delay.
- Skew between any outputs is less than 100 ps.
- 2.5V or 3.3V Supply range.
- Enhanced DDR and SDRAM Output Drive selected by I2C.
- Available in 28 pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION

FBOUT	1	28	SEL_DDR
PD#	2	27	DDR5T_SDRAM10
DDR0T_SDRAM0	3	26	DDR5C_SDRAM11
DDR0C_SDRAM1	4	25	VDD3.3_2.5
VDD3.3_2.5	5	24	GND
GND	6	23	DDR4T_SDRAM8
DDR1T_SDRAM2	7	22	DDR4C_SDRAM9
DDR1C_SDRAM3	8	21	VDD3.3_2.5
VDD3.3_2.5	9	20	GND
BUF_IN	10	19	DDR3T_SDRAM6
GND	11	18	DDR3C_SDRAM7
DDR2T_SDRAM4	12	17	GND
DDR2C_SDRAM5	13	16	SCLK
VDD3.3_2.5	14	15	SDATA

Note: #: Active Low

DESCRIPTIONS

The PLL103-06 is designed as a 3.3V/2.5V buffer to distribute high-speed clocks in PC applications. The device has 12 outputs. These outputs can be configured to support 3 unbuffered standard SDR (Single Data Rate) DIMMS and 2 DDR DIMMS. The PLL103-06 can be used in conjunction with the PLL202-04 or similar clock synthesizer for the VIA Pro 266 chipset.

The PLL103-06 also has an I2C interface, which can enable or disable each output clock. When power up, all output clocks are enabled (has internal pull up).

DDR SDRAM Buffer with 2 DDR or 3 SDRAM DIMMS

PIN DESCRIPTIONS

Name	Number	Type	Description
FBOUT	1	O	Feedback clock for chipset. Output voltage depends on VDD3.3_2.5V.
BUF_IN	10	I	Reference input from chipset. 3.3V input for STANDARD SDRAM mode; 2.5V input for DDR-ONLY mode.
PD	2	I	Power Down Control input. When low, it will tri-state all outputs.
SEL_DDR	28	I	Input configure for DDR-ONLY mode or STANDARD SDR mode. 1 = DDR-ONLY mode (when VDD3.3_2.5 select 2.5V); 0 = SDR mode (when VDD3.3_2.5 select 3.3V). In DDR-ONLY mode, all outputs will be configured as DDR outputs. In STANDARD SDR mode, all outputs will be configured as SDRAM outputs.
DDR[0:5]T_SDRAM [0,2,4,6,8,10]	3,7,12,19, 23,27	O	When SEL_DDR=1, these outputs provide DDR mode outputs; when SEL_DDR=0, these outputs provide standard SDRAM mode outputs. Voltage swing depends on VDD3.3_2.5.
DDR[0:5]C_SDRAM [1,3,5,7,9,11]	4,8,13,18, 22,26	O	When SEL_DDR=1, these outputs provide complementary copies of BUF_IN; when SEL_DDR=0, these outputs provide standard SDRAM mode outputs. Voltage swing depends on VDD3.3_2.5.
VDD3.3_2.5	5,9,14,21,25	P	When VDD=2.5V, SEL_DDR=1. DDR-ONLY mode is selected; when VDD=3.3V, SEL_DDR=0. STANDARD SDRAM mode is selected.
GND	6,11,17, 20,24	P	Ground.

DDR SDRAM Buffer with 2 DDR or 3 SDRAM DIMMS

I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	-
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Data Protocol	<p>This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).</p> <p>Following the acknowledge of this address byte, in Write Mode: the Command Byte and Byte Count Byte must be sent by the master but ignored by the slave, in Read Mode: the Byte Count Byte will be read by the master then all other Data Byte. Byte Count Byte default at power-up is = (0x09).</p>							

I2C CONTROL REGISTERS

1. BYTE 6: Outputs Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	28	1	SEL_DDR (I2C is ready only, value is set through pin28)
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	1	1	FBOUT
Bit 3	27, 26	1	DDR5T_SDRAM10, DDR5C_SDRAM11
Bit 2	-	1	Reserved
Bit 1	23, 22	1	DDR4T_SDRAM8, DDR4C_SDRAM9
Bit 0	-	1	Reserved

DDR SDRAM Buffer with 2 DDR or 3 SDRAM DIMMS

2. BYTE 7: Outputs Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	19, 18	1	DDR3T_SDRAM6, DDR3C_SDRAM7
Bit 5	12, 13	1	DDR2T_SDRAM4, DDR2C_SDRAM5
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	7, 8	1	DDR1T_SDRAM2, DDR1C_SDRAM3
Bit 1	-	1	Reserved
Bit 0	3, 4	1	DDR0T_SDRAM0, DDR0C_SDRAM1

DDR SDRAM Buffer with 2 DDR or 3 SDRAM DIMMS

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V _{DD}	V _{SS} -0.5	7.0	V
Input Voltage, dc	V _I	V _{SS} -0.5	V _{DD} +0.5	V
Output Voltage, dc	V _O	V _{SS} -0.5	V _{DD} +0.5	V
Storage Temperature	T _S	-65	150	°C
Ambient Operating Temperature	T _A	0	70	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. Operating Conditions

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V _{DD3.3}	3.135	3.465	V
Supply Voltage	V _{DD2.5}	2.375	2.625	V
Input Capacitance	C _{IN}		5	pF
Output Capacitance	C _{OUT}		6	pF

3. Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V _{IH}	All Inputs except I2C	2.0		V _{DD} +0.3	V
Input Low Voltage	V _{IL}	All inputs except I2C	V _{SS} -0.3		0.8	V
Input High Current	I _{IH}	V _{IN} = V _{DD}			TBM	uA
Input Low Current	I _{IL}	V _{IN} = 0			TBM	uA
Output High Voltage	V _{OH}	I _{OL} = -12mA, V _{DD} = 2.375V	1.7			V
Output Low Voltage	V _{OL}	I _{OL} = 12mA, V _{DD} = 2.375V			0.6	V
Output High Current	I _{OH}	V _{DD} = 2.375V, V _{OUT} =1V	-18	-32		mA
Output Low Current	I _{OL}	V _{DD} = 2.375V, V _{OUT} =1.2V	26	35		mA

Note: TBM: To be measured

DDR SDRAM Buffer with 2 DDR or 3 SDRAM DIMMS

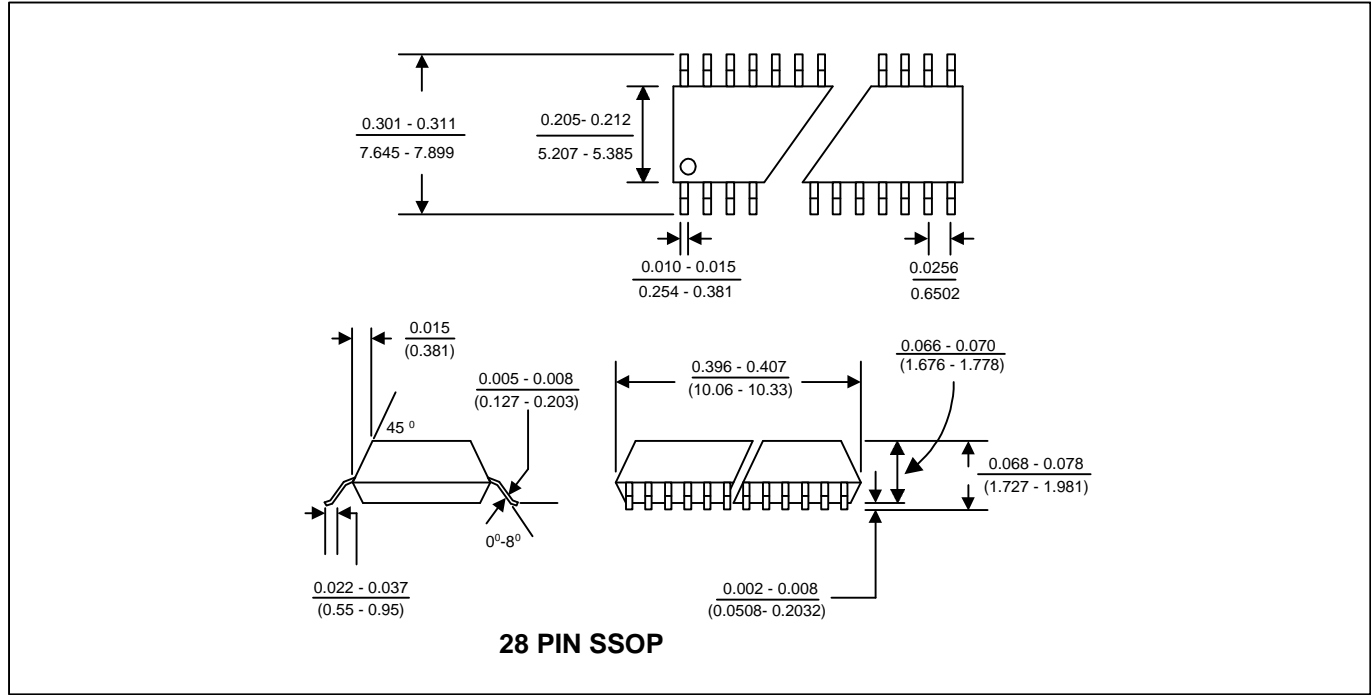
3. Electrical Specifications (Continued)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (DDR-only mode)	I _{DD}	Unloaded outputs, 133MHz			TBM	mA
Supply Current (SDRAM mode)	I _{DD}	Unloaded outputs, 133MHz			TBM	mA
Supply Current	I _{DDS}	PD = 0			TBM	mA
Output Crossing Voltage	V _{OC}		(VDD/2) -0.1	VDD/2	(VDD/2)+ 0.1	V
Output Voltage Swing	V _{OUT}		0.7		VDD-0.4	V
Duty Cycle	D _T	Measured @ 1.5V	45	50	55	%
Max. Operating Frequency			66		170	MHz
Rising Edge Rate	T _{OR}	Measured @ 0.4V ~ 2.4V	1.0	1.5	2.0	V/ns
Falling Edge Rate	T _{OF}	Measured @ 2.4V ~ 0.4V	1.0	1.5	2.0	V/ns
DDR Rising Edge Rate	T _{OR}	Measured between 20% to 80% of output	0.25	0.6	1.0	V/ns
DDR Falling Edge Rate	T _{OF}	Measured between 20% to 80% of output	0.25	0.6	1.0	V/ns
Clock Skew(pin to pin)	T _{SKEW}	All outputs equally loaded			100	ps
Stabilization Time	T _{ST}				0.1	ms

Note: TBM: To be measured

DDR SDRAM Buffer with 2 DDR or 3 SDRAM DIMMS

PACKAGE INFORMATION



ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL103-06 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL
PACKAGE TYPE
X=SSOP

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by PhaseLink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.